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TDK5111F

315 MHz ASK/FSK Transmitter in 10-pin Package

Version 1.1

Wireless Control Components

Never stop thinking.

Edition 2007-09-18

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315 MHz ASK/FSK Transmitter in 10-pin Package

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27	Increased ESD-values	
28-30,32	Added Max.-and Min.-values (Current, Power)	
32	Added output power and temperature drift of output power values	
28, 30, 32	Added values of frequency range and for possible enhance of frequency range	

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1 Product Description

1.1 Overview

The TDK 5111 F is a single chip ASK/FSK transmitter for operation in the frequency band 311 ... 317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

1.2 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- frequency range 311 ... 317 MHz
- high efficiency power amplifier (typically 10 dBm)
- low supply current
- voltage supply range 2.1 ... 4 V
- temperature range –40 ... +125°C
- power down mode
- crystal oscillator 9.84 MHz
- FSK-switch
- divided clock output for µC
- low external component count

1.3 Application

- Tire pressure monitoring systems
- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Table 1 Order information

Type	Ordering Code	Package
TDK5111F	SP000056181	PG-TSSOP-10
available on tape and reel		

2 Functional Description

2.1 Pin Configuration

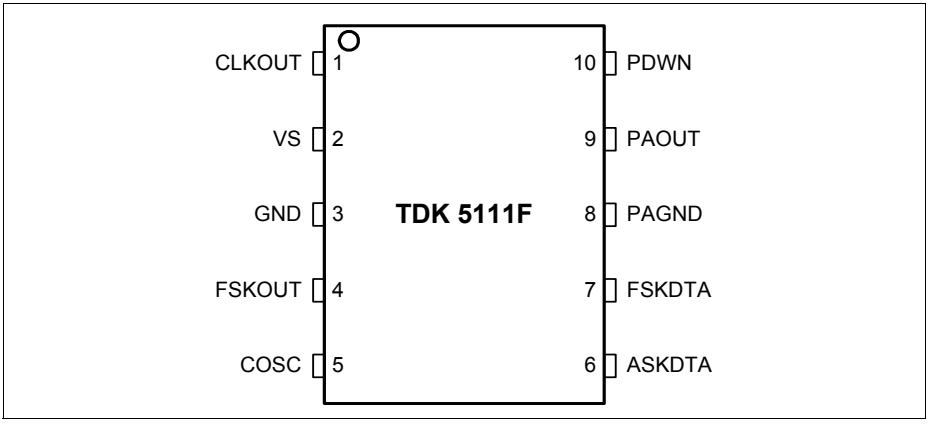


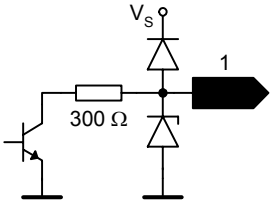
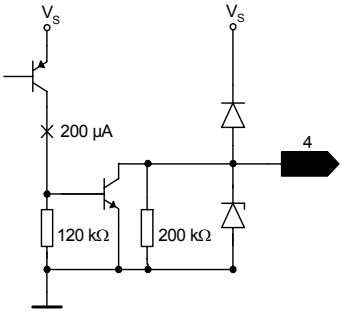
Figure 1 IC Pin Configuration

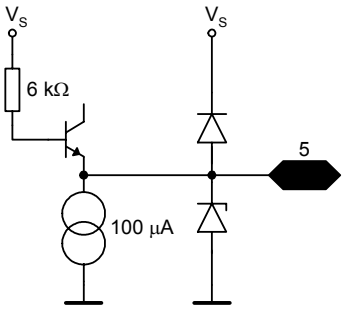
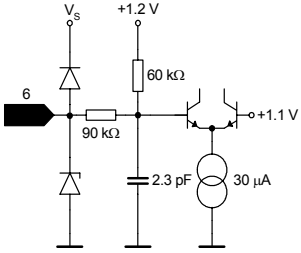
2.2 Pin Definition and Functions

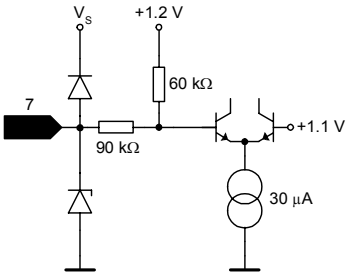
Table 2 Pin Definition and Functions - Overview

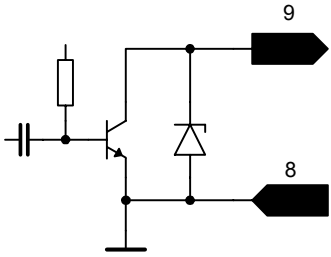
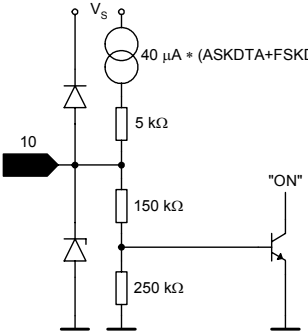
Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (615.2 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	FSKOUT	Frequency Shift Keying Switch Output
5	COSC	Crystal Oscillator Input (9.84 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (315 MHz)
10	PDWN	Power Down Mode Control

Table 3 Pin Definition and Function[1]

Pin No.	Symbol	Interface Schematic	Function
1	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock frequency is 615.2 kHz.
2	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND		General ground connection.
4	FSKOUT		This pin is connected to a switch to GND (pin 3). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.

Pin No.	Symbol	Interface Schematic	Function
5	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
6	ASKDTA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.

Pin No.	Symbol	Interface Schematic	Function
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 4) to GND (pin 3). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.

Pin No.	Symbol	Interface Schematic	Function
8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by either setting FSKDTA or ASKDTA to a logic high-state.

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode.
In Power Down Mode, the values are zero or high-ohmic.

2.3 Functional Block Diagram

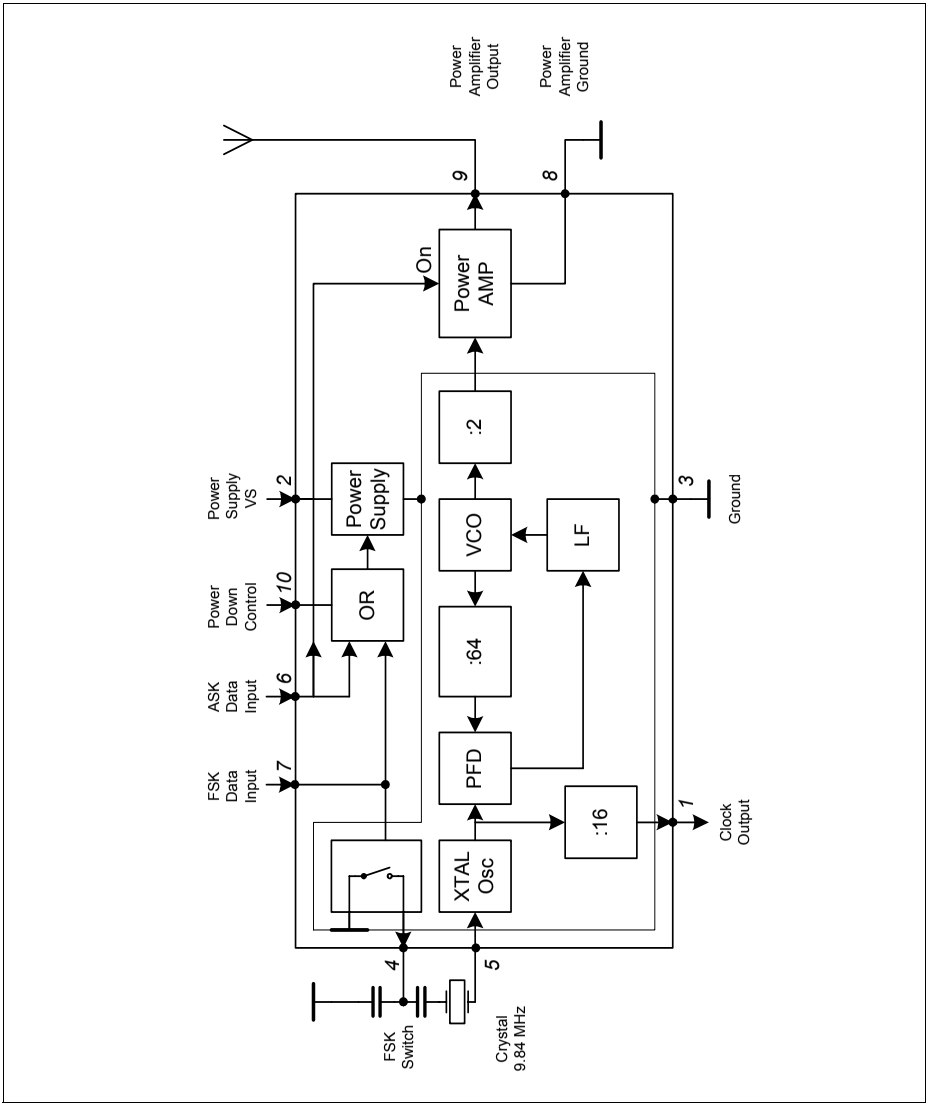


Figure 2 Functional Block Diagram

2.4 Functional Block Description

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 630MHz. The oscillator signal is fed both, to the synthesizer divider chain and (via a 1:2 divider) to the power amplifier. The overall division ratio of the asynchronous synthesizer divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates at 9.84 MHz.

The crystal frequency is divided by 16. The resulting 615.2 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 4).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 4 FSKDTA - FSK Switch

FSKDTA (pin7)	FSK Switch
Low[1)]	CLOSED
Open[2)], High[3)]	OPEN

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off by the signal at ASKDTA (pin 6).

Table 5 ASKDTA - Power Amplifier

ASKDTA (pin6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

2.4.4 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.4.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

2.4.4.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The settling time of the PLL is determined mainly by the turn on time of the crystal oscillator and is in the range of 1 msec depending on the used crystal.

The current consumption is typically 4mA.

2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 14 mA when using a proper transforming network at PAOUT, see Figure 8.

2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10).
When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3

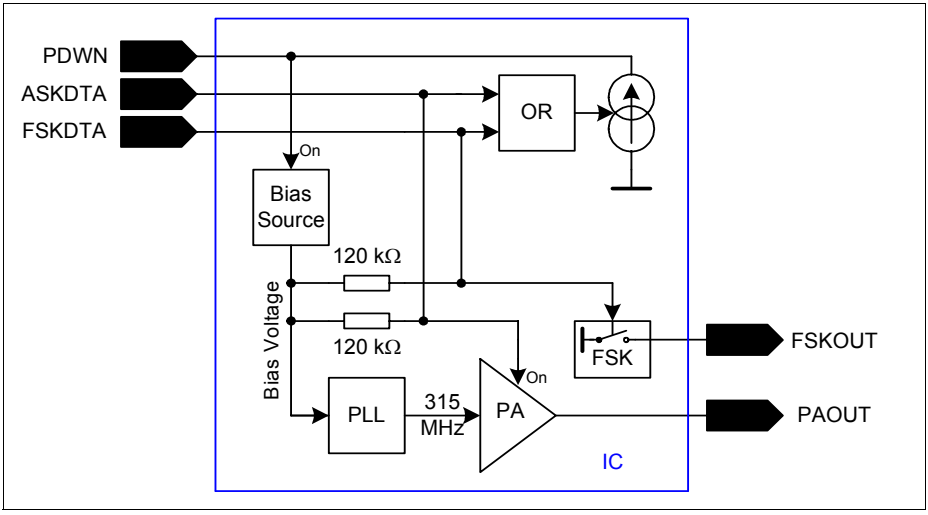


Figure 3 Power mode control circuitry

Table 6 provides a listing of how to get into the different power modes

Table 6 Power Modes

PDWN	FSKDTA	ASKDTA	MODE
Low[1)]	Low, Open	Low, Open	POWER DOWN
Open[2)]	Low	Low	
High[3)]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7V (PDWN)
Voltage at pin < 0.5V (FSKDTA, ASKDTA)

2) Open: Pin open

3) High: Voltage at pin > 1.5V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.5 Recommended Timing Diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

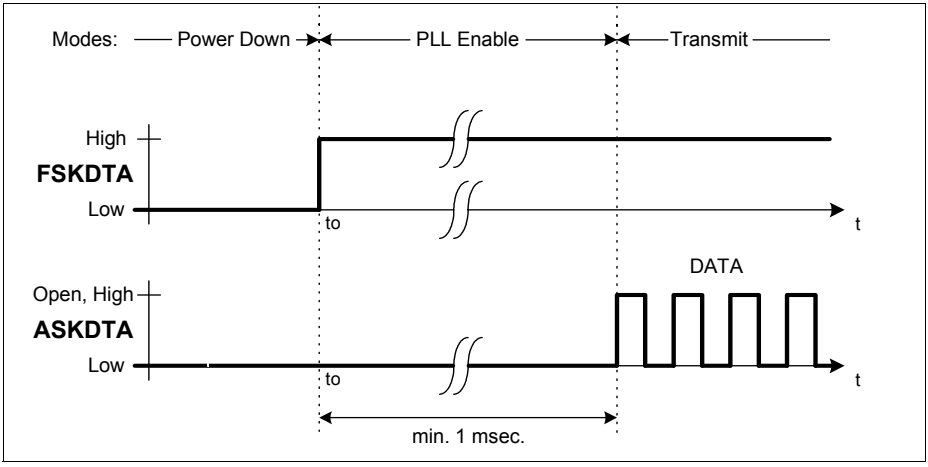


Figure 4 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected.

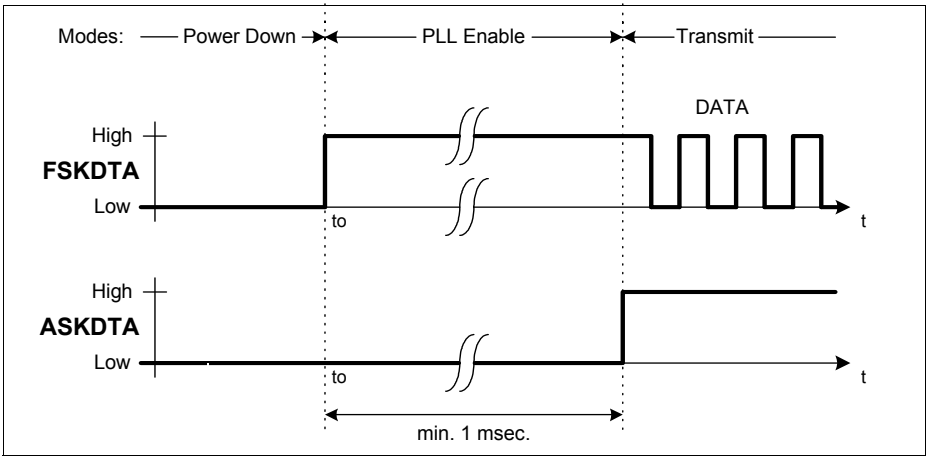


Figure 5 FSK Modulation

In case of FSK Modulation without using PDWN it should be considered, that a too small value of C_2 (referring to Figure 8 and the BOM) could possibly enlarge the start-up time of the oscillator significantly.

Alternative ASK Modulation, FSKDTA not connected.

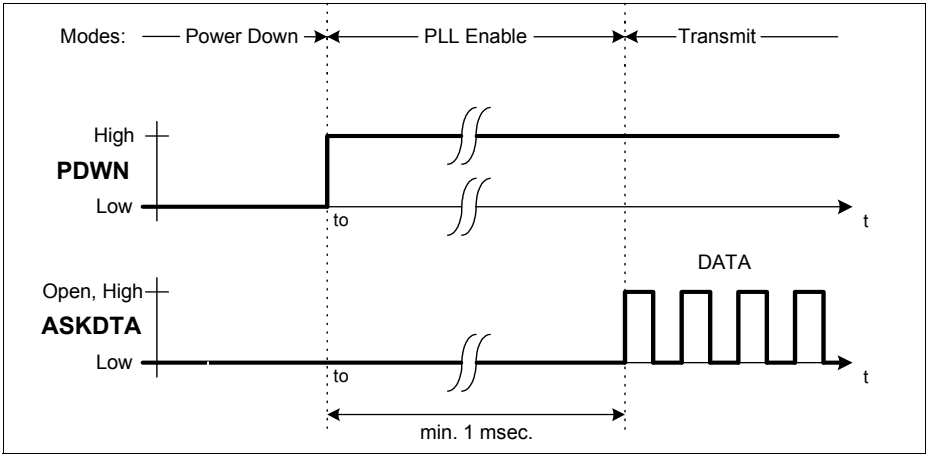


Figure 6 Alternative ASK Modulation

Alternative FSK Modulation

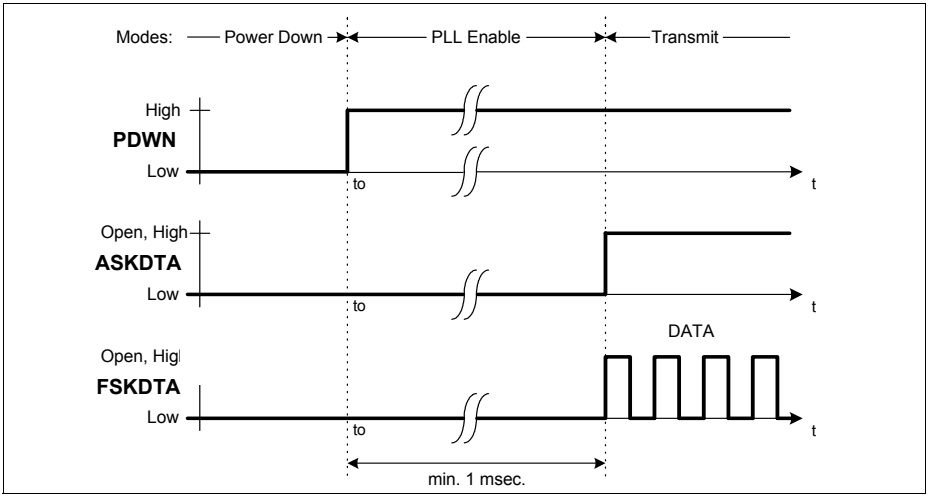


Figure 7 Alternative FSK Modulation

3 Applications

3.1 50 Ohm-Output Testboard Schematic

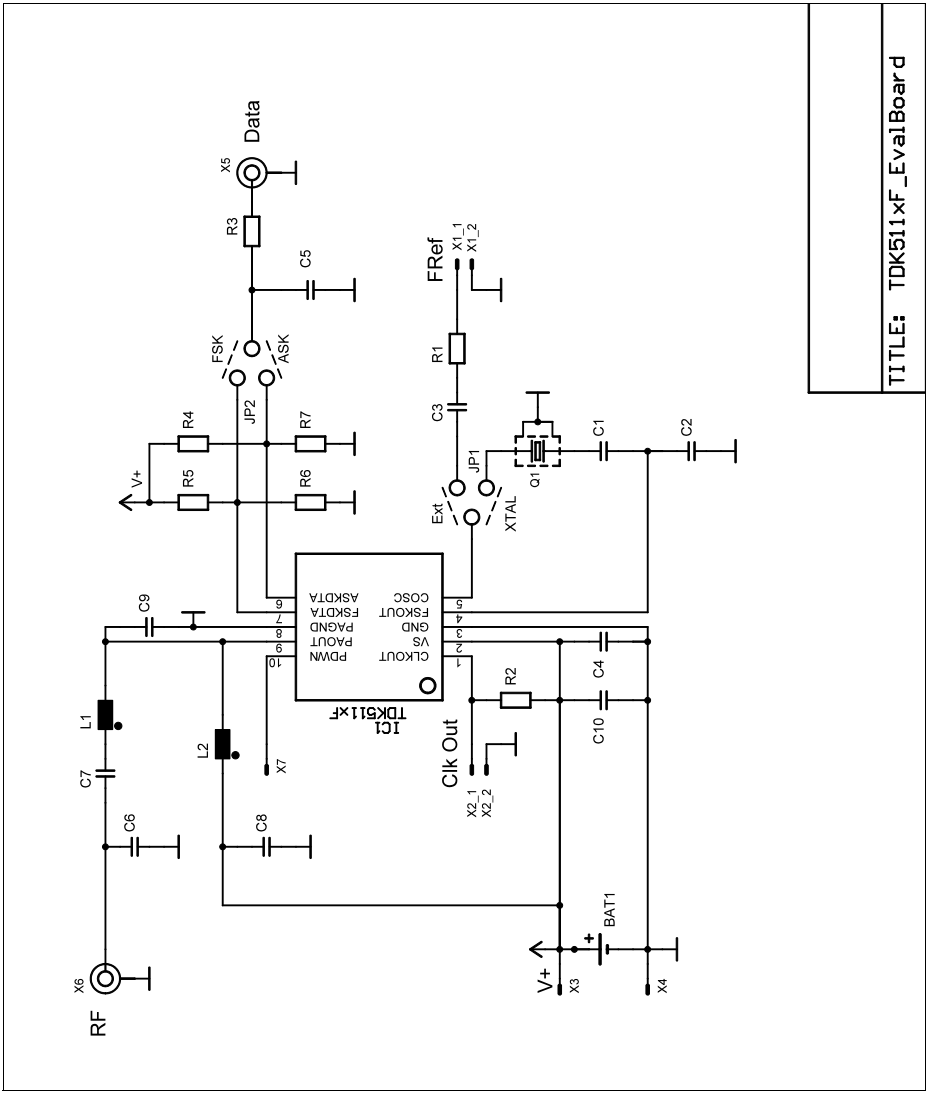


Figure 8 50 Ohm-output testboard schematic

3.2 50 Ohm-Output Testboard Layout

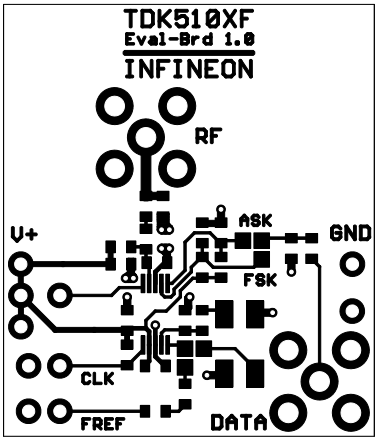


Figure 9 Top Side of TDK5111 F-Testboard with 50 Ohm-Output

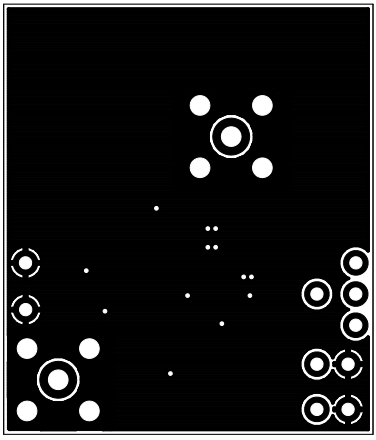


Figure 10 Bottom Side of TDK5111 F-Testboard with 50 Ohm-Output

3.3 Bill of Material (50 Ohm-Output Evalboard)

Reference	Value	Specification
R1	open	
R2	open	
R3	4k7	0603, +/-5%
R4	12k	0603, +/-5%
R5	open	
R6	15k	0603, +/-5%
R7	open	
C1	15p	0603, C0G, +/-0,1p
C2	6p8	0603, C0G, +/-1%
C3	open	
C4	open	
C5	100p	0603, X7R, +/-10%
C6	12p	0603, C0G, +/-1%
C7	100p	0603, C0G, +/-1%
C8	1n	0603, C0G, +/-5%
C9	6p8	0603, C0G, +/-0,1p
C10	47n	0603, X7R, +/-10%
L1	56n	EPCOS SIMID 0603-C, +/-2%
L2	100n	EPCOS SIMID 0603-C, +/-2%
X1	n.e.	
X2	n.e.	
X3	Pin	single-pole connector, 2,54mm
X4	Pin	single-pole connector, 2,54mm
X5	SMA-connector	
X6	SMA-connector	
X7	n.e.	
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	9843.75 kHz, CL=12pF	Tokyo Denpa TSS-3B 9843.75 kHz Spec.No. 1053-921
IC1	TDK5111F	

3.4 Application Hints on the Crystal Oscillator

Application Hints on the crystal oscillator

The crystal oscillator achieves a turn on time in the range of 1 msec depending on the used crystal. To achieve this, a NIC oscillator type is implemented in the TDK 5111 F. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.

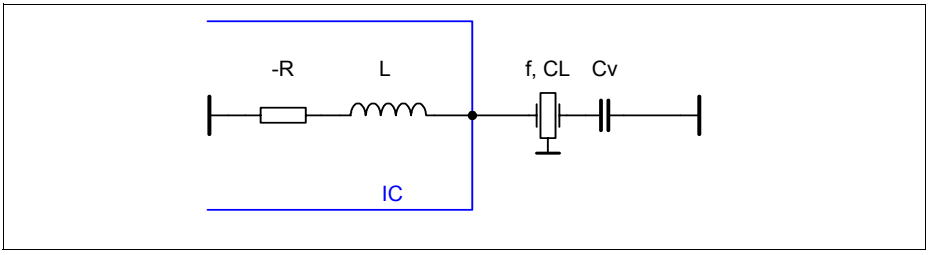


Figure 11 Application Hints

Formula 1:

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L}$$

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

Example for the ASK-Mode:

Referring to the application circuit, in ASK-Mode the capacitance C2 is replaced by a short to ground. Assume a crystal frequency of 9.84 MHz and a crystal load capacitance of CL = 12 pF. The inductance L at 9.84 MHz is about 4.6 µH. Therefore C1 is calculated to 10 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C1$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.

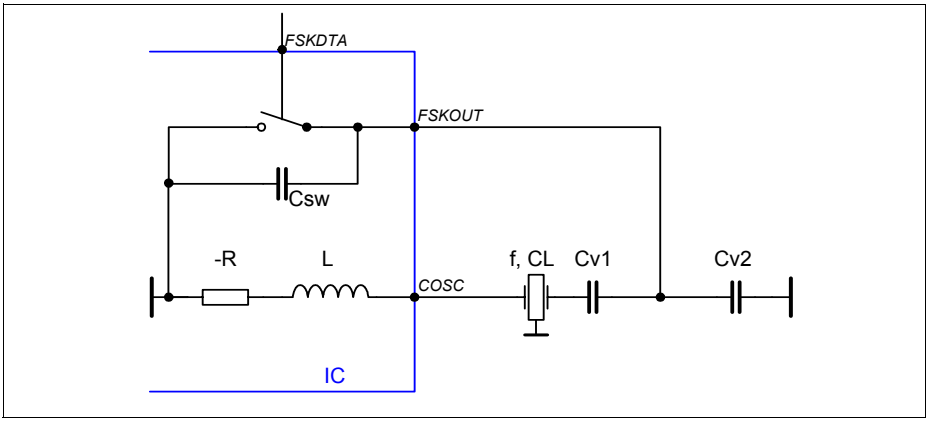


Figure 12 FSK Mode

The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small frequency deviations (up to +/- 400 ppm), the two desired load capacitances can be calculated with the formula below.

$$CL\pm = \frac{CL \mp C0\frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}{1\pm\frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}$$

C_L: crystal load capacitance for nominal frequency

C_0: shunt capacitance of the crystal

f: frequency

ω: $\omega = 2\pi f$: angular frequency

N: division ratio of the PLL

df: peak frequency deviation

Because of the inductive part of the TDK 5111 F, these values must be corrected by Formula 1 on the preceding page. The value of Cv± can be calculated.

$$Cv\pm = \frac{1}{\frac{1}{CL\pm} + \omega^2 L}$$

If the FSK switch is closed, Cv± is equal to Cv1 (C1 in the application diagram). If the FSK switch is open, Cv2 (C2 in the application diagram) can be calculated.

$$Cv2 = C2 = \frac{Csw * Cv1 - (Cv+) * (Cv1 + Csw)}{(Cv+) - Cv1}$$

Csw: parallel capacitance of the FSK switch (3 pF incl. layout parasitics)

Remark: These calculations are only approximations. The necessary values depend on the layout also and must be adapted for the specific application board.

3.5 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 7 Clock Output

fCLKOUT=615.2 kHz	
CL[pF]	RL[kOhm]
5	39
10	18
20	10

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

3.6 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta << \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 13. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.

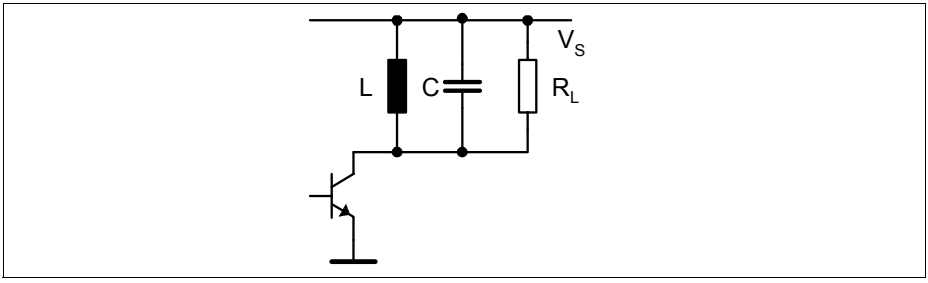


Figure 13 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^2}{2 * P_O}$$

The theoretical value of R_{LC} for an RF output power of P_o= 10dBm (10mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.01} = 450\ \Omega$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S.
The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to $i_C * u_{CE}$ is minimized. This is particularly true for small current flow angles of $\theta << \pi$.