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TDK5111

ASK/FSK Transmitter 315 MHz

Data Sheet

Revision 1.1, 2002-10-31

Wireless Control

Revision History		
Current Version: Version 1.1 as of 31.10.2002		
Previous Version: 1.0 as of March 2002		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
5-4, 5-7	5-4, 5-7	Tolerances of Lcosc specified Value of Iclkout corrected

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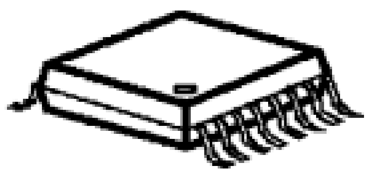
Product Info

General Description

The TDK 5111 is a single chip ASK/FSK transmitter for the frequency band 314-317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additionally features like a power down mode, a low power detect and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- high efficiency power amplifier typically 10 dBm @ 3 V
- frequency range 314-317 MHz
- ASK/FSK modulation
- low supply current typ. 13 mA@3V
- voltage supply range 2.1 - 4 V
- power down mode
- low voltage sensor
- programmable divided clock output for µC
- low external component count

Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDK 5111	Q67100-H2046	P-TSSOP-16
available on tape and reel		

2 Product Description

Contents of this Chapter

2.1 Overview

The TDK 5111 is a single chip ASK/FSK transmitter for the frequency band 314-317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features like a power down mode, a low power detect and a divided clock output are implemented. The IC can be used for both ASK and FSK modulation.

2.2 Applications

- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

2.3 Features

- fully integrated frequency synthesizer
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- power down mode
- low voltage sensor
- programmable divided clock output for µC
- low external component count

2.4 Package Outlines

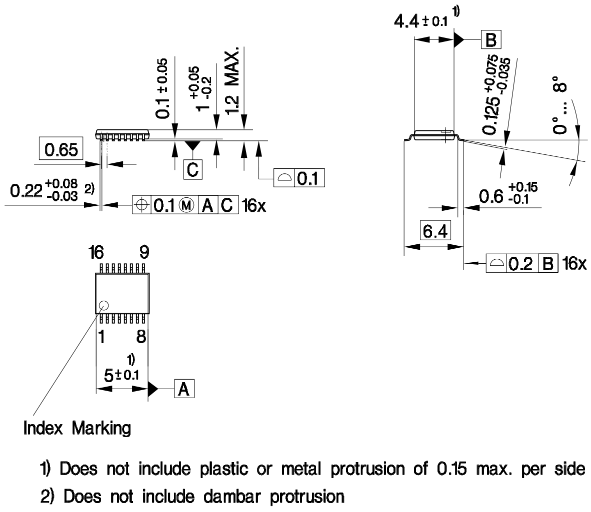
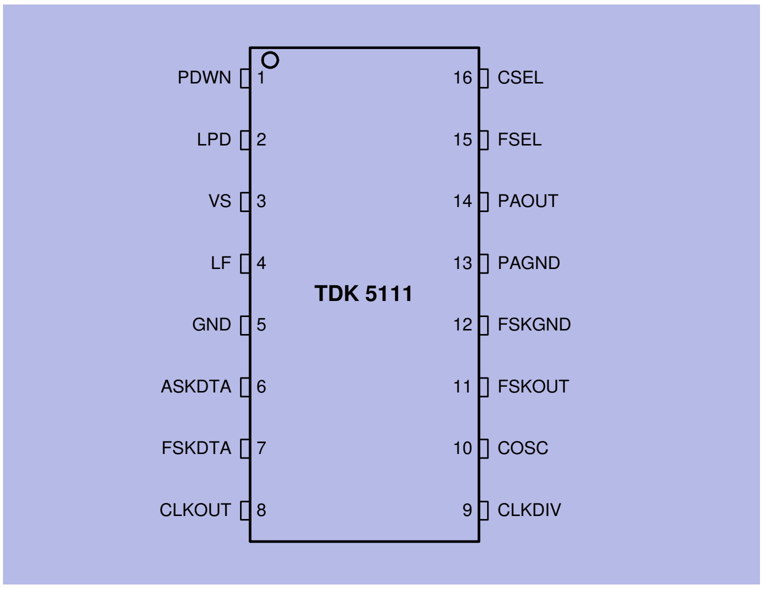


Figure 2-1 P-TSSOP-16

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration



Pin_config.wmf

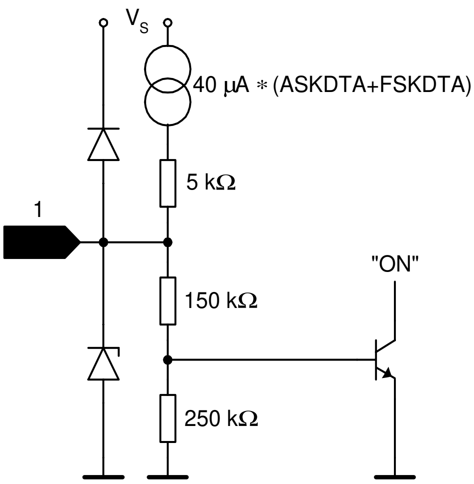
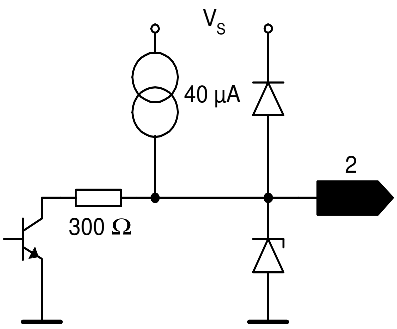
Figure 3-1 IC Pin Configuration

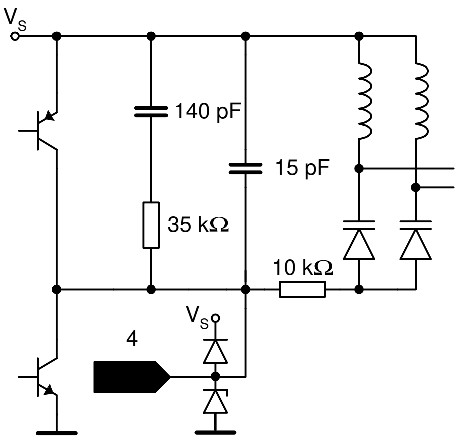
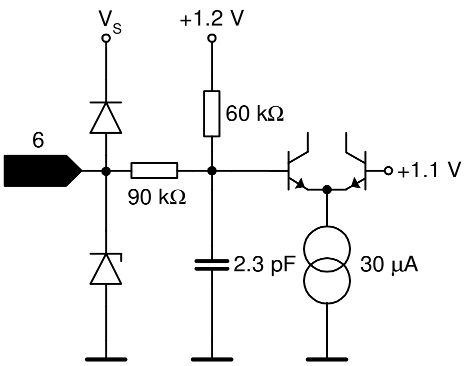
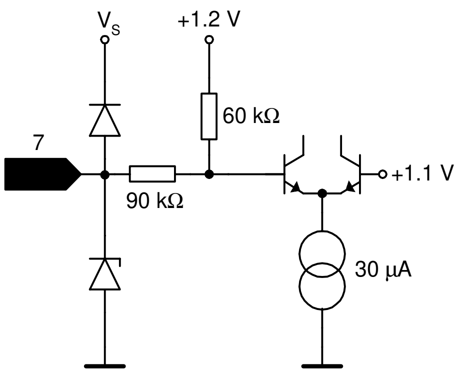
Table 3-1

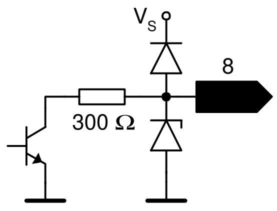
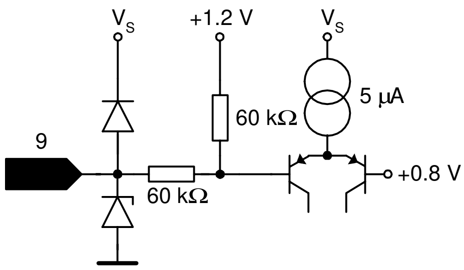
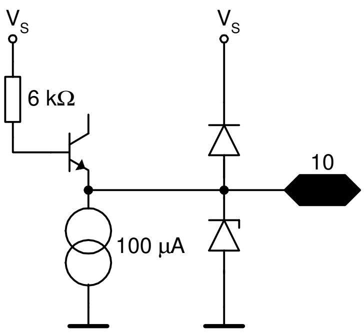
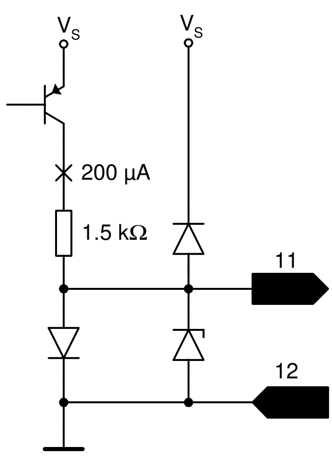
Pin No.	Symbol	Function
1	PDWN	Power Down Mode Control
2	LPD	Low Power Detect Output
3	VS	Voltage Supply
4	LF	Loop Filter
5	GND	Ground
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	CLKOUT	Clock Driver Output
9	CLKDIV	Clock Divider Control
10	COSC	Crystal Oscillator Input
11	FSKOUT	Frequency Shift Keying Switch Output
12	FSKGND	Frequency Shift Keying Ground
13	PAGND	Power Amplifier Ground
14	PAOUT	Power Amplifier Output
15	FSEL	Frequency Range Selection: Has to be shorted to ground for 315 MHz operation
16	CSEL	Crystal Frequency Selection: Has to be left open

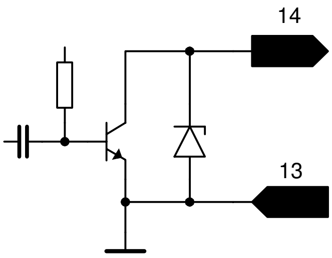
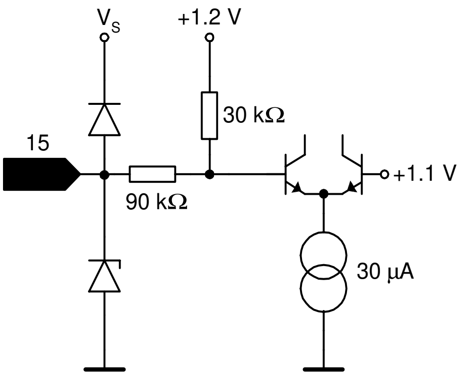
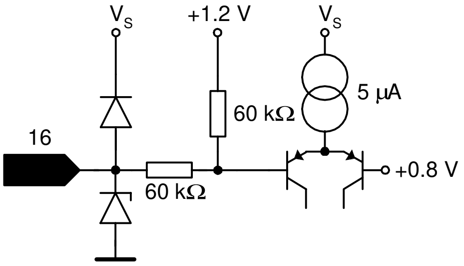
3.2 Pin Definitions and Functions

Table 3-2

Pin No.	Symbol	Interface Schematic[1)]	Function
1	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by setting FSKDTA or ASKDTA to a logic high-state.
2	LPD		This pin provides an output indicating the low-voltage state of the supply voltage VS. VS < 2.15 V will set LPD to the low-state. An internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.
3	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 5) as short as possible.

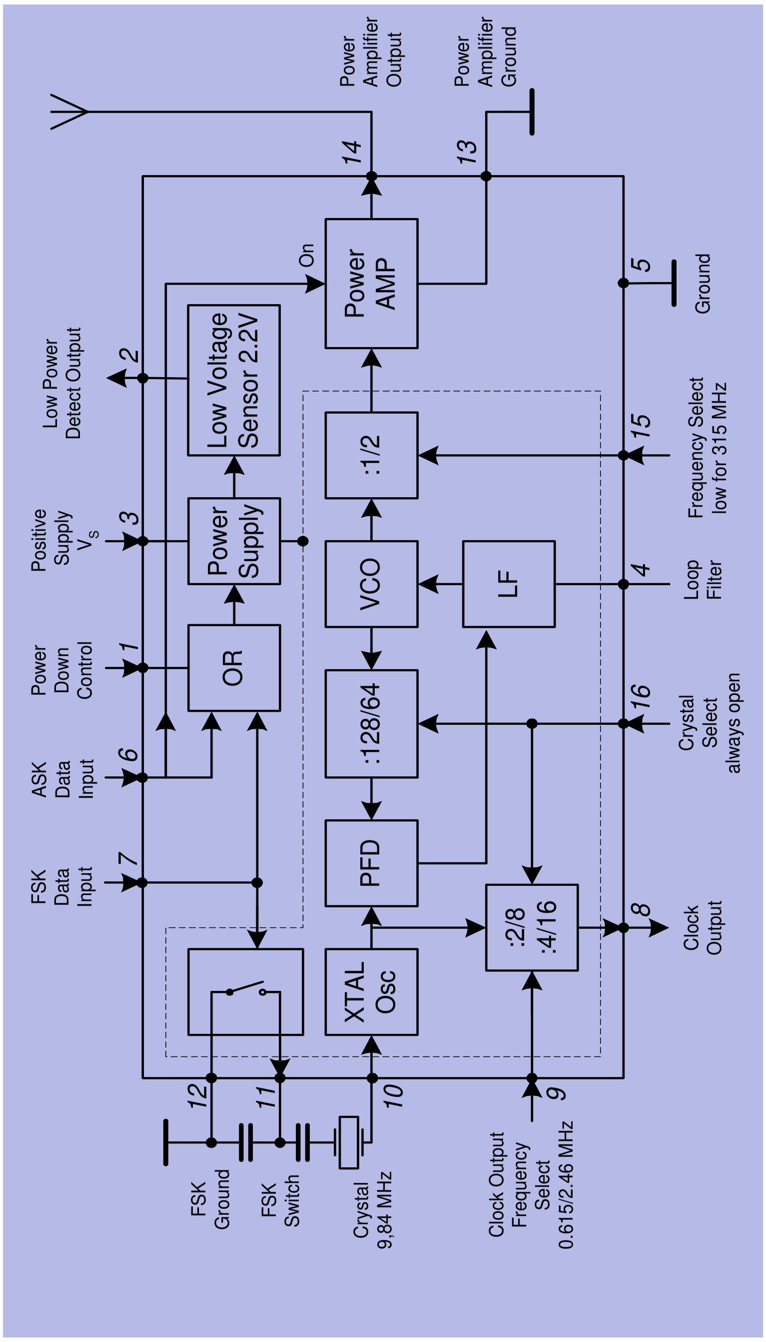
4	LF		Output of the charge pump and input of the VCO control voltage. The loop bandwidth of the PLL is 150 kHz when only the internal loop filter is used. The loop bandwidth may be reduced by applying an external RC network referencing to the positive supply VS (pin 3).
5	GND		General ground connection.
6	ASKDTA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 11) to FSKGND (pin 12). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.

8	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. A clock frequency of 2.46 MHz is selected by a logic low at CLKDIV input (pin 9). A clock frequency of 615 kHz is selected by a logic high at CLKDIV input (pin 9).
9	CLKDIV		This pin is used to select the desired clock division rate for the CLKOUT signal. A logic low (CLKDIV < 0.2 V) applied to this pin selects the 2.46 MHz output signal at CLKOUT (pin 8). A logic high (CLKDIV open) applied to this pin selects the 615 kHz output signal at CLKOUT (pin 8).
10	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
11	FSKOUT		This pin is connected to a switch to FSKGND (pin 12). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.
12	FSKGND		Ground connection for FSK modulation output FSKOUT.

13	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 14) has to be concentrated to this pin.
14	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching net-work.
15	FSEL		**This pin has to be shorted to ground to select the 315 MHz transmitter frequency range.** A logic low (FSEL < 0.5 V) applied to this pin sets the transmitter to the 315 MHz fre-quency range. A logic high (FSEL open) applied to this pin sets the transmitter to the 630 MHz fre-quency range.
16	CSEL		This pin is used to select the desired refer-ence frequency. A logic high (CSEL open) applied to this pin sets the internal frequency divider to accept a reference frequency of 9.84 MHz.

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode. In Power Down Mode, the values are zero or high-ohmic.

3.3 Functional Block diagram



Funct_Block_Diagram.wmf

Figure 3-2 Functional Block diagram

3.4 Functional Blocks

3.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 630 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip. In all 315 MHz applications, the CSEL pin is not connected (logic high).

3.4.2 Crystal Oscillator

The crystal oscillator operates at 9.84 MHz. Frequencies of 615 kHz or 2.46 MHz are available at the clock output CLKOUT (pin 8) to drive the clock input of a micro controller.

The frequency at CLKOUT (pin 8) is controlled by the signal at CLKDIV (pin 9)

Table 3-3

CLKDIV (pin 9)	CLKOUT Frequency
Low[1]	2.46 MHz
Open[2]	615 kHz

1) Low: Voltage at pin < 0.2 V
2) Open: Pin open

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 11).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 3-4

FSKDTA (pin7)	FSK Switch
Low[1]	CLOSED
Open[2], High[3]	OPEN

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

3.4.3 Power Amplifier

For operation at 315 MHz, the power amplifier is fed with the VCO frequency divided by 2. It is possible to feed the power amplifier directly from the voltage controlled oscillator. This is controlled by FSEL (pin 15) as described in the table below. This is not recommended for this frequency range.

Table 3-5

FSEL (pin 15)	Radiated Frequency Band
Low[1)]	315 MHz
Open[2)]	630 MHz (not recommended)

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open

The Power Amplifier can be switched on and off
by the signal at ASKDTA (pin 6).

Table 3-6

ASKDTA (pin 6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 14) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 14) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 13) in order to reduce the amount of coupling to the other circuits.
In all 315 MHz applications, the pin FSEL is connected to ground.

3.4.4 Low Power Detect

The supply voltage is sensed by a low power detector. When the supply voltage drops below 2.15 V, the output LPD (pin 2) switches to the low-state. To minimize the external component count, an internal pull-up current of 40 µA gives the output a high-state at supply voltages above 2.15 V.

The output LPD (pin 2) can either be connected to ASKDTA (pin 6) to switch off the PA as soon as the supply voltage drops below 2.15 V or it can be used to inform a micro-controller to stop the transmission after the current data packet.

3.4.5 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

3.4.5.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.25 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

3.4.5.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 4 mA.

3.4.5.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

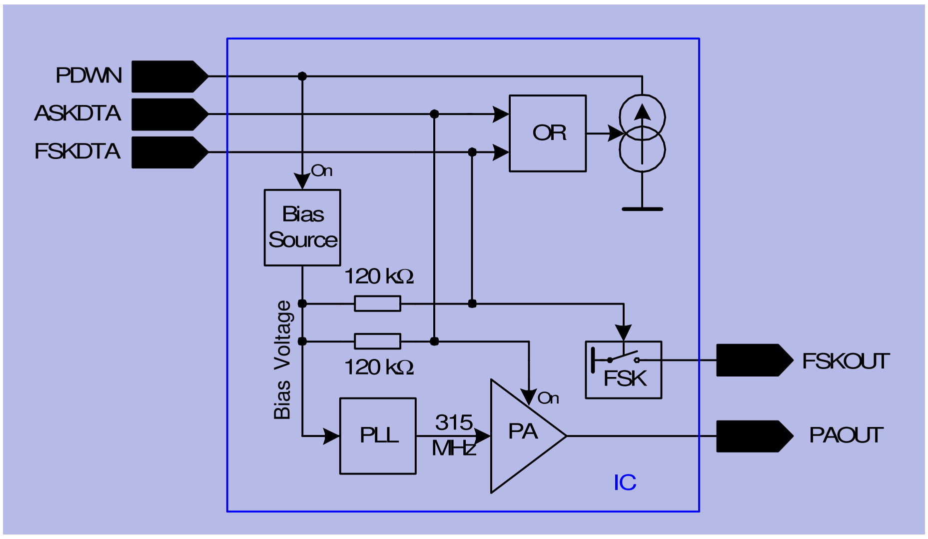
The current consumption of the IC is typically 13 mA when using a proper transforming network at PAOUT, see Figure 4-1.

3.4.5.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin 1). When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 3-5.



Power_Mode.wmf

Figure 3-5 Power mode control circuitry

Table 3-7 provides a listing of how to get into the different power modes

Table 3-7

PDWN	FSKDTA	ASKDTA	MODE
Low1)	Low, Open	Low, Open	POWER DOWN
Open2)	Low	Low	
High3)	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7 V (PDWN)
Voltage at pin < 0.5 V (FSKDTA, ASKDTA)
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

3.4.6 Recommended timing diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

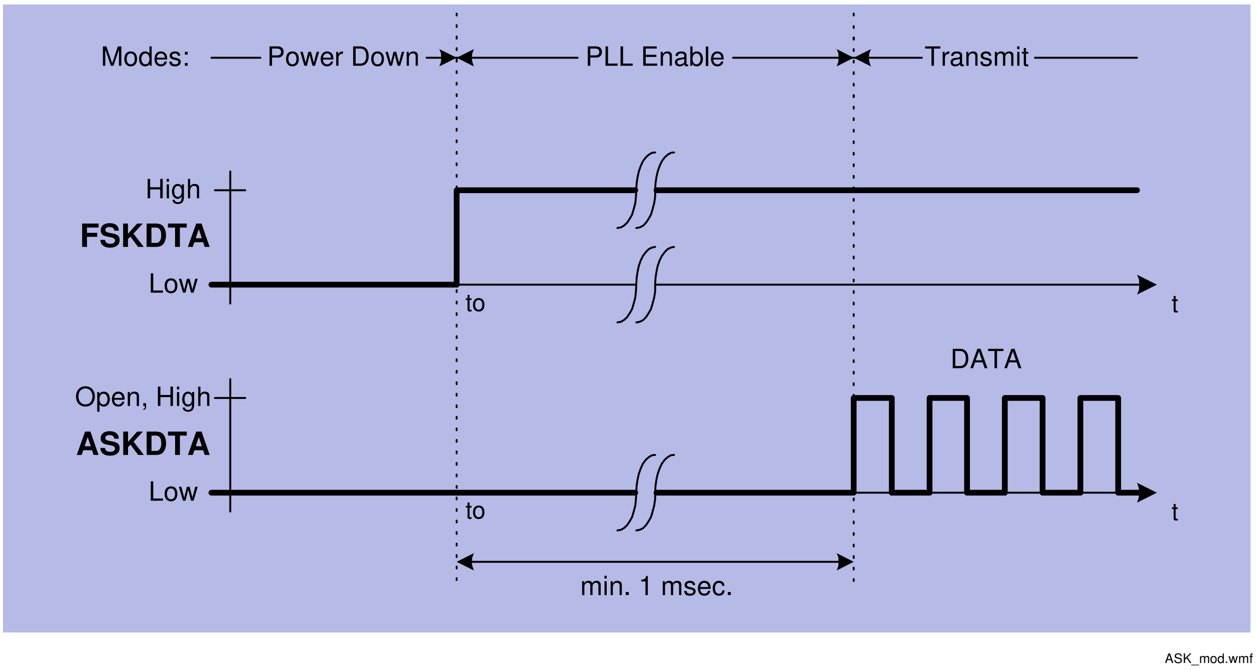


Figure 3-6 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected

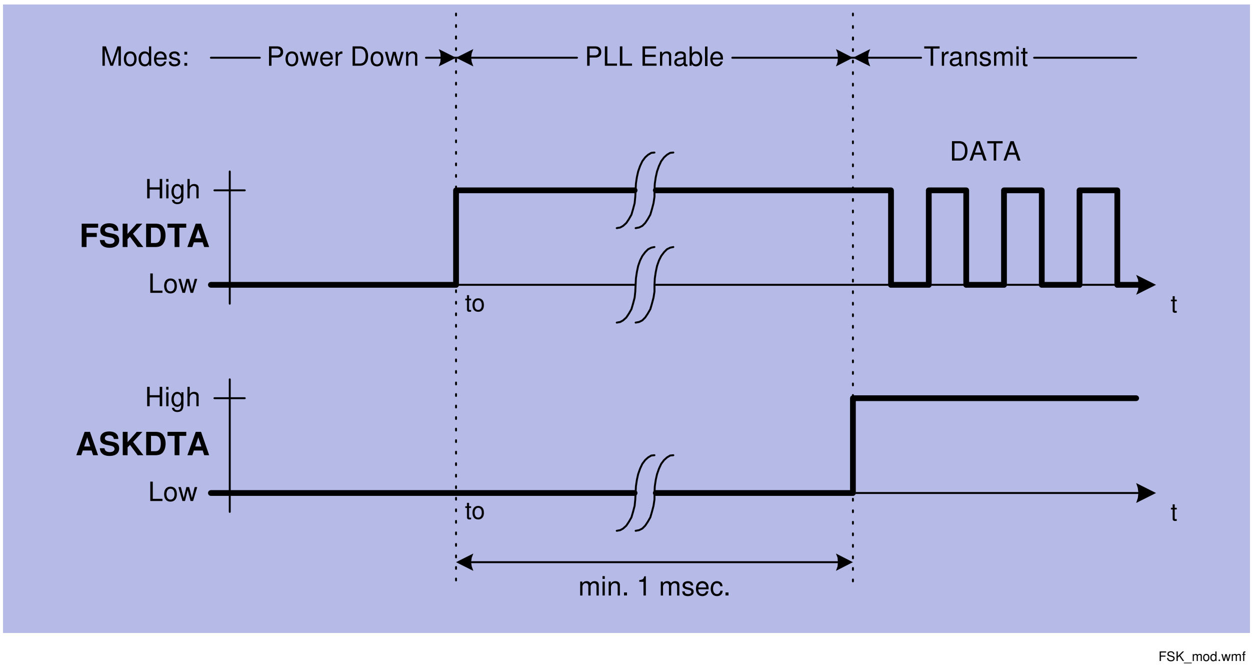


Figure 3-7 FSK Modulation

Alternative ASK Modulation, FSKDTA not connected.

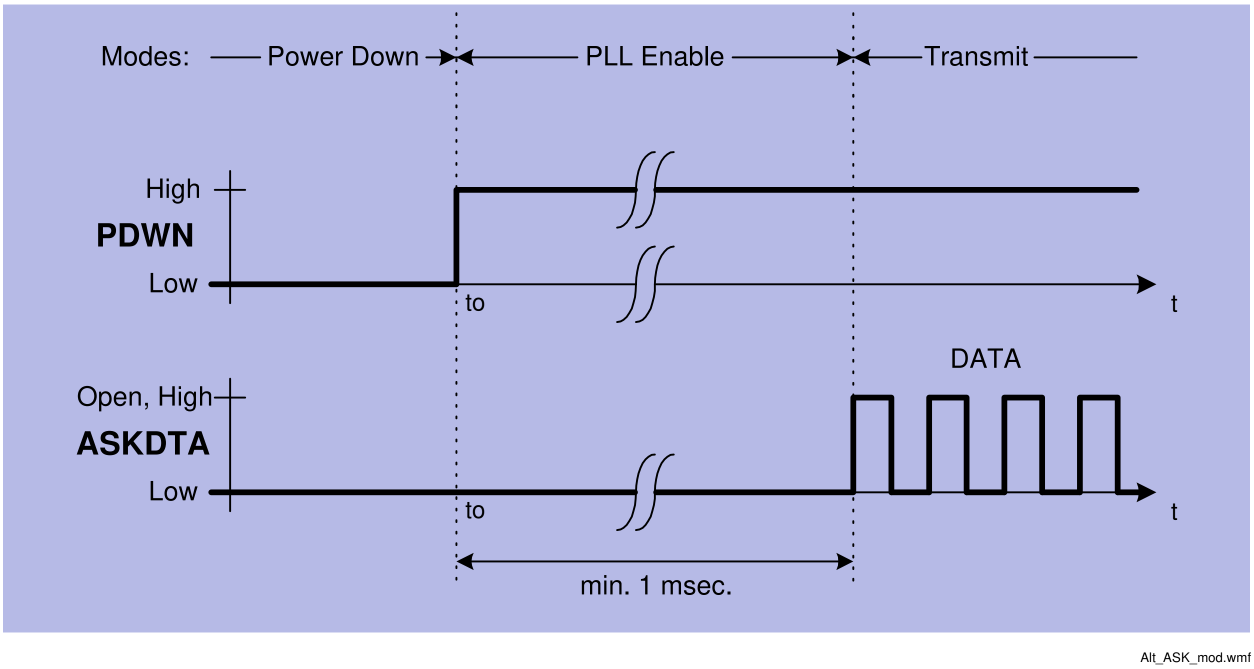


Figure 3-8 Alternative ASK Modulation

Alternative FSK Modulation

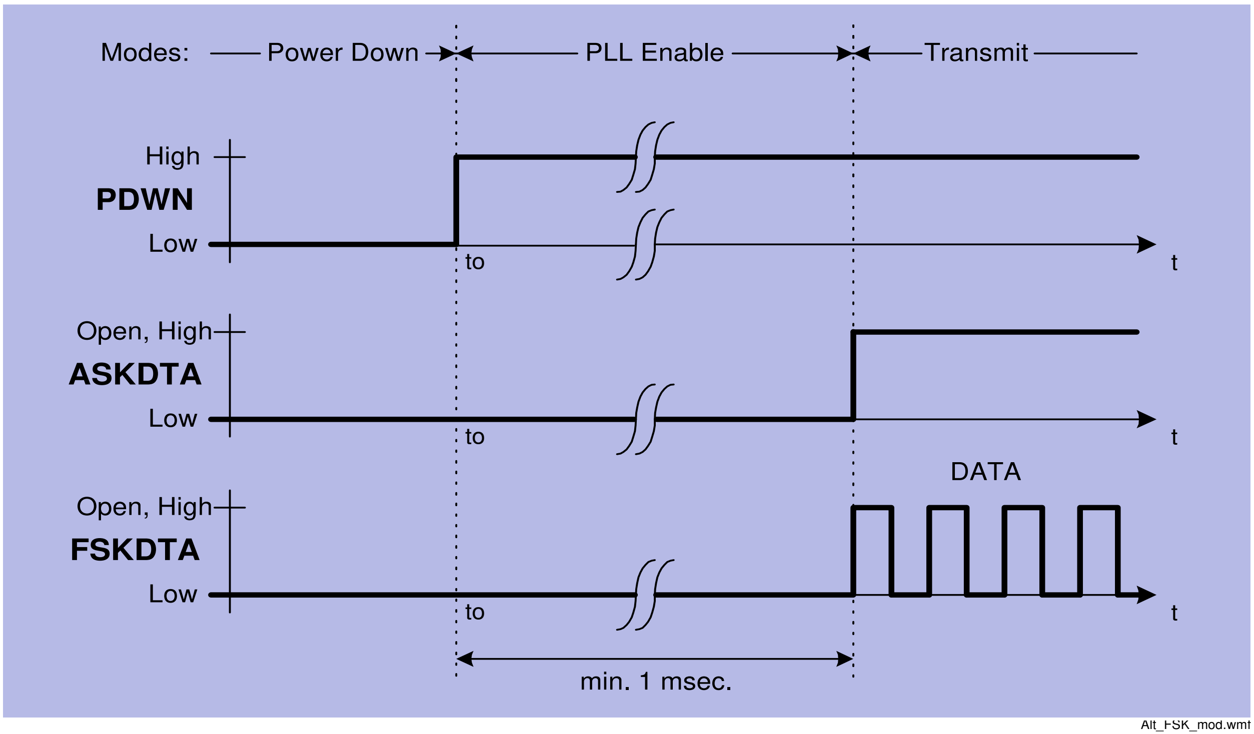
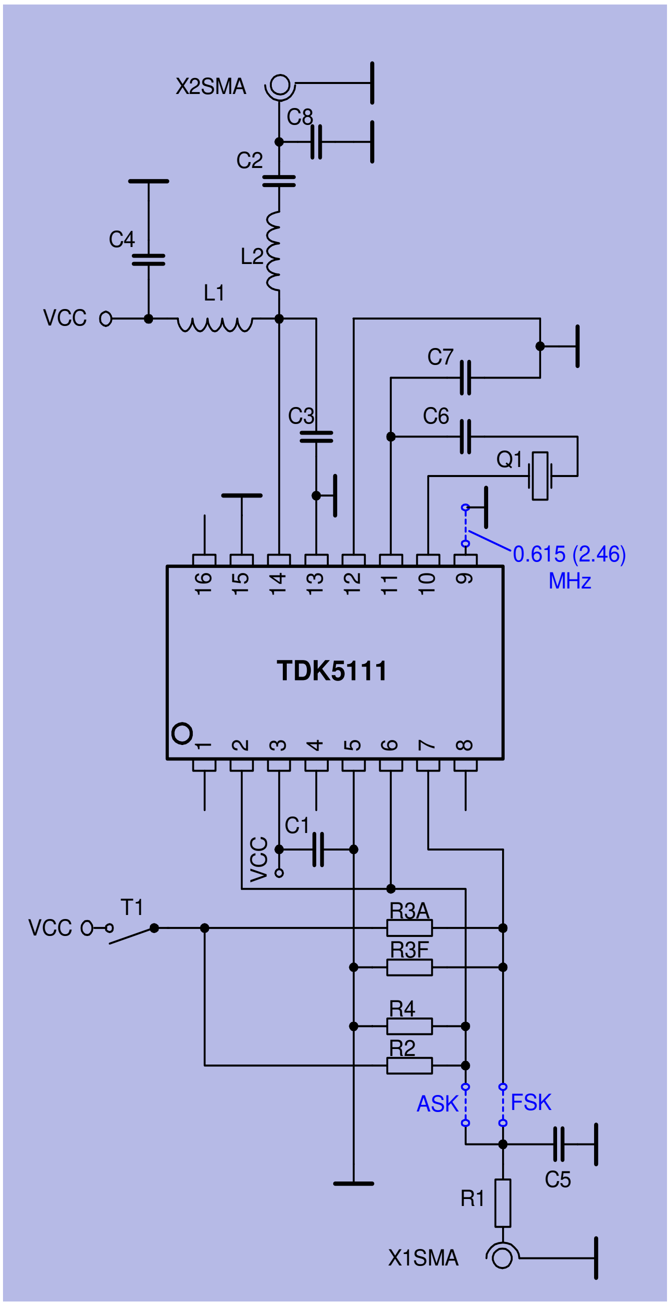


Figure 3-9 Alternative FSK Modulation

4 Applications

Contents of this Chapter

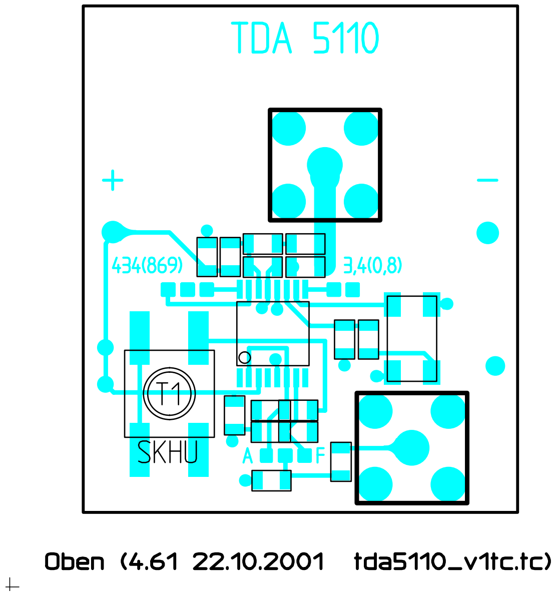
4.1 50 Ohm-Output Testboard: Schematic



50ohm_test_v5.wmf

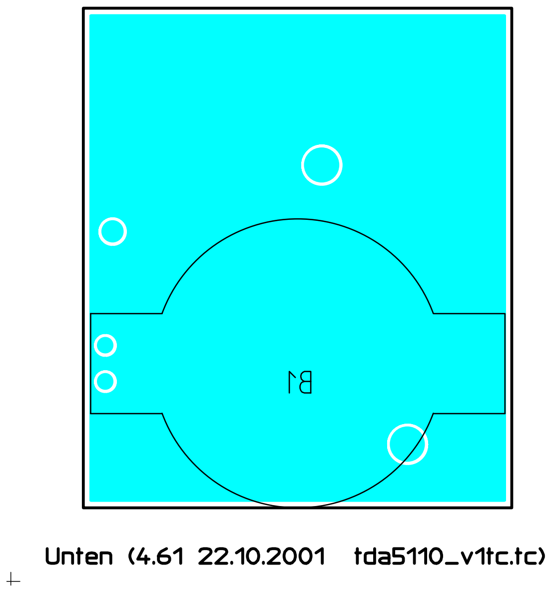
Figure 4-1 50 Ω-Output testboard schematic

4.2 50 Ohm-Output Testboard: Layout



tda5110_v1_pcboben.pdf

Figure 4-2 Top Side of TDK 5111-Testboard with 50 Ω-Output.
It is the same board as used for the TDK5110.



tda5110_v1_pcbunten.pdf

Figure 4-3 Bottom Side of TDK 5111-Testboard with 50 Ω-Output.
It is the same board as used for the TDK5110.

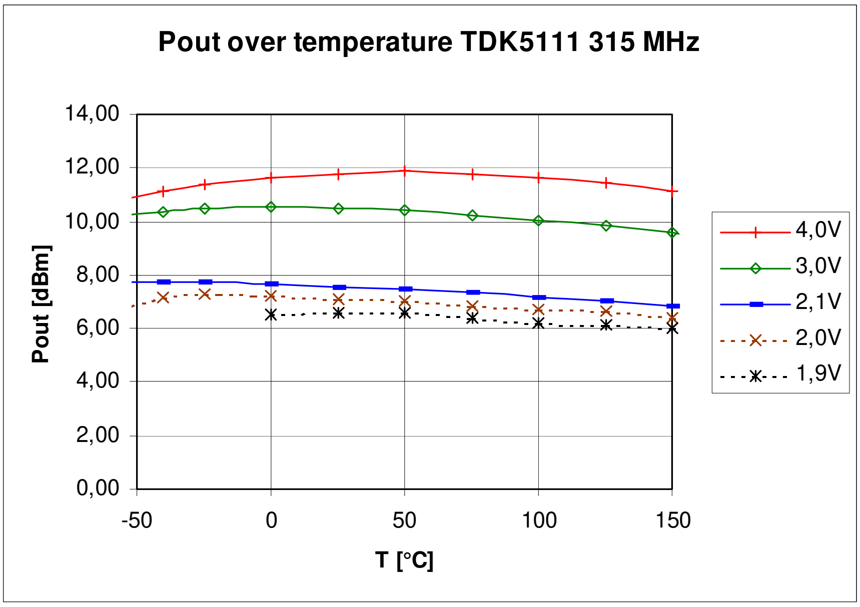
4.3 50 Ohm-Output Testboard: Bill of material

Table 4-1 Bill of material

Part	Value	ASK	FSK	Specification
R1	4.7kΩ			0805, ± 5%
R2			12kΩ	0805, ± 5%
R3A		15kΩ		0805, ± 5%
R3F			15kΩ	0805, ± 5%
R4	open			0805, ± 5%
C1	47nF			0805, X7R, ± 10%
C2	47pF			0805, COG, ± 5%
C3	10pF			0805, COG, ± 1%
C4	330pF			0805, COG, ± 5%
C5	1nF			0805, X7R, ± 10%
C6		8.2pF	15pF	15pF: 0805, COG, ± 1% 8.2pF: 0805, COG, ± 0.1pF
C7		0Ω Jumper	6.8pF	0805, COG, ± 0.1pF 0805, 0Ω Jumper
C8	22pF			0805, COG, ± 5%
L1	120nH			TOKO LL2012-J
L2	33nH			TOKO LL2012-J
Q1	9843.75 kHz, CL=12pF			Tokyo Denpa TSS-3B 9843.75 kHz Spec.No. 10-50221
IC1	TDK5111			
T1	Push-button			replaced by a short
X1	SMA-S			SMA standing
X2	SMA-S			SMA standing

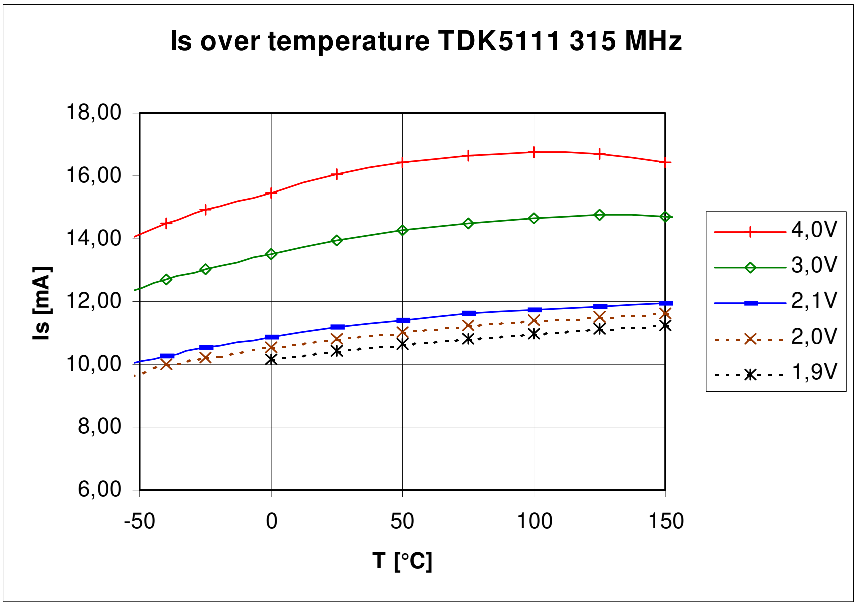
4.4 50 Ohm-Output Testboard: Measurement results

Note the specified operating range: 2.1 V to 4.0 V and –40°C to +125°C.



Pout_over_Temp_315.wmf

Figure 4-4 Pout over Temperature of the 50Ω-testboard with TDK5111 at 315 MHz

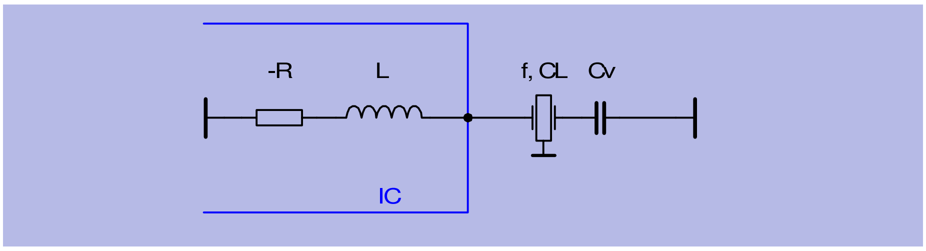


is_over_temp_315.wmf

Figure 4-5 Is over temperature of the 50Ω-testboard with TDK5111 at 315 MHz

4.5 Application Hints on the Crystal Oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TDK 5111. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} \qquad (1)$$

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

Example for the ASK-Mode:

Referring to the application circuit, in ASK-Mode the capacitance C7 is replaced by a short to ground. Assume a crystal frequency of 9.84 MHz and a crystal load capacitance of CL = 12 pF. The inductance L at 9.84 MHz is about 4.4 µH. Therefore C6 is calculated to 10 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C6$$