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Trenz Electronic GmbH info@trenz-electronic.de www.trenz-electronic.de Spartan-3E FPGA Industrial Micromodule

User Manual

Features

- High-density plug-in Xilinx Spartan-3E module
- **USB 2.0** interface with high speed (480 Mbit/s) data rate
- Large SPI flash for configuration and user storage accessible via USB or SPI connector
- Large **DDR-SDRAM**
- FPGA configuration is implemented via JTAG, SPI Flash or USB
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters (1 A for each voltage rail: 1.2 V, 2.5 V, 3.3 V)
- Power supply via USB or B2B (carrier board)
- Flexible expansion via high-density shockproof B2B (board-to-board) connectors
- Most I/O's on the B2B connectors are routed as LVDS pairs
- Evenly spread supply pins for good signal integrity

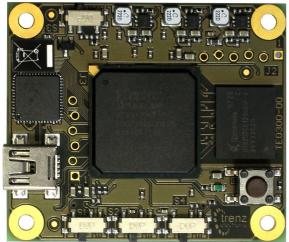


Figure 2: TE0300: top view.

- Industrial temperature grade available on request
- Low-cost, versatile and ruggedized design

Specifications

- FPGA: Xilinx Spartan-3E XC3S500E XC3S1600E
- USB controller: Cypress EZ-USB FX2 USB 2.0 microcontroller CY7C68013A-56LFX
- Non volatile memory: 16 MBit 64 Mbit SPI Flash for FPGA-configuration and user data
- Volatile memory: 512 Mbit x 16 DDR SDRAM with up to 666 Mbyte/s
- Up to 110 FPGA user I/Os
- Supply voltage range: 4.0 V 5.5 V
- 1 push-button
- 1 LED
- Small size (only 40.5 mm x 47.5 mm)

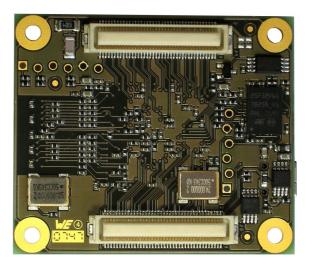


Figure 1: TE0300: bottom view.

Table of Contents

Features	1
Specifications	1
Applications	
Description	3
Physical Features	
Power Supply	
FPGA User I/Os	
User Button and LED	
Configuration Switches	
JTAG and SPI	8
Clock Networks	
On-board Memories	
Module Configuration	
Changes from TE0300-00 to TE0300-01	24
Ordering Information	24
Revision History	
Legal Notices.	25
Environmental protection	
Appendix	

Applications

- IP (intellectual property) development
- Digital signal processing
- Image processing
- Cryptography
- Industrial control
- Low-power design
- General-purpose prototyping platform

Description

The FPGA industrial micromodule integrates a leading edge Xilinx Spartan-3E FPGA, an USB 2.0 microcontroller, configuration Flash, DDR SDRAM and power supplies on a tiny footprint. A large number of configurable I/Os are provided via B2B mini-connectors.

The module is intended to be used as an OEM board, or to be combined with our carrier boards. It is a powerful system widely used for educational and research activities.

Boards with other configurations, larger FPGA's or equipped with industrial temperature grade parts are available on request.

Software for SPI flash programming over USB as well as reference designs for high speed data transfer over USB are included.

Physical Features

Board Dimensions

The module measures 40.50 mm by 47.50 mm.

Board-to-Board Connectors

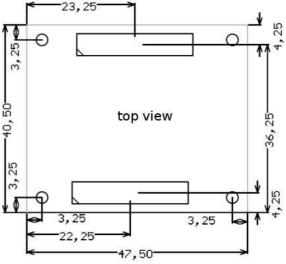


Figure 3: module dimensions in mm (top view).

The module has two B2B (board-to-board) receptacle connectors (J4 and J5) for a total of 160 contacts (Figure 5).



Figure 5: micromodule receptacle.

The ordering numbers of the connector receptacles are given in Table 1.

supplier	header	
Digikey	H11113CT-ND H11113TR-ND H11113DKR-ND	
Hirose	DF17(3.0)-80DS-0.5V(57)	
Trenz Electronic	22684	

Table 1: equivalent part numbers ofthe receptacle connectors J4 and J5.

The on-board receptacles mate with their corresponding headers on the carrier board (Figure 6).



P. OF Header

Figure 7: stacking height (h).

The stacking height of the TE0300 B2B connectors is 7 (seven) mm. The stacking height does not include the solder paste thickness.

USB Connector

The micromodule uses a mini-USB (B type) receptacle connector.



Figure 6: mating header.

The ordering number of the headers is given in Table 2.

supplier	header	
Digikey	H11148DKR-ND H11148TR-ND	
	H11148CT-ND	
Hirose	DF17(4.0)-80DP-0.5V(57)	
Trenz Electronic	22938	

Table 2: equivalent part numbers ofthe mating connectors.

Figure 7 shows the definition of stacking height featured by the combination of the TE0300 receptacle with its corresponding header.

Figure 8: mini-USB (B type) receptacle connector.

Power Supply

The module can be powered by the B2B connector or the USB connector. If both power supplies are available, the B2B connector power supply takes precedence, disabling the USB power supply automatically.

B2B Connector Power Supply

The B2B connector power supply requires a single nominal 5 V DC power supply. The power is usually supplied to the module through the 5 V contacts (5Vb2b) of the B2B connectors J5 (see Appendix). The recommended minimum supply voltage is 4 V. The maximum supply voltage is 5.5 V. The recommended maximum continuous supply current is 1.5 A.

USB Power Supply

The module is powered by the USB connector if the following conditions are met:

- the module is equipped with an USB connector,
- the module is connected to a USB bus,
- no power supply is provided by the B2B connectors.

In this case, other components (e.g. extension or carrier boards) may also be powered by the corresponding 5 Volt line (5V) of the B2B connector J5.

On-board Power Rails

Three on-board voltage regulators provide the following power supply rails needed by the components on the micromodule:

- 1.2 V, 1 A max
- 2.5 V, 1 A max
- 3.3 V, 1 A max

The power rails are available for the FPGA and can be shared with a baseboard by the **corresponding** lines of the B2B connectors J4 and J5. Please note that the **power consumption of the FPGA is highly dependent on the design** actually loaded. So please use a tool like Xilinx Xpower to determine the expected power consumption.

Even if the provided voltages of the module are not used on the baseboard, it is recommended to bypass them to ground with 10 nF - 100 nF capacitors.

I/O Banks Power Supply

The Spartan-3E architecture organizes I/Os into four I/O banks (see Table 3).

Bank	Supply Voltage (V)	Min (V)	Max (V)
В0	VccIO	1.2	3.3
B1	2,5	-	-
B2	3,3	-	-
B3	3,3	-	-

Table 3: I/O banks power supply.

Voltage for banks B1, B2 and B3 is fixed respectively to 2,5 V, 3,3 V and 3,3 V.

Voltage VccIO for bank B0 shall span from 1.2 V to 3.3 V. VccIO can be supplied either externally or internally to the micro-module.

Warning! Spartan-3 I/Os are not 5 V tolerant. Applying more than the recommended operating voltages at any pin, results in a damaged FPGA (see Xilinx Answer AR#19146).

Externally Supplied VccIO

VccIO can be externally supplied over the B2B connector J4. If bank B0 is not used, then VccIO can be left open.

Internally Supplied VccIO

If VccIO is **not** externally supplied, it can be internally supplied by **one** of the internal power rails of 2.5 V and 3.3 V. This is possible by short-circuiting **one** of the two pad pairs placed on the right of connector J4 at the top right corner of the bottom side of the micromodule.

Figure 9 shows how to short-circuit VccIO to internal 3.3 V power rail.

Figure 10 shows how to short-circuit VccIO to internal 2.5 V power rail.

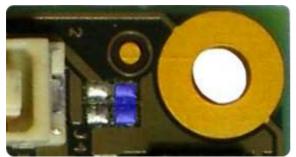


Figure 9: R102 pad pair (blue highlight) for 3.3 V internal supply.

Two suitable ways of shirt-circuiting the paid pair are by means of a zero-ohm 0603 (1608 metric) chip resistor or a solder blob.

FPGA User I/Os

A total of 110 FPGA user I/Os are available on corresponding contacts of B2B connectors J4 and J5 (see Appendix).

- 37 differential digital I/O pairs: each pair is configurable as 2 single-ended digital I/Os, corresponding to a maximum of 74 single-ended digital I/Os;
- 4 differential clock input pairs: each pair is configurable as differential digital I/O pair or 2 single-ended clock inputs or 2 single-ended digital I/Os (or combination thereof), corresponding to from a maximum of 8 independent clock inputs to a maximum of 8 independent digital I/Os;
- 1 differential clock input pair: the pair is configurable as differential digital input pair or as 2 single-ended clock inputs or 2 single-ended digital inputs (or combination thereof), corresponding to from a maximum of 2 independent clock inputs to a maximum of 2 independent digital inputs;
- 21 single-ended digital I/Os;
- 5 single-ended inputs.

Table 4 summarizes the maximum available FPGA user I/Os divided by supply voltage.

type	VccIO	3.3 V
diff. I/O pairs	≤ 18	≤ 23
diff inputs	≤ 1	none
diff. clocks	≤ 4	≤ 1
s. e. I/Os	≤ 46	≤ 58
s. e. inputs	≤ 2	≤ 4
s. e. clocks	≤ 8	≤ 3

Table 4: maximum FPGA user I/Os by supply voltage.

Differential Pairs

The micromodule has a total of 42 differential signal pairs routed pairwise with a differential impedance of 100 ohm to adjacent connector pins. These lines can be used for high speed signaling up to 666 Mbit/s per differential pair (see Xilinx Application Note XAPP485).

User Button and LED

LED

The LED is lit when the U_LED line (pin R10) is set high as detailed in the following table.

Signal	FPGA pin	FPGA ball
U_LED	IO_L15P_2 (bank 2)	R10

Table 5: user led signal details.

Push Button

The push button is connected to the PB input (pin V16). as detailed in the following table.

Signal	FPGA pin	FPGA ball
РВ	IP (bank 2)	V16

Table 6: user button signal details.

The input is normally low. The input is pulled up when pressed.

Configuration Switches

The micromodule hosts 4 DIP switches on the top side: S1; S2, S3 and S4.

For customers requesting a sufficient amount of units, the micromodules can be manufactured replacing the switches by fixed connections.

DIP Switch S1

S1 enables / disables the communication between the Cypress EZ-USB FX2 micro-controller and the I2C CMOS Serial EEP-ROM.

Turn S1 off when programming the USB EEPROM (storing the USB vendor ID and device ID). This will force the USB microcontroller to provide its default vendor ID and device ID.

S1	position
EEPROM (on)*	EEPROM <u>en</u> abled
Off (off)	EEPROM <u>dis</u> abled

Table 7: S1 (* default: EEPROM).

For further information, please read paragraph "Software Configuration".

DIP Switch S2

S2 enables / disables the reset line. The reset line (available also on 2 contacts of the B2B connector) resets the USB micro-controller and the FPGA.

S2 has to be turned off (*Reset*) if the user wants to program the SPI Flash memory in direct mode. For programming the SPI Flash memory in indirect mode over JTAG, S2 has to be turned on (*Run*).

S2	position	
Run (on)*	system running	
Reset (off)	system reset	

Table 8: S2 (*default: Run).

For further information, please read paragraph "Software Configuration".

DIP Switch S3

S3 conditionally / unconditionally enables the 1.2 V and 2.5 V power rails.

When S3 is turned on, the 1.2 V and 2.5 V power rails are controlled by the USB microcrocontroller. At start-up, the USB microcontroller switches off the 1.2 V and 2.5 V power rails and starts up the module in low-power mode. After enumeration, the USB microcontroller firmware switches the 1.2 V and 2.5 V power rails on, if enough current is available from the USB bus.

When S3 is turned off, the 1.2 V and 2.5 V power rails are always enabled.

S3	position
FX2 PON (on)*	rails controlled by FX2
PON (off)	rails always enabled

Table 9: S3 (* default: FX2 PON).

Warning! When S3 is turned on (*FX2 PON*), make sure that no signals are applied to the input pins when power-rails are disabled by the USB microcontroller.

The 3.3 V power-rail though is out of the control of the USB-microcontroller and is supplied down-converting the 5 V power supply provided by either the USB-bus or the B2B receptacle connector. In this case, signals that are applied to the 3.3 V I/O

banks do not need to be disconnected when power-rails are disabled by the USB microcontroller.

DIP Switch S4

S4 enables / disables the FPGA configuration through the SPI interface. The FPGA configuration through the JTAG interface cannot be disabled.

When S4 is turned on, the FPGA tries to configure from the SPI Flash memory. The FPGA can be configured by the JTAG interface at any time.

When S4 is turned off, the FPGA waits to be configured by the JTAG interface.

For further information about direct (pure SPI) / indirect (SPI over JTAG) in-system programming of SPI flash memories, please see Xilinx Application Notes XAP-P951 "Configuring Xilinx FPGAs with SPI Serial Flash" and XAPP974 "Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs".

S4	position	
SPI (on)*	FPGA configuration: JTAG + SPI	
JTAG (off)	FPGA configuration: JTAG	

Table 10: S4 (* default: SPI).

Warning! When downloading via parallel JTAG programmer to FPGA, it can happen that programming fails with Error: "'1' : *Programming terminated. DONE did not go high.*" Try setting DIP switch S4 to JTAG-only. A bug in certain Xilinx iMPACT versions can cause this.

DIP Switches Overview

Figure 11 summarizes functions and location of the four DIP switches.

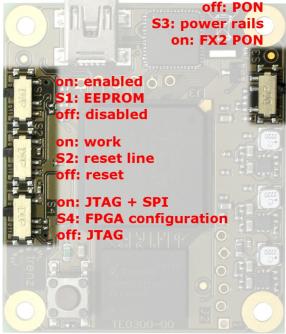
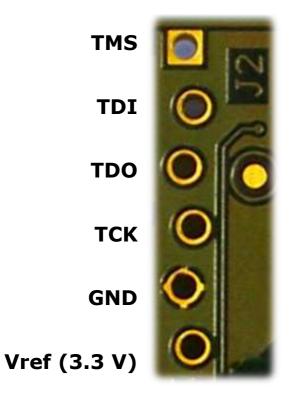


Figure 11: DIP switches overview. **JTAG and SPI**

The offset holes for J2 and J3 allow a removable press fit of standard 0.100 inch header pins to connect the fly wires without any soldering necessary.

JTAG Header

JTAG signals are available on the dedicated header J2 through a JTAG programmer with flying leads as described in Table 11.



SPI /S
SPI D
SPI Q
SPI /C
GND
Vref (3.3 V)

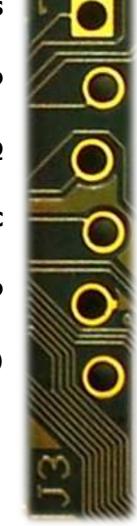


Table 13: SPI header (J3).

Clock Networks

24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the USB microcontroller and the FPGA as detailed in Table 14.

Table 11: JTAG header (J2).

SPI Header

SPI signals are routed to / from bank 2 of the FPGA as detailed in Table 12 and made available on the dedicated header J3 accessible through an SPI programmer with flying leads as described in Table 13.

Signal	FPGA pin	FPGA ball
SPI /S	IO_L01P_2	U3
SPI D	IO_L03N_2	T4
SPI Q	IO_L16N_2	N10
SPI /C	IO_L26N_2	U16

Table 12: SPI signal details (bank 2).

Signal	FPGA pin	FPGA ball
24MHZ1	IO_L12P_2 (bank 2)	N9

Table 14: 24 MHz clo	ck signal details.
----------------------	--------------------

Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in Table 15.

Signal	FPGA pin	FPGA ball
100MHZ 125MHZ	GCLK0 (bank 2)	U10

Table 15: main clock signal details.

Standard frequencies are 100 MHz and 125 MHz (please visit Trenz Electronic website for current ordering information). The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM). For customized boards, this clock can be changed according to user requirements.

Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the USB microcontroller and bank3 of the FPGA as detailed in Table 16.

Signal	FPGA pin	FPGA ball
IFCLK	LHCLK5 (bank 3)	K4

Table 16: interface clock signal details (bank 3).

Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx data sheet DS485 "Digital Clock Manager (DCM) Module" (dcm_module.pdf) and Xilinx application note XAPP462 "Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs" (xapp462.pdf).

On-board Memories

The TE0300 has three on-board memories:

- DDR SDRAM
- SPI Flash
- serial EEPROM

DDR SDRAM

TE0300 modules have a 512Mb DDR SDRAM component for operation (code and data) accessible through the FPGA.

Commercial-grade modules mount the following component:

Micron Technology MT46V32M16BN-6

Industrial-grade modules mount the following component:

Micron Technology MT46V32M16BN-6 IT

You can get the exact part number of the component mounted on your module from the Micron FBGA decoder:

http://www.micron.com/support/part_info /fbga/decoder

When developing DDR SDRAM designs with Xilinx tools (e.g. MIG, MPMC, ...), you should select the following product type:

MT46V32M16-6.

Should it be not available, you can use one of the following product types:

- MT46V32M16-5
- MT46V32M16XX-5B
- MT46V32M16BN-5B
- MT46V32M16FN-5B
- MT46V32M16P-5B
- MT46V32M16TG-5B

TE0300 modules with the following part numbers

- TE0300-00
- TE0300-00-4I5C
- TE0300-00B
- TE0300-01
- TE0300-01B
- TE0300-01BLP

are assembled with

Qimonda HYB25DC512160CF-6

512Mb DDR SDRAM components. When developing DDR SDRAM designs with Xilinx tools, you should select the following product type:

HYB25D512160BF-6.

SPI Flash

TE0300 modules have a

STMicroelectronics M25P32

32-Mbit, low voltage, serial Flash memory with 75 MHz SPI bus interface for configuration and operating storage accessible through USB or SPI.

Serial EEPROM

TE0300 modules have a

Micron Technology 24LC128

128K I2C CMOS Serial EEPROM. It used for EZ-USB FX2 firmware, vendor ID and device ID storage. EEPROM accessible through the EZ-USB FX2 microcontroller.

Module Configuration

This section describes how to configure the TE0300 module and access some of its resources.

The JTAG interface allows a fast, frequent but volatile configuration of the TE0300 module. However, only through the JTAG

interface it is possible to develop and debug with Xilinx tools (e.g. Xilinx Chip-Scope, Xilinx Microprocessor Debugger.

The SPI interface allows a fast, frequent and non-volatile configuration of the TE0300 module.

Configuration of the TE0300 module through a USB host is recommended for occasional, non-volatile on-site operations such as firmware upgrade.

System Requirements

TE0300 modules can be configured through a host computer with the following system requirements:

- Operating system: Microsoft Windows 2000, Microsoft Windows XP, Microsoft Vista;
- Xilinx ISE 10.1 or later for indirect SPI in-system programming (see Xilinx Answer AR #25377);
- Xilinx EDK for some reference designs;
- Interface: USB host;
- JTAG/SPI USB cable with flying leads.

EZ-USB FX2 Microcontroller Firmware

If the EEPROM has never been programmed before (virgin board), S1 can be switched to **EEPROM**. The USB microcontroller will detect an empty EEPROM and will provide its default vendor ID and device ID to the USB host.

DIP switch	on (left)	off (right)
S1	EEPROM	-
S2	Run	-
S3	Х	х
S4	Х	Х

If the EEPROM has been programmed before (EEPROM not empty), S1 must be switched to **Off**. The USB microcontroller will detect a missing EEPROM and will provide its default vendor ID and device ID to the USB host.

DIP switch	on (left)	off (right)
S1	-	Off
S2	Run	-
S3	Х	Х
S4	Х	Х



Generic USB Microcontroller Driver installation

If the USB microcontroller (Cypress EZ-ESB FX2) driver is not installed on the host computer, then the easiest way to do it is the following:

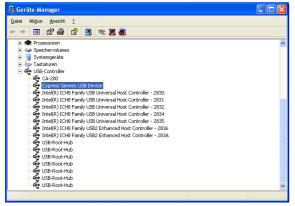
- disconnect the micromodule or leave the micromodule unconnected;
- configure the micromodule such that the USB microcontroller will provide its default vendor ID and device ID to the USB host (i.e. S1 = OFF -- see paragraph "EZ-USB FX2 Microcontroller Firmware");
- connect the micromodule to the host computer through the USB interface;
- wait until the operating system detects new hardware and starts the hardware assistant;
- if S1 is not already switched to EEP-ROM, do it now;
- answer the hardware assistant questions as shown in the following example.





Assistent für das Suchen neuer Hardware		
	Fertigstellen des Assistenten Die Software für die folgende Hardware wurde installiert:	
100	Cypress Generic USB Device	
	Klicken Sie auf "Fertig stellen", um den Vorgang abzuschließen.	
	< Zurück Fertig stellen Abbrechen	

Check that in the "Device Manager" under "USB-Controller" the "Cypress Generic USB Device" has been added.



Now the USB microcontroller can be accessed from the host computer through dedicated software.

EZ-USB FX2 EEPROM Programming

First of all, check that S1 is actually switched to EEPROM.

The USB EEPROM can be programmed by opening the dedicated software "Cypress USB Console" (double click the "CyConsole.exe" file in the "1st_program\CyConsole" folder).

🐨 Cypress USB Co	onsole				
File Options Help					
èr 🖸 🖸 🖾	 Selected Script: 		ж	8 C	¥
Select Device					
	e Name		idows Device Mgr	(from .inf)	
4 USB	Device	Cypress Gen	eric USB Device		
	×.	, in the second s			
Device Properties C	ontrol Endpt Xfers 0	ther Endpt Xfers M	isc.		
VendorID 0	x04B4	Class	0xFF		
ProductID 0	x8613		assOxFF		
Manufacturer			ol 0xFF		
Product		bodDe	evice 0xA001		
Senar Number					
Device Configuration	s (1)				
Value	Attributes	Max Power			
0x01	0x80	0x32 (100 mA)			_
Configuration Interfac	es (4)				
Intfc Alt Setting	Class	Subclass	Protocol		^
0 0	0xFF (Vendor)	0xFF	0xFF		
0 1 0 2	0xFF (Vendor) 0xFF (Vendor)	0xFF 0xFF	0xFF 0xFF		~
Interface Endpoints (i í				
Address	Attributes	Max Pkt Size	e Interval		
				_	

Click "Options > EZ-USB Interface" to Open EZ-USB Interface window.

🐨 EZ-USB Interface
Device USB Device Clear Load Mon S EEPROM Select Mon
Get Dev Get Conf Get Pipes Get Strings Download Re-Load Lig EEPROM URB Stat HOLD RUN
Vend Reg Reg 0x00 Value 0x0000 Index 0x0000 Length 0 Dir 0 0UT V Hex Bytes C0 84 04 81 00 01 00 V
Iso Trans Pipe Length 128 Packet Size Packets
Bulk Trans Pipe Length 64 Hex Bytes 5
Reset Pipe Abort Pipe File Trans Pipe
Set IFace Interface 0 AltSetting 0
 (*)
No. Contraction of the second s

"S EEPROM" button refers to the small EE-PROM (256 bytes) whereas the "Lg EEP-ROM" refers to the large EEPROM (64 KB). Press the "Lg_EEPROM" button, select the "USB.iic" file and press the "Open" button to start writing to EEPROM.

Suchen in:	TE0300		•	🗢 🗈 💣 🔠	•
Zuletzt /erwendete D	in driver CyConsole				
Desktop Eigene Dateien					
Arbeitsplatz	Dateiname:	usb.iic		-	Ö <u>f</u> fnen
	1707/00 T 1000				

DIP switch	on (left)	off (right)
S1	EEPROM	-
S2	Run	-
S3	FX2 PON	-
S4	Х	х

Reconnect the USB cable to run the newly uploaded firmware in the USB microcontroller. Under the default switch configuration, the USB microcontroller is now ready to provide dedicated vendor ID and device ID. Wait until the operating system detects new hardware and starts the hardware assistant and answer the hardware assistant questions as shown in the following example.

Upgrade progress is displayed in status window and is completed when "Download Successful" text is displayed.

→ EZ-USB Interface	
Device USB Device Clear Load Mon S EEPROM Select Mon	
Get Dev Get Conf Get Pipes Get Strings Download Re-Lozd Lig EEPROIX URB Stat	HOLD RUN
Vend Reg Reg 0x00 Value 0x084E Index 0x0000 Length 0 Dir 0 OUT - Hex By	tes CO B4 04 81 00 01 00 💌
Iso Trans Pipe Length 128 Packet Size Packets	
Bulk Trans Pipe Length 64 Hex Bytes 5	•
Reset Pipe Abort Pipe File Trans Pipe	
Set IFace Interface 0 AltSetting 0	
	^
Nownload 12 bytes: addr=d91	
0000 78 7F E4 F6 D8 FD 75 81 3E 02 05 E6	
Nownload 96 bytes: addr=84e	
0000 BB 01 0C KS 82 29 F5 82 K5 83 3A F5 83 K0 22 50	
0010 06 K9 25 82 F8 K6 22 BB FE 06 K9 25 82 F8 K2 22	
0020 E5 82 29 F5 82 E5 83 3A F5 83 E4 93 22 F8 BB 01	
0030 0D E5 82 29 F5 82 E5 83 3A F5 83 E8 F0 22 50 06 0040 E9 25 82 C8 F6 22 BB FE 05 E9 25 82 C8 F2 22 EB	
JU4U - M9 25 82 08 F6 22 88 FM U5 M9 25 82 08 F2 22 M8 JU5D - 9F F5 F0 RA 9R 42 F0 R9 9D 42 F0 R8 9C 45 F0 22	
Joso 97 PS PO EM 96 42 PO E9 90 42 PO E8 90 45 PO 22 Formie 8051 Reset (00)	
Novnloading file: C:\TE0300\usb.iic	
ownloading 4096 bytes to addr=0	
Counloading 4096 bytes to addr=0 Counloading 1331 bytes to addr=1000	

Disconnect the USB cable.

Dedicated USB Firmware Driver Installation

Check the configuration switches against the following table:









Check that in the "Device Manager" under "USB-Controller" the "DEWESoft USB Device 0" has been added.

Geräte-Manager	
Datei Aktion Ansicht 2	
⊢ → 🔟 🖨 😫 🚨	
🗈 🐲 Prozessoren	^
🗄 🥪 Speichervolumes	
🗄 🖳 Systemgeräte	
🗉 🦥 Tastaturen	
🗄 🚓 USB-Controller	
ି 🖨 CA-200	
- 🕰 DEWESoft USB Device 0	
- 🕰 Intel(R) ICH8 Family USB Universal Host Controller - 2830	
- 쎭 Intel(R) ICH8 Family USB Universal Host Controller - 2831	
- 🖨 Intel(R) ICH8 Family USB Universal Host Controller - 2832	
🛶 🙀 Intel(R) ICH8 Family USB Universal Host Controller - 2834	
🛶 🙀 Intel(R) ICH8 Family USB Universal Host Controller - 2835	
- 🕰 Intel(R) ICH8 Family USB2 Enhanced Host Controller - 2836	
- 😴 Intel(R) ICH8 Family USB2 Enhanced Host Controller - 283A	
- 🕰 USB-Root-Hub	
- 🕰 USB-Root-Hub	
- 😴 USB-Root-Hub	
- 🙀 USB-Root-Hub	
- 😴 USB-Root-Hub	~

FWU File Generation

The TE0300 micromodule can be configured by means of a firmware-upgrade (FWU) file (see next section "Micromodule Configuration" for further reference). The first step in generating the FWU file is to generate the *fpga.bin* file corresponding to a given FPGA design.

Open Xilinx IMPACT from Start / Programs / Xilinx ISE / Accessories / Impact

Select "create new project".

💱 iMPACT Project	X
I want to	
C load most recent project default	ipf Browse
	Load most recent project file when iMPACT starts
 create a new project (.ipf) defau 	tipf Browse
01	
<u>K</u>	

Select "prepare PROM file".



Set "PROM File Name" to "fpga" and change "Location" to a suitable name and location.

🕵 iMPACT - Specify Xilinx PROM Device	
Auto Select PROM	
Enable Revisioning	
Number of Revisions:	
Enable Compression	
Select a PROM (bits): Unspecifier	- Add
Position Part flam	
	Delete All
< <u>B</u> ack	<u>N</u> ext > Cancel

Select "BIN" as output.

🐉 iMPACT - Prepare PROM Files	
I want to target a	
Xiinx PROM	
C Generic Parallel PROM	
C 3rd-Party SPI PROM	
C PROM Supporting Multiple Design Versions: Spartan3E MultiBoot	Ŧ
- PROM File Format	
C MCS C TEK C UFP ("C" format)	
C EXO @ BIN C ISC	
C HEX 🔲 Swap Bits	
Checksum Fill Value (2 Hex Digits): FF	
PROM File Name: fpga	
Location: C:\Xilinx\	owse
< <u>B</u> ack <u>N</u> ext>	Cancel

Check "Auto Select PROM".



Navigate to your project's IMPLEMENTA-TION folder and select "download.bit".

dd Device				? >
Look jn:	implementation	•	🗢 🗈 💣 🎫	
2	ache	Distance Contraction Contractico Contracti	pper	
	Chipscope_icon_0_wrapper	Crs232_wrapper		
Recent	Chipscope_opb_iba_0_wrapper	Contemporation Science Contemporation Contemporatio Contemporation Contemporation Contemporation	_wrapper	
	dcm_0_wrapper	🚞 spi_adc_0_wrap	per	
	dcm_1_wrapper	🚞 spi_mon_0_wra	pper	
	C debug_module_wrapper	best_mux_0_wr	apper	
Desktop	Contir_wrapper	📼 download . bit		
	C dlmb_wrapper	🗖 download_cclkte	emp.bit	
	ilmb_cntlr_wrapper	🖻 system bit		
🚬	ilmb_wrapper			
My Documents	imb_bram_wrapper			
	mb_opb_wrapper			
	microblaze_0_wrapper			
My Computer	opb_dma_0_wrapper			
my computer	opb_fx2_0_wrapper			
	1			
My Network	File name: download.bit		-	<u>O</u> pen
Places	-			
	Files of type: FPGA Bit Files	.".bit)	•	Cancel



Click GENERATE FILE or select from menu Operations / Generate file.

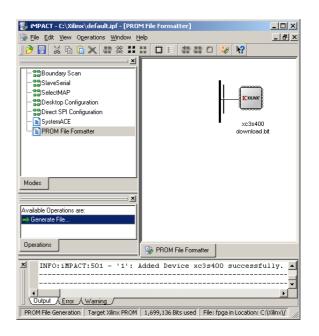
The following warning is a normal situation.

🐉 Warning 🛛 🛛 🗶		
⚠	WARNING:MPACT:2257 - Startup Clock has been changed to 'Cclk' in the bitstream stored in memory, but the original bitstream file remains unchanged.	
	OK	

This is probably the one and only file with your design.

퉳 Add D	evice	×
?	Would you like to add another device file to	
~	Data Stream: 0	
	<u>Y</u> es	

Congratulations!



You are done.

	ult.ipf - [PROM File Formatter]	
Ele Edit View Operations	s Window Help 좋※ ### 슈티 참 많 0 😵 🕅	
Bounday Scan SaveSeta SaveSeta SaveSeta SolentAP Deskor Configuration Deskor Configuration Deskor SPE Configuration Deskore SPE Configuration PROM File Formater Modes Available Operations are Generate File		
Operations	ROM File Formatter	
Writing file "C	C:\Xilinx\//fpga.prm". C:\Xilinx\//fpga.sig".	× •
Output A Error A Warnin		

Don't forget to save your project for further use

🐉 Exit iMPACT		×
😲 Do you wa	nt to save project	file before exiting?
Yes	No	Cancel

Once you have got your *fpga.in* file, you can proceed and generate your FWU file. The FWU file is a ZIP file containing 3 files:

- Bootload.ini booting settings
- fpga.bin FPGA programming file
- usb.bin FX2 firmware

To create your FWU file, you need to

- replace the existing *USBFWUTool\FWUs\fpga.bin* with the latest *fpga.bin* (*Bootload.ini* and *usb.bin* are always unchanged)
- zip the 3 files
- change the "*zip" file extension to* "*fwu"*
- upload the file as explained in the next section (Micromodule Configuration).

Warning! file and path names are given and must NOT be changed!

Micromodule Configuration

The micromodule can now be programmed with its dedicated firmware upload tool. Turn S1, S2, S3 and S4 on. Open the dedicated firmware upgrade tool "USB Firmware Upgrade Tool" (double click the "US-BFirmwareUpgradeTool.exe" file in the "USBFWUTool" folder).

🖶) USB Firmv	vare Upgrade Tool
Device: US	B Device
File name:	Upload
	Version: 2.6

Press the "..." button corresponding to the "File name" field and select for instance the sample firmware upload file "TE0300_v1012.fwu" in the "USBFWUTool\FWUs" folder.

Öffnen			? 🛛
<u>S</u> uchen in:	FwUs		-
Zuletzt verwendete D Desktop Eigene Dateien	E 7E0300_v0	512.fwu	
Arbeitsplatz			
Netzwerkumgeb	Dateiname:	TE0300_v0812.fwu	Öffnen
ung	Dateityp:	FW Update Files (*.fwu)	Abbrechen
😨) USB Firr	nware Up	grade Tool	×
Device:	USB Device		
File name:	C:\TE0300\I	USBFWUTool\FWUs\TE0300_v1012.	Upload
		Ye	rsion: 2.6

Press the "Upload" button to upload the micromodule firmware and check the "FPGA uploading..." progress bar.

🕄 USB Firmware Upgrade Tool	×
Device: USB Device	
File name: C:\TE0300\USBFWUTool\FWUs\TE0300_v1012.	Upload
FPGA uploading (22%)	Version: 2.6

After successful completion of the firmware upload procedure, the following message should pop up.

USB Firm	ware Upgrade Tool 🔯
Firmware	upgrade successful!

Reboot the micromodule with the new firmware by disconnecting and reconnecting the USB cable. You may want to test the sample application "TE0300_API_Example.exe" in the "TE0300_API_Example\Debug" folder.

To generate your own firmware upload file, please read the document "Generating_FWU_file.doc" in the "USB-FWUTool" folder.

SPI Direct In-System Programming (ISP)

Make sure S2 is switched to "Reset" (off) during programming.

Connect the host computer to the micromodule through both the SPI flying leads cable and the USB cable.

Start Xilinx ISE iMPACT. The following example shows the case of iMPACT 9.2. If the "iMPACT Project" window pops up, press the "Cancel" button.

😻 iMPACT Project							×
I want to							
load most recent project	default.ipf				~ [Browse	
		📃 Load	most recent pro	ject file when il	MPACI	l starts	
 create a new project (.ipf) 	default.ipf					Browse	
	<u>D</u> K		<u>C</u> ancel]			

Double click the "Direct SPI Configuration" option in the "Modes" panel.

🔋 MPACT 📃 🗖	\times
Ble Edit Yew Operations Options Quiput Debug Window Help	
2 2 3 3 3 3 4 3 4 4 4 4 5 4 4 5 4 4 5 4 4 5 4 5	
Flows X INFACT Processo X	
Blooksisten Blooksist Statution Statution Des Statutions Model for Formation	
Modes Operations http://www.xdinx.com	1
V Valores to JUPACT	8
Data Frey Water	2
S Cutput Enx: Warning	
Six Cristing D	l las

Right click the "Direct SPI Configuration" panel to add a device and select "Add SPI Device".

	ns Qutput Debug Window Help		
	11 II I	8	
ME	× MRACT Processes	×	
Boundary Scan SlaveSeilal SelectMAP Desktop Conliguration	Available Operations are:	Add SPI Device Clof4D Cable Auto Connect Cable Setup	
Spinect SPI Configuration SystemACE PROM File Formatter		Right click to Add Device or Identify Device	
odes	Operations	Se Direct SPI Configuration	

You can now select the file corresponding to your device. In the following example, we will show how to select the micromodule reference device "blinking.mcs" in the "TE0300" folder.



Select the part name corresponding to the SPI flash present on the module (STMicroelectronics M25P32, a 32 Mbit (4M x 8) Serial Flash memory).

😵 Select Device Part Name				
Select PROM				
Part Name:	M25P32			
<u> </u>	<u>Cancel</u> Help			

iMPACT should now look like this.

	juration)		
Ele Edit Yew Operations Opt	jons Qutput Debug Window Help	6	10
B K B B X # 3		1 12	
ions	X MPACT Processes	×	-
Brundery Scan SlaveSerial Desktop Configuration Desktop Configuration Desktop Configuration SystemACE PROM File Formatter	Avelable Operations are: ■● Program ■● Vielly ■● Erase ■● Erase ■● Reachask		
Nodes	Operations	Sk Direct SPI Configuration	
Welcome to iMPACT // *** BATCH CND :			
'1': Loading file ' INFO:1MPACT - Elaps done.			
'1': Londing file IHFO:HBACT - Eleps done. // *** BATCH CND :	E:/TE0300/blinkin.mcs' ed time = 0 sec.		2
'l'i Loading file ' HWF0:INPACT - Elaps done. // *** BATCH CHD :	E:/TE0300/blinkin.mcs' ed time = 0 sec.		2

Right click the SPI PROM device and select the "Program" operation.

S WPACT - [Direct SPI Configurat				
Be Elle Edit Yew Operations Options	Qutput Debug Window Help			- B - S
🔁 🖥 🖌 🖻 🎧 🗙 🛱 🍀 🗄	HOI ##0 4 12			
Flows X Image: Struct Symplemial Image: Struct Symplemial Image: Struct Symplemial Image: Struct Symplemial	NEMOT Processes X Available Operations are: Hogan Hogan Hogan Vesty Ease #Stark Check Readback	SOLK MOGI SS_P TO SS TO SS_P TO	Produm Verify Bros Broshock. Roshock. Assign New Configuration File	
Hodes	Operations	Si Direct SPI Configuration		
'1': Loading file 'E:/' INFO:INPACT - Elapsed : done.	Node -spi Added Device M25P32 succes			6
C Dutput Error Warning				8
cost - waring			No	Cable Connection

In the "Programming Properties" window, just leave the default settings and press the "OK" button.

perios ROM Programming Properties perties	Programming Properties General Programming Properties
	Venity
	General CPLD And PROM Properties
	Erase Before Programming Read Protect
	PROM/CoolRunner-II Usercode (8 Hex Digits)
	CPLD Specific Properties
	Write Protect Functional Test On-The-Fly Program
	XPLA UES Enter up to 13 characters
	PROM Specific Properties
	Load FPGA Parallel Mode Use D4 for CF
	Spartan34N Programming Properties
	Data Protect Data Lockdown
	FPGA Device Specific Programming Properties
	Pulse PROG Program Key
	Assert Cable INIT during programming

iMPACT will first erase the memory (notice the mismatch between the two progress indicators)

? 🔀
Cancel

and then write it (notice the match between the two progress indicators).

🐉 Progress Dialog [10%]		
nd		
10%		
	Cancel	
	nd	

After successful programming, you should read the message "Program Succeeded" popping up for a few seconds in the "Direct SPI Configuration" panel.

S MPACT - [Direct SPI Configur	ation)			
Be Edt Yew Operations Output	Window Help			
🔁 🖥 🕹 🖗 🍈 🗙 🖶 🎘	1	¥?		
	X MRACT Processes	×		
Brundary Scan SlaveSenial SlaveSenial SelectMAP Debloc Configuration B Subrect SPI Configuration B Subren/CE B PROM File Formatter	Available Operations are: Program Program Program Program Plank Check Plank Check Plank Check	SOLK MOSI SPI SS_n m25p32 MISO	Program Succeeded	
Modes	Operations	Se Direct SPI Configuration		
	<pre>ting Operation. .ce, omente pleted. eration. per. gegrem -p 1 -e -v -defaul 6° (in hex). cessfully. ing Operation. ce, contexts pleted. eration.</pre>	CYNEFIOR O		
Cutput Enor Warning				2
			Configuration Platform Cable USB 6 P	etz usb-hs

Switch S2 back to the "Run" position. In case you uploaded the test design, you should see the on-board led blinking at 0.5 Hz.

For further information about direct (pure SPI) in-system programming of SPI Flash memories, please see Xilinx Application Note XAPP951 "Configuring Xilinx FPGAs with SPI Serial Flash".

SPI Indirect In-System Programming (ISP)

Check the configuration switches against the following table:

DIP switch	on (left)	off (right)
S1	Х	х
S2	Run	
S3	-	PON
S4	Х	Х

Connect the host computer to the micromodule through both the SPI flying leads cable and the USB cable.

Start Xilinx ISE iMPACT. The following example shows the case of iMPACT 10.1. If the "iMPACT Project" window pops up, press the "Cancel" button.

🔯 iMPACT Project				×
I want to				
Ioad most recent project	default.ipf		~	Browse
		Load most recent pr	oject file when iMPAC	CT starts
 create a new project (.ipf) 	default.ipf			Browse
_			_	
	<u>ο</u> κ	Cancel		

Double click the "Boundary Scan" option in the "Modes" panel.

le Edit Yew Operations Options Quit		
> 目 % № 億 × 豊 ※ □		
	NRACT Processes ×	
Boundary Scen		
SaveSerial SelectMAP		
Desktop Configuration		
Direct SPI Configuration		
Sutem/CE		
PROM File Formalter		
0		
odes	Operations	http://www.xiinx.com
Welcome to iMPACT iMPACT Vermion: 10.1		
iMPACT Version: 10.1		
IMPACT Version: 10.1		
IMPACT Version: 10.1		
1893CT Version: 10.1		
iMPACT Version: 10.3		
MPACT Version: 10.3		

Right click the "Boundary Scan" to initialize the chain and select "Initialize Chain".

Ele Edit Yew Operations Options		¥2	
	MPACT Processes × Available Operations are:		
fodes	Operations	😼 Boundary Scan	
Welcome to iMPACT iMPACT Version: 10.1 // *** BATCH CHD : setM // *** BATCH CHD : setM			
iMPACT Version: 10.1 // *** BATCH CND : setM			

An "Assign New Configuration File" dialog window should pop up automatically. You can now select the file corresponding to your design. In the following example, we will show how to select the micromodule reference design "blinking.bit" in the "TE0300" folder. Do not forget to select the "Enable Programming of SPI Flash Device Attached to this FPGA" option in the same window.

😺 Assign	New Configuration File
Look jn:	🔄 E:/TE0300/ 💽 🖝 🏢 🏢
`	
🗀 1st_pr 📼 blinkin	ogram
🖬 blinkin	······································
Els asses	Line ha
File <u>n</u> ame:	blinkin.bit
File <u>t</u> ype:	All Design Files (*.bit *.rbt *.nky *.isc *.bsd) Cancel
	Cancel <u>A</u> ll <u>Bypass</u>
	O None
	 Enable Programming of SPI Flash Device Attached to this FPGA
	C Enable Programming of BPI Flash Device Attached to this FPGA

An "Add PROM File" dialog window should pop up automatically. You can now select the file corresponding to your design. In the following example, we will show how to select the micromodule reference design "blinking.mcs" in the "TE0300" folder.

Suchen in:	Contemp_TEC	300	•	+ 1	🗂 🛄	
	blinkin.mcs					
Zuletzt verwendete D						
Desktop						
Eigene Dateien						
3						
Arbeitsplatz						
					- Si - 20	
letzwerkumgeb	Dateiname:	blinkin.mcs			•	Ö <u>f</u> fnen
ung	Dateityp:	MCS Files (*.mcs)			-	Abbrechen

Select now the SPI Flash corresponding to the one present on the module (STMicroelectronics M25P32 in the example, a 32 Mbit (4M x 8) Serial Flash memory).

🐉 FPGA SPI Flash Asso	ciation 🛛 🔀
Select SPI Flash FPGA xc3s1200e	SPI Flash M25P32
	Cancel

iMPACT should now look like this.

		الكالك
File Edit Wew Operations Output	at Debug Window Help	
H K B G X # #	## 01 # #0 4 N	
ions	X MPACT Processes X	
Boundary Scan SlaveSetial SlaveSetial Solatop Configuration Desitop Configuration Desito SPI Configuration System/ICE PRIOM File Formatter	Anded Department which of the office which of the Department Denoted which of the Department Denoted which of	
Nodes	Operations 😼 Boundary Scan	
Firsware hex file ver Type = 0x0004. ESM option: 00000ACE PLD file version = 00 FLD version = 0012h PROGRESS_EXD - End 0 Elapsed Eine = Attempting to identi PROGRESS_START - Sta Identifying tohain co INFO:INFACT:1777 -	100. Iliuzilo,1/IE/deta/vush_vip.kex = 1301. Izzion = 1000. 487001. 0111. 1 sec. 1 sec.	
INFO:1MPACT:501 - '1 done. PROGRESS_END - End O Elapsed time =	0 sec.	
done. PROGRESS_END - End O	uperation. O pec.	

Right click the "Flash" device and select the "Program" operation.

	tions Output Debug Window Help			
B X 0 0 X # 1		142		(11)(2)
	X MEACT Property	X		
Brundey Scen SlaveSenial Desitop Configuration Desitop SPI Configuration System//CE PROM File Formater	Avaibble Operations are: ■● Pogsam ■● Velly ■● Earle ■● Bank Check ■● Rescback	SOLK MOSI SOLK SS_n 75532 Milliones	Program Verify Drase Bandwark.check Randwark Assign New Configuration File	
lodes	Operations	Direct SPI Configuration		
	932 '1': Added Device M25P32 st			
INFO: 1MPACT - Elaps done.		-att: packageName -value ""		

In the "Device Programming Properties" window, just leave the default settings and press the "OK" button.

Device Programming Properties - Device	1 Programming Properties	
Category		
 Boundary-Scan Device 1 (FPGA, xc3s1200e) 		
Device 1 (Attached FLASH, M25P32.)	Property Name	Value
	Verity	
	General CPLD And PROM Properties	
	Erase Before Programming	
	FPGA Device Specific Programming Properties	
	Assert Cable INIT during programming	
	After programming Flash	automatically load FPGA with currently assigned bits
	ОК	Cancel Apply Help

iMPACT will first erase the memory

🐉 Progress Dialog [1%]	? 🛛
Executing command	
1%	
	Cancel

and then write it.

😺 Progress	Dialog [10%]	? 🔀
Executing com	mand	
	10%	
		Cancel
		C

After successful programming, you should read the message "Program Succeeded" popping up for a few seconds in the "Boundary Scan" panel.

3 🖥 🖌 🖻 ն 🗙 😂 8		4 N2	
ME	X MRACT Processes	× Rasht click device to select operations	
Boundary Scan	Available Operations are:	Frank Carl of the Poster operations	
SlaveSenial	Program	(Inclusion)	
SelectMAP	-Veily		
Desktop Configuration	Erase	TDI Exeme	
22 Direct SPI Configuration	Blank Check		
System/CE	Readback	xc3x1200e	
PROM File Formatter	Get Device Checkours		10 m
		TDO Program Succee	ded
odes	Operations		
odes	Upenabona	Boundary Scan	
Decryptor security	aec	9	
DCT matched			
legacy input error			
status of GTS CFG B			
status of GVE		4	
status of GHIGH		1 1	
value of NODE pin H	n		
value of NODE pin H			
value of NODE pin H		0	
value of CFG RDY (I	NIT B)	1 1	
DONEIN input from D	ONE pin	1 1	
	d while trying to write FI		
	efore or after decrypt ope		
	used in proper sequence	: 0	
	Status register values:		
	0111 1001 1000 0000 0000 0		
	1': Completed downloading	bit file to device.	
	Checking done pindone.		
'1': Programmed suc PROGRESS END - End			
	Di sec.		
proposed class =	UI DEU.		
			2

Switch S3 back to the "FX PON" position. In case you uploaded the reference design, you should see the on-board led blinking at 0.5 Hz.

For further information about indirect (SPI over JTAG) in-system programming of SPI Flash memories, please see Xilinx Application Note XAPP974 "Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs".

Changes from TE0300-00 to TE0300-01

Clocks

TE0300-00 has a 50MHz secondary clock, whereas TE0300-01 has a 125MHz secondary clock.

Volatile Memory Interface

TE0300-00 could access the DDR SDRAM *only* with Xilinx OPB (on-chip peripheral bus) cores.

TE0300-01 can *also* access the DDR SDRAM through the dedicated Xilinx MIG (memory interface generator) memory interface.

B2B Connectors

Contact 14 of connector J5 has been extended from an input in TE0300-00 to an I/O in TE0300-01. Therefore hardware designs developed for the TE0300-00 are compatible with the TE0300-01 whereas those developed for the TE0300-01 are compatible with the TE0300-00 if that contact is configured as input.

Contact 76 of connector J5 has mistakenly been described as I/O in TE0300-00, but it has always been an input-only contact as documented for TE0300-01.

Connector J4 has not been changed.

LED

With TE0300-00, the LED is lit when the U_LED line on pin T15 is set high whereas with TE0300-01 the LED is lit when the U_LED line on pin R10 is set high.

Ordering Information

For the latest product details and available options, please visit:

www.trenz-electronic.de

shop.trenz-electronic.de

Revision History

Rev	Date	Who	Description
0.1	2008-04-24	FDR	created
1.0	2008-08-01	FDR	completed
1.01	2008-08-08	Π	50MHz to 125MHz clock
1.02	2008-10-17	FDR	U_LED for
			TE0300-00
1.03	2008-10-17	FDR	updated FUT from 1.9 to 2.6

Rev	Date	Who	Description
1.04	2008-10-27	FDR	DIP switches overview
1.05	2008-10-29	FDR	stacking height
1.06	2008-12-08	FDR	DIP switches revised
1.07	2009-02-16	FDR	fixed DIP switches overview picture
1.08	2009-03-09	FDR	clarified warning regarding 3.3 V power-rail
1.09	2009-03-16	FDR	fixed and improved switch settings
1.10	2009-06-03	FDR	added "FWU File Generation" section
1.11	2009-07-23	FDR	clarified changes/LED section
1.12	2009-08-24	FDR	added FPGA signal details for main user signals
1.13	2009-09-01	FDR	improved "On- board Memories" chapter
1.14	2009-09-03	FDR	improved clock, memory and con- figuration chapters
1.14	2009-10-23	FDR	PREPARE_FW de- scription removed
1.15	2010-05-14	FDR	Added reference design summaries.
1.16	2010-01-20	FDR	Fixed JTAG image.
1.17	2010-01-21	FDR	Fixed pin-out de- scription for pin 57 (B0_L08_N). Add note on offset hole connectors.
1.18	2011-03-25	FDR	Updated Hirose connectors part numbers
1.19	2011-10-04	AIK	Updated diagrams and ToC

 Table 17: revision history.

Legal Notices

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