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TE0320 Series User Manual

Xilinx Spartan-3A DSP Industrial-Grade FPGA Micromodule

Overview

The TE0320 is an industrial-grade FPGA micromodule integrating a leading-edge *Xilinx Spartan-3A DSP* FPGA, a USB 2.0 microcontroller, 32-bit wide 128 MByte DDR RAM, 4 MByte Flash memory for configuration and operation, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via robust board-to-board (B2B) connectors. All this on a tiny footprint, **smaller than a credit card**, at the most competitive price. Hardware and software development environment as well as reference designs are available at: www.trenz-electronic.de.

Sample Applications

- Cryptographic hardware module
- Digital signal processing
- Embedded educational platform
- Embedded industrial OEM platform
- Embedded system design
- Emulation platforms
- FPGA graphics
- Image processing
- IP (intellectual property) cores
- Low-power design
- Parallel processing
- Rapid prototyping
- Reconfigurable computing
- System-on-Chip (SoC) development

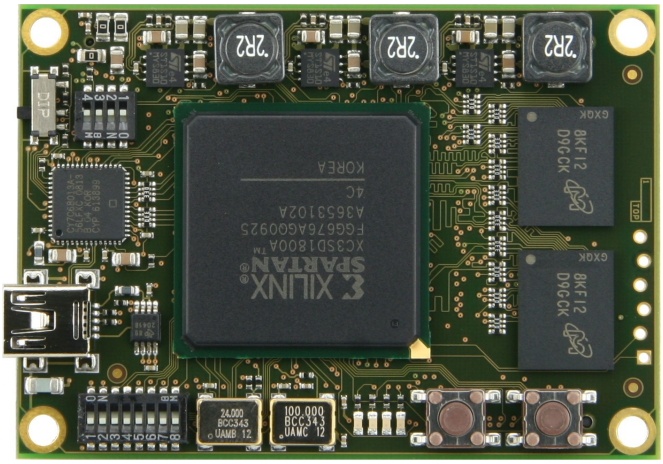

Figure 2: TE0320, top view.

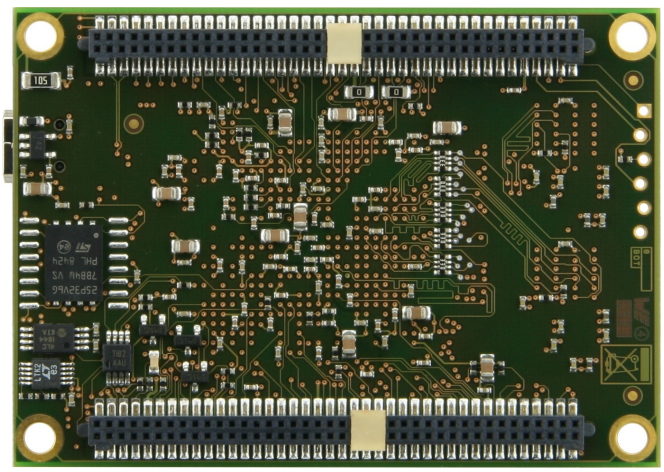

Figure 1: TE0320, bottom view.

Key Features

- Industrial-grade **Xilinx Spartan-3A DSP** FPGA module (1800 k gates or 3400 k gates)
- USB 2.0 (**Hi-Speed USB**) interface with a signalling bit rate of up to 480 Mbit/s
- 32-bit wide 1 Gbit **DDR SDRAM**
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Large **SPI Flash** memory (for configuration and operation) accessible through:
  - B2B connector (SPI direct)
  - FPGA
  - JTAG port (SPI indirect)
  - USB bus (Firmware Upgrade Tool)
- On-board 100 MHz oscillator for high performance
- On-board 24 MHz oscillator available to user
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters capable of 3 A each
- Power supply range: 4.0 - 7.0 V
- Power supply via USB or B2B (carrier board)
- 4 LEDs, 2 push buttons, 8 DIP switches.
- Plug-on module with 2 female 1.27 mm pitch header connectors
- 109 FPGA I/O pins (+ 10 dual-purpose pins) available on B2B connectors
- Evenly spread supply pins for good signal integrity
- Assembly options for cost or performance optimization available on request

Table of Contents

1 Block Diagram

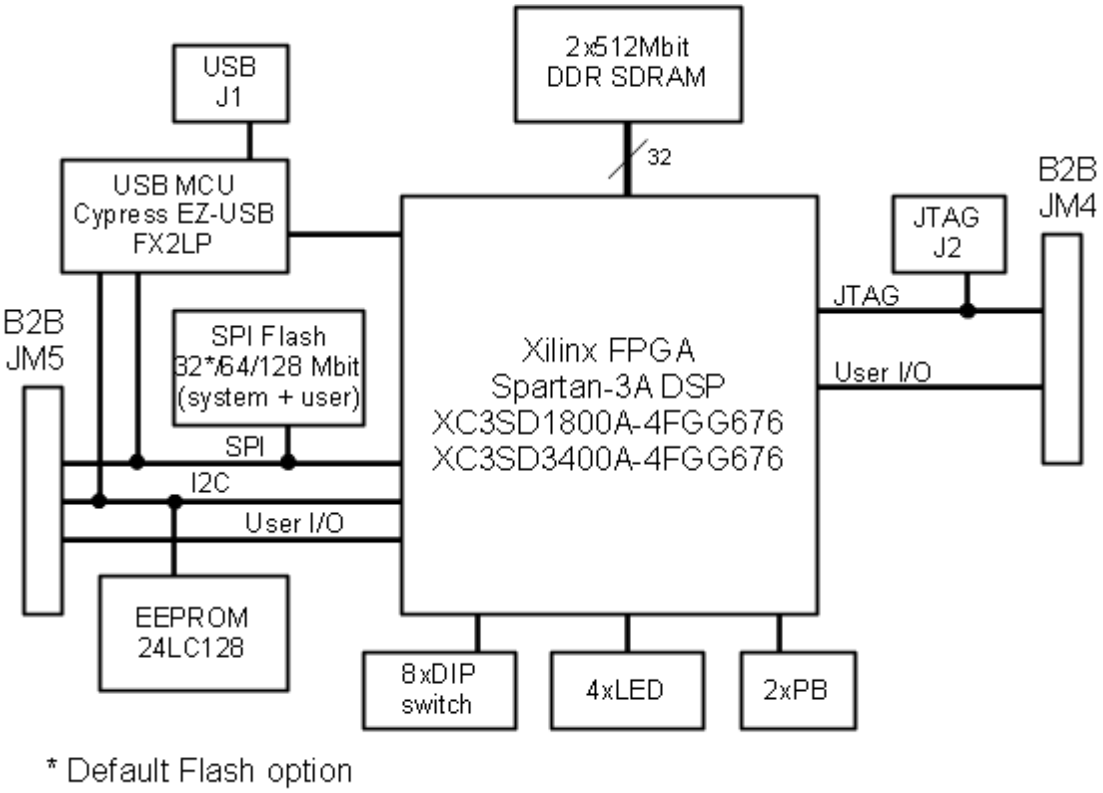

Figure 3: TE0320 block diagram

2 Module options

FPGA options

Module can be ordered with Spartan-3A DSP XC3SD1800A or XC3SD3400A chip.

Flash options

Module can be ordered with 32, 64 or 128 Mbit SPI Flash chip.

Temperature grade options

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

3 Specifications

- FPGA: Xilinx Spartan-3A DSP:
  - XC3SD1800A-4FGG676C, XC3SD1800A-4FGG676I or
  - XC3SD3400A-4FGG676C, XC3SD3400A-4FGG676I
- Cypress EZ-USB FX2LP™ USB microcontroller, high speed USB peripheral controller
  - CY7C68013A-56LTXC (commercial grade) or
  - CY7C68013A-56LTXI (industrial grade)
- Numonyx M25P32[1] / M25P64 / M25P128:
  low voltage, serial Flash memory with 75 MHz SPI bus interface
- 2 × 16-bit data-bus 512 Mbit DDR SDRAM (connected in parallel as a virtual 1 × 32-bit data-bus DDR SDRAM)
- Microchip Technology 24LC128I-ST
  128 kbit I2C CMOS serial EEPROM
- 3 × STMicroelectronics ST1S10:
  3 A, 900 kHz, monolithic synchronous step-down regulator
  3 A for each power rail: 1.2 V, 2.5 V, 3.3 V
- Texas Instruments TPS3705–33DGN
  processor supervisory circuits with power-fail and watchdog
- 100 MHz oscillator (system + user)
- 24 MHz oscillator (system + user)
- 2 × CviLux CBC1-80-2-M110-2P
  1.27 mm (50 mil = .050") pitch 80-pin double row socket (female) header board-to-board (B2B) connectors with key and pegs
- 109 FPGA IO Pins routed to the B2B connector
- 6-pin JTAG header
- 1 × USB mini-B receptacle (device)
- 1 × LED (system)
- 4 × LED (user)
- 2 × push button (user)
- 4 × DIP switches (system)
- 1 × slide switch (system)
- 8 × DIP switch (user)

1 Default module configuration contain 32 MBit Flash

4 Board Dimensions

TE0320 measures 68.0 × 48.0 mm.

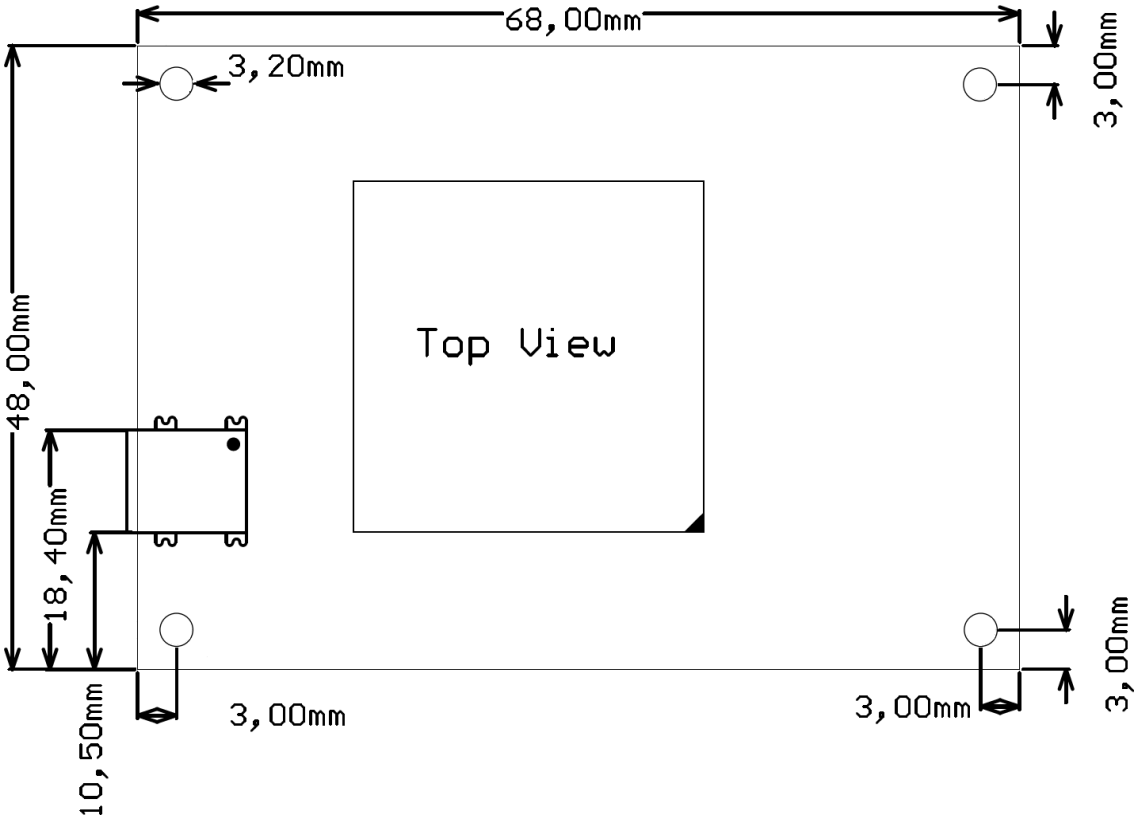

Figure 4: dimensional drawing.

TE0320 can reach a minimum vertical height of about 6 mm if push buttons and USB receptacle are not assembled.

Two mated standard TE0320 connectors have a nominal mated height of 6.0 mm. Processing conditions and solder paste thickness affects such height, resulting in an effective mating heights of 7.0 mm. Therefore the recommended stand-off (distance bolts) height is 7 mm.

TE0320 has 4 mounting holes, one in each corner. The module can be fixed by screwing M3 screws (ISO 262) into a carrier board through those mounting holes.

TE0320 weighs about 25 g.

5 Power Supply

5.1 Power Supply Range

The power supply range of TE0320 is 4.0 V to 7.0 V.

5.2 Power Supply Sources

TE0320 can be power supplied in two ways:

- through USB connector J1,
- through B2B connector JM5 (pins 1 to 4).

The power supply source is determined by assembly option. See Figure 5.

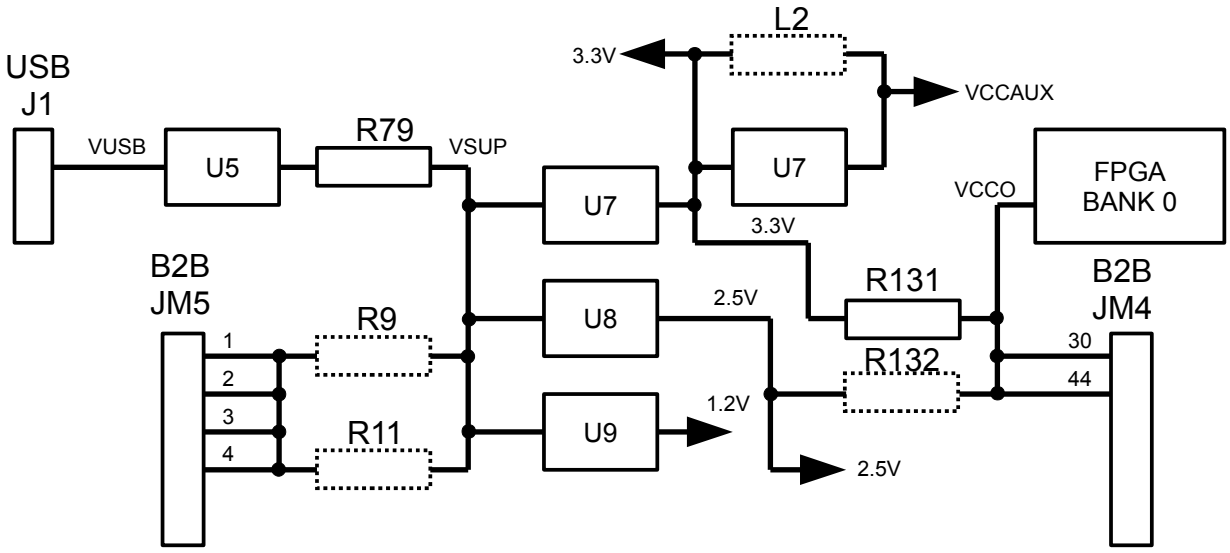

Figure 5: Power supply options diagram

If resistors R9 and R11 are populated and R12 is not populated, then TE0320 is power supplied through JM5 (B2B connector).

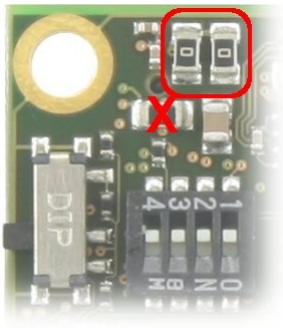

Figure 6: assembly combination for power supply through JM5.

If resistors R9 and R11 are not populated and R12 is populated, then TE0320 is power supplied through J1 (USB bus).

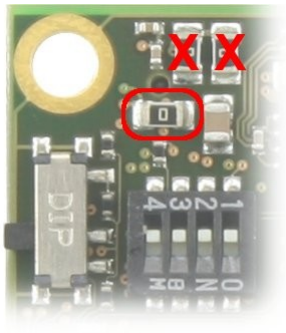

Figure 7: assembly combination for power supply through J1.

Any other assembly combination of R9, R11 and R12 is not allowed.

5.3 On-Board Power Rails

According to the Xilinx Spartan-3A DSP literature, there are the following power supply pin types:

- V_{CCAUX}: dedicated auxiliary power supply pins
- V_{CCINT}: dedicated internal core logic power supply pins
- V_{CCO}: supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.

TE0320 has the following power rails on-board:

- Vsup

  It is the main internal power rail irrespective of the external power supply. It is supplied by either Vb2b or Vusb. It manages power distribution, conversion and supervision. It is routed also to connector JM5 as a user power supply output.
- Vb2b

  It is the main power rail when the module is supplied from B2B connector JM5.
- Vusb

  It is the main power rail when the module is supplied from USB mini-B connector J1. The maximum current than can be provided to J1 is determined by the USB power source.
- 3.3V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the module and connectors JM4 and JM5.
- 2.5V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the DDR SDRAM and connectors JM5.
- 1.2V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the V_{CCINT} power supply pins and connectors JM5.
- VCCAUX

Here there are two assembly options:

(a) if inductor L2 is not populated and the low-noise low drop-out regulator U6 is populated, VCCAUX power rail is supplied with its nominal voltage of 2.5 V. This is the recommended option for noise-sensitive circuitry such as clocking and timing infrastructures.

Figure 8: assembly option for VCCAUX = 2.5 V (bottom view).

(b) if the ferrite bead L2 is populated and U6 is not populated, the 3.3V power rail is simply filtered to generate VCCAUX power rail. This is the recommended option for cost-sensitive applications. In this case

(b.1) ensure the noise level on power rail VCCUAX is suitable to your application;

(b.2) avoid the connection of noise sources to power rail VCCUAX.

Figure 9: assembly option for VCCAUX = 3.3 V (bottom view).

Any other assembly combination of L2 and U6 is not allowed.

- VCCCIO0

VCCCIO0 supplies V_{CCO} to FPGA bank 0. The following assembly options are possible:

(a) if both resistors R131 and R132 are not populated, VCCCIO0 power can be supplied through pins 30 and 44 of B2B connector JM4.

Figure 10: assembly option for VCCAUX = off (bottom view).

Pins 30 and 44 of JM4 are power supply **inputs** in this case.

(b) if resistor R131 is not populated and R132 is populated, VCCCIO0 power rail is set to power rail 2.5V (nominal voltage = 2.5 V).

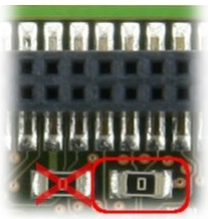

Figure 11: assembly option for VCCAUX = 2.5 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

(c) if resistor R131 is populated and R132 is not populated, VCCCIO0 power rail is set to power rail 3.3V (nominal voltage = 3.3 V). This is the default.

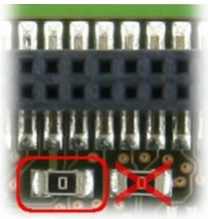

Figure 12: assembly option for VCCCIO0 = 3.3 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

Assembly option where both R131 and R132 are populated is not allowed.

1.2 V, 2.5 V and 3.3 V voltage rails are provided by corresponding step-down regulator DC/DC converters, each one capable of providing up to 3 A of output current. These three regulators are synchronized to switch with 120° phase lag, to improve EMC, and to reduce input ripple. The synchronization circuit can be omitted in cost sensitive applications (please contact Trenz Electronic).

Power supply inputs and outputs are made available at B2B connectors JM4 and JM5 for user applications.

Each pin of B2B connectors JM4 and JM5 is capable of a maximum current of 1.0 A.

power-rail name	nominal voltage (V)	maximum current (A)	power source	system supply	user supply
Vb2b	4.0 to 7.0	4.0 (4 pin × 1.0 A/pin)	JM5	module	-
Vusb	5.0	0.5	J1	module	-
Vsup	4.0 to 7.0	< 0.5	Vusb	3 × DC/DC DC/DC sync power-fail	JM5 (≤1.0 A)
		< 4	Vb2b		
3.3V	3.3	3.0	Vsup ► DC/DC	module	JM4 (≤1.0 A) JM5 (≤1.0 A)
2.5V	2.5	3.0	Vsup ► DC/DC	DDR SDRAM	JM5 (≤1.0 A)
1.2V	1.2	3.0	Vsup ► DC/DC	VCCINT	JM5 (≤1.0 A)
VCCAUX	2.5	0.3	3.3V ► LDO	VCCAUX	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		
VCCCIO0	2.5	< 3.0	2.5V	VCCO (bank 0)	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		JM4 (≤1.0 A)
	1.10 to 3.60	2.0 (2 pin × 1.0 A/pin)	JM4 (30 + 44)		JM4 (30 / 44)

Table 1: On-board power rails summary.

5.4 Power Supervision

5.4.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the rail remains below the threshold voltage (2.93 V). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset. The delay time of 200 ms starts after the rail has risen above the threshold voltage.

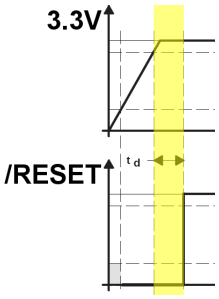

Figure 13: Power-on reset with fixed delay time of 200 ms.

After this delay, the /RESET line is reset high and the FPGA configuration can

start. When the rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again.

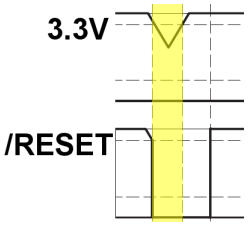

Figure 14: Reset assertion on power drop with fixed delay time of 200 ms.

5.4.2 Power Fail

TE0320 integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring Vsup power rail.

An additional power-fail circuit can be used, to monitor the input voltage. At 4.4V, a power-fail signal (/PFO) is sent to the FPGA. Should you wish or need another threshold voltage, please contact Trenz Electronic.

6 Inputs and Outputs

6.1 Board-to-Board Connectors

The module has two B2B (board-to-board) connectors (JM4 and JM5) with the following features:

- gender: female
- overall number of contacts: 160
- contacts per connector: 80
- rows per connector: 2
- pitch: 1.27 mm = 50 mil = .050"

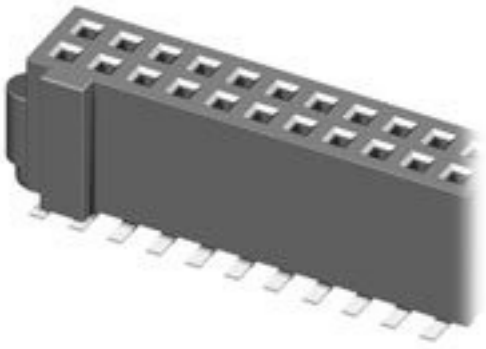

Figure 15: Board to board connector assembled on the TE0320.

Trenz Electronic recommends to mate the standard B2B connectors with the following ones:

- 2 x W+P 6110-080-00-10-PPTR
  1.27 mm (50 mil = .050") pitch 80-pin double row boxed plug (male) header board-to-board (B2B) connectors.

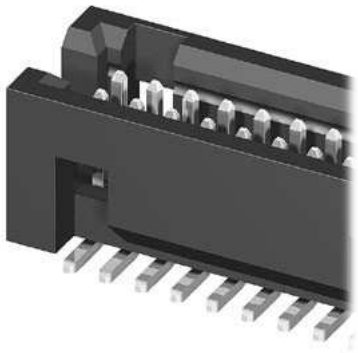

Figure 16: Close-up of the recommended mating B2B connector.

This connector couple offers the following two advantages:

- the module is protected against polarity inversion;
- the connection presents a mechanical resistance sufficient for most applications.

Ordering codes for connectors JM4 / JM5 and their mating connectors are given

in Table 2.

	gender	W+P	Trenz Electronic
B2B connector JM4 + JM5	female	6060-080-46-00-10-10-PPTR	23758
B2B mating connector	male	6110-080-00-10-PPTR	23749

Table 2: Ordering codes of recommended B2B connectors.

The mating height of connectors 6060-080-46-00-10-10-PPTR and 6110-080-00-10-PPTR is 6mm.

Connectors JM4 and JM5 can mate also with any 1.27 mm (50 mil = .050") pitch male header connectors with up to 2 × 40 pins. Figure 17.

Figure 17: sample matching header connector.

Connectors JM4 and JM5 and are placed on the bottom side of the module as shown in Figure 18.

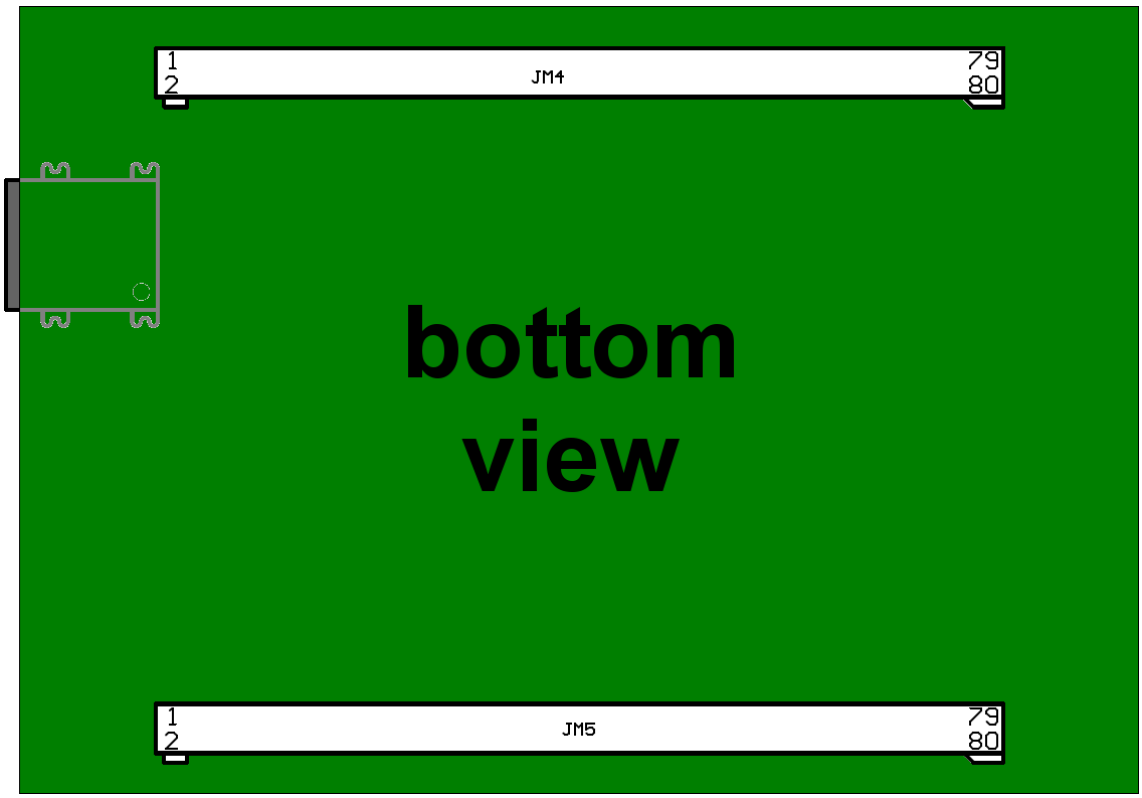

Figure 18: female header connectors JM4 and JM5 (bottom view).

6.2 USB Interface

USB communication can be performed in one of the following two ways:

- through a USB connector
- through USB lines at one B2B connector.

Only one connection type at one time is allowed.

6.2.1 USB Connector

TE0320 is provided with a USB mini-B receptacle (device) connector J1 on the top side.

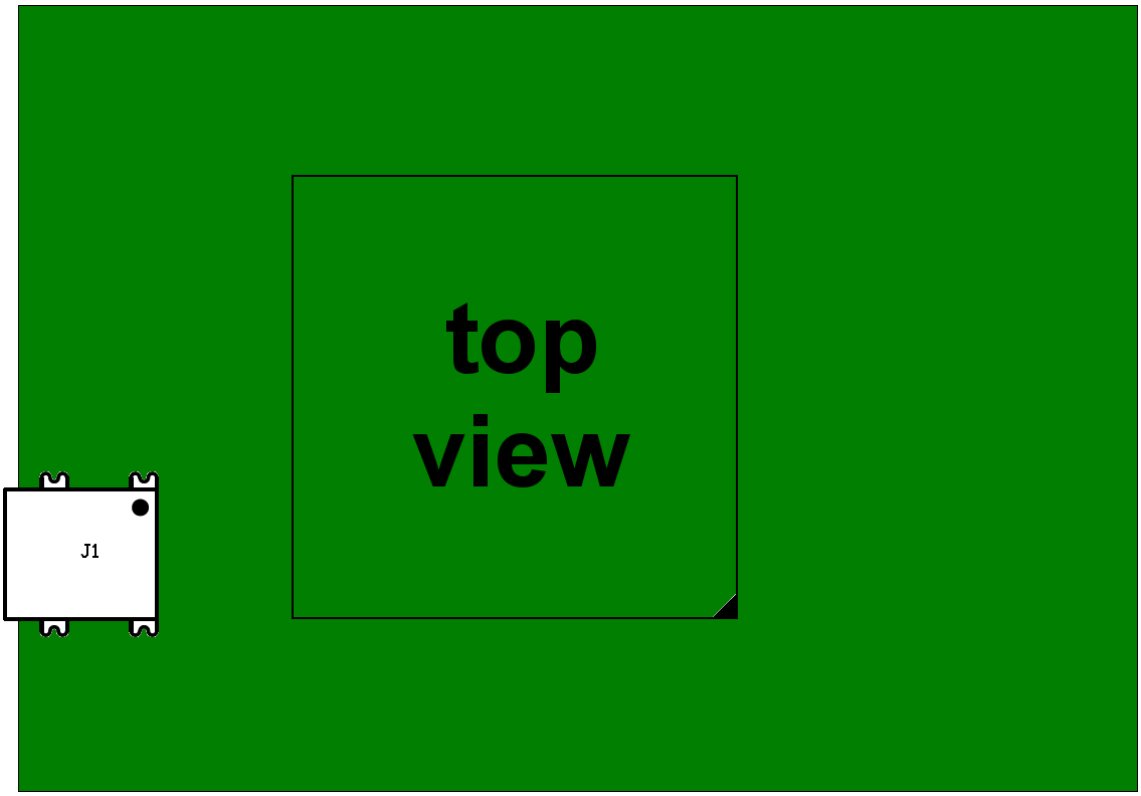

Figure 19: USB connector (top view).

Figure 20: USB mini-B receptacle (device) connector.

Figure 21 shows a sample USB connection between computer and TE0320 for both configuration and operation. The USB cable provides for

- Power supply.
- Configuration by means of the Firmware Upgrade Tool (FUT), recommended for field upgrades. Please use a dedicated JTAG Adapter during development.
- Data communication channel during operation.

Figure 21: sample USB connection (TE0320 side).

In order to minimize the stub on USB lines and improve communication quality, the connection to both USB pins of B2B connector JM4 can be interrupted by removing resistors R3 and R4.

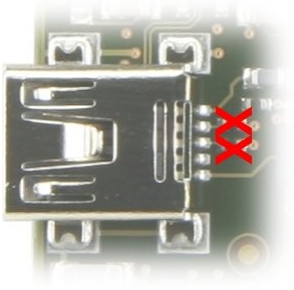

Figure 22: resistors R3 and R4 removed for lower stub on USB lines.

Should you require a module version without connector J1, please contact Trenz Electronic.

6.2.2 USB Pins

USB communication can be performed over 2 pins of B2B connector JM4 as

detailed in Table 3. Ensure resistors R3 and R4 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

pin number	pin name	signal name	description
4	B2B_D_P	D_P	USB data + (D+)
6	B2B_D_N	D_N	USB data - (D-)

Table 3: USB pins at B2B connector JM4.

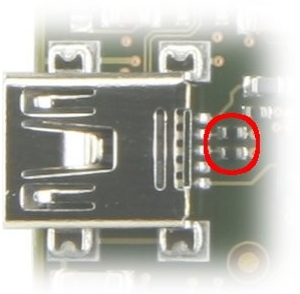

Figure 23: Resistors R3 and R4 required for USB communication over B2B connector JM4.

6.3 JTAG Interface

6.3.1 JTAG connector J2

JTAG signals are available on the gender-inverted standard 6-pin JTAG header connector J2 as shown in Figure 24.

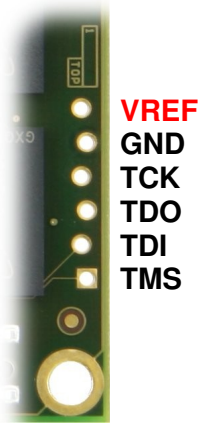

Figure 24: JTAG connector J2.

To connect your computer to JTAG connector J2 you typically need

- a JTAG cable with standard 6-pin JTAG female header;
- a 2.54 mm pitch 1 × 6 pin gender changer header.

Some examples of JTAG cable set are listed in Table 4.

JTAG cable	flying leads	software	gender changer
Xilinx Platform Cable USB	included	Xilinx iMPACT	1 × 6 pin
Digilent XUP USB-JTAG Programming Cable	XUP Fly Wire Assembly	Xilinx iMPACT	1 × 6 pin

Digilent JTAG-USB Full Speed Module	not needed	Digilent Adept 2.0	1 × 6 pin

Table 4: some examples of JTAG cable set.

Figure 25 shows a standard 6-pin JTAG female header, in this case flying leads, with a gender changer header.

Figure 26 shows how a JTAG cable, in this case a Xilinx Platform Cable USB with flying leads and gender changer, is connected to a TE0320.

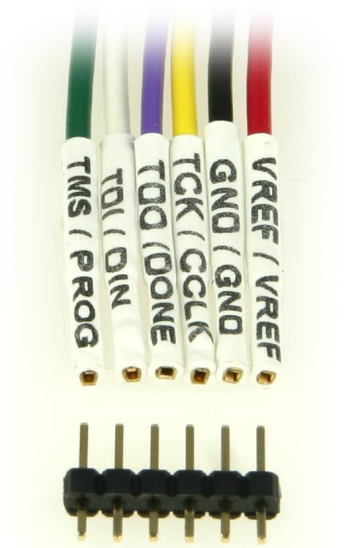

Figure 25: standard 6-pin JTAG female header with gender changer.

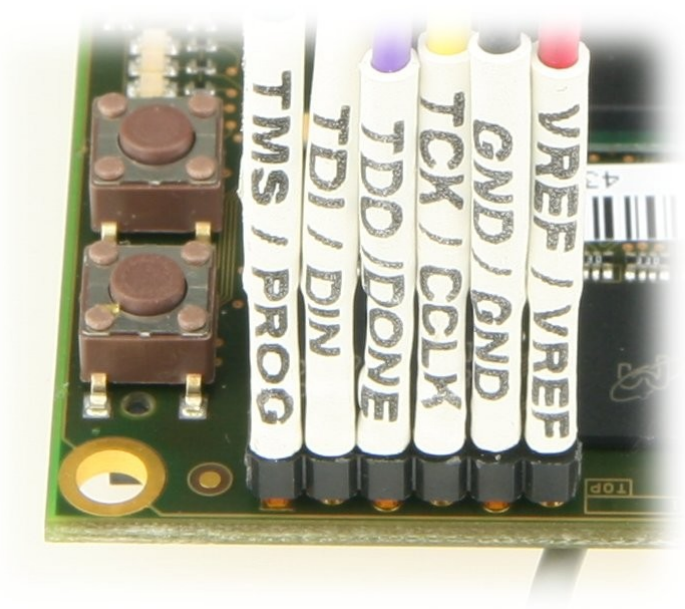

Figure 26: sample JTAG cable connection ((TE0320 side).

Figure 27 shows a recommended set-up for TE0320 configuration and operation. The USB cable provides for power supply and data communication channel. The JTAG is ideal for quick configuration and effective debugging.

Figure 27: recommended TE0320 set-up.

6.3.2 JTAG lines at B2B connector JM4

JTAG signal lines are also available at B2B connector JM4. See Table 40 for additional information on these signals.

6.4 I2C bus

TE0320 has a flexible I2C bus on-board as outlined in Figure 28.

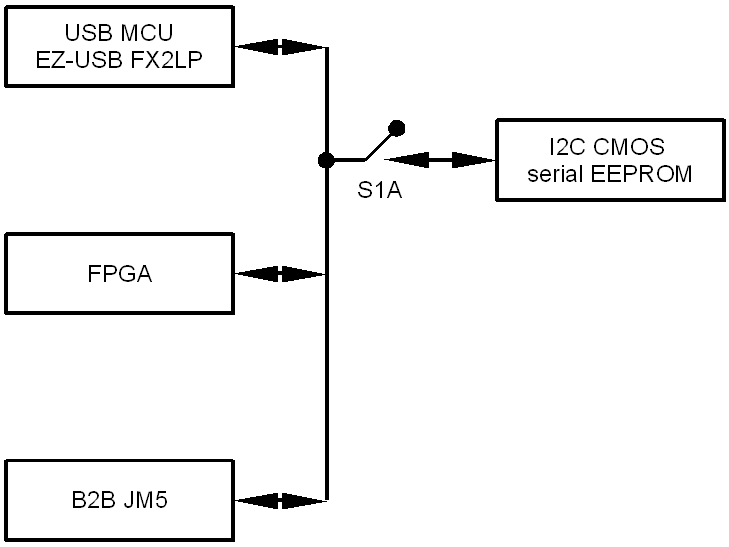

Figure 28: I2C bus topology.

The I2C signals on the TE0320 are listed and described in Table 5.

name	definition	description
SDA	serial data	This is a bidirectional pin used to transfer addresses and data into and out of a device.
SCL	serial clock	This signal is used to synchronize the data transfer to and from a device.

Table 5: I2C signals summary.

The I2C bus is typically used by the USB microcontroller to write USB firmware to the serial EEPROM. In this case,

- the I2C port of the FPGA must be set in slave mode (SCL pin as input),
- the device attached to the I2C port of B2B JM5 connector must be set to slave mode.

The USB microcontroller can operate just in I2C master mode (default operation). If the user wants to set another device attached to the I2C bus as master device, the USB microcontroller shall three-state (Z = high impedance) its SCL and SDA pins.

If the FPGA is set to I2C master mode, it can write to or read from serial EEPROM (always slave mode) and B2B connector JM5 (attached device set to slave mode).

If the device attached to the I2C port of B2B JM5 connector is set to master mode, it can write to or read from serial EEPROM (always slave mode) and FPGA I2C port (set to slave mode).

Possible I2C operation modes are summarized in Table 6.

core	EZ-USB FX2LP	FPGA (SDA = I/O)	B2B JM5	serial EEPROM
default	**master**	slave SCL = I	slave	slave
custom	inactive SCL = SDA = Z	**master** SCL = O	slave	slave
custom	inactive SCL = SDA = Z	slave SCL = I	**master**	slave

Table 6: I2C bus modes summary.

TE0320 reference design includes an HDL core managing the fast mode (400 kHz) I2C communication between the Xilinx MicroBlaze embedded soft-processor and the EZ-USB FX2LP USB microcontroller.

I2C pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os),
as these bus signals are pulled up to 3.3V.

6.5 SPI bus

TE0320 has a flexible SPI bus on-board as outlined in Figure 29.

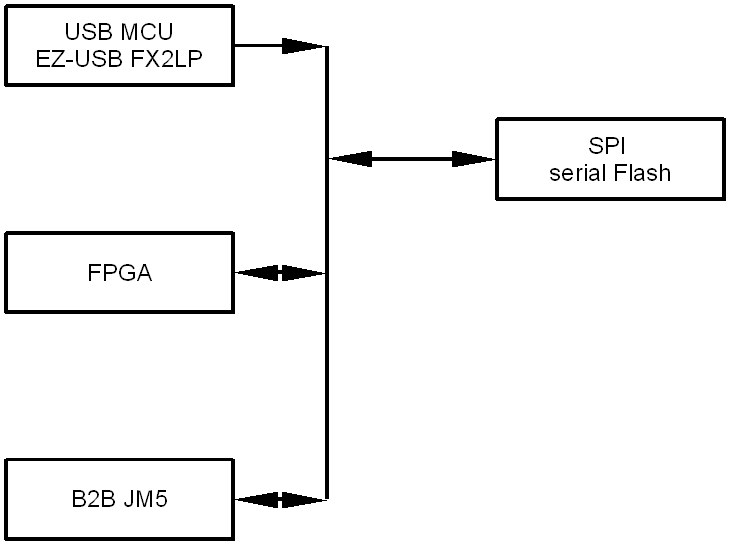

Figure 29: SPI bus topology.

SPI signals on the TE0320 are listed and described in Table 7.

name	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is **high,** the device is **disabled** and SPI_Q is at high impedance (Z).
		When this input signal is **low**, the device is **enabled.**
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

Table 7: SPI signals summary.

SPI signal pin-out of the TE0320 is summarized in Table 8.

name	FPGA ball	JM5 pin
SPI_Q	AF24	18
SPI_D	AB15	12
SPI_/C	AE24	22
SPI_/S	AA7	20

Table 8: SPI pin-out summary.

SPI pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table 9 and Table 10. Any other usage of the SPI bus is neither supported nor recommended.

6.5.1 SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

(d) EZ-USB ► Flash
the USB microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)

(e) FPGA ◄ Flash
the FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.

In case (b), the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
EZ-USB ► Flash	FUT API	**master**	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA ◄ Flash	FUT API	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave
B2B JM5 ► Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 0)	slave

Table 9: SPI bus modes for configuration.

The PROM file (containing the FPGA configuration bitstream) can be written to the SPI serial Flash memory (slave) also through the SPI pins of B2B connector JM5 (attached device set to master mode). In this case, the FPGA shall be turned off or three-stated to release its shared SPI pins and the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

6.5.2 SPI bus for operation

A plurality of usage combinations of the SPI bus during operation is made available to the user as suggested in Table 10.

description	usage	EZ-USB FX2LP	FPGA	B2B JM5	serial Flash
EZ-USB ◄► Flash	custom	**master**	off (S2 = FX2PON, FX2_PS_EN = 0)	deselected	slave
FPGA ◄► Flash	custom	inactive SPI_* = Z	**master** (SPI_/S = 1)	deselected	slave
B2B JM5 ◄► Flash	custom	inactive SPI_* = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 0)	slave
EZ-USB ◄► B2B JM5	custom	**master** SPI_/S = 1	off (S2 = FX2PON, FX2_PS_EN = 0)	slave	deselected
EZ-USB ◄► B2B JM5	custom	slave SPI_/C = Z	off (S2 = FX2PON, FX2_PS_EN = 0)	**master** (SPI_/S = 1)	deselected

Table 10: SPI bus modes for operation.

Other combinations of master and slave units are neither supported nor recommended.

6.6 LEDs

6.6.1 System LED D1

LED D1 is connected to the DONE pin. The DONE pin is powered by the VCCAUX supply.

The FPGA actively drives the DONE pin Low during configuration. Thus, LED D1 is unconditionally turned off during configuration.

To have LED D1 turned on or off after successful configuration, please see paragraph 11 Recommended Design Tools Settings.

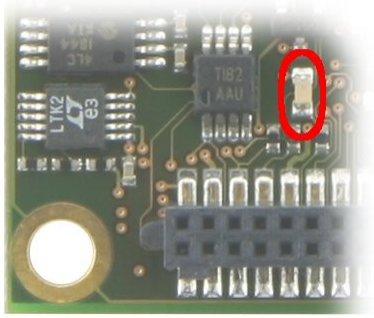

Figure 30: DONE LED D1 (bottom side).

6.6.2 User LEDs D[5:8]

TE0320 is provided with 4 user LEDs. A LED is lit when the corresponding signal listed in Table 11 is set high (logical 1).

LED	signal	FPGA ball	FPGA pin	bank
D5	UL1	R20	IO_L22N_1	1
D6	UL2	V23	IO_L21P_1	1
D7	UL3	R19	IO_L22P_1	1
D8	UL4	U24	IO_L23N_1 VREF_1	1

Table 11: user LEDs signal details..

6.7 Push-Buttons S[3:4]

TE0320 is provided with 2 user buttons. A signal listed in Table 12 is set low (logical 0) when a push button is pressed, and vice-versa.

switch	signal	FPGA ball	FPGA pin	bank	default input	input when pressed
S3	PB1	U23	IO_L23P_1	1	logical 1	logical 0
S4	PB2	R22	IO_L25N_1	1	logical 1	logical 0

Table 12: user push-buttons signal details.

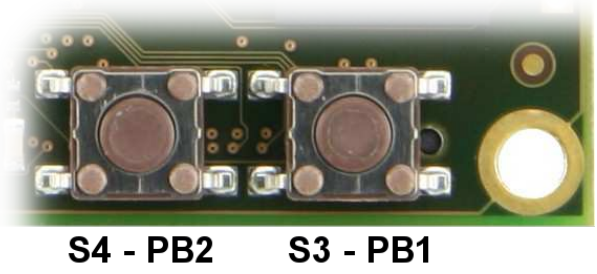

Figure 31: push buttons PB1 and PB2.

Warning! on some boards, PB1 and PB2 labels might be exchanged. Please take Figure 31 as reference.

6.8 Switches

TE0320 is provided with the following slide switches:

- S1: 4 x DIP slide switches (system)
- S2: 1 x slide switch (system)
- S5: 8 × DIP slide switches (user)

6.8.1 DIP Slide Switches S1[A:D]

TE0320 is provided with 4 system DIP slide switches as shown in Figure 32: S1A, S1B, S1C, S1D.

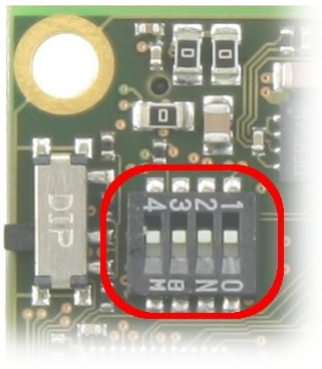

Figure 32: DIP slide switches S1[A:D].

Please note the 4 switch labels are on one side and the <ON> label is on the opposite side.

DIP slide switches S1[A:D] condition the value of some system signals as described in Table 13.

switch	S1 label	signal name	<OFF>	<ON>
S1A	1	EEPROM serial data	the USB microcontroller CANNOT read / write the serial EEPROM	the USB microcontroller can read / write the serial EEPROM
S1B	2	M2	mode pin M2 = 1	M2 = 0
S1C	3	M1	mode pin M1 = 1	M1 = 0
S1D	4	/MR (master reset)	module reset	module running

Table 13: S1X settings description.

DIP slide switches S1A is ON by default, to allow the USB microcontroller to read the serial EEPROM and enumerate as a custom/specific USB device. When DIP slide switches S1A is ON, the USB microcontroller can (re)write the serial EEPROM to, for example, store a (new) custom/specific firmware. When DIP slide switch is OFF, the USB microcontroller cannot read the serial EEPROM and enumerates as a generic USB device.