Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Introduction

Zynq™-7000 All Programmable SoCs are available in -3, -2, and -1 speed grades, with -3 having the highest performance. Zynq-7000 device DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in the commercial, extended, or industrial temperature ranges.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Zynq-7000 AP SoC (XC7Z030, XC7Z045, and XC7Z100) data sheet, part of an overall set of documentation on the Zynq-7000 devices, is available on the Xilinx website at www.xilinx.com/zynq. All specifications are subject to change without notice.

DC Characteristics

Table 1: **Absolute Maximum Ratings** [1]

Symbol	Description	Min	Max	Units
Processing System (PS)				
V_{CCPINT}	PS primary logic supply	−0.5	1.1	V
V_{CCPAUX}	PS auxiliary supply voltage	−0.5	2.0	V
V_{CCPLL}	PS PLL supply	−0.5	2.0	V
V_{CCO_DDR}	PS DDR I/O supply	−0.5	2.0	V
V_{CCO_MIO}[2]	PS MIO I/O supply	−0.5	3.6	V
V_{PREF}	PS input reference voltage	−0.5	2.0	V
V_{PIN}[2][3][4][5][6]	PS DDR and MIO I/O input voltage	−0.5	V_{CCO_DDR} + 0.5 V_{CCO_MIO} + 0.5	V
	PS DDR and MIO I/O input voltage for V_{REF} and differential I/O standards	−0.5	2.625	V
Programmable Logic (PL)				
V_{CCINT}	PL internal supply voltage	−0.5	1.1	V
V_{CCAUX}	PL auxiliary supply voltage	−0.5	2.0	V
V_{CCBRAM}	PL supply voltage for the block RAM memories	−0.5	1.1	V
V_{CCO}	PL output drivers supply voltage for 3.3V HR I/O banks	−0.5	3.6	V
	PL output drivers supply voltage for 1.8V HP I/O banks	−0.5	2.0	V
V_{CCAUX_IO}	Auxiliary supply voltage	−0.5	2.06	V
V_{REF}	Input reference voltage	−0.5	2.0	V
V_{IN}[3][4][5][6]	I/O input voltage	−0.5	V_{CCO} + 0.5	V
	I/O input voltage for V_{REF} and differential I/O standards	−0.5	2.625	V

Table 1: **Absolute Maximum Ratings** [1] *(Cont'd)*

Symbol	Description	Min	Max	Units
V_{CCBATT}	Key memory battery backup supply	−0.5	2.0	V
GTX Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTX transmitter and receiver circuits	−0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTX transmitter and receiver termination circuits	−0.5	1.32	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	−0.5	1.935	V
$V_{MGTREFCLK}$	GTX transceiver reference clock absolute input voltage	−0.5	1.32	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	−0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	−0.5	1.26	V
I_{DCIN}	DC input current for receiver input pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
I_{DCOUT}	DC output current for transmitter pins DC coupled $V_{MGTAVTT}$ = 1.2V	–	14	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	−0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	−0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	−65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies [7]	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies [7]	–	+260	°C
T_j	Maximum junction temperature [7]	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
3. The lower absolute voltage specification always applies.
4. For I/O operation, refer to UG471: *7 Series FPGAs SelectIO Resources User Guide* or UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*.
5. The maximum limit applied to DC signals.
6. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
7. For soldering guidelines and thermal considerations, see UG865, *Zynq-7000 All Programmable SoC Packaging and Pinout Specification*.

Table 2: **Recommended Operating Conditions** [1][2]

Symbol	Description	Min	Typ	Max	Units
PS					
V_{CCPINT}[3]	PS internal supply voltage	0.95	1.00	1.05	V
V_{CCPAUX}	PS auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCPLL}	PS PLL supply voltage	1.71	1.80	1.89	V
V_{CCO_DDR}	PS DDR supply voltage	1.14		1.89	V
V_{CCO_MIO}[4]	PS supply voltage for MIO banks	1.71	–	3.465	V
V_{PIN}[5]	PS DDR and MIO I/O input voltage	−0.20	–	V_{CCO_DDR} + 0.20 V_{CCO_MIO} + 0.20	V
	PS DDR and MIO I/O input voltage for V_{REF} and differential I/O standards	−0.20	–	2.625	V

Table 2: **Recommended Operating Conditions [1][2] *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
PL					
V_{CCINT}	Internal supply voltage	0.97	1.00	1.03	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCBRAM}	Block RAM supply voltage	0.97	1.00	1.03	V
V_{CCO}[6][7]	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN}[5]	I/O input voltage	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage for V_{REF} and differential I/O standards	–0.20	–	2.625	
I_{IN}[8]	Maximum current through any (PS or PL) pin in a powered or unpowered bank when forward biasing the clamp diode	–	–	10	mA
V_{CCBATT}[9]	Battery voltage	1.0	–	1.89	V
GTX Transceiver					
$V_{MGTAVCC}$[10]	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz[11][12]	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	
$V_{MGTAVTT}$[10]	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}$[10]	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V
$V_{MGTAVTTRCAL}$[10]	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:
1. All voltages are relative to ground. The PL and PS share a common ground.
2. For the design of the power distribution system consult UG933, *Zynq-7000 All Programmable SoC PCB Design and Pin Planning Guide.*
3. When the processor cores operate $F_{CPU\_6X4X\_621\_MAX}$ at 1 GHz (-3E speed grade), the V_{CCPINT} minimum is 0.97V and the V_{CCPINT} maximum is 1.03V.
4. Applies to both MIO supply banks V_{CCO_MIO0} and V_{CCO_MIO1}.
5. The lower absolute voltage specification always applies.
6. Configuration data is retained even if V_{CCO} drops to 0V.
7. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
8. A total of 200 mA per PS or PL bank should not be exceeded.
9. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
10. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs GTX/GTH Transceivers User Guide.*
11. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
12. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}[2]	PL die input capacitance at the pad	–	–	8	pF
C_{PIN}[2]	PS die input capacitance at the pad	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40) for commercial (C), industrial (I), and extended (E) temperature devices	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50) for commercial (C), industrial (I), and extended (E) temperature devices	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60) for commercial (C), industrial (I), and extended (E) temperature devices	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PS I/O and 3.3V HR I/O Banks[1]**

AC Voltage Overshoot	% of UI @−40°C to 100°C	AC Voltage Undershoot	% of UI @−40°C to 100°C
V_{CCO} + 0.40	100	−0.40	100
V_{CCO} + 0.45	100	−0.45	61.7
V_{CCO} + 0.50	100	−0.50	25.8
V_{CCO} + 0.55	100	−0.55	11.0
V_{CCO} + 0.60	46.6	−0.60	4.77
V_{CCO} + 0.65	21.2	−0.65	2.10
V_{CCO} + 0.70	9.75	−0.70	0.94
V_{CCO} + 0.75	4.55	−0.75	0.43
V_{CCO} + 0.80	2.15	−0.80	0.20
V_{CCO} + 0.85	1.02	−0.85	0.09
V_{CCO} + 0.90	0.49	−0.90	0.04
V_{CCO} + 0.95	0.24	−0.95	0.02

Notes:
1. A total of 200 mA per bank should not be exceeded.

Table 5: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for PL 1.8V HP I/O Banks[1][2]**

AC Voltage Overshoot	% of UI @−40°C to 100°C	AC Voltage Undershoot	% of UI @−40°C to 100°C
V_{CCO} + 0.40	100	−0.40	100
V_{CCO} + 0.45	100	−0.45	100
V_{CCO} + 0.50	100	−0.50	100
V_{CCO} + 0.55	100	−0.55	100
V_{CCO} + 0.60	50.0	−0.60	50.0
V_{CCO} + 0.65	50.0	−0.65	50.0
V_{CCO} + 0.70	47.0	−0.70	50.0
V_{CCO} + 0.75	21.2	−0.75	50.0
V_{CCO} + 0.80	9.71	−0.80	50.0
V_{CCO} + 0.85	4.51	−0.85	28.4
V_{CCO} + 0.90	2.12	−0.90	12.7
V_{CCO} + 0.95	1.01	−0.95	5.79

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
$I_{CCPINTQ}$	PS quiescent V_{CCPINT} supply current	XC7Z030	122	122	122	mA
		XC7Z045	122	122	122	mA
		XC7Z100				mA
$I_{CCPAUXQ}$	PS quiescent V_{CCPAUX} supply current	XC7Z030	13	13	13	mA
		XC7Z045	13	13	13	mA
		XC7Z100				mA
I_{CCDDRQ}	PS quiescent V_{CCO_DDR} supply current	XC7Z030	4	4	4	mA
		XC7Z045	4	4	4	mA
		XC7Z100				mA
I_{CCINTQ}	PL quiescent V_{CCINT} supply current	XC7Z030	246	246	246	mA
		XC7Z045	611	611	611	mA
		XC7Z100				mA
I_{CCAUXQ}	PL quiescent V_{CCAUX} supply current	XC7Z030	56	56	56	mA
		XC7Z045	131	131	131	mA
		XC7Z100				mA
I_{CCAUX_IOQ}	PL quiescent V_{CCAUX_IO} supply current	XC7Z030	2	2	2	mA
		XC7Z045	2	2	2	mA
		XC7Z100				mA
I_{CCOQ}	PL quiescent V_{CCO} supply current	XC7Z030	4	4	4	mA
		XC7Z045	4	4	4	mA
		XC7Z100				mA
$I_{CCBRAMQ}$	PL quiescent V_{CCBRAM} supply current	XC7Z030	11	11	11	mA
		XC7Z045	23	23	23	mA
		XC7Z100				mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate static power consumption for conditions other than those specified.

PS Power-On/Off Power Supply Requirements

The recommended power-on sequence is V_{CCPINT}, V_{CCPAUX} and V_{CCPLL} together, then the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCPAUX}, V_{CCPLL} and the PS V_{CCO} supplies (V_{CCO_MIO0}, V_{CCO_MIO1}, and V_{CCO_DDR}) have the same recommended voltage levels, then they can be powered by the same supply and ramped simultaneously. Xilinx recommends powering V_{CCPLL} with the same supply as V_{CCPAUX}, with an optional ferrite bead filter.

For V_{CCO_MIO0} and V_{CCO_MIO1} voltages of 3.3V:

- The voltage difference between V_{CCO_MIO0} /V_{CCO_MIO1} and V_{CCPAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

PS Power-on Reset

The PS provides the power on reset (PS_POR_B) input signal which must be held Low until all PS power supplies are stable and within operating limits. Additionally, PS_POR_B must be held Low until PS_CLK is stable for 2,000 clocks.

PL Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to $0.3 \times T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to $0.3 \times T_{VCCINT}$ (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

PS—PL Power Sequencing

The PS and PL power supplies are fully independent. There are no sequencing requirements between the PS (V_{CCPINT}, V_{CCPAUX}, V_{CCPLL}, V_{CCO_DDR}, V_{CCO_MIO0}, and V_{CCO_MIO1}) and PL (V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCO}, V_{CCAUX_IO}, $V_{MGTAVCC}$, $V_{MGTAVTT}$, $V_{MGTVCCAUX}$, and V_{CCADC}) power supplies.

Power Supply and PS Reset Requirements

Table 7 shows the minimum current, in addition to I_{CCQ}, that is required by Zynq-7000 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The Zynq-7000 device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 7: **Power-On Current for Zynq-7000 Devices[1]**

Device	$I_{CCPINTMIN}$ Typ[2]	$I_{CCPAUXMIN}$ Typ[2]	$I_{CCDDRMIN}$ Typ[2]	$I_{CCINTMIN}$ Typ[2]	$I_{CCAUXMIN}$ Typ[2]	I_{CCOMIN} Typ[2]	I_{CCAUX_IOMIN} Typ[2]	$I_{CCBRAMMIN}$ Typ[2]	Units
XC7Z030	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 900 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XC7Z045	$I_{CCPINTQ}$ + 70 mA	$I_{CCPAUXQ}$ + 40 mA	I_{CCDDRQ} + 130 mA per bank	I_{CCINTQ} + 1400 mA	I_{CCAUXQ} + 60 mA	I_{CCOQ} + 90 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90 mA	mA
XC7Z100									mA

Notes:

1. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to calculate maximum power-on currents.
2. Typical values are specified at nominal voltage, 25°C.

Table 8: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCPINT}$	Ramp time from GND to 90% of V_{CCPINT}		0.2	50	ms
$T_{VCCPAUX}$	Ramp time from GND to 90% of V_{CCPAUX}		0.2	50	ms
T_{VCCO_DDR}	Ramp time from GND to 90% of V_{CCO_DDR}		0.2	50	ms
T_{VCCO_MIO}	Ramp time from GND to 90% of V_{CCO_MIO}		0.2	50	ms
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625$V and $V_{CCO\_MIO} - V_{CCPAUX} > 2.625$V	$T_J = 100°C$[1]	–	500	ms
		$T_J = 85°C$[1]	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

PS I/O Levels

Table 9: **PS DC Input and Output Levels**[1]

Bank	I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
		V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
MIO	LVCMOS18	−0.300	35% V_{CCO_MIO}	65% V_{CCO_MIO}	V_{CCO_MIO} + 0.300	0.450	V_{CCO_MIO} − 0.450	8	−8
MIO	LVCMOS25	−0.300	0.700	1.700	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} − 0.400	8	−8
MIO	LVCMOS33	−0.300	0.800	2.000	3.450	0.400	V_{CCO_MIO} − 0.400	8	−8
MIO	HSTL_I_18	−0.300	V_{PREF} − 0.100	V_{PREF} + 0.100	V_{CCO_MIO} + 0.300	0.400	V_{CCO_MIO} − 0.400	8	−8
DDR	SSTL18_I	−0.300	V_{PREF} − 0.125	V_{PREF} + 0.125	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 − 0.470	V_{CCO_DDR}/2 + 0.470	8	−8
DDR	SSTL15	−0.300	V_{PREF} − 0.100	V_{PREF} + 0.100	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 − 0.175	V_{CCO_DDR}/2 + 0.175	13.0	−13.0
DDR	SSTL135	−0.300	V_{PREF} − 0.090	V_{PREF} + 0.090	V_{CCO_DDR} + 0.300	V_{CCO_DDR}/2 − 0.150	V_{CCO_DDR}/2 + 0.150	13.0	−13.0
DDR	HSUL_12	−0.300	V_{PREF} − 0.130	V_{PREF} + 0.130	V_{CCO_DDR} + 0.300	20% V_{CCO_DDR}	80% V_{CCO_DDR}	0.1	−0.1

Notes:

1. Tested according to relevant specifications.

Table 10: **PS Complementary Differential DC Input and Output Levels**

Bank	I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
		V, Min	V,Typ	V, Max	V,Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DDR	DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	−0.100
DDR	DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO_DDR}/2) − 0.150	(V_{CCO_DDR}/2) + 0.150	13.0	−13.0
DDR	DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO_DDR}/2) − 0.175	(V_{CCO_DDR}/2) + 0.175	13.0	−13.0
DDR	DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO_DDR}/2) − 0.470	(V_{CCO_DDR}/2) + 0.470	8.00	−8.00

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q–$\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

PL I/O Levels

Table 11: **SelectIO DC Input and Output Levels**[(1)(2)]

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	8	−8
HSTL_I_12	−0.300	V_{REF} − 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	−6.3
HSTL_I_18	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	8	−8
HSTL_II	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	16	−16
HSTL_II_18	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	16	−16
HSUL_12	−0.300	V_{REF} − 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	−0.1
LVCMOS12	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	−0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} − 0.450	Note 5	Note 5
LVCMOS25	−0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} − 0.400	Note 6	Note 6
LVCMOS33	−0.300	0.800	2.000	3.450	0.400	V_{CCO} − 0.400	Note 6	Note 6
LVTTL	−0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	−0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	−0.1
PCI33_3	−0.500	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	−0.5
SSTL12	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 − 0.150	V_{CCO}/2 + 0.150	14.25	−14.25
SSTL135	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 − 0.150	V_{CCO}/2 + 0.150	13.0	−13.0
SSTL135_R	−0.300	V_{REF} − 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 − 0.150	V_{CCO}/2 + 0.150	8.9	−8.9
SSTL15	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 − 0.175	V_{CCO}/2 + 0.175	13.0	−13.0
SSTL15_R	−0.300	V_{REF} − 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 − 0.175	V_{CCO}/2 + 0.175	8.9	−8.9
SSTL18_I	−0.300	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 − 0.470	V_{CCO}/2 + 0.470	8	−8
SSTL18_II	−0.300	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 − 0.600	V_{CCO}/2 + 0.600	13.4	−13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in 3.3V I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see UG471: *7 Series FPGAs SelectIO Resources User Guide*.

Table 12: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–		Note 5	
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 14.
7. LVDS is specified in Table 15.

Table 13: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

Table 14: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information.

Table 15: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in ISE® Design Suite 14.5 v1.06 and Vivado® Design Suite 2013.1 v1.06 for the -3, -2, and -1 speed grades.

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Zynq-7000 devices.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 16 correlates the current status of each Zynq-7000 device on a per speed grade basis.

Table 16: **Zynq-7000 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	**Preliminary**	**Production**
XC7Z030		-3	-2, -1
XC7Z045		-3	-2, -1
XC7Z100		-2, -1	

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 17 lists the production released Zynq-7000 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 17: **Zynq-7000 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations		
	-3	-2	-1
XC7Z030		ISE 14.5 v1.06 and Vivado 2013.1 v1.06	
XC7Z045		ISE 14.5 v1.06 and Vivado 2013.1 v1.06	
XC7Z100			

Notes:
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

PS Performance Characteristics

For further design requirement details, refer to UG585, *Zynq-7000 All Programmable SoC Technical Reference Manual*.

Table 18: **CPU Clock Domains Performance**

Symbol	Clock Ratio	Description	Speed Grade			Units
			-3	-2	-1	
$F_{CPU\_6X4X\_621\_MAX}$[1][2]	6:2:1	Maximum CPU clock frequency	1000	733	667	MHz
$F_{CPU\_3X2X\_621\_MAX}$		Maximum CPU_3X clock frequency	500	367	333	MHz
$F_{CPU\_2X\_621\_MAX}$		Maximum CPU_2X clock frequency	333	244	222	MHz
$F_{CPU\_1X\_621\_MAX}$		Maximum CPU_1X clock frequency	167	122	111	MHz
$F_{CPU\_6X4X\_421\_MAX}$[1]	4:2:1	Maximum CPU clock frequency	710	600	533	MHz
$F_{CPU\_3X2X\_421\_MAX}$		Maximum CPU_3X clock frequency	355	300	267	MHz
$F_{CPU\_2X\_421\_MAX}$		Maximum CPU_2X clock frequency	355	300	267	MHz
$F_{CPU\_1X\_421\_MAX}$		Maximum CPU_1X clock frequency	178	150	133	MHz

Notes:
1. The maximum frequency during BootROM execution is 500 MHz across all speed specifications.
2. When the processor cores operate $F_{CPU\_6X4X\_621\_MAX}$ at 1 GHz (-3E speed grade), the V_{CCPINT} minimum is 0.97V and the V_{CCPINT} maximum is 1.03V.

Table 19: **PS DDR Clock Domains Performance**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F_{DDR3_MAX}	Maximum DDR3 interface performance	1333	1066	1066	Mb/s
F_{DDR3L_MAX}	Maximum DDR3L interface performance	800	800	800	Mb/s
F_{DDR2_MAX}	Maximum DDR2 interface performance	800	800	800	Mb/s
F_{LPDDR2_MAX}	Maximum LPDDR2 interface performance	800	800	800	Mb/s
F_{DDRCLK_2XMAX}	Maximum DDR_2X clock frequency	444	408	355	MHz

Notes:
1. All performance numbers apply to both internal and external V_{REF} configurations.

PS Switching Characteristics

Clocks

Table 20: **System Reference Clock Input Requirements**

Symbol	Description	Min	Typ	Max	Units
$T_{JTPSCLK}$	PS_CLK RMS clock jitter tolerance	–	–	±0.5	%
$T_{DCPSCLK}$	PS_CLK duty cycle	40	–	60	%
$T_{RFPSCLK}$	PS_CLK rise and fall time	–	4	–	ns
F_{PSCLK}	PS_CLK frequency	30	–	60	MHz

Notes:

1. Tested to commercial (C) and extended (E) temperature ranges only. See Temperature in Table 2.

Table 21: **PS PLL Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T_{LOCK_PSPLL}	PLL maximum lock time	60	60	60	µs
F_{PSPLL_MAX}	PLL maximum output frequency	2000	1800	1600	MHz
F_{PSPLL_MIN}	PLL minimum output frequency	780	780	780	MHz

Resets

Table 22: **PS Reset Requirements**

Symbol	Description	Min	Typ	Max	Units
T_{PSPOR}	Required PS_POR_B assertion time[1]	100	–	–	µs
T_{PSRST}	Required PS_SRST_B assertion time	3	–	–	PS_CLK Clock Cycles

Notes:

1. PS_POR_B needs to be asserted low until PS supply voltages reach minimum levels.

PS Configuration

Table 23: **Processor Configuration Access Port Switching Characteristics**

Symbol	Description	Min	Typ	Max	Units
F_{PCAPCK}	Maximum processor configuration access port (PCAP) frequency	–	–	100	MHz

DDR Memory Interfaces

Table 24: **DDR3 Interface Switching Characteristics (1333 Mb/s)**[1]

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	95	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	222	–	ps
T_{DQSS}	Output clock to DQS skew	–0.11	0.08	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	465	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	528	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

Table 25: **DDR3 Interface Switching Characteristics (1066 Mb/s)**[1]

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	100	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	315	–	ps
T_{DQSS}	Output clock to DQS skew	–0.10	0.10	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	560	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	658	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.5V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses $V_{IH}(AC)$ or the falling edge of DQ that crosses $V_{IL}(AC)$ to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses $V_{IL}(DC)$ or the falling edge of DQ that crosses $V_{IH}(DC)$ to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IH}(AC)$ or the falling edge of CMD/ADDR that crosses $V_{IL}(AC)$ to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses $V_{IL}(DC)$ or the falling edge of CMD/ADDR that crosses $V_{IH}(DC)$ to V_{REF} of CLK.

Table 26: **DDR3L Interface Switching Characteristics (800 Mb/s)**[1]

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	321	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	380	–	ps
T_{DQSS}	Output clock to DQS skew	–0.12	0.04	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	636	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	853	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.35V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 27: **LPDDR2 Interface Switching Characteristics (800 Mb/s)**[1]

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	111	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	318	–	ps
T_{DQSS}	Output clock to DQS skew	0.91	1.10	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	132	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	363	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 28: **LPDDR2 Interface Switching Characteristics (400 Mb/s)[1]**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	561	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	852	–	ps
T_{DQSS}	Output clock to DQS skew	0.91	1.08	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	617	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	918	–	ps

Notes:
1. Recommended V_{CCO_DDR} = 1.2V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.

Table 29: **DDR2 Interface Switching Characteristics (800 Mb/s)[1]**

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	147	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	376	–	ps
T_{DQSS}	Output clock to DQS skew	–0.07	0.08	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	732	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	938	–	ps

Notes:
1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.
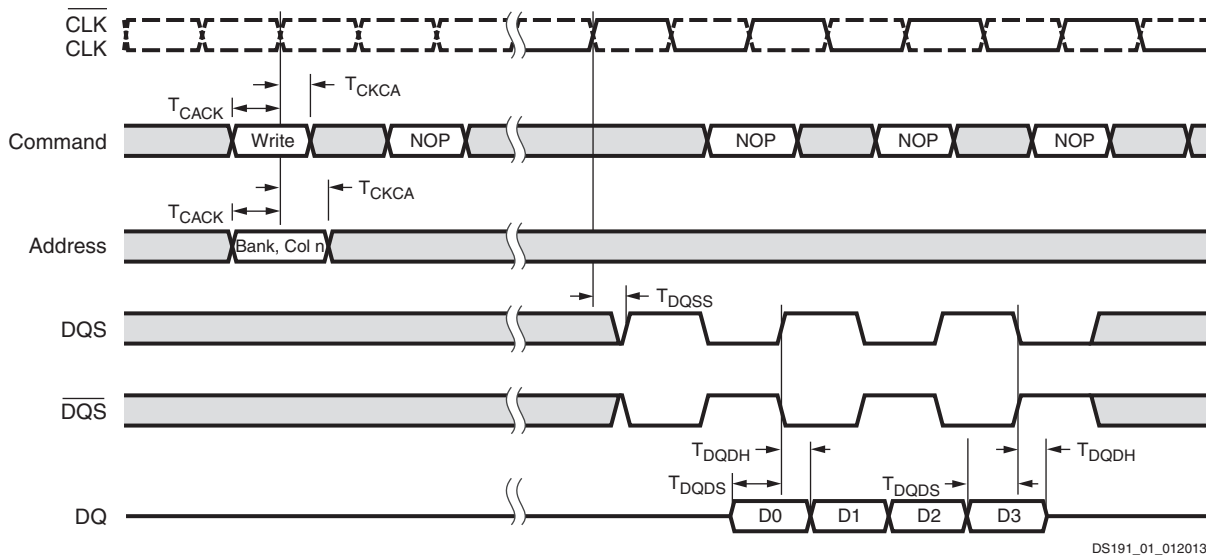
Table 30: **DDR2 Interface Switching Characteristics (400 Mb/s)**[1]

Symbol	Description	Min	Max	Units
$T_{DQVALID}$	Input data valid window	500	–	ps
T_{DQDS}[2]	Output DQ to DQS skew	385	–	ps
T_{DQDH}[3]	Output DQS to DQ skew	662	–	ps
T_{DQSS}	Output clock to DQS skew	−0.11	0.06	T_{CK}
T_{CACK}[4]	Command/address output setup time with respect to CLK	1760	–	ps
T_{CKCA}[5]	Command/address output hold time with respect to CLK	1739	–	ps

Notes:

1. Recommended V_{CCO_DDR} = 1.8V ±5%.
2. Measurement is taken from either the rising edge of DQ that crosses V_{IH}(AC) or the falling edge of DQ that crosses V_{IL}(AC) to V_{REF} of DQS.
3. Measurement is taken from either the rising edge of DQ that crosses V_{IL}(DC) or the falling edge of DQ that crosses V_{IH}(DC) to V_{REF} of DQS.
4. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IH}(AC) or the falling edge of CMD/ADDR that crosses V_{IL}(AC) to V_{REF} of CLK.
5. Measurement is taken from either the rising edge of CMD/ADDR that crosses V_{IL}(DC) or the falling edge of CMD/ADDR that crosses V_{IH}(DC) to V_{REF} of CLK.
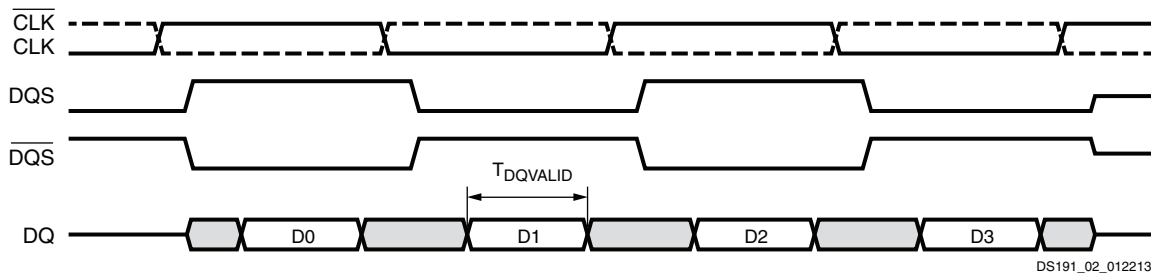

Figure 1: **DDR Output Timing Diagram**

Figure 2: **DDR Input Timing Diagram**

Static Memory Controller

Table 31: **SMC Interface Delay Characteristics**[1][2]

Symbol	Description	Min	Max	Units
$T_{NANDDOUT}$	NAND_IO output delay from last register to pad	4.12	6.45	ns
$T_{NANDALE}$	NAND_ALE output delay from last register to pad	5.08	6.33	ns
$T_{NANDCLE}$	NAND_CLE output delay from last register to pad	4.87	6.40	ns
T_{NANDWE}	NAND_WE_B output delay from last register to pad	4.69	5.89	ns
T_{NANDRE}	NAND_RE_B output delay from last register to pad	5.12	6.44	ns
T_{NANDCE}	NAND_CE_B output delay from last register to pad	4.68	5.89	ns
$T_{NANDDIN}$	NAND_IO setup time and input delay from pad to first register	1.48	3.09	ns
$T_{NANDBUSY}$	NAND_BUSY setup time and input delay from pad to first register	2.48	3.33	ns
T_{SRAMA}	SRAM_A output delay from last register to pad	3.94	5.73	ns
$T_{SRAMDOUT}$	SRAM_DQ output delay from last register to pad	4.66	6.45	ns
T_{SRAMCE}	SRAM_CE output delay from last register to pad	4.57	5.95	ns
T_{SRAMOE}	SRAM_OE_B output delay from last register to pad	4.79	6.13	ns
$T_{SRAMBLS}$	SRAM_BLS_B output delay from last register to pad	5.25	6.74	ns
T_{SRAMWE}	SRAM_WE_B output delay from last register to pad	5.12	6.48	ns
$T_{SRAMDIN}$	SRAM_DQ setup time and input delay from pad to first register	1.93	3.05	ns
$T_{SRAMWAIT}$	SRAM_WAIT setup time and input delay from pad to first register	2.26	3.15	ns

Notes:

1. All parameters do not include the package flight time and register controlled delays.
2. Refer to the ARM® PrimeCell® Static Memory Controller (PL350 series) Technical Reference Manual for more SMC timing details.

Quad-SPI Interfaces

Table 32: **Quad-SPI Interface Switching Characteristics**[1][2]

Symbol	Description	Min	Typical	Max	Units
Feedback Clock Enabled					
$T_{DCQSPICLK1}$	Quad-SPI clock duty cycle	44	–	56	%
$T_{QSPICKO1}$	Data and slave select output delay	–0.10	–	3.40	ns
$T_{QSPIDCK1}$	Input data setup time	2.00	–	–	ns
$T_{QSPICKD1}$	Input data hold time	1.30	–	–	ns
$T_{QSPISSCLK1}$	Slave select asserted to next clock edge	1	–	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS1}$	Clock edge to slave select deasserted	1	–	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK1}$	Quad-SPI device clock frequency	–	–	100[3]	MHz
Feedback Clock Disabled					
$T_{DCQSPICLK2}$	Quad-SPI clock duty cycle	44	–	56	%
$T_{QSPICKO2}$	Data and slave select output delay	–0.10	–	3.80	ns
$T_{QSPIDCK2}$	Input data setup time[4]	$11 - \dfrac{1}{F_{QSPI\_REF\_CLK}}$	–	–	ns
$T_{QSPICKD2}$	Input data hold time	$\dfrac{1}{2 \times F_{QSPICLK2}}$	–	–	ns
$T_{QSPISSCLK2}$	Slave select asserted to next clock edge	1	–	–	$F_{QSPI\_REF\_CLK}$ cycle
$T_{QSPICLKSS2}$	Clock edge to slave select deasserted	1	–	–	$F_{QSPI\_REF\_CLK}$ cycle
$F_{QSPICLK2}$	Quad-SPI device clock frequency	–	–	40	MHz
Feedback Clock Enabled or Disabled					
$F_{QSPI\_REF\_CLK}$	Quad-SPI reference clock frequency	–	–	200	MHz

Notes:
1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, feedback clock pin has no load. Quad-SPI single slave select 4-bit I/O mode.
2. Dual slave select 4-bit stacked I/O configuration is not covered.
3. Requires appropriate component selection/board design.
4. Use 0 ns as the input data setup time when the calculated $T_{QSPIDCK2}$ value is negative.
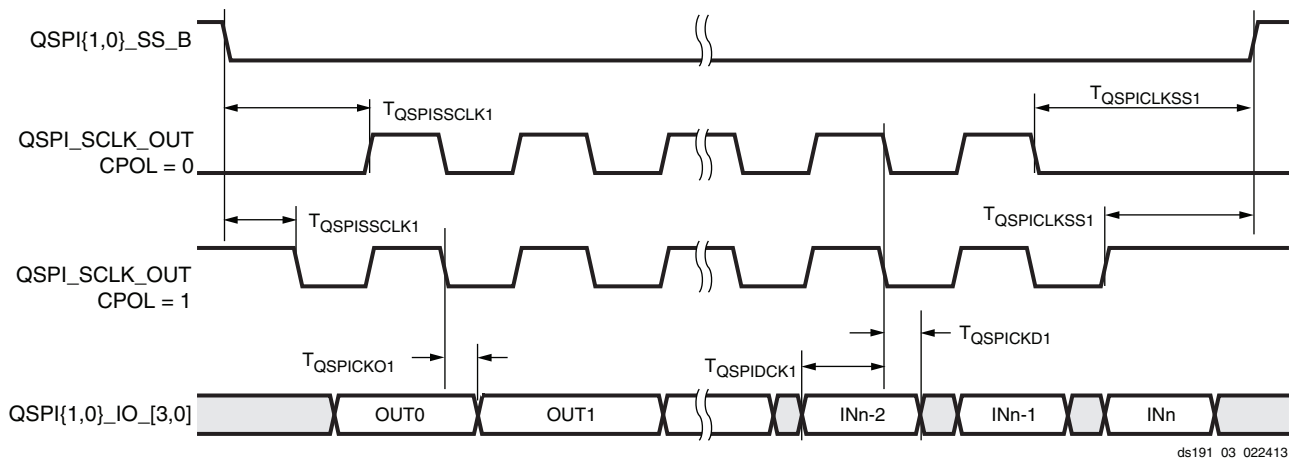

ds191_03_022413

Figure 3: **Quad-SPI Interface (Feedback Clock Enabled) Timing Diagram**
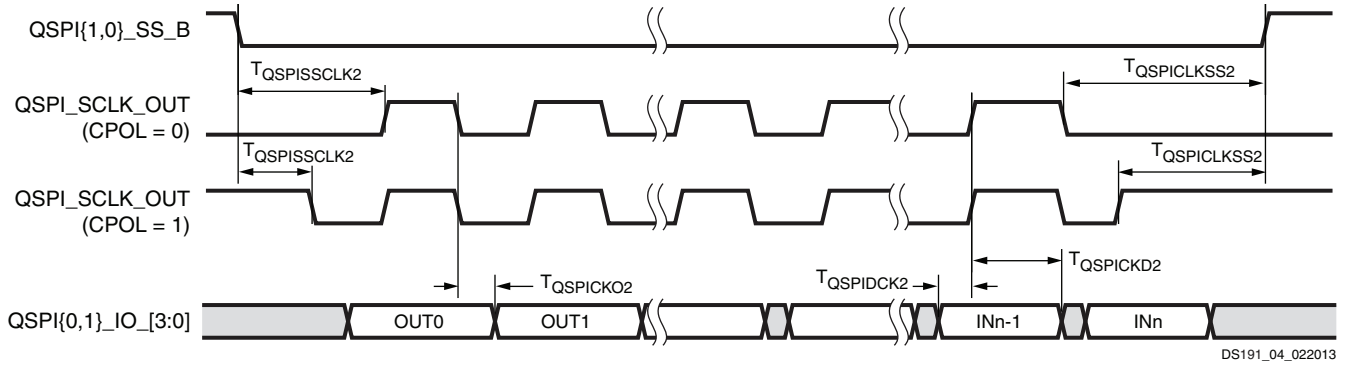
DS191_04_022013

Figure 4: **Quad-SPI Interface (Feedback Clock Disabled) Timing Diagram**

ULPI Interfaces

Table 33: **ULPI Interface Clock Receiving Mode Switching Characteristics**[1][2]

Symbol	Description	Min	Typ	Max	Units
$T_{ULPIDCK}$	Input setup to ULPI clock, all inputs	3.00	–	–	ns
$T_{ULPICKD}$	Input hold to ULPI clock, all inputs	1.00	–	–	ns
$T_{ULPICKO}$	ULPI clock to output valid, all outputs	1.70	–	8.86	ns
$F_{ULPICLK}$	ULPI device clock frequency	–	60	–	MHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads, 60 MHz device clock frequency.
2. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.
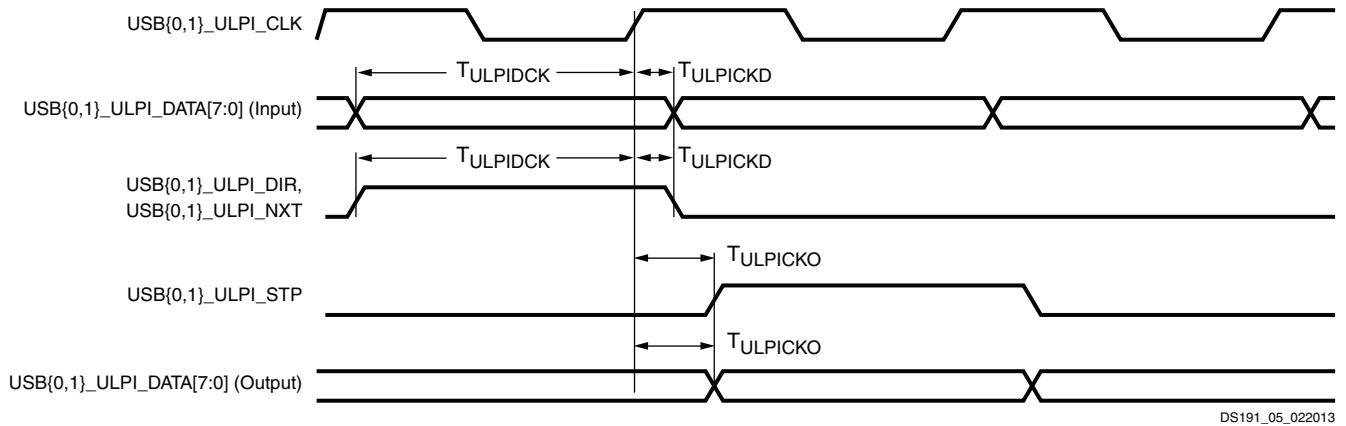

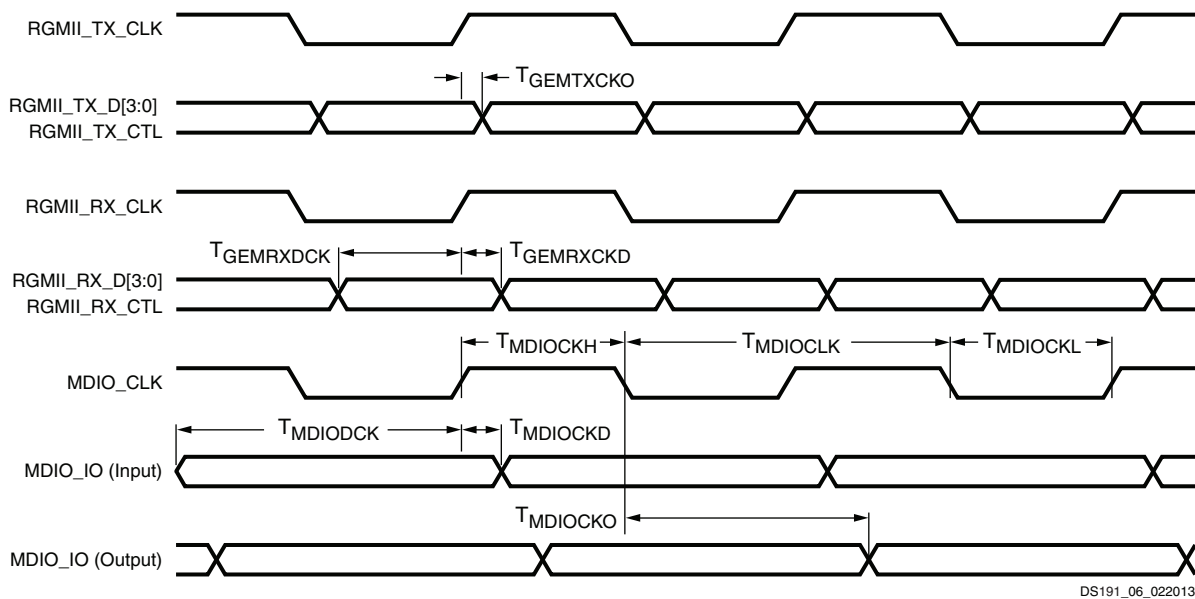DS191_05_022013

Figure 5: **ULPI Interface Timing Diagram**

RGMII and MDIO Interfaces

Table 34: **RGMII and MDIO Interface Switching Characteristics**[1][2][3]

Symbol	Description	Min	Typ	Max	Units
$T_{DCGETXCLK}$	Transmit clock duty cycle	45	–	55	%
$T_{GEMTXCKO}$	RGMII_TX_D[3:0], RGMII_TX_CTL output clock to out time	−0.50	–	0.50	ns
$T_{GEMRXDCK}$	RGMII_RX_D[3:0], RGMII_RX_CTL input setup time	0.80	–	–	ns
$T_{GEMRXCKD}$	RGMII_RX_D[3:0], RGMII_RX_CTL input hold time	0.80	–	–	ns
$T_{MDIOCLK}$	MDC output clock period	400	–	–	ns
$T_{MDIOCKH}$	MDC clock High time	160	–	–	ns
$T_{MDIOCKL}$	MDC clock Low time	160	–	–	ns
$T_{MDIODCK}$	MDIO input data setup time	80	–	–	ns
$T_{MDIOCKD}$	MDIO input data hold time	0	–	–	ns
$T_{MDIOCKO}$	MDIO data output delay	−20	–	170	ns
$F_{GETXCLK}$	RGMII_TX_CLK transmit clock frequency	–	125	–	MHz
$F_{GERXCLK}$	RGMII_RX_CLK receive clock frequency	–	125	–	MHz
$F_{ENET\_REF\_CLK}$	Ethernet reference clock frequency	–	125	–	MHz

Notes:
1. Test conditions: LVCMOS25, fast slew rate, 8 mA drive strength, 15 pF loads. Values in this table are specified during 1000 Mb/s operation.
2. LVCMOS25 slow slew rate and LVCMOS33 are not supported.
3. All timing values assume an ideal external input clock. Actual design system timing budgets should account for additional external clock jitter.

Figure 6: **RGMII Interface Timing Diagram**

SD/SDIO Interfaces

Table 35: **SD/SDIO Interface High Speed Mode Switching Characteristics**[1]

Symbol	Description	Min	Typ	Max	Units
T$_{DCSDHSCLK}$	SD device clock duty cycle	–	50	–	%
T$_{SDHSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
T$_{SDHSDCK}$	Input setup time, all inputs	3.00	–	–	ns
T$_{SDHSCKD}$	Input hold time, all inputs	1.05	–	–	ns
F$_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
F$_{SDHSCLK}$	High speed mode SD device clock frequency	0	–	50	MHz

Notes:

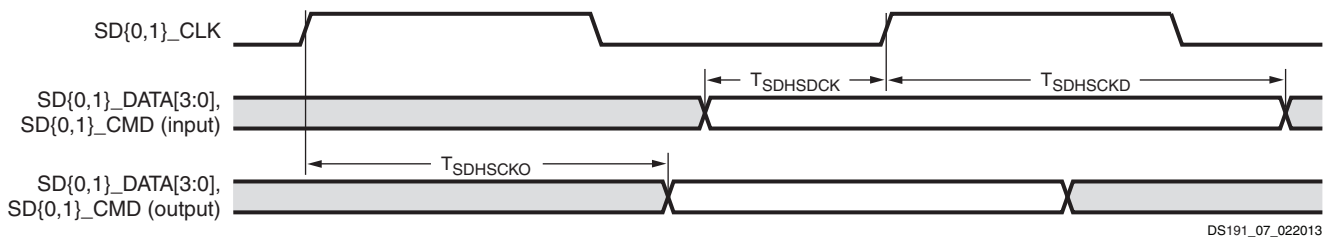1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

Figure 7: **SD/SDIO Interface High Speed Mode Timing Diagram**

Table 36: **SD/SDIO Interface Switching Characteristics**[1]

Symbol	Description	Min	Typ	Max	Units
T$_{DCSDSCLK}$	SD device clock duty cycle	–	50	–	%
T$_{SDSCKO}$	Clock to output delay, all outputs	2.00	–	12.00	ns
T$_{SDSDCK}$	Input setup time, all inputs	4.00	–	–	ns
T$_{SDSCKD}$	Input hold time, all inputs	3.00	–	–	ns
F$_{SD\_REF\_CLK}$	SD reference clock frequency	–	–	125	MHz
F$_{SDIDCLK}$	Clock frequency in identification mode	–	–	400	MHz
F$_{SDSCLK}$	Standard mode SD device clock frequency	0	–	50	MHz

Notes:

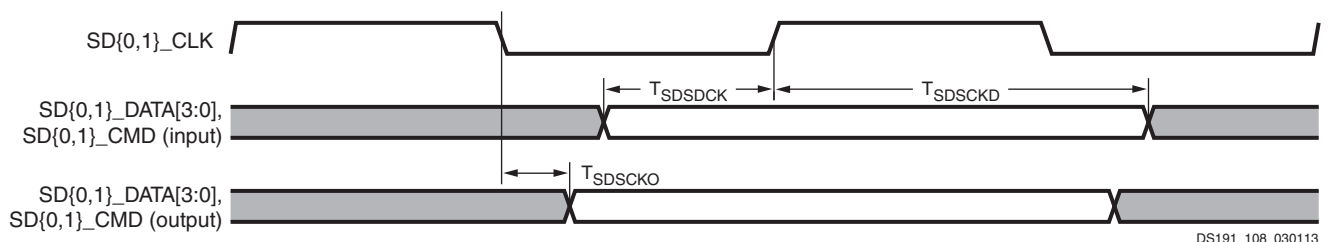1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

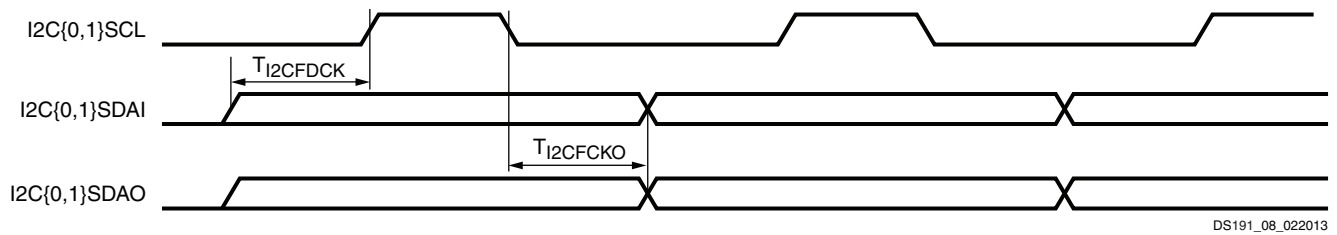*Figure 8:* **SD/SDIO Interface Standard Mode Timing Diagram**

I2C Interfaces

Table 37: **I2C Fast Mode Interface Switching Characteristics**[1]

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CFCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CFCKO}$	I2C{0,1}SDAO clock to out delay	–	–	900	ns
$T_{I2CFDCK}$	I2C{0,1}SDAI setup time	100	–	–	ns
$F_{I2CFCLK}$	I2C{0,1}SCL clock frequency	–	–	400	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

Figure 9: **I2C Fast Mode Interface Timing Diagram**

Table 38: **I2C Standard Mode Interface Switching Characteristics**[1]

Symbol	Description	Min	Typ	Max	Units
$T_{DCI2CSCLK}$	I2C{0,1}SCL duty cycle	–	50	–	%
$T_{I2CSCKO}$	I2C{0,1}SDAO clock to out delay	–	–	3450	ns
$T_{I2CSDCK}$	I2C{0,1}SDAI setup time	250	–	–	ns
$F_{I2CSCLK}$	I2C{0,1}SCL clock frequency	–	–	100	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.
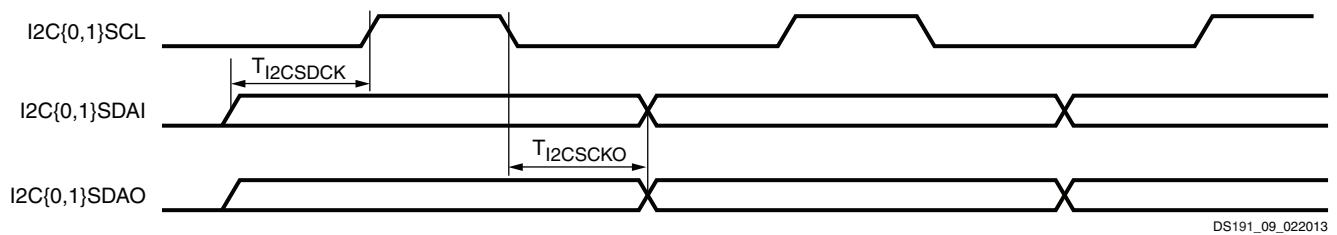
Figure 10: **I2C Standard Mode Interface Timing Diagram**