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3-Volt Advanced Boot Block Flash Memory

28F008/800B3, 28F016/160B3, 28F320B3, 28F640B3

Datasheet

Product Features

- Flexible SmartVoltage Technology
  - —2.7 V–3.6 V Read/Program/Erase
  - —12 V V_{PP} Fast Production Programming
- 1.65 V–2.5 V or 2.7 V–3.6 V I/O Option
  - —Reduces Overall System Power
- High Performance
  - —2.7 V–3.6 V: 70 ns Max Access Time
- Optimized Block Sizes
  - —Eight 8-KB Blocks for Data,Top or Bottom Locations
  - —Up to One Hundred Twenty-Seven 64-KB Blocks for Code
- Block Locking
  - —V_{CC}-Level Control through WP#
- Low Power Consumption
  - —9 mA Typical Read Current
- Absolute Hardware-Protection
  - —V_{PP} = GND Option
  - —V_{CC} Lockout Voltage
- Extended Temperature Operation
  - —–40 °C to +85 °C
- Automated Program and Block Erase
  - —Status Registers
- Intel® Flash Data Integrator Software
  - —Flash Memory Manager
  - —System Interrupt Manager
  - —Supports Parameter Storage, Streaming Data (e.g., Voice)
- Extended Cycling Capability
  - —Minimum 100,000 Block Erase Cycles Guaranteed
- Automatic Power Savings Feature
  - —Typical I_{CCS} after Bus Inactivity
- Standard Surface Mount Packaging
  - —48-Ball CSP Packages
  - —40- and 48-Lead TSOP Packages
- Density and Footprint Upgradeable for common package
  - —8-, 16-, 32- and 64-Mbit Densities
- ETOX™ VIII (0.13 µm) Flash Technology
  - —16 and 32-Mbit Densities
- ETOX™ VII (0.18 µm) Flash Technology
  - —16-, 32- and 64-Mbit Densities
- ETOX ™ VI (0.25µm) Flash Technology
  - —8-, 16-, and 32-Mbit Densities
- The x8 option not recommended for new designs

The Intel® 3-Volt Advanced Boot Block flash memory, manufactured on Intel's latest 0.13 µm and 0.18 µm technologies, represent a feature-rich solution at overall lower system cost. The 3-Volt Advanced Boot Block Flash Memory products in x16 will be available in 48-lead TSOP and 48-ball CSP packages. The x8 option of this product family will be available only in 40-lead TSOP and 48-ball µBGA* packages. Additional information on this product family can be obtained by accessing Intel's website at: http://www.intel.com/design/flash.

Notice: This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest data sheet before finalizing a design.

Order Number: 290580-016
April 2002

Contents

Revision History

Number	Description
-001	Original version
-002	Section 3.4, V_{PP} *Program and Erase Voltages*, added Updated Figure 9: *Automated Block Erase Flowchart* Updated Figure 10: *Erase Suspend/Resume Flowchart* (added program to table) Updated Figure 16: *AC Waveform: Program and Erase Operations* (updated notes) I_{PPR} maximum specification change from ±25 µA to ±50 µA Program and Erase Suspend Latency specification change Updated Appendix A: *Ordering Information* (included 8 M and 4 M information) Updated Figure, Appendix D: *Architecture Block Diagram* (Block info. in words not bytes) Minor wording changes
-003	Combined byte-wide specification (previously 290605) with this document Improved speed specification to 80 ns (3.0 V) and 90 ns (2.7 V) Improved 1.8 V I/O option to minimum 1.65 V (Section 3.4) Improved several DC characteristics (Section 4.4) Improved several AC characteristics (Sections 4.5 and 4.6) Combined 2.7 V and 1.8 V DC characteristics (Section 4.4) Added 5 V V_{PP} read specification (Section 3.4) Removed 120 ns and 150 ns speed offerings Moved *Ordering Information* from Appendix to Section 6.0; updated information Moved *Additional Information* from Appendix to Section 7.0 Updated figure Appendix B, *Access Time vs. Capacitive Load* Updated figure Appendix C, *Architecture Block Diagram* Moved Program and Erase Flowcharts to Appendix E Updated *Program Flowchart* Updated *Program Suspend/Resume Flowchart* Minor text edits throughout
-004	Added 32-Mbit density Added 98H as a reserved command (Table 4) A_1–A_{20} = 0 when in read identifier mode (Section 3.2.2) Status register clarification for SR3 (Table 7) V_{CC} and V_{CCQ} absolute maximum specification = 3.7 V (Section 4.1) Combined I_{PPW} and I_{CCW} into one specification (Section 4.4) Combined I_{PPE} and I_{CCE} into one specification (Section 4.4) Max Parameter Block Erase Time (t_{WHQV2}/t_{EHQV2}) reduced to 4 sec (Section 4.7) Max Main Block Erase Time (t_{WHQV3}/t_{EHQV3}) reduced to 5 sec (Section 4.7) Erase suspend time @ 12 V (t_{WHRH2}/t_{EHRH2}) changed to 5 µs typical and 20 µs maximum (Section 4.7) *Ordering Information* updated (Section 6.0) Write State Machine Current/Next States Table updated (Appendix A) Program Suspend/Resume Flowchart updated (Appendix F) Erase Suspend/Resume Flowchart updated (Appendix F) Text clarifications throughout
-005	µBGA package diagrams corrected (Figures 3 and 4) I_{PPD} test conditions corrected (Section 4.4) 32-Mbit ordering information corrected (Section 6) µBGA package top side mark information added (Section 6)
-006	V_{IH} and V_{IL} Specification change (Section 4.4) I_{CCS} test conditions clarification (Section 4.4) Added Command Sequence Error Note (Table 7) Data sheet renamed from *Smart 3 Advanced Boot Block 4-Mbit, 8-Mbit, 16-Mbit Flash Memory Family.* Added device ID information for 4-Mbit x8 device Removed 32-Mbit x8 to reflect product offerings Minor text changes
-007	Corrected RP# pin description in Table 2, *3 Volt Advanced Boot Block Pin Descriptions* Corrected typographical error fixed in *Ordering Information*

Number	Description
-008	4-Mbit packaging and addressing information corrected throughout document
-009	Corrected 4-Mbit memory addressing tables in Appendices D and E
-010	Max I_{CCD} changed to 25 µA V_{CC}Max on 32 M (28F320B3) changed to 3.3 V
-011	Added 64-Mbit density and faster speed offerings Removed access time vs. capacitance load curve
-012	Changed references of 32Mbit 80ns devices to 70ns devices to reflect the faster product offering. Changed VccMax=3.3V reference to indicate the affected product is the 0.25µm 32Mbit device. Minor text edits throughout document.
-013	Added New Pin-1 indicator information on 40 and 48Lead TSOP packages. Minor text edits throughout document.
-014	Added specifications for 0.13 micron product offerings throughout document
-015	Minor text edits throughout document.
-016	Adjusted ordering information. Adjusted specifications for 0.13 micron product offerings. Revised and corrected DC Characteristics Table. Adjusted package diagram information. Minor text edits throughout document.

1.0 Introduction

This datasheet contains the specifications for the 3-Volt Advanced Boot Block Flash Memory family, which is optimized for portable, low-power, systems. This family of products features 1.65 V–2.5 V or 2.7 V–3.6 V I/Os, and a low V_{CC}/V_{PP} operating range of 2.7 V–3.6 V for Read, Program, and Erase operations. In addition, this family is capable of fast programming at 12 V. Throughout this document, the term "2.7 V" refers to the full voltage range 2.7 V–3.6 V (except where noted otherwise) and "V_{PP} = 12 V" refers to 12 V ±5%. Section 1.0 and 2.0 provide an overview of the Flash Memory family including applications, pinouts, and pin descriptions. Section 3.0 describes the memory organization and operation for these products. Sections 4.0 and 5.0 contain the operating specifications. Finally, Sections 6.0 and 7.0 provide ordering and other reference information.

The 3-Volt Advanced Boot Block Flash Memory features the following:

- Enhanced blocking for easy segmentation of code and data or additional design flexibility
- Program Suspend to Read command
- V_{CCQ} input of 1.65 V–2.5 V or 2.7 V–3.6 V on all I/Os. See Figures 1 through 4 for pinout diagrams and V_{CCQ} location
- Maximum program and erase time specification for improved data storage.

Table 1. 3-Volt Advanced Boot Block Feature Summary

Feature	28F008B3, 28F016B3	28F800B3, 28F160B3, 28F320B3[3], 28F640B3	Reference
V_{CC} Read Voltage	2.7 V– 3.6 V		Section 4.2, Section 4.4
V_{CCQ} I/O Voltage	1.65 V–2.5 V or 2.7 V– 3.6 V		Section 4.2, 4.4
V_{PP} Program/Erase Voltage	2.7 V– 3.6 V or 11.4 V– 12.6 V		Section 4.2, 4.4
Bus Width	8 bit	16 bit	Table 3
Speed	70 ns, 80 ns, 90 ns, 100 ns, 110 ns		Section 4.5
Memory Arrangement	1024 Kbit x 8 (8 Mbit), 2048 Kbit x 8 (16 Mbit)	512 Kbit x 16 (8 Mbit), 1024 Kbit x 16 (16 Mbit), 2048 Kbit x 16 (32 Mbit), 4096 Kbit x 16 (64 Mbit)	Section 2.2
Blocking (top or bottom)	Eight 8-Kbyte parameter blocks **and** Fifteen 64-Kbyte blocks (8 Mbit) or Thirty-one 64-Kbyte main blocks (16 Mbit) Sixty-three 64-Kbyte main blocks (32 Mbit) One hundred twenty-seven 64-Kbyte main blocks (64 Mbit)		Section 2.2 Appendix C
Locking	WP# locks/unlocks parameter blocks All other blocks protected using V_{PP}		Section 3.3 Table 8
Operating Temperature	Extended: –40 °C to +85 °C		Section 4.2, 4.4
Program/Erase Cycling	100,000 cycles		Section 4.2, 4.4
Packages	40-lead TSOP[1], 48-Ball µBGA* CSP[2]	48-Lead TSOP, 48-Ball µBGA CSP[2], 48-Ball VF BGA[4]	Figure 4, Figure 5

NOTES:
1. 32-Mbit and 64-Mbit densities not available in 40-lead TSOP.
2. 8-Mbit densities not available in µBGA* CSP.
3. V_{CC}Max is 3.3 V on 0.25µm 32-Mbit devices.

1.1 Product Overview

Intel provides the most flexible voltage solution in the flash industry, providing three discrete voltage supply pins: V_{CC} for Read operation, V_{CCQ} for output swing, and V_{PP} for Program and Erase operation. All 3-Volt Advanced Boot Block Flash Memory products provide program/erase capability at 2.7 V or 12 V (for fast production programming), and read with V_{CC} at 2.7 V. Since many designs read from the flash memory a large percentage of the time, 2.7 V V_{CC} operation can provide substantial power savings.

The 3-Volt Advanced Boot Block Flash Memory products are available in either x8 or x16 packages in the following densities: (see Section 6.0, “Ordering Information” on page 39 for availability.)

- 8-Mbit (8, 388, 608-bit) flash memory organized as 512 Kwords of 16 bits each or 1024 Kbytes of 8-bits each
- 16-Mbit (16, 777, 216-bit) flash memory organized as 1024 Kwords of 16 bits each or 2048 Kbytes of 8-bits each
- 32-Mbit (33, 554, 432-bit) flash memory organized as 2048 Kwords of 16 bits each
- 64-Mbit (67, 108, 864-bit) flash memory organized as 4096 Kwords of 16 bits each

The parameter blocks are located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The upper two (or lower two) parameter blocks can be locked to provide complete code security for system initialization code. Locking and unlocking is controlled by WP# (see Section 3.3, “Block Locking” on page 17 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for Program and Erase operations, including verification, thereby unburdening the microprocessor or microcontroller. The status register indicates the status of the WSM by signifying block erase or word program completion and status.

The 3-Volt Advanced Boot Block flash memory is also designed with an Automatic Power Savings (APS) feature, which minimizes system current drain and allows for very low power designs. This mode is entered following the completion of a read cycle (approximately 300 ns later).

The RP# pin provides additional protection against unwanted command writes that may occur during system reset and power-up/down sequences due to invalid system bus conditions (see Section 3.6, “Power-Up/Down Operation” on page 19).

Section 3.0, “Principles of Operation” on page 10 gives detailed explanation of the different modes of operation. Section 4.4, “DC Characteristics” on page 23 provides complete current and voltage specifications. Refer to Section 4.5, “AC Characteristics —Read Operations” on page 27 for read, program, and erase performance specifications.

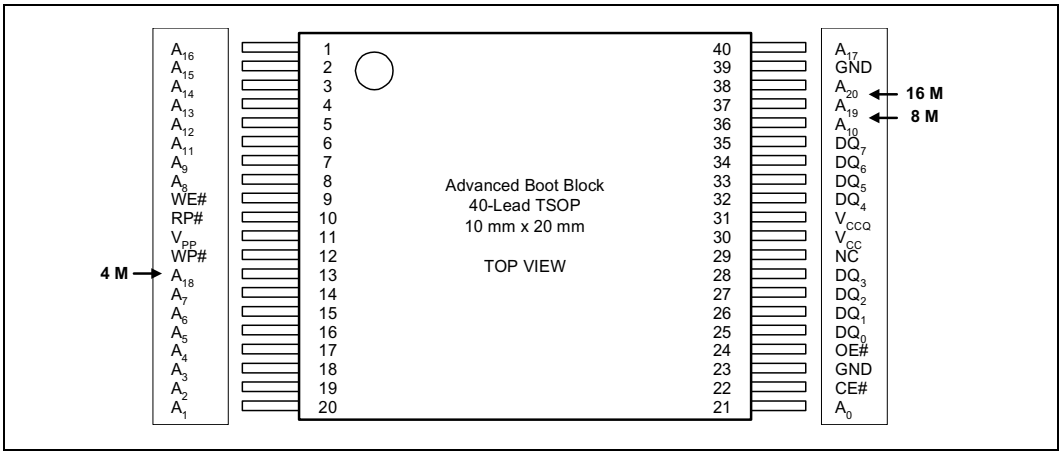
2.0 Product Description

This section explains device pin description and package pinouts.

2.1 Package Pinouts

The 3-Volt Advanced Boot Block flash memory is available in 40-lead TSOP (x8, Figure 1), 48-lead TSOP (x16, Figure 2), 48-ball µBGA(x8 and x16, Figure 4 and Figure 5, respectively), and 48-ball VF BGA (x16, Figure 5) packages. In all figures, pin changes necessary for density upgrades have been circled.

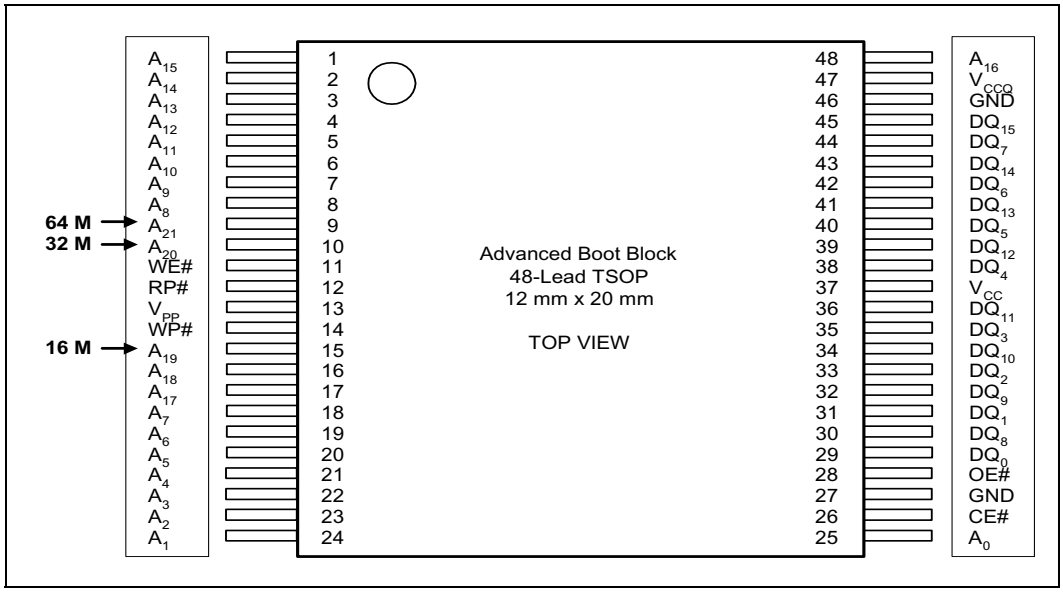
Figure 1. 40-Lead TSOP Package for x8 Configurations



0580_01

NOTES:
1. 40-Lead TSOP available for 8-Mbit and 16-Mbit densities only.
2. Lower densities will have NC on the upper address pins. For example, an 8-Mbit device will have NC on Pin 38.

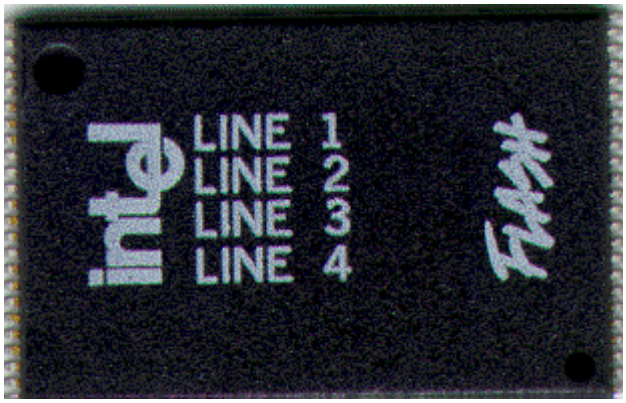
Figure 2. 48-Lead TSOP Package for x16 Configurations



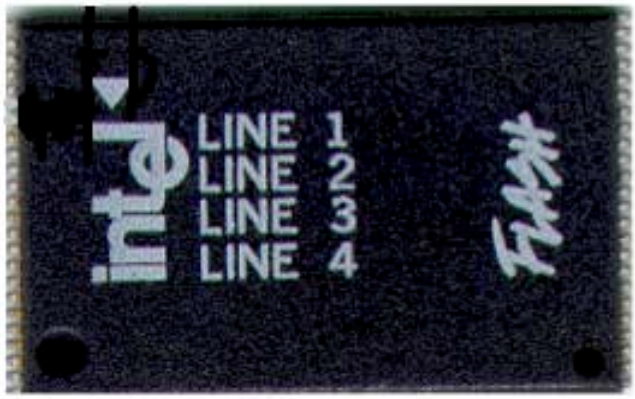
0580_02

Figure 3. New Mark for Pin-1 indicator for 40-Lead 8 Mb, 16 Mb TSOP and 48-Lead 8 Mb, 16 Mb and 32 Mb TSOP

Current Mark:



New Mark:



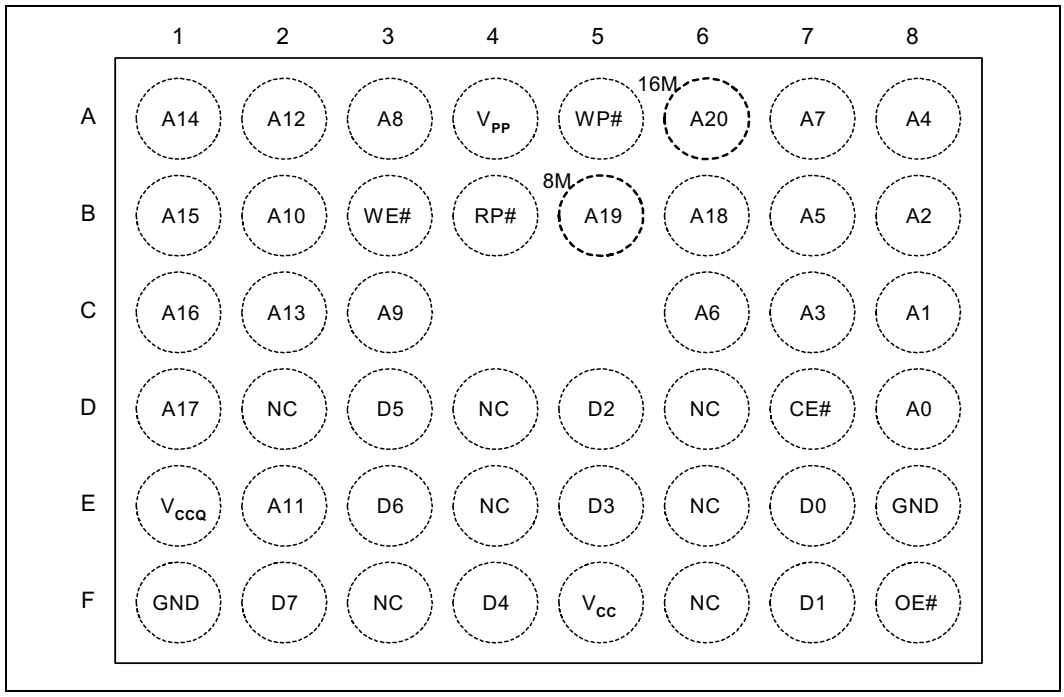
Note: The topside marking on 8 Mb, 16 Mb, and 32 Mb Advanced & Advanced + Boot Block 40L and 48L TSOP products will convert to a white ink triangle as a Pin-1 indicator. Products without the white triangle will continue to use a dimple as a Pin-1 indicator. There are no other changes in package size, materials, functionality, customer handling, or manufacturability. Product will continue to meet stringent Intel quality requirements.

Products Affected are Intel Ordering Codes:

Ordering Information Valid Combinations

	40-Lead TSOP	48-Lead TSOP
Ext. Temp. 32 Mbit		TE28F320B3TC70 TE28F320B3BC70 TE28F320B3TC90 TE28F320B3BC90 TE28F320B3TA100 TE28F320B3BA100 TE28F320B3TA110 TE28F320B3BA110
Ext. Temp. 16 Mbit	TE28F016B3TA90(3) TE28F016B3BA90(3) TE28F016B3TA110(3) TE28F016B3BA110(3)	TE28F160B3TC70 TE28F160B3BC70 TE28F160B3TC80 TE28F160B3BC80 TE28F160B3TA90(3) TE28F160B3BA90(3) TE28F160B3TA110(3) TE28F160B3BA110(3)
Ext. Temp. 8 Mbit	TE28F008B3TA90(3) TE28F008B3BA90(3) TE28F008B3TA110(3) TE28F008B3BA110(3)	TE28F800B3TA90(3) TE28F800B3BA90(3) TE28F800B3TA110(3) TE28F800B3BA110(3)

Figure 4. x8 48-Ball µBGA* Chip Size Package (Top View, Ball Down)

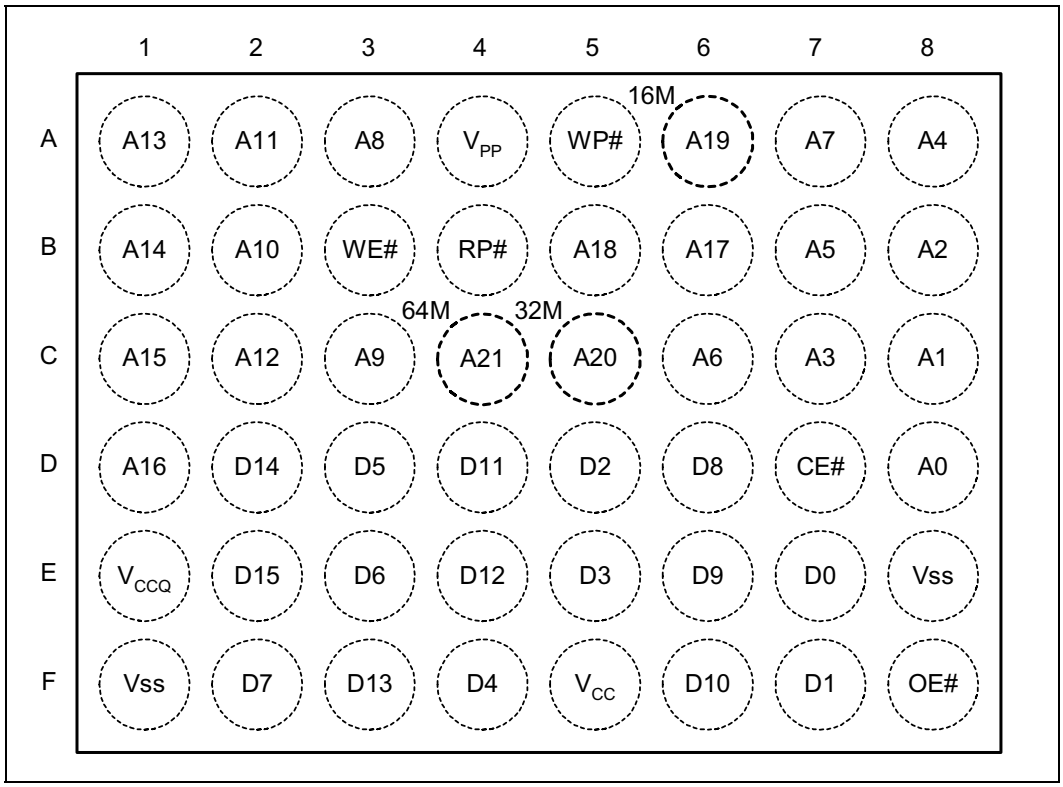


0580_04

NOTES:

1. Shaded connections indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Routing is not recommended in this area. A_{20} is the upgrade address for the 16-Mbit device.

Figure 5. x16 48-Ball Very Fine Pitch BGA and µBGA* Chip Size Package (Top View, Ball Down)



0580_03

NOTES:

1. Shaded connections indicate the upgrade address connections. Lower density devices will not have the upper address solder balls. Routing is not recommended in this area. A_{19} is the upgrade address for the 16-Mbit device. A_{20} is the upgrade address for the 32-Mbit device. A_{21} is the upgrade address for the 64-Mbit device.
2. Table 2, “3-Volt Advanced Boot Block Pin Descriptions” on page 9 details the usage of each device pin.

Table 2. 3-Volt Advanced Boot Block Pin Descriptions

Symbol	Type	Name and Function
A_0–A_{21}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a program or erase cycle. 28F008B3: A[0-19], 28F016B3: A[0-20], 28F800B3: A[0-18], 28F160B3: A[0-19], 28F320B3: A[0-20], 28F640B3: A[0-21]
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Inputs commands to the Command User Interface when CE# and WE# are active. Data is internally latched. Outputs array, identifier and status register data. The data pins float to tri-state when the chip is de-selected or the outputs are disabled.
DQ_8–DQ_{15}	INPUT/ OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data on the second CE# and WE# cycle during a Program command. Data is internally latched. Outputs array and identifier data. The data pins float to tri-state when the chip is de-selected. **Not included on x8 products.**
CE#	INPUT	**CHIP ENABLE:** Activates the internal control logic, input buffers, decoders and sense amplifiers. CE# is active low. CE# high de-selects the memory device and reduces power consumption to standby levels.
OE#	INPUT	**OUTPUT ENABLE:** Enables the device's outputs through the data buffers during a Read operation. OE# is active low.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the Command Register and memory array. WE# is active low. Addresses and data are latched on the rising edge of the second WE# pulse.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Uses two voltage levels (V_{IL}, V_{IH}) to control reset/deep power-down mode. **When RP# is at logic low, the device is in reset/deep power-down mode**, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). **When RP# is at logic high, the device is in standard operation**. When RP# transitions from logic-low to logic-high, the device defaults to the read array mode.
WP#	INPUT	**WRITE PROTECT:** Provides a method for locking and unlocking the two lockable parameter blocks. **When WP# is at logic low, the lockable blocks are locked**, preventing Program and Erase operations to those blocks. If a Program or Erase operation is attempted on a locked block, SR.1 and either SR.4 [program] or SR.5 [erase] will be set to indicate the operation failed. **When WP# is at logic high, the lockable blocks are unlocked** and can be programmed or erased. See Section 3.3 for details on write protection.
V_{CCQ}	INPUT	**OUTPUT V_{CC}:** Enables all outputs to be driven to 1.8 V – 2.5 V while the V_{CC} is at 2.7 V–3.3 V. If the V_{CC} is regulated to 2.7 V–2.85 V, V_{CCQ} can be driven at 1.65 V–2.5 V to achieve lowest power operation (see Section 4.4*)*. This input may be tied directly to V_{CC} (2.7 V–3.6 V).
V_{CC}		**DEVICE POWER SUPPLY:** 2.7 V–3.6 V
V_{PP}		**PROGRAM/ERASE POWER SUPPLY:** Supplies power for Program and Erase operations. V_{PP} may be the same as V_{CC} (2.7 V–3.6 V) for single supply voltage operation. For fast programming at manufacturing, 11.4 V–12.6 V may be supplied to V_{PP}. This pin cannot be left floating. Applying 11.4 V–12.6 V to V_{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum (see Section 3.4 for details). $V_{PP} < V_{PPLK}$ protects memory contents against inadvertent or unintended program and erase commands.
GND		**GROUND:** For all internal circuitry. All ground inputs **must** be connected.
NC		**NO CONNECT:** Pin may be driven or left floating.

2.2 Block Organization

The 3-Volt Advanced Boot Block is an asymmetrically blocked architecture that enables system integration of code and data within a single flash device. Each block can be erased independently of the others up to 100,000 times. For the address locations of each block, see the memory maps in Appendix C.

2.2.1 Parameter Blocks

The 3-Volt Advanced Boot Block flash memory architecture includes parameter blocks to facilitate storage of frequently updated small parameters (i.e., data that would normally be stored in an EEPROM). The word-rewrite functionality of EEPROMs can be emulated using software techniques. Each device contains eight parameter blocks of 8 Kbytes/4 Kwords (8192 bytes/4,096 words) each.

2.2.2 Main Blocks

After the parameter blocks, the remainder of the array is divided into equal-size main blocks (65,536 bytes/32,768 words) for data or code storage. The 8-Mbit device contains 15 main blocks; 16-Mbit flash has 31 main blocks; 32-Mbit has 63 main blocks; 64-Mbit has 127 main blocks.

3.0 Principles of Operation

Flash memory combines EEPROM functionality with in-circuit electrical program-and-erase capability. The 3-Volt Advanced Boot Block Flash Memory family utilizes a Command User Interface (CUI) and automated algorithms to simplify Program and Erase operations. The CUI allows for 100% CMOS-level control inputs and fixed power supplies during erasure and programming.

When $V_{PP} < V_{PPLK}$, the device will execute only the following commands successfully: Read Array, Read Status Register, Clear Status Register, and Read Identifier. The device provides standard EEPROM read, standby, and Output-Disable operations. Manufacturer identification and device identification data can be accessed through the CUI. All functions associated with altering memory contents, namely program and erase, are accessible via the CUI. The internal Write State Machine (WSM) completely automates Program and Erase operations, while the CUI signals the start of an operation and the status register reports status. The CUI handles the WE# interface to the data and address latches, as well as system status requests during WSM operation.

3.1 Bus Operation

3-Volt Advanced Boot Block flash memory devices read, program, and erase in-system via the local CPU or microcontroller. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles. Four control pins dictate the data flow in and out of the flash component: CE#, OE#, WE#, and RP#. Table 3 summarizes these bus operations.

Table 3. Bus Operations[1]

Mode	Note	RP#	CE#	OE#	WE#	DQ_{0-7}	DQ_{8-15}
Read (Array, Status, or Identifier)	2–4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	D_{OUT}
Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Standby	2	V_{IH}	V_{IH}	X	X	High Z	High Z
Reset	2, 7	V_{IL}	X	X	X	High Z	High Z
Write	2, 5–7	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}	D_{IN}

NOTES:
1. 8-bit devices use only DQ[0:7], 16-bit devices use DQ[0:15].
2. X must be V_{IL}, V_{IH} for control pins and addresses.
3. See *DC Characteristics* for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, V_{PP4} voltages.
4. Manufacturer and device codes may also be accessed in read identifier mode (A_1–A_{21} = 0). See Table 5.
5. Refer to Table 6 for valid D_{IN} during a Write operation.
6. To program or erase the lockable blocks, hold WP# at V_{IH}.
7. RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

3.1.1 Read

The flash memory has four read modes available: read array, read identifier, read status, and read query. These modes are accessible independent of the V_{PP} voltage. The appropriate Read Mode command must be issued to the CUI to enter the corresponding mode. Upon initial device power-up or after exit from reset, the device automatically defaults to read-array mode.

CE# and OE# must be driven active to obtain data at the outputs. CE# is the device selection control; when active, it enables the flash memory device. OE# is the data output control, and it drives the selected memory data onto the I/O bus. For all read modes, WE# and RP# must be at V_{IH}. Figure 8 illustrates a read cycle.

3.1.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins are placed in a high-impedance state.

3.1.3 Standby

Deselecting the device by bringing CE# to a logic-high level (V_{IH}) places the device in standby mode, which substantially reduces device power consumption without any latency for subsequent read accesses. In standby, outputs are placed in a high-impedance state independent of OE#. If deselected during Program or Erase operation, the device continues to consume active power until the Program or Erase operation is complete.

3.1.4 Deep Power-Down / Reset

From read mode, RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read-access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write can be initiated. After this wake-up interval, normal operation is restored. The CUI resets to read-array mode, and the status register is set to 80H. Figure 10A illustrates this case.

If RP# is taken low for time t_{PLPH} during a Program or Erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence:

1. When RP# goes low, the device shuts down the operation in progress, a process that takes time t_{PLRH} to complete.
2. After this time t_{PLRH}, the part will either reset to read-array mode (if RP# has gone high during t_{PLRH}, Figure 10B), or enter reset mode (if RP# is still logic low after t_{PLRH}, Figure 10C).
3. In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be waited before a Read or Write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when RP# goes high.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, the processor expects to read from the flash memory. Automated flash memories provide status information when read during program or Block-Erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.1.5 Write

A write occurs when both CE# and WE# are low and OE# is high. Commands are written to the Command User Interface (CUI) using standard microprocessor write timings to control Flash operations. The CUI does not occupy an addressable memory location. The address and data buses are latched on the rising edge of the second WE# or CE# pulse, whichever occurs first. Figure 9 illustrates a Program and Erase operation. Table 6 shows the available commands, and Appendix A provides detailed information on moving between the different modes of operation using CUI commands.

Two commands modify array data: Program (40H), and Erase (20H). Writing either of these commands to the internal Command User Interface (CUI) initiates a sequence of internally timed functions that culminate in the completion of the requested task (unless that operation is aborted by either RP# being driven to V_{IL} for t_{PLRH} or an appropriate Suspend command).

3.2 Modes of Operation

The flash memory has four read modes (read array, read identifier, read status, and read query; see Appendix B), and two write modes (program and block erase). Three additional modes (erase suspend to program, erase suspend to read, and program suspend to read) are available only during suspended operations. Table 4 summarizes the commands used to reach these modes. Appendix A is a comprehensive chart showing the state transitions.

3.2.1 Read Array

When RP# transitions from V_{IL} (reset) to V_{IH}, the device defaults to read-array mode and will respond to the read-control inputs (CE#, address inputs, and OE#) without any additional CUI commands.

When the device is in read-array mode, four control signals control data output.

- WE# must be logic high (V_{IH})
- CE# must be logic low (V_{IL})
- OE# must be logic low (V_{IL})
- RP# must be logic high (V_{IH})

In addition, the address of the preferred location must be applied to the address pins. If the device is not in read-array mode, as would be the case after a Program or Erase operation, the Read Array command (FFH) must be written to the CUI before array reads can occur.

Table 4. Command Codes and Descriptions

Code	Device Mode	Description
00, 01, 60, 2F, C0, 98	Invalid/ Reserved	Unassigned commands that should not be used. Intel reserves the right to redefine these codes for future functions.
FF	Read Array	Places the device in read-array mode, such that array data will be output on the data pins.
40	Program Set-Up	This is a two-cycle command. The first cycle prepares the CUI for a program operation. The second cycle latches addresses and data information and initiates the WSM to execute the program algorithm. The flash outputs status register data when CE# or OE# is toggled. A Read Array command is required after programming to read array data. See Section 3.2.4.
10	Alternate Program Set-Up	(See 40H/Program Set-Up)
20	Erase Set-Up	Prepares the CUI for the Erase Confirm command. If the next command is not an Erase Confirm command, then the CUI will (a) set both SR.4 and SR.5 of the status register to a “1,” (b) place the device into the read-status-register mode, and (c) wait for another command. See Section 3.2.5.
D0	Erase Confirm Program / Erase Resume	If the previous command was an Erase Set-Up command, then the CUI will close the address and data latches, and begin erasing the block indicated on the address pins. During erase, the device will only respond to the Read Status Register and Erase Suspend commands. The device will output status-register data when CE# or OE# is toggled. If a Program or Erase operation was previously suspended, this command will resume that operation.
B0	Program / Erase Suspend	Issuing this command will begin to suspend the currently executing Program/Erase operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR.2) or erase suspend (SR.6), and the WSM status bit (SR.7) to a “1” (ready). The WSM will continue to idle in the SUSPEND state, regardless of the state of all input-control pins except RP#, which will immediately shut down the WSM and the remainder of the chip, if it is driven to V_{IL}. See Section 3.2.4.1 and Section 3.2.4.1.
70	Read Status Register	This command places the device into read-status-register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device automatically enters this mode after a Program or Erase operation has been initiated. See Section 3.2.3.
50	Clear Status Register	The WSM can set the block-lock status (SR.1), V_{PP} status (SR.3), program status (SR.4), and erase status (SR.5) bits in the status register to “1,” but it cannot clear them to “0.” Issuing this command clears those bits to “0.”
90	Read Identifier	Puts the device into the intelligent-identifier-read mode, so that reading the device will output the manufacturer and device codes (A_0 = 0 for manufacturer, A_0 = 1 for device, all other address inputs must be 0). See Section Section 3.2.2.

NOTE: See Appendix A for mode transition information.

3.2.2 Read Identifier

To read the manufacturer and device codes, the device must be in read-identifier mode, which can be reached by writing the Read Identifier command (90H). Once in read-identifier mode, $A_0 = 0$ outputs the manufacturer's identification code, and $A_0 = 1$ outputs the device identifier (see Table 5) Note: A_1–$A_{21} = 0$. To return to read-array mode, write the Read-Array command (FFH).

Table 5. Read Identifier Table

Size	Mfr. ID	Device Identifier	
		-T (Top Boot)	-B (Bottom Boot)
28F004B3	0089H	D4H	D5H
28F400B3		8894H	8895H
28F008B3	0089H	D2H	D3H
28F800B3		8892H	8893H
28F016B3		D0H	D1H
28F160B3	0089H	8890H	8891H
28F320B3		8896H	8897H
28F640B3		8898H	8899H

3.2.3 Read Status Register

The device status register indicates when a Program or Erase operation is complete, and the success or failure of that operation. To read the status register, issue the Read Status Register (70H) command to the CUI. This causes all subsequent Read operations to output data from the status register until another command is written to the CUI. To return to reading from the array, issue the Read Array (FFH) command.

The status-register bits are output on DQ_0–DQ_7. The upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status Register command.

The contents of the status register are latched on the falling edge of OE# or CE#, which prevents possible Bus errors that might occur if status-register contents change while being read. CE# or OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the status register indicate whether or not the WSM was successful in performing the preferred operation (see Table 7 on page 17).

3.2.3.1 Clearing the Status Register

The WSM sets status bits 1 through 7 to "1," and clears bits 2, 6, and 7 to "0," but cannot clear status bits 1 or 3 through 5 to "0." Because bits 1, 3, 4, and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before

reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. Note, again, that the Read Array command must be issued before data can be read from the memory array.

3.2.4 Program Mode

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write that specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program preferred bits of the addressed location, then verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location being changed to a "0." If users attempt to program "1"s, the memory cell contents do not change and no error occurs.

The status register indicates programming status: while the program sequence executes, status bit 7 is "0." The status register can be polled by toggling either CE# or OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the program-status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set, then V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted on a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status-register reads, be sure to reset the CUI to read-array mode.

3.2.4.1 Suspending and Resuming Program

The Program Suspend halts the in-progress program operation to read data from another location of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status-register data after the Program Suspend command is written. Polling status-register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to "1"). t_{WHRH1}/t_{EHRH1} specify the program-suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands while program is suspended are Read Status Register, Read Identifier, and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the program process and status-register bits SR.2 and SR.7 will automatically be cleared. After the Program Resume command is written, the device automatically outputs status-register data when read (see Appendix E for *Program Suspend and Resume Flowchart*). V_{PP} must remain at the same V_{PP} level used for program while in program-suspend mode. RP# must also remain at V_{IH}.

3.2.5 Erase Mode

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to "1." Only one block can be erased at a time. The WSM will execute a sequence of internally timed events to program all bits within the block to "0," erase all bits within the block to "1," then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a "0."

When the status register indicates that erasure is complete, check the erase-status bit to verify that the Erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the status register will be set to a "1," indicating an erase failure. If V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an Erase error, and SR.3 is set to a "1" to identify that V_{PP} supply voltage was not within acceptable limits.

After an Erase operation, clear the status register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status-register reads, it is advisable to place the flash in read-array mode after the erase is complete.

3.2.5.1 Suspending and Resuming Erase

Since an Erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from—or program data to—another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI requests that the WSM pause the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the Erase operation has been suspended.

A Read Array/Program command can now be written to the CUI in order to read data from/program data to blocks other than the one currently suspended. The Program command can subsequently be suspended to read yet another array location. The only valid commands while Erase is suspended are Erase Resume, Program, Read Array, Read Status Register, or Read Identifier. During erase-suspend mode, the chip can be placed in a pseudo-standby mode by taking CE# to V_{IH}, which reduces active current consumption.

Erase Resume continues the erase sequence when CE# = V_{IL}. As with the end of a standard Erase operation, the status register must be read and cleared before the next instruction is issued.

Table 6. Command Bus Definitions (1,4)

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array		Write	X	FFH			
Read Identifier	2	Write	X	90H	Read	IA	ID
Read Status Register		Write	X	70H	Read	X	SRD
Clear Status Register		Write	X	50H			
Program	3	Write	X	40H / 10H	Write	PA	PD
Block Erase/Confirm		Write	X	20H	Write	BA	D0H
Program/Erase Suspend		Write	X	B0H			
Program/Erase Resume		Write	X	D0H			

NOTES:

PA: Program Address **PD:** Program Data **BA:** Block Address
IA: Identifier Address **ID:** Identifier Data **SRD:** Status Register Data

1. Bus operations are defined in Table 3.
2. Following the Intelligent Identifier command, two Read operations access manufacturer and device codes. A_0 = 0 for manufacturer code, A_0 = 1 for device code. A_1–A_{21} = 0.
3. Either 40H or 10H command is valid although the standard is 40H.
4. When writing commands to the device, the upper data bus [DQ_8–DQ_{15}] should be either V_{IL} or V_{IH}, to minimize current draw.

Table 7. Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check Write State Machine bit first to determine word program or block-erase completion, before checking program or erase-status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When erase suspend is issued, WSM halts execution and sets both WSMS and ESS bits to “1.” ESS bit remains set at “1” until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erasure 0 = Successful Block Erase	When this bit is set to “1,” WSM has applied the max. number of erase pulses to the block and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Word Program 0 = Successful Word Program	When this bit is set to “1,” WSM has attempted but failed to program a word.
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} Low Detect, Operation Abort 0 = V_{PP} OK	The V_{PP} status bit does not provide continuous indication of V_{PP} level. The WSM interrogates V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if V_{PP} has not been switched on. The V_{PP} is also checked before the operation is verified by the WSM. The V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} max and V_{PP1} min or between V_{PP1} max and V_{PP4} min.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When program suspend is issued, WSM halts execution and sets both WSMS and PSS bits to “1.” PSS bit remains set to “1” until a Program Resume command is issued.
SR.1 = BLOCK LOCK STATUS 1 = Program/Erase attempted on locked block; Operation aborted 0 = No operation to locked blocks	If a Program or Erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	This bit is reserved for future use and should be masked out when polling the status register.

NOTE: A Command Sequence Error is indicated when SR.4, SR.5, and SR.7 are set.

3.3 Block Locking

The 3-Volt Advanced Boot Block flash memory architecture features two hardware-lockable parameter blocks.

3.3.1 WP# = V_{IL} for Block Locking

The lockable blocks are locked when WP# = V_{IL}; any program or Erase operation to a locked block will result in an error, which will be reflected in the status register. For top configuration, the top two parameter blocks (blocks #133 and #134 for the 64 Mbit, #69 and #70 for the 32 Mbit, blocks #37 and #38 for the 16 Mbit, blocks #21 and #22 for the 8 Mbit, blocks #13 and #14 for the 4 Mbit) are lockable. For the bottom configuration, the bottom two parameter blocks (blocks #0 and #1 for 4 /8 /16 /32/64 Mbit) are lockable. Unlocked blocks can be programmed or erased normally (unless V_{PP} is below V_{PPLK}).

3.3.2 WP# = V_{IH} for Block Unlocking

WP# = V_{IH} unlocks all lockable blocks.

These blocks can now be programmed or erased.

Note that RP# does not override WP# locking as in previous Boot Block devices. WP# controls all block locking and V_{PP} provides protection against spurious writes. Table 8 defines the write-protection methods.

Table 8. Write-Protection Truth Table for the Advanced Boot Block Flash Memory Family

V_{PP}	WP#	RP#	Write Protection Provided
X	X	V_{IL}	All Blocks Locked
V_{IL}	X	V_{IH}	All Blocks Locked
≥ V_{PPLK}	V_{IL}	V_{IH}	Lockable Blocks Locked
≥ V_{PPLK}	V_{IH}	V_{IH}	All Blocks Unlocked

3.4 V_{PP} Program and Erase Voltages

Intel® 3-Volt Advanced Boot Block products provide in-system programming and erase at 2.7 V. For customers requiring fast programming in their manufacturing environment, 3-Volt Advanced Boot Block includes an additional low-cost 12-V programming feature.

The 12-V V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during program and Erase operations for a maximum of 1000 cycles on the main blocks, and 2500 cycles on the parameter blocks. V_{PP} may be connected to 12 V for a total of 80 hours maximum.

Warning: Stressing the device beyond these limits may cause permanent damage.

During Read operations or idle times, V_{PP} may be tied to a 5-V supply. For Program and Erase operations, a 5-V supply is not permitted. The V_{PP} must be supplied with either 2.7 V–3.6 V or 11.4 V–12.6 V during Program and Erase operations.

3.4.1 V_{PP} = V_{IL} for Complete Protection

The V_{PP} programming voltage can be held low for complete write protection of all blocks in the flash device. When V_{PP} is below V_{PPLK}, any Program or Erase operation will result in a error, prompting the corresponding status-register bit (SR.3) to be set.

3.5 Power Consumption

Intel flash devices have a tiered approach to power savings that can significantly reduce overall system power consumption. The Automatic Power Savings (APS) feature reduces power consumption when the device is selected but idle. If the CE# is deasserted, the flash enters its standby mode, where current consumption is even lower. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

3.5.1 Active Power

With CE# at a logic-low level and RP# at a logic-high level, the device is in the active mode. Refer to the DC Characteristic tables for I_{CC} current values. Active power is the largest contributor to overall system power consumption. Minimizing the active current could have a profound effect on system power consumption, especially for battery-operated devices.

3.5.2 Automatic Power Savings (APS)

Automatic Power Savings provides low-power operation during read mode. After data is read from the memory array and the address lines are quiescent, APS circuitry places the device in a mode where typical current is comparable to I_{CCS}. The flash stays in this static state with outputs valid until a new location is read.

3.5.3 Standby Power

With CE# at a logic-high level (V_{IH}) and the device in read mode, the flash memory is in standby mode, which disables much of the device circuitry, and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the status of the OE# signal. If CE# transitions to a logic-high level during Erase or Program operations, the device will continue to perform the operation and consume corresponding active power until the operation is completed.

System engineers should analyze the breakdown of standby time versus active time, and quantify the respective power consumption in each mode for their specific application. This approach will provide a more accurate measure of application-specific power and energy requirements.

3.5.4 Deep Power-Down Mode

The deep power-down mode is activated when RP# = V_{IL} (GND ± 0.2 V). During read modes, RP# going low de-selects the memory and places the outputs in a high-impedance state. Recovery from deep power-down requires a minimum time of t_{PHQV} (see *AC Characteristics—Read Operations,* Section 4.5).

During program or erase modes, RP# transitioning low will abort the in-progress operation. The memory contents of the address being programmed or the block being erased are no longer valid as the data integrity has been compromised by the abort. During deep power-down, all internal circuits are switched to a low-power savings mode (RP# transitioning to V_{IL} or turning off power to the device clears the status register).

3.6 Power and Reset Considerations

3.6.1 Power-Up/Down Characteristics

In order to prevent any condition that may result in a spurious write or erase operation, it is recommended to power-up V_{CC} and V_{CCQ} together. Conversely, V_{CC} and V_{CCQ} must power-down together. It is also recommended to power-up V_{PP} with or slightly after V_{CC}. Conversely, V_{PP} must powerdown with or slightly before V_{CC}.

If V_{CCQ} and/or VPP are not connected to the V_{CC} supply, then V_{CC} should attain V_{CC}Min before applying VCCQ and VPP. Device inputs should not be driven before supply voltage = VCCMin. Power supply transitions should only occur when RP# is low.