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TEA19031AT

USB-PD controller for SMPS

Rev. 2 — 1 December 2017 Product data sheet

1 General description

The TEA19031AT is a highly configurable secondary side SMPS controller that is available in many factory configured versions. Section 15 gives an overview of the off-the-shelf available versions of the TEA19031AT. To inquire about the possibilities of customer-specific versions, contact your local sales representative.

The TEA19031AT supports the following protocols:

- USB Power Delivery (USB-PD) 2.0 (certified: 2017-03-22; test ID: 100054)
- USB type-C v1.2

Together with the TEA193x primary controller and the TEA199x secondary side Synchronous Rectifier (SR) controller, a Switched Mode Power Supply (SMPS) can be built.

The SMPS has a small form factor and ultra-high efficiency over the entire load range. This power supply has an extremely low no-load input power (< 30 mW). It meets efficiency requirements like CoC Tier-2, EuP lot 6, and DOE v6. The complete SMPS system can be built at low cost with a minimum number of external components.

The TEA19031AT has a high level of digital integration. It incorporates all circuits, including a charge pump to drive an external NMOS load switch directly. It also incorporates a USB PD Physical Interface (PHY) and an integrated driver for fast output discharge.

The output voltage and output current are continuously measured. They are used to control the SMPS. The NTC pin can continuously measure the adapter temperature or the temperature in the cable/connector. Optionally, the NTC pin can also be used for other features, like OTP or Synchronous Rectification (SR). The die temperature of the TEA19031AT is measured and protected via an internal temperature sensor.

The TEA19031AT provides best-in-class charging safety. To ensure the safe operation of the SMPS, it incorporates all required protections. These protections cover up to 19 different failure use cases (see Section 2.3).

To ensure correct operation under all conditions, all protections are implemented in hardware. So, when the microcontroller stops, the protections are still functional.

If an output short circuit occurs, the power dissipation from the mains input in the adapter is less than 50 mW.

For output voltage/current regulation, and protection, only a single optocoupler is required in the application. The TEA19031AT operates in Constant Voltage (CV) mode with better than 2 % Voltage accuracy or in Constant Current (CC) mode with better than 2 % full load current accuracy.

2 Features and benefits

2.1 General

- Best-in-class full safe application for high-power adapters, which gives complete protection against overload conditions in the load (e.g. phone)
- Wide output voltage operating range (2.9 V to 20 V)
- Ultra-high efficiency together with TEA193x QR/DCM controller and TEA199x SR controller
- Very low no-load power (< 30 mW for the complete system solution)
- High power density
- Dedicated SW pin to drive external NMOS directly
- Constant Voltage (CV) and Constant Current (CC) control
- Precise voltage and current control with low minimum step size (voltage 12-bit DAC, current 10-bit DAC)
- Continuous accurate measurement of output voltage and output current
- Low-cost SO10 package (suitable for reflow soldering and wave soldering)
- Low-cost Bill Of Materials (BOM; ≈15 external components)
- Embedded MCU (with ROM, RAM, and MTP memory)
- Discharge pin for fast discharge
- Built-in series regulator and cable compensation
- Non-volatile MTP memory for storage of system configuration parameters

2.2 Protocol support

- USB-PD 2.0 (certified: 2017-03-22; test ID: 100054) and USB type C v1.2
- Supports unstructured Vendor Defined Messages (VDMs).

2.3 Protections

- Internal OverTemperature Protection (OTP)
- Adaptive OverVoltage Protection (OVP)
- Adaptive UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)
- UnderVoltage LockOut (UVLO) protection
- Output Short Protection (OSP)
- Open-SUpply Protection (OSUP)
- Overvoltage protection CC1, and CC2 pins
- Soft short protection at the CC1 and CC2 pins
- Soft short protection at the output

Due to dedicated functionality to drive an external load switch, which is available in hardware, the TEA19031AT ensures safe operation under all conditions.

3 Applications

- USB-PD 2.0 and USB type-c v1.2 chargers with optional VDM support for smartphones, tablets, and laptops

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA19031AET/1	SO10	plastic small outline package; 10 leads; body width: 3.9 mm; body thickness 1.35 mm	SOT1437-1
TEA19031AFT/1			
TEA19031AGT/1			
TEA19031AMT/1			
TEA19031AOT/1			
TEA19031AQT/1			

5 Marking

Table 2. Marking

Type number	Marking code
TEA19031AET/1	EA19031AE
TEA19031AFT/1	EA19031AF
TEA19031AGT/1	EA19031AG
TEA19031AMT/1	EA19031AM
TEA19031AOT/1	EA19031AO
TEA19031AQT/1	EA19031AQ

6 Block diagram

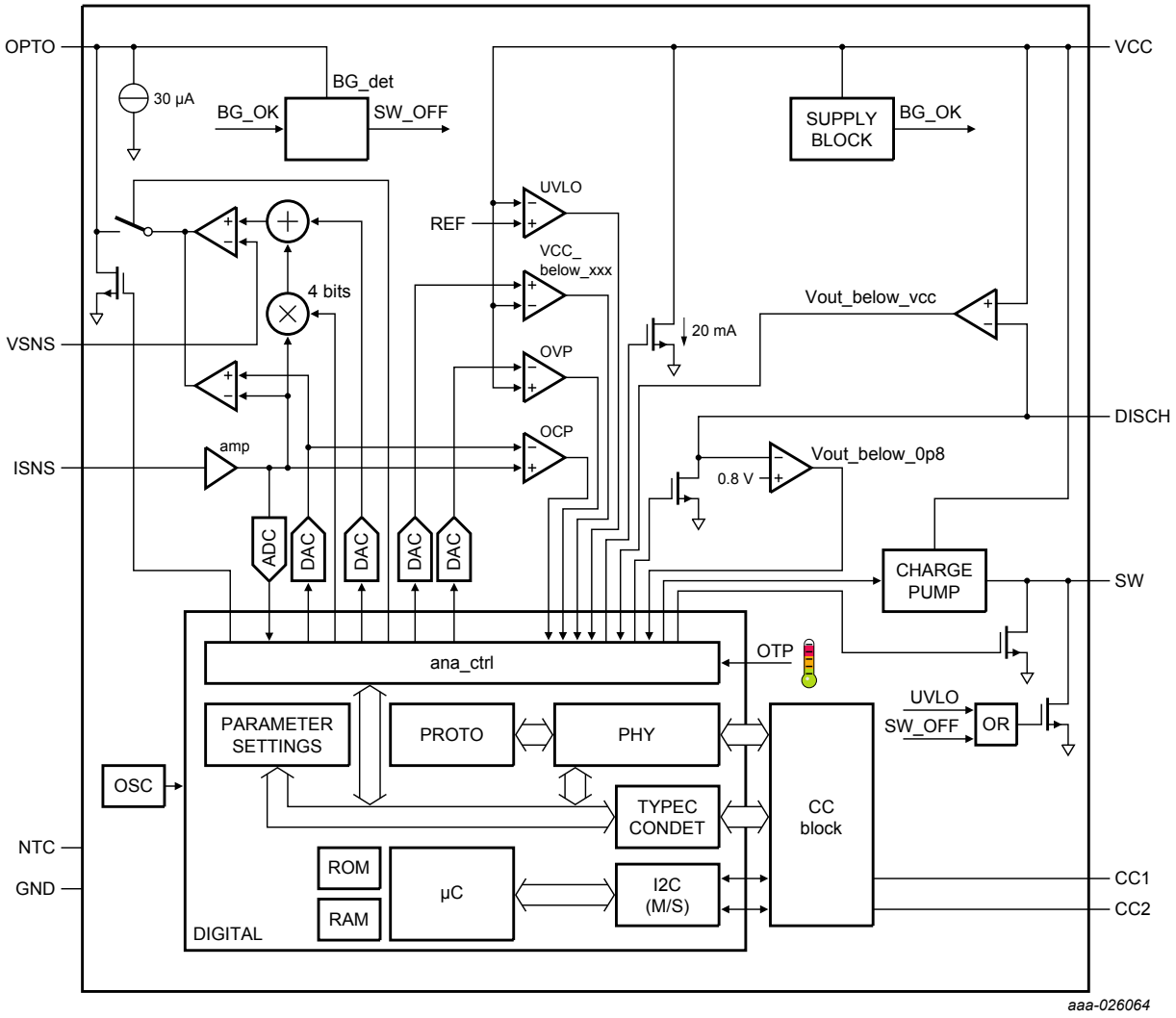


Figure 1. TEA19031AT block diagram

7 Pinning information

7.1 Pinning

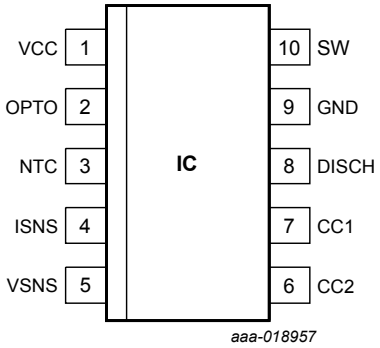


Figure 2. TEA19031AT pinning diagram (SOT1437-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VCC	1	supply voltage
OPTO	2	OPTO driver
NTC	3	external temperature measurement
ISNS	4	current sense input
VSNS	5	voltage sense input
CC2	6	type C CC2 line detection and USB-PD communication
CC1	7	type C CC1 line detection and USB-PD communication
DISCH	8	fast discharge sink
GND	9	ground
SW	10	NMOS gate drive output

8 Functional description

The TEA19031AT can be considered as a versatile replacement for the well-known TL431 shunt regulator series, where:

- The VSNS pin takes the role of the REF input of the TL431
- The OPTO pin the role of the cathode
- The GND pin the role of the anode

In addition to the Constant Voltage (CV) mode, which is regulated via the VSNS pin, the system supports Constant Current (CC) mode. The current control loop is regulated and the cable compensation is added via the ISNS pin.

Alternatively, the ISNS input can be used for OverCurrent Protection (OCP). Several other protections are available. For guaranteed safety, all protections are implemented in hardware. So, even when the microcontroller stops, the protections are still functional.

The output voltage and the output current can be controlled via USB-PD using the CC pins.

The output current and the output voltage are continuously measured via an integrated AD-converter. The values can be requested via the USB-PD protocol. The applied time constant of the digital filter is initialized via the firmware. A dedicated signal that indicates a stable output voltage/output current for a reliable measurement is available. It can be used, for example, to determine and monitor the resistance of the cable connected between the charger and the portable device.

The external temperature, measured via the NTC pin is continuously monitored. From the NTC voltage and applied current, the controller calculates the corresponding temperature. This temperature is communicated to the portable device. For some variants, an OTP function is also added to this external temperature measurement.

The available protections, in combination with the NMOS load switch, ensure a fully safe operation with only one optocoupler required. When the optocoupler fails, the primary OVP ensures a safe application, as its level can be set at a fixed percentage above the maximum regulated output voltage. All essential protections are implemented in hardware. They are independent from the processor actions.

The TEA19031AT fully supports the type-C connector standard.

When a Type C receptacle is used, the CC1/CC2 pair is used for plug attach/detach detection. After a detection, communication takes place via the same CC pins according to the USB-PD communication standard.

The USB-PD specification requires the use of a load switch and certain discharge behavior of the output voltage at the connector V_{bus}. So, to drive the gate of an external NMOS switch, the TEA19031AT is equipped with an SW pin. To be able to discharge V_{bus} using an external resistor in series with an internal switch, the TEA19031AT is also equipped with a DISCH pin.

8.1 Start-up and supply

The TEA19031AT is supplied via the VCC pin connected to the secondary DC voltage of an AC-to-DC SMPS converter (see Figure 6). To control the primary side controller, this VCC voltage is regulated via an integrated voltage/current control loop with external loop compensation and an external optocoupler. This optocoupler is part of the gain loop of the primary side SMPS controller.

At each start-up and after power-on reset, the optocoupler current is initially zero. So, the AC-to-DC converter starts up with full output power, resulting in a rapid increase of the VCC voltage. Due to the low $V_{CC(start)}$ level (≈3 V), the TEA19031AT ensures that it is fully operating before the V_{CC} reaches the default initial regulation levels. These default values of the initial regulation levels are programmed in the non-volatile memory (MTP) are 5 V and 3 A, respectively.

At power-on reset, the safe default values, which are read from MTP, are set.

When the V_{CC} voltage is below the UVLO level, the external NMOS load switch is off. When the output is shorted while the load switch is closed, the UVLO is also triggered. The load switch is then immediately opened and the system restarts after the safe restart timer.

When the V_{CC} exceeds the UVLO level, all circuits, the initial DAC value, and the resistive divider ratio are initialized. The system regulates the output to 5 V with a limited output current of 3 A.

To minimize the output voltage overshoot after start-up, an internal 20 mA current sink is applied to VCC when the VCC voltage exceeds $V_{o(default)}$ × 1.05. The sink current remains active until the VCC voltage has dropped to below $V_{o(default)}$ × 1.05 again.

After the output voltage has stabilized, the load switch is turned on and the system waits for an attach. As long as no load is attached, the VCC supply current is reduced by disabling some internal circuitry. In this way, the no-load input power is minimized.

When the voltage on only one of the CC pins drops to below the $V_{IH(Rd)}$ level, an attach is detected.

If an attach is detected, all internal circuitries are enabled. The voltages can be changed via the USB-PD protocol.

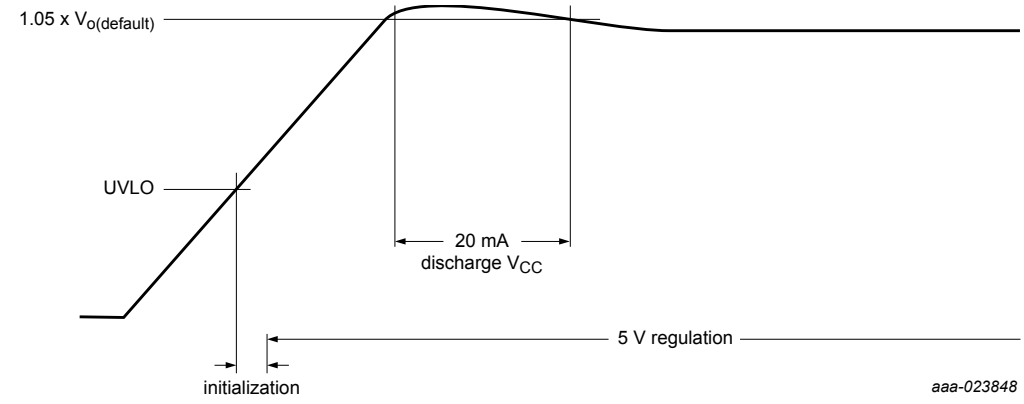


Figure 3. Start-up sequence

The TEA19031AT can continuously operate on supply voltages up to 21 V. The OVP level is set to default 120 % or 125 % of the programmed output voltage. The UVP level

is continuously set to default 60 % of the programmed output voltage. The voltage on the VCC pin is used to detect an OVP and UVP.

If the supply voltage drops to below the UVLO level, the system returns to the no-supply state and opens the load switch.

8.2 Voltage loop

The analog Constant Voltage (CV) loop regulates VCC such that the voltage on the VSNS pin equals the internal reference voltage. For the TEA19031AET and TEA19031AFT (maximum output 20 V), with the external resistor divider from the VCC pin to the VSNS pin at 1/8.325, the output is 8.325 times the voltage on the VSNS pin. Any deviation from this external resistor value results in a different gain value and so a different output voltage. The CV loop is regulated by varying the current drawn into the OPTO pin, so it is compatible with the optocoupler feedback used in most AC-to-DC converters. An external series RC combination between the OPTO and VSNS pins defines the dynamic behavior of the integrating part. An external resistor in series with the optocoupler defines the dynamic behavior of the proportional part of the regulation loop (see Section 13.3). For the TEA19031AGT and TEA19031AQTapplications up to 13 V, the gain is set to 5.476. So these applications require an external resistor divider of 1/5.476. The resistor divider layout must be close to the TEA19031AT (see Section 13.1 for details).

The TEA19031AT incorporates several protections. All these protections operate in safe restart mode. The load switch is opened immediately. When the fault condition disappears after a certain delay and V_{CC} is at the default value again, the load switch is closed. For more information on the protections (see Section 8.11).

When a new voltage is requested via the USB-PD communication protocol, the internal reference voltage is updated to this new setting within 20 µs. The control loop via the optocoupler generates the requested output voltage following the speed of the SMPS system. If there is a transition down, a predefined ramp down sequence is followed to prevent that a high undershoot occurs. The ramp down is done via a parabolic slope control. For a transition up, no special measures are required to prevent an overshoot when a protection is triggered. The reason is that the charging current of the loop capacitor lifts the voltage on the VSNS pin when the V_{CC} voltage in the application increases.

The parabolic discharge curve (see Figure 4; patent pending) initially causes the voltage loop to saturate, due to the initial rapid ramp down. However, it allows the loop to recover and to resume regulation toward the end of the curve. The total parabolic sequence time is chosen such that no undershoot under the final end value occurs.

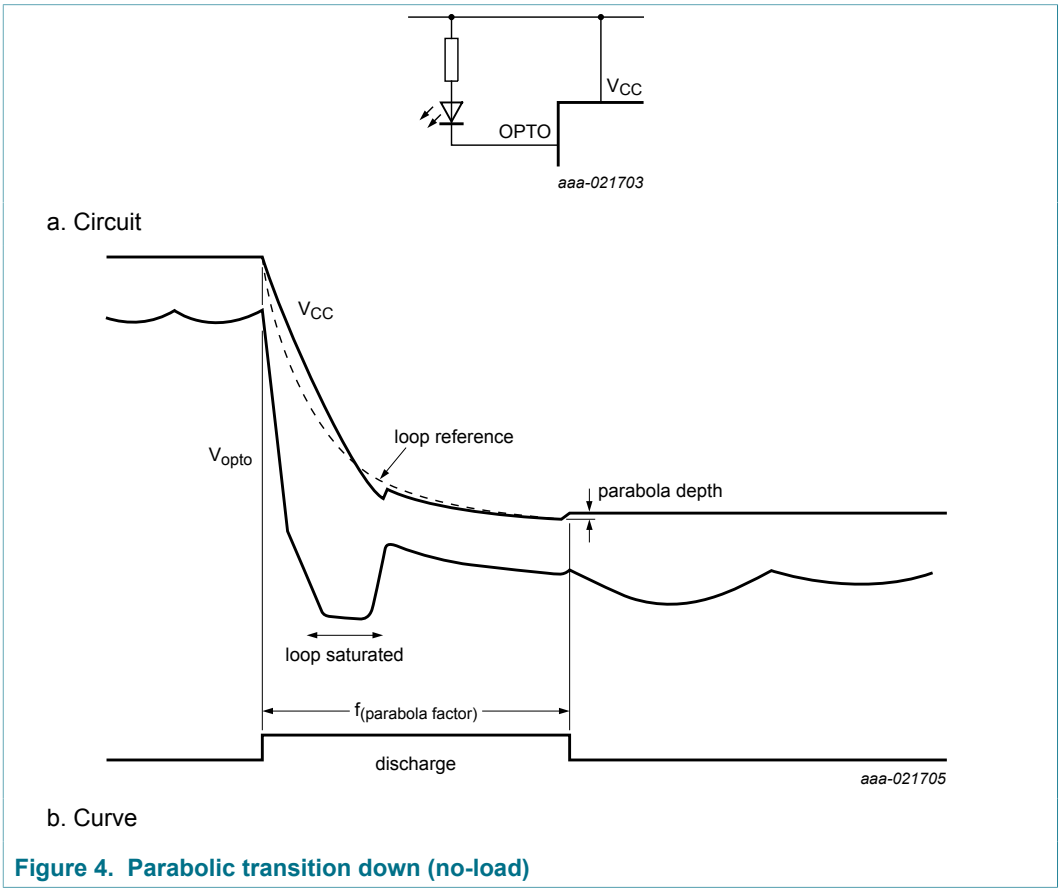


Figure 4. Parabolic transition down (no-load)

8.3 Current loop

The voltage drop across a small external series resistor between the output return terminal and the converter ground is supplied to the ISNS pin and is a measure for the output current. Internally, an amplifier boosts up the voltage at the ISNS pin by a gain factor 50. The boosted voltage is then converted to a current with an internal resistance gain value. For the TEA19031AET, the TEA19031AFT, the TEA19031AMT, and the TEA19031AOT to comply with this internal resistance gain, the external resistor must be exactly 10 mΩ (see Section 15). For the TEA19031AGT and the TEA19031AQT, it must be 5 mΩ (see Section 15).

Any deviation from the MTP value, e.g. due to PCB-layout imperfections, causes a current error and must be corrected (see Section 13.2).

The external resistor value and internal multiplication factor must be such that the output of the amplifier is limited to 2.5 V. If, for example, the maximum output current is 5 A, an external resistor of below 10 mΩ (e.g. 5 mΩ) must be used for a multiplication factor of 50.

For SMPS voltage and current stability reasons, an external series RC combination must be connected between the OPTO pin and the ISNS pin (see Section 13.4).

8.4 Cable compensation

The cable compensation is proportional with the R_{sense} and the resistive divider. The maximum cable compensation for a 1 A current can be calculated with the following equation: R_{sense} * 8 / R_{div}.

When R_{sense} is 10 mΩ and the resistive divider is 1/8.325, the maximum cable compensation is 666 mV/A. MTP sets the default cable compensation and can be read in Section 15. Setting the cable compensation above 200 mV/A is not recommendable.

8.5 Load switch

The load can be disconnected from the adapter output voltage via an external low-cost NMOS transistor (see Figure 6). The load switch is connected between VCC and V_{bus}. To control the NMOS, the TEA19031AT has a dedicated switch drive output (SW pin). This output is supplied with an output voltage of 6 V above V_{CC} via an internal charge pump.

As long as V_{CC} is below the UVLO level or if the VCC connection is open, the SW pin is held low, ensuring that the load switch is off. To ensure that the NMOS is also kept off when the SW pin is disconnected, an external (high-ohmic) resistor is required between the gate of the NMOS and V_{bus}.

To overcome the influence of the back-gate diode, it is also possible to apply two NMOS switches in series, with their sources connected together.

8.6 Discharge function

The DISCH pin, which has an internal low-ohmic switch, provides the means to discharge the output V_{bus} quickly. An external resistor in series limits the maximum current and the IC dissipation.

To check if the output voltage has dropped to below 0.8 V, a second comparator is implemented. This voltage drop is a requirement of the USB-PD specification (vSafe0V) if there is a hard reset.

When the internal DISCH switch is activated, the voltage at the DISCH pin is always low, because of the external current limiting resistor. A mechanism has been implemented to check the real output voltage. During a hard reset discharge sequence, when V_{CC} is below vSafe5V, the switch is opened every millisecond for 20 µs to check the output voltage at the end of the 20 µs period. The check of the output voltage is done until the voltage remains below 0.7 V and the hard reset discharge sequence is terminated. For this check to work properly, the capacitance on the DISCH pin and the external current limiting resistor must have a time constant that is short enough.

To ensure that the output remains low, a 1 mA sink current is present on the DISCH pin when both the load switch and discharge switch are off. The period that the DISCH pin is active in unattached state is typically 100 ms by default. The reason for this limitation is to prevent that excessive power dissipation occurs when an external V_{bus} voltage is applied.

8.7 Detach detection

If the type C cable is disconnected, the output voltage of the TEA19031AT application returns to its default value (5 V) after 200 µs.

8.8 Internal temperature measurement

The internal die temperature is continuously monitored. The temperature readout is used to make an overtemperature protection (see Table 4).

8.9 External temperature measurement

The TEA19031AT includes a dedicated NTC pin. The NTC pin can be used to, e.g., measure the adapter temperature or the cable connector temperature. The temperature value is continuously available to be sent to the portable device using one of the protocols (e.g. via VDMs in the USB-PD protocol).

For accurate temperature measurement over the complete temperature range, the external NTC is supplied via an adaptive and trimmed internal current source (see Figure 5).

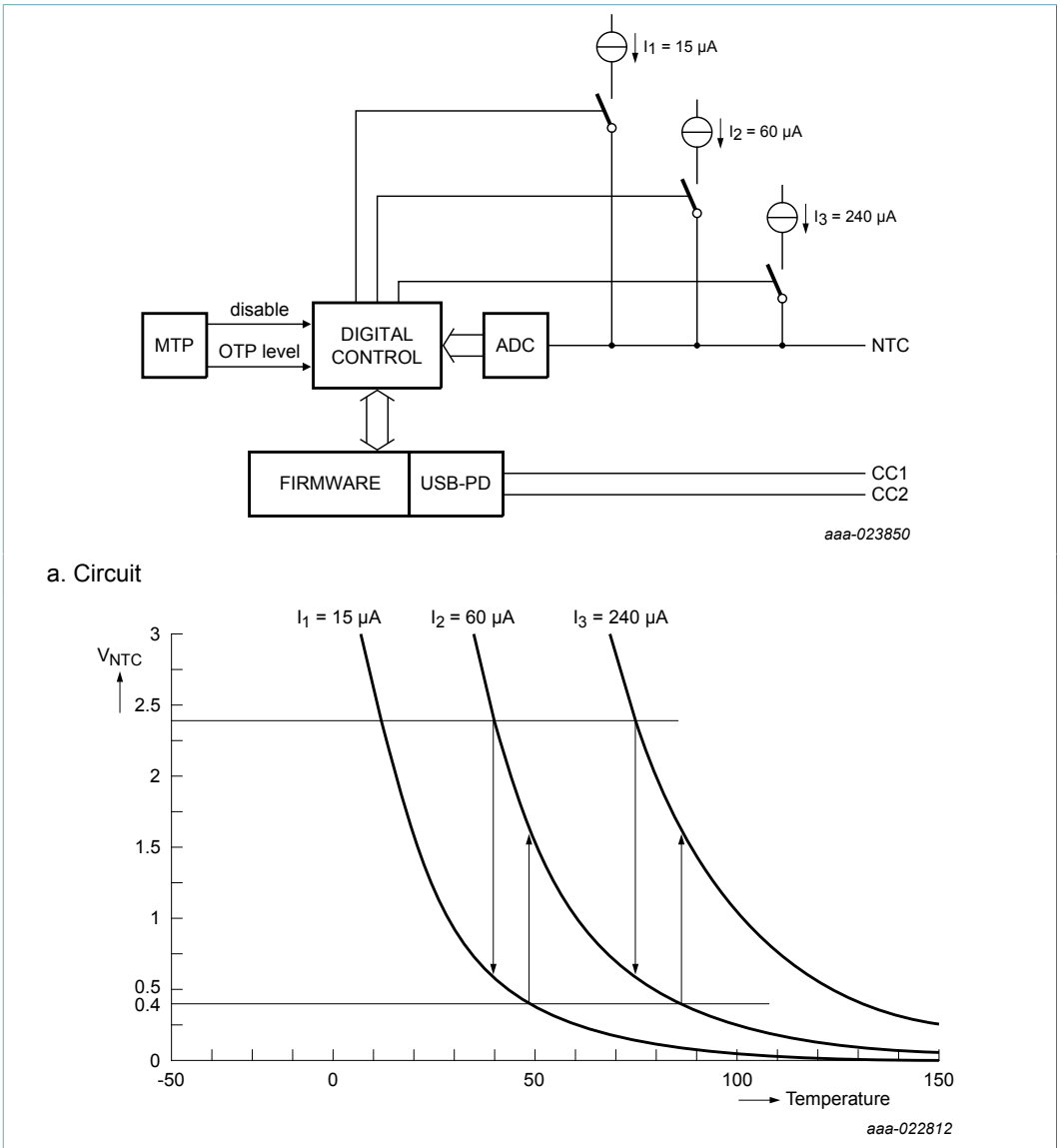


Figure 5. External NTC is supplied via adaptive current sources

The voltage at the NTC pin is measured via an internal A-to-D converter. If the voltage on the NTC pin drops to below 400 mV, the source current of the pin is increased. If the voltage on this pin exceeds 2.4 V, the source current of the pin is decreased. In this way, the temperatures are measured with a better than 5 °C accuracy for a range of 0 °C to > 120 °C when using a typical external resistor.

Optionally, an OTP function can be added to these pins. The OTP level can be initialized via the MTP and handled by the hardware, which ensures a proper OTP function that is independent of the firmware. Depending on the type, the OTP is enabled or disabled (see Section 15).

8.10 Communication

The TEA19031AT hardware supports using the CC wire in a USB Type-C cable.

The USB Type-C connectors and cables support all protocols. If a type C receptacle is used, V_{bus} is only connected to the converter output via the load switch when an attach is detected on one of the CC pins.

8.10.1 USB Type-C

The TEA19031AT adheres to the USB Type-C 1.2 specification (see Ref. 2) in the sense that the distinct pull-up current values support attach/detach and current capability advertising. The attach/detach detection is done in the hardware. So, if there is a detach, a return of V_{bus} to vSafe5V is always ensured. The hardware implementation of the return of V_{bus} to vSafe5V eliminates the risk of software implementations where V_{bus} may stay at an unsafe level if the program execution stalls.

8.10.2 USB-PD

The TEA19031AT supports the USB-PD 2.0 specification (certified: 2017-03-22; test ID: 100054).

Maximum seven different Power Data Objects (PDO) can be defined in non-volatile memory. By default, limited PDOs are supported with different current levels (see Section 15). All PDO currents are protected with an OCP.

8.10.3 Discover identification

The TEA19031AT supports the discover identification protocol in USB-PD. It is possible to program different VID, PID, and BCD values in dedicated memory addresses with an NXP tool, using VDMs.

8.10.4 MTP configuration

The TEA19031AT is configurable via MTP. The different types are defined in Section 15.

8.11 Protections

All protections, except UVP and the external OTP, are implemented completely in the hardware. Table 4 gives an overview of the available protections.

8.11.1 Protections overview

Table 4. Overview of protections

Protection	Description	Implementation	Default value	Filter
UVLO	undervoltage lockout	hardware	2.8 V (fixed)	-
OVP	overvoltage protection	hardware	120 % or 125 % × PDO	30 µs
OCP	overcurrent protection	hardware	120 % × PDO	25 ms
OTP (internal)	overtemperature protection	hardware	115 °C	-
OTP external	overtemperature protection	software	90 °C[1]	-
UVP	undervoltage protection	software	60 % × PDO	-
OSUP	open-supply (VCC) protection	hardware	-	-
OV_CC1_CC2	overvoltage protection CC1 and CC2 pins	hardware	-	10 µs analog

[1] The NTC readout and OTP levels are defined with an NTC of 47 kΩ and a B-constant of 4108. It means that the OTP triggers with an impedance of about 4 kΩ. Adding an extra resistor of 1.8 kΩ in series with this NTC increases the OTP by 20 °C to 110 °C. The temperature readout is not accurate anymore. Also, an NTC of 100 kΩ gives the same 20 °C offset. It also results in an OTP level of approximately 110 °C.

8.11.2 Secondary side safe restart protection

When a safe restart protection is triggered, the load switch is immediately turned off. The voltage loop is regulated to the initial value (5 V typical). As the load switch is immediately turned off before the regulation reduces the output power, the VCC voltage may increase. To ensure that the VCC voltage has dropped to a safe value, before the load switch is turned on again, V_{CC} is discharged via an internal current source of 20 mA if it exceeds the level of $V_{o(default)}$ × 1.05.

When the protection is triggered, the safe restart timer is started. After 1 s, a restart sequence is performed, which reinitializes all circuits.

8.11.3 UnderVoltage LockOut (UVLO)

The level at which the UVLO protection is triggered is fixed. When V_{CC} drops to below the UVLO level, the load switch is immediately turned off. All settings are reset to their initial values. Internal circuitries are disabled.

8.11.4 OverVoltage Protection (OVP)

When the level is higher than the default voltage (normally 5 V, but can be adjusted via MTP), the OVP level is set as a percentage (120 % or 125 %) of the requested output voltage level. When V_{CC} continuously exceeds this level for longer than the minimum OVP time (default 30 µs), the OVP protection is triggered.

8.11.5 OverCurrent Protection (OCP)

The default TEA19031AT setting is CC mode where the current loop defines maximum current. However, for higher output power types (e.g. for computer applications), the OCP mode is set. If the output current is continuously higher than the chosen current level for more than the OCP blanking time, OCP is triggered.

8.11.6 Internal OTP

When the internally measured temperature exceeds the OTP setting, OTP is triggered. The value is 115 °C.

8.11.7 External OTP

When the externally measured temperature exceeds the programmed OTP settings, OTP is triggered. Section 15 gives the programmed temperatures for the different types.

8.11.8 NTC pin

The NTC function can be used to measure external temperature. The temperature can be read via VDMs. The NTC readout is only valid with a 47 kΩ NTC resistor and a B-constant of 4108 or a similar NTC.

8.11.9 Open-SUpply Protection (OSUP)

When the supply is not available anymore, the voltage on the OPTO pin is used to turn off the external NMOS load switch actively.

The supply ensures the functioning of the TEA19031AT. Because of this protection, the load can never be damaged if the supply is not available anymore.

8.11.10 UnderVoltage Protection (UVP)

The UVP level is set as a percentage requested output voltage level (60 %). The reaction to a triggering of UVP is programmed in the firmware. The protection is a safe restart protection. The level can never be lower than the UVLO level.

8.11.11 Output Short Protection (OSP)

At a shorted output, the VCC voltage drops to below the UVLO level. The load switch is turned off. After the programmed safe restart time, the output is enabled again. When the VCC voltage exceeds the UVLO level, the primary controller initially limits the maximum output power.

Because the safe restart time is set to 1 s, the dissipation is limited to < 50 mW. This limitation prevents that the application heats up when the output is shorted.

8.11.12 OVP CC1 and CC2 pins (OV_CC1_CC2)

When the CC1 or CC2 pin is shorted to V_{bus}, OVC_CC is triggered. OVC_CC is a safe restart protection. When output voltage is present, this protection is active. When the voltage at the pin exceeds 4.5 V, the protection is triggered. This OVP_CC has some detection filtering. It only switches on after 150 µs (typical).

8.11.13 Soft-short protection CC pins

The CC pins are also protected with a soft-short protection. The impedance levels on the CC lines are checked. If they are not in alignment with the USB-PB protocol, the output is protected.

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCC}	voltage on pin VCC		−0.5	+26	V
V_{OPTO}	voltage on pin OPTO		−0.5	+26	V
V_{CC1}	voltage on pin CC1		−0.5	+26	V
V_{CC2}	voltage on pin CC2		−0.5	+26	V
V_{SW}	voltage on pin SW		−0.5	V_{CC} + 9	V
V_{DISCH}	voltage on pin DISCH		−0.5	+26	V
V_{VSNS}	voltage on pin VSNS		−0.5	+3.6	V
V_{ISNS}	voltage on pin ISNS		−0.5	+3.6	V
V_{NTC}	voltage on NTC pin		−0.5	+3.6	V
General					
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−40	+150	°C
ElectroStatic Discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM)	−2000	+2000	V
		Charged Device Model (CDM)	−500	+500	V
		Machine Model (MM)	−200	+200	V

10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCC}	voltage on pin VCC		0	21	V
V_{OPTO}	voltage on pin OPTO		0	21	V
V_{CC1}	voltage on pin CC1		0	5	V
V_{CC2}	voltage on pin CC2		0	5	V
V_{SW}	voltage on pin SW		0	V_{CC} + 6	V
V_{DISCH}	voltage on pin DISCH		0	21	V
V_{VSNS}	voltage on pin VSNS		0	3.3	V
V_{ISNS}	voltage on pin ISNS		0	3.3	V
V_{NTC}	voltage on pin NTC		0	3.3	V
General					
T_j	junction temperature		−25	+125	°C

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC test board	115	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	JEDEC test board	44	K/W

12 Characteristics

Table 8. Characteristics

T_{amb} = 25 °C; V_{CC} = 5.0 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply (VCC pin)							
$V_{th(UVLO)}$	undervoltage lockout threshold	falling		-	-	2.9	V
I_{CC}	current on VCC pin	unattached; V_{CC} = 5 V		-	1.8	-	mA
		nominal; V_{CC} = 5 V		-	4.25	-	mA
$I_{CC(dch)}$	discharge supply current	discharge current of VCC during safe restart protection; depends on load conditions		-	20	-	mA
		extra discharge current; $V_{CC} = V_{o(default)}$		-	20	-	mA
V_{os}	overshoot voltage			-	1.05 × $V_{o(default)}$	-	V
CC1/CC2 section (CC1 and CC2 pins)							
Type C							
I_{pu}	pull-up current	current source for DFP pull-up indication					
		default current		−64	−80	−96	µA
		1.5 A mode		−166	−180	−194	µA
		3 A mode		−304	−330	−356	µA
V_{IH}	HIGH-level input voltage	with standard 5.1 kΩ pull-down resistance					
		default current		1.5	1.6	1.7	V
		1.5 A mode		1.5	1.6	1.7	V
		3 A mode		2.45	2.60	2.75	V
V_{IL}	LOW-level input voltage	with standard 5.1 kΩ pull-down resistance					
		default current		0.15	0.2	0.25	V
		1.5 A mode		0.35	0.40	0.45	V
		3 A mode		0.75	0.80	0.85	V
V_{ovp}	overvoltage protection voltage	CC1 and CC2 pins		-	4.5	-	V
USB-PD normative specification							
f_{bit}	bit rate	BMC bit rate		270	300	330	Kbps
USB-PD transmitter normative specification							
t_{fall}	fall time	10 % and 90 % amplitude points; minimum is underloaded condition		300	-	650	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rise}	rise time	10 % and 90 % amplitude points; minimum is underloaded condition		300	-	650	ns
V_o	output voltage	signal voltage swing		1.05	1.125	1.2	V
Z_o	output impedance	transmitter	[1]	-	45	-	Ω
USB-PD receiver normative specification							
C_{in}	input capacitance	receiver		-	250	-	pF
$t_{fltr(lim)}$	time constant limiting filter	receiver bandwidth		100	-	-	ns
z_i	input impedance	receiver		10	-	-	MΩ
V_i	input voltage	receiver comparator					
		low level		-	0.55	-	V
		high level		-	0.8	-	V
		hysteresis		-	250	-	mV
Voltage control (VSNS pin)							
V_{ref}	reference voltage	input voltage range on the VSNS pin to control the voltage loop		0.3	-	2.4	V
V_{acc}	voltage accuracy	voltage loop; V_{snsref} = 2 V		−2	-	+2	%
		measurement voltage accuracy		−2	-	+2	%
g_m	transconductance	VCC in; OPTO out		4	-	-	mA/mV
$g_{(max)}$	maximum gain	cable compensation at maximum		-	8	-	mV/mV
Current control (ISNS pin)							
I_{ref}	reference current	parameter is programmed in MTP 10 bits		6	-	40	mV
I_{out}	output current	current loop accuracy; R_{sense} = 5 mΩ					
		0.5 A < I_{out} < 5 A	[2]	−100	-	+100	mA
		I_{out} = 5 A		−2	-	+2	%
		measurement current accuracy; R_{sense} = 5 mΩ					
		I_{out} < 5 A		−100	-	+100	mA
		I_{out} > 5 A		−3	-	+3	%
g_m	transconductance	gain current; amplifier = 50		200	-		mA/mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
NTC pin							
$I_{O(NTC)}$	output current on pin NTC	high temperatures[3]		−228	−240	−252	µA
T_{acc}	temperature accuracy	NTC temperature		−5	-	+5	°C
T_{res}	temperature resolution	temperature measurement		−1	-	+1	°C
Protections							
V_{ovp}	overvoltage protection voltage	overvoltage is programmed in MTP.		3	-	25	V
$V_{ovp(acc)}$	overvoltage protection voltage accuracy	V_{ovp} = 6 V		−3	-	+3	%
$V_{ocp(acc)}$	overcurrent protection voltage accuracy	voltage at ISENSE input pin		−3	-	+3	%
$V_{uvp(acc)}$	undervoltage protection voltage accuracy			−3	-	+3	%
$I_{CC(dch)}$	discharge supply current	during safe restart protection		-	20	-	mA
SW driver							
R_O	output resistance	switch-on		-	80	-	kΩ
		switch-off		-	600	-	Ω
DISCH part (DISCH pin)							
$V_{det(rst)}$	reset detection voltage	hard reset		0.65	0.70	0.75	V
R_{dch}	discharge resistance			-	3	-	Ω
t_{act}	active time	maximum on-time during attach state		-	100	-	ms
OPTO pin							
$I_{O(min)}$	minimum output current			-	30	-	µA
$I_{O(max)}$	maximum output current			3.75	5	6.25	mA
Internal oscillator							
$f_{osc(int)}$	internal oscillator frequency			-	10	-	MHz
Internal temperature protection							
T_{otp}	overtemperature protection trip	switch-on		105	115	125	°C

[1] In the application, an additional resistor can be added to fulfill the USP-PD specification

[2] The current sense pin can be used accurately from 6 mV up to 40 mV. The result is a current range that depends on the R_{sense} resistor. (e.g. with 10 mΩ, the range is between 600 mA and 4 A). If the input voltage is below 3 mV, the readout current reports a fixed current of 50 mA.

[3] See Figure 5.

13 Application information

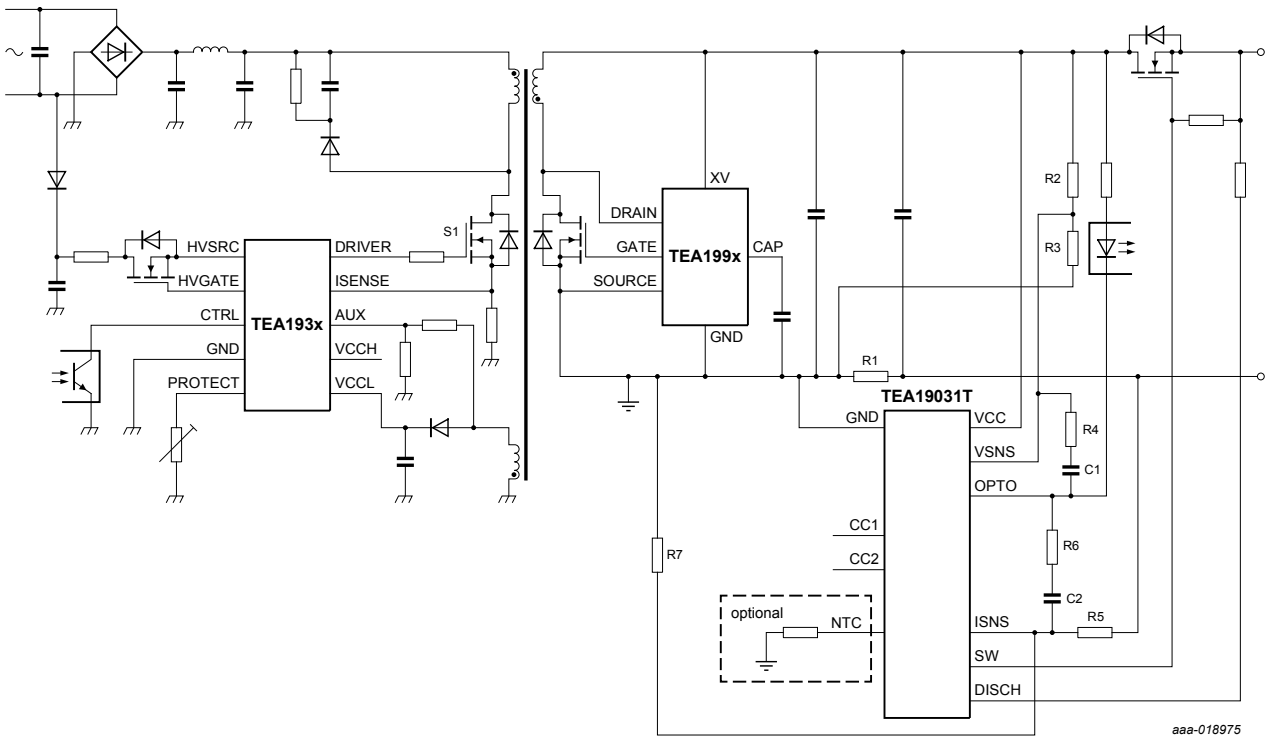


Figure 6. Typical application diagram, including TEA193x TEA199x (low-side SR), and TEA19031AT

13.1 Resistor divider

The resistor divider (R3 / (R2 + R3) connected from the VCC pin to the VSNS pin must reduce the output voltage to < 2.5 V for the maximum output voltage. For 20 V applications, a divider ratio of 1/8.325 is chosen. For applications with a maximum output voltage that does not exceed 12 V, a ratio of 1/5.476 gives the best performance. The reference of the ground of this resistor divider must be connected as close as possible to the GND pin of the TEA19031AT. High-load currents in this ground connection must be prevented.

13.2 Sense resistor

The accuracy of the sense resistor R1 is very important. Any deviation from the value in MTP gives an offset in the current measurement. Because the sense resistor is very low-ohmic, the layout of the connections in the PCB can give major deviations from its initial value.

To overcome this, several options are available:

- Change the MTP-resistor value so that it is in line with the typical resistor value of the sense resistor including the PCB tracks.
- Change the sense resistor value so that the complete value is matching the typical MTP value (10 mΩ).
- Choose the sense resistor value slightly higher (e.g. +15 % than the default MTP value. Trim the value with a resistor divider so that the (R7 / (R5 + R7)) × (R1 + R_{PCB}) matches the MTP default value. R_{PCB} is the resistance of copper wires and the resistance change of the sense resistor due to its soldering profile.

To prevent temperature changes in the current sense measurements, the sense resistor must have a zero temperature coefficient. Also, to ensure accuracy and temperature stability, keep the PCB resistance as low as possible. To prevent magnetic coupling to these parts, which results in pollution in output currents, the length and the area of the connection must be kept as small as possible.

13.3 Voltage loop

An integrator network is connected between the VSNS pin and the optocoupler in the application diagram. The recommended values of these components are:

- R2 = 160 kΩ to 180 kΩ
- R4 = 1 kΩ
- C1 = 10 nF; for the integral part

To prevent magnetic coupling to these parts, which results in pollution in output voltage, the length and the area of the connection must be kept as small as possible.

13.4 Current loop

For Applications that use the CC loop, an integrator network is connected between the ISNS pin and the optocoupler in an application. The recommended values of these components are:

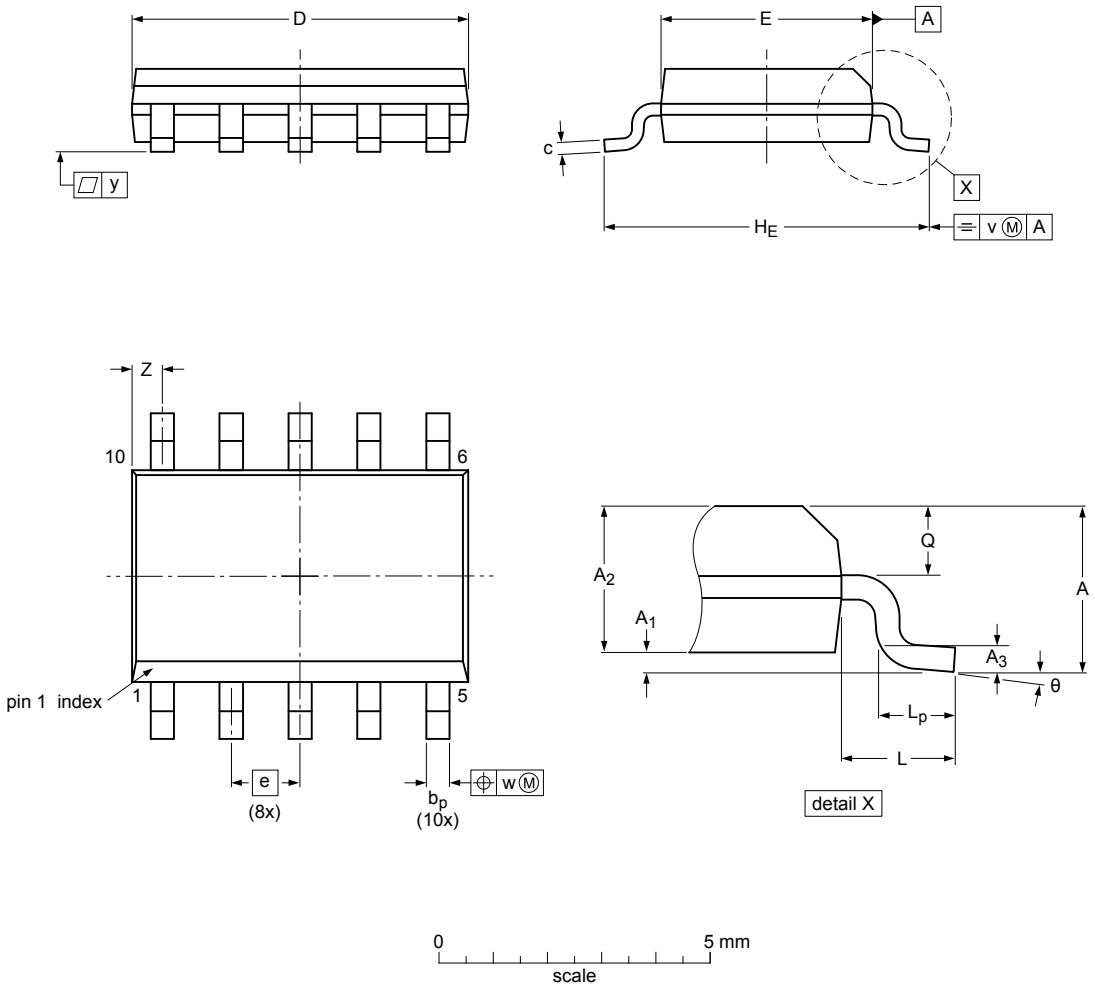
- R5 = 330 Ω when R_{sense} = 10 mΩ; R5 = 160 Ω when R_{sense} = 5 mΩ
- R6 = 5 kΩ
- C2 = 100 nF; for the integral part

To prevent magnetic coupling to these parts, which results in pollution in output currents, the length and the area of the connection must be kept as small as possible.

For applications that only use the OCP mode, these three components can be omitted.

14 Package outline

SO10: plastic small outline package; 10 leads; body width 3.9 mm; body thickness 1.35 mm **SOT1437-1**



Dimensions

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.75	0.25	1.45		0.49	0.25	6.3	4.0		6.20		1.00	0.70				0.70	8°
	nom		0.18	1.35	0.25	0.43	0.22	6.2	3.9	1.27	6.00	1.05	0.70	0.65	0.25	0.25	0.1	0.56	4°
	min		0.10	1.25		0.36	0.19	6.1	3.8		5.80		0.40	0.60				0.30	0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot1437-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1437-1						~~15-02-09~~ 15-03-06

Figure 7. Package outline SOT108-1 (SO10)

15 Appendix: Internal parameters setting per type

In this section, the internal parameter settings per type are given.

15.1 TEA19031AET

Table 9 gives an overview of the function settings in the TEA19031AET.

Table 9. Internal parameter settings

Function	TEA19031AET
power rating	45 W
default output voltage	5 V
default maximum output current	3 A
NTC function[1]	NTC
OVP level	120 %
NTC-OVP protection level[1]	-
external sense resistor	10 mΩ
external resistor divider VCC/VSNS	8.325
cable compensation	67 mV/A
PDO1	
voltage	5 V
current	3 A
PDO2	
voltage	9 V
current	3 A
PDO3	
voltage	12 V
current	3 A
PDO4	
voltage	15 V
current	3 A
PDO5	
voltage	20 V
current	2.26 A
PDO6	
voltage	off
current	off