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UM10972

TEA1916DB1262 digital resonant 240 W/12 V power supply demo board

Rev. 1.1 — 8 June 2018

User manual

COMPANY PUBLIC

Document information

Information	Content
Keywords	TEA1916DB1262, TEA19161T, TEA19162T TEA1995T 240 W, LLC, resonant, half-bridge, PFC, controller, converter, burst mode, power supply, demo board, high efficiency, 80+ certification
Abstract	The TEA19161T is a digital LLC controller. It is used in combination with the PFC controller TEA19162T.Combining these two ICs with the SR controller TEA1995T at the secondary side results in a high-efficient resonant converter over the whole output power range. This document describes such a resonant power supply design with a 240 W (12 V/20 A) typical output power. It operates in normal mode for high and medium power levels, in low-power mode at medium and low power levels, and in burst mode at (very) low power levels. Low-power mode and burst mode operation provide a reduction of power losses, resulting in a higher efficiency at lower output power levels. Power levels for switching over from one mode to another mode can be selected by adjusting component values. The efficiency at high power levels is well above 90 %. No-load power consumption is well below 100 mW. At 250 mW output power, the input power is well below the 500 mW (complies easily with EUP lot6).

Table 1. Revision history

Rev	Date	Description
v.1.1	20180608	second, updated issue
Modifications:	• Section 7 "Bill of Materials" has been updated. • Section 9.2 "PFC coil" has been updated.	
v.1	20171201	first issue

1 Introduction

Warning		
		The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This user manual describes the TEA1916DB1262 240 W power supply board using the TEA19161T, TEA19162T, and TEA1995T. The user manual contains a functional description and a set of preliminary measurements to show the main characteristics.

1.1 TEA19161T and TEA19162T

The TEA19161T is a Half-Bridge Converter (HBC). The TEA19162T is a controller for Power Factor Correction (PFC). Both ICs provide drive functionality for the related discrete MOSFETs.

The resonant controller part (TEA19161T) is a high-voltage controller for a zero voltage switching LLC resonant converter. The resonant controller includes:

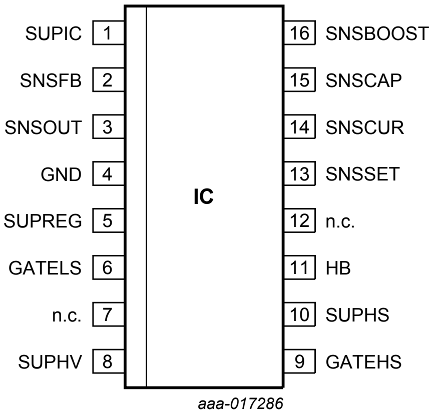
- A high-voltage shift circuit
- A high-voltage internal start-up switch
- Several protection features, like OverCurrent Protection (OCP), Open-Loop Protection (OLP), Capacitive Mode Protection (CMP), and a general purpose latched protection input

The TEA19162T is a PFC controller. To ensure efficient operation of the PFC, the TEA19162T incorporates quasi-resonant operation at high power levels and quasi-resonant operation with valley skipping at lower power levels. OCP, OverVoltage Protection (OVP), and demagnetization sensing ensure safe operation under all conditions. To improve the overall performance significantly, the TEA19161T and TEA19162T work together.

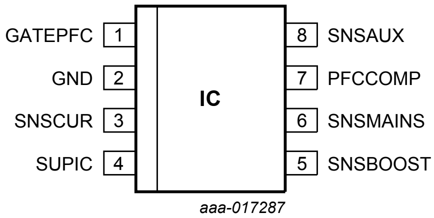
With the TEA1995T as a synchronized rectifier controller at the secondary side, MOSFETs can be used instead of rectifying diodes, improving the overall efficiency of the complete system even more.

The combination of PFC, resonant controller, and SR controller makes these devices suitable for all kinds of applications. Especially for application requiring high efficiency over the whole power range from no load to maximum output load.

1.1.1 Pinning



a. TEA19161T



b. TEA19162T

Figure 1. Pinning diagrams

1.2 TEA1995T

The TEA1995T is the first product of a new generation of Synchronous Rectifier (SR) controller ICs for switched-mode power supplies. It incorporates an adaptive gate drive method for maximum efficiency at any load.

The TEA1995T is a dedicated controller IC for synchronous rectification on the secondary side of resonant converters. It includes two driver stages for driving the SR MOSFETs, which rectify the outputs of the central tap secondary transformer windings. The two-gate driver stages have their own sensing inputs and operate independently.

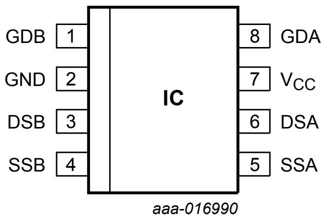
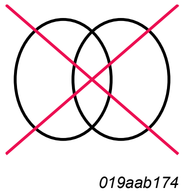


Figure 2. TEA1995T pinning diagram

2 Safety warning

The board must be connected to mains voltage. Avoid touching the demo board while it is connected to the mains voltage. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation of the mains phase using a variable transformer is always recommended. Figure 3 shows the symbols that identify the isolated and non-isolated devices.

a. Isolated



b. Not isolated

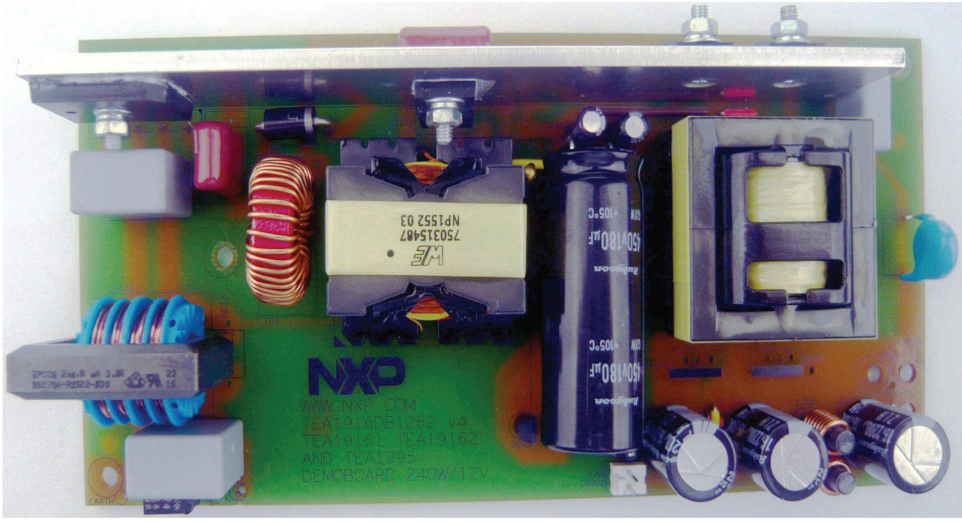
Figure 3. Isolation symbols

3 Specifications

Table 2. Specifications

Symbol	Description	Value	Conditions
Input			
V_i	input voltage	90 V (RMS) to 264 V (RMS)	AC
f_i	input frequency	47 Hz to 63 Hz	
$P_{i(noload)}$	no-load input power	< 100 mW	at 230 V/50 Hz
$P_{i(load=250mW)}$	standby power consumption	< 450 mW	at 230 V/50 Hz
Output			
V_o	output voltage	12 V	
I_o	output current	0 A to 20 A	continuous
$I_{o(max)}$	maximum output current	25 A	with OPP
$I_{o(peak)max}$	maximum peak output current	30 A	t < 50 ms
t_{hold}	hold time	> 10 ms	at 115 V/60 Hz; full load
t_{start}	start time	≤ 0.5 s	at 115 V/60 Hz
η	efficiency	≥ 89 %	average according to CoC

4 Board photographs



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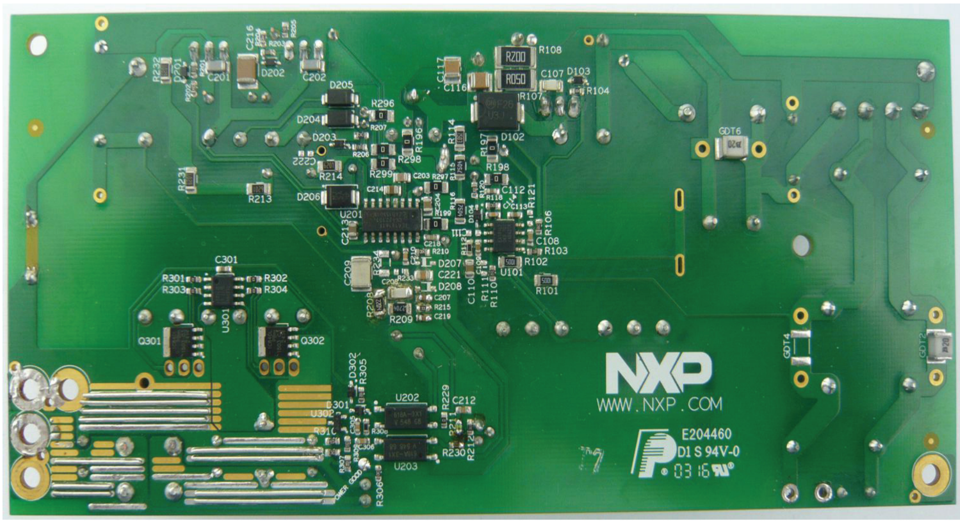
a. Top view



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b. Bottom view

Figure 4. TEA1916DB1262 prototype 240 W demo board

The board can operate at a mains input voltage between 90 V (RMS) and 264 V (RMS; universal mains).

The TEA1916DB1262demo board contains two subcircuits:

- A BCM-type PFC converter
- A resonant LLC-type HBC converter

To achieve an optimized resonant power board, the converters are working together.

The purpose of the TEA1916DB1262 prototype demo board is to evaluate the operation of the combination of converters (TEA19161T, TEA19162T, and TEA1995T) in a single output supply, which includes all modes. The performance passes general standards, including the EuP lot6 requirements. It can be used as a starting point for further development.

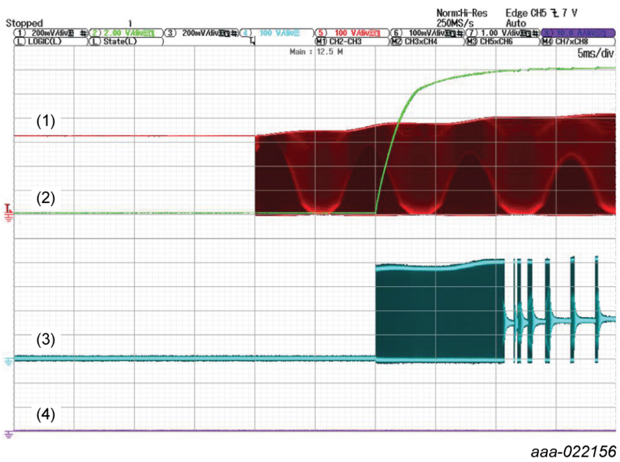
5 Performance measurements

5.1 Test facilities

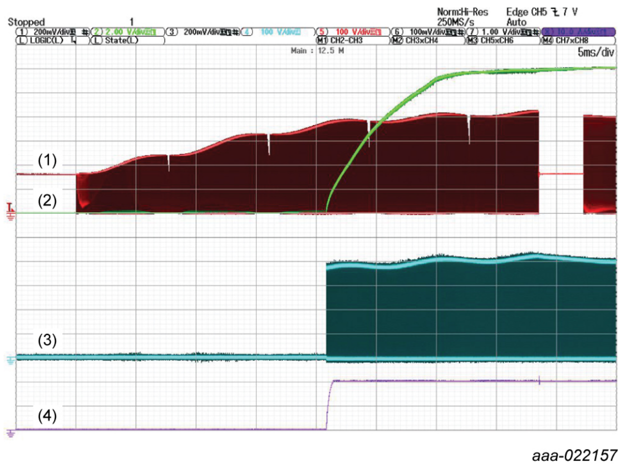
- Oscilloscope: Yokogawa DL9140L
- AC Power Source: Agilent 6812B
- Electronic load: Agilent 6063B
- Digital power meter: Yokogawa WT210

5.2 Start-up behavior

The rise time of the output voltage (measured from 10 % to 90 % point of the nominal output) is between 6 ms and 10 ms. The rise time depends on the output current load.



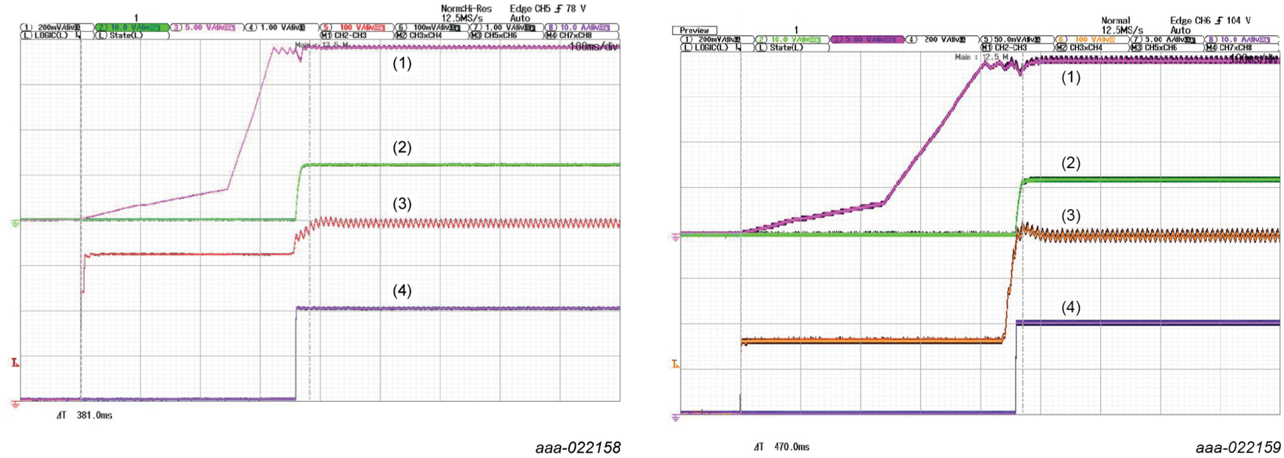
a. Start-up at 230 V mains and no load (0 A)



b. Start-up at 115 V mains and nominal load (20 A)

(1) PFC
(2) HBC
(3) V_{out}
(4) I_{out}

Figure 5. Start-up behavior



a. Start-up time = 381 ms at V_{mains} = 230 V (RMS) mains (I_{out} = 20 A)

b. Start-up time = 495 ms at V_{mains} = 115 V (RMS) mains (I_{out} = 20 A)

(1) V_{SUPIC}
(2) V_{out}
(3) V_{bulk}
(4) I_{out}

Figure 6. Start-up time at different mains voltages

Table 3. Start-up time

Condition	Start-up time (ms)
115 V/60 Hz	470
230 V/50 Hz	380
requirement	< 500

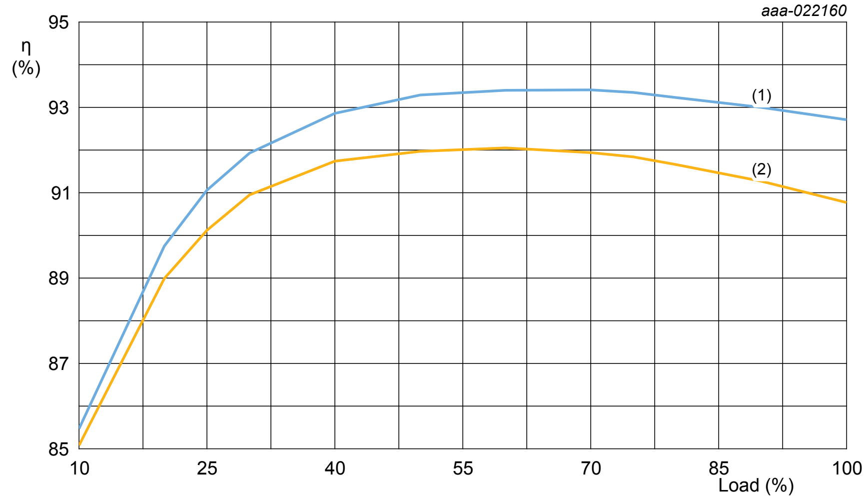
5.3 Efficiency

5.3.1 Efficiency characteristics

To determine the efficiency, the output voltage (not taking into account the losses in an output connection cable) on the TEA1916DB1262 demo board was measured.

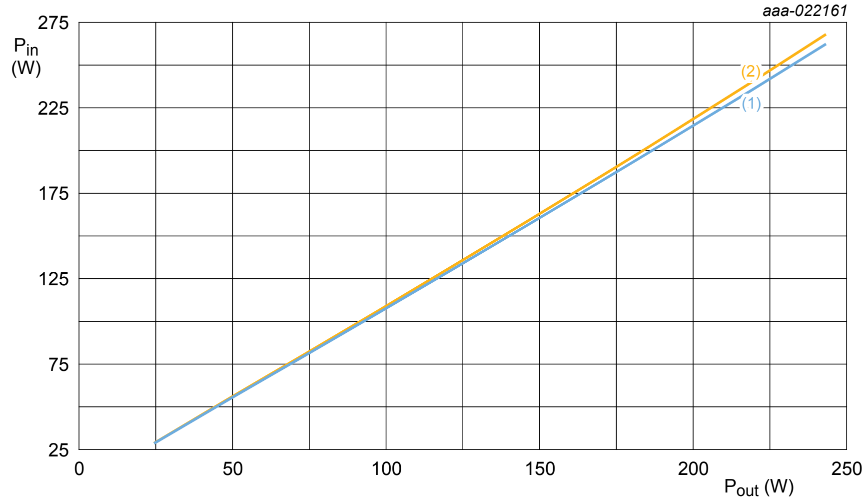
Table 4. Efficiency results

Condition	CoC efficiency average requirement (%)	Average	25 % load	50 % load	75 % load	100 % load
115 V/60 Hz	> 89	91.17	90.12	91.97	91.84	90.77
230 V/50 Hz	> 89	92.6	91.06	93.29	93.2	92.71



1. V_{mains} = 230 V (RMS)
2. V_{mains} = 115 V (RMS)

Figure 7. Efficiency curve



1. V_{mains} = 230 V (RMS)
2. V_{mains} = 115 V (RMS)

Figure 8. Power consumption

5.3.2 No-load power consumption

Power consumption performance of the total application board at no load was measured with a Yokogawa WT210 digital power meter. To measure the power consumption over a long time, the integration time function was used.

Table 5. Output voltage and power consumption at no load

Condition	ENERGY STAR 2.0 requirement	Output voltage	Power consumption
115 V/60 Hz	≤ 500 mW	12.2 V	46 mW
230 V/50 Hz	≤ 500 mW	12.2 V	51 mW

5.3.3 Standby load power consumption

Power consumption performance of the total application board at standby load was measured with a Yokogawa WT210 digital power meter. To measure the power consumption over a long time, the integration time function was used.

Table 6. Output voltage and power consumption at no load

Condition	ENERGY STAR 2.0 requirement	Output voltage	Power consumption
115 V/60 Hz	250 mW	12.2 V	356 mW
230 V/50 Hz	250 mW	12.2 V	357 mW
Requirement			< 500 mW

5.3.4 Power factor correction

Table 7. Output voltage and power consumption at no load

Condition	ENERGY STAR 2.0 requirement	Output power	Power factor
115 V/60 Hz	≥ 0.9 mW	240 W	0.992
115 V/60 Hz	-	120 W	0.976
230 V/50 Hz	-	240 W	0.945
230 V/50 Hz	-	120 W	0.911

5.4 Low-power mode and burst mode operation

To reach a high efficiency at medium/low and standby output power, the low-power mode and burst mode are introduced.

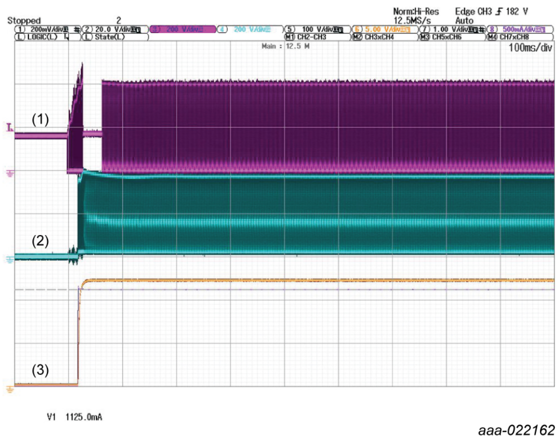
In low-power mode, the behavior of the half-bridge converter is changed compared to the standard behavior at maximum output power. The result is a higher efficiency that is close to the expected efficiency at maximum load.

The power level for leaving the high-power mode and entering the low-power mode can be adjusted. Here the power level is set at 53.4 W.

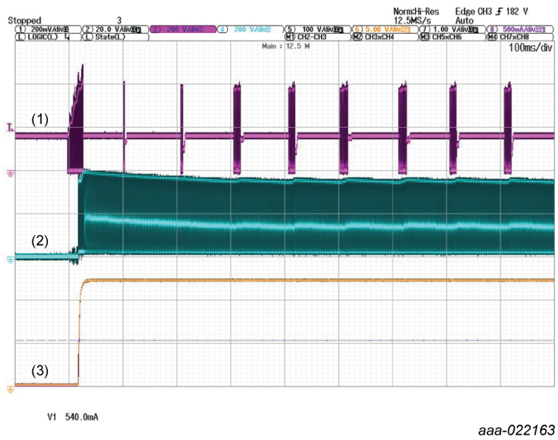
Below 21.3 W, the HBC converter enters burst mode, which improves the overall efficiency at lower output loads.

Finally, when the output power level is further reduced, the PFC converter enters burst mode.

The power supply consumes more power without low-power mode and burst mode.



a. PFC continues switching until regulation level is reached, swaps after that to normal mode when P_{out} is low. The measurement example shows the result at Pout = 13.8 W.



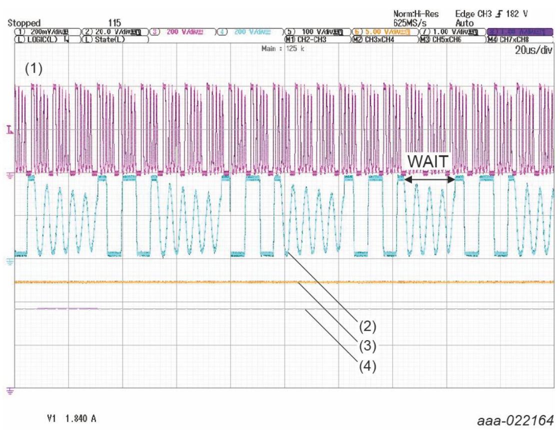
b. FC continues switching until regulation level is reached, then swaps to burst mode when P_{out} is very low. The measurement example shows the result at P_{out} = 6.6 W.

(1) PFC

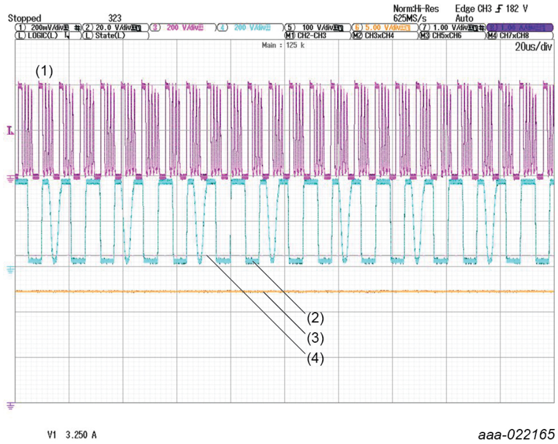
(2) HBC

(3) V_{out}

Figure 9. HBC burst mode operation after initial start-up



a. The “wait” time increases at lower output power when the HBC operates in low-power mode. The measurement example shows the result at P_{out} = 22.5 W.



b. The “wait” time decreases at higher output power when the HBC operates in low-power mode. The measurement example shows the result at P_{out} = 39.7 W.

(1) PFC

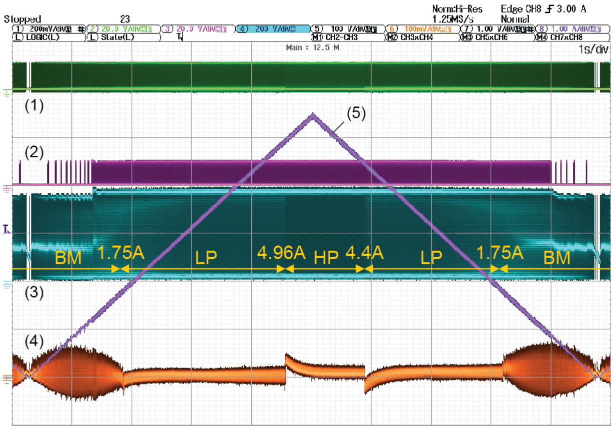
(2) HBC

(3) V_{out}

(4) I_{out}

Figure 10. HBC low-power mode operation

5.5 Operation mode transitions



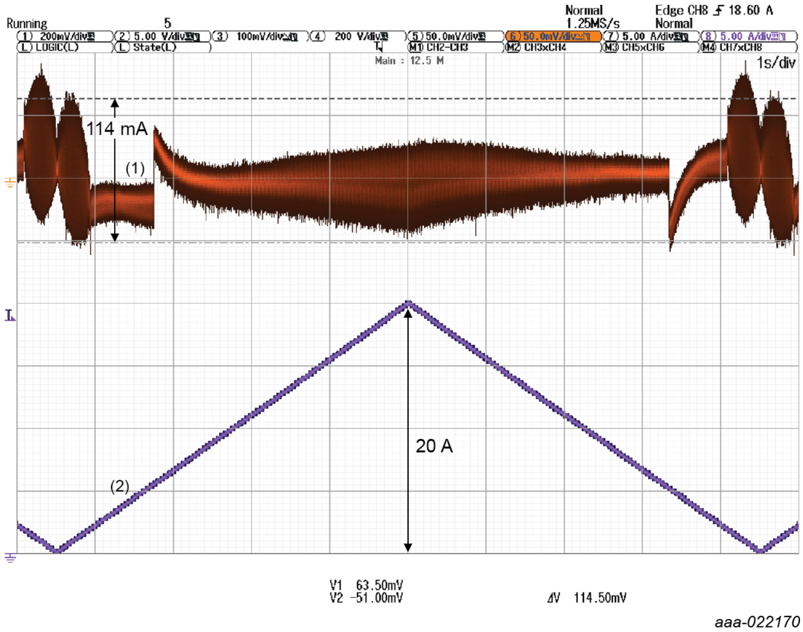
(1) GATELS
(2) GATEPFC
(3) HBC
(4) $V_{out(ripple)}$
(5) I_{out}

Figure 11. Transitions HP - LP - BM

Table 8. Mode transitions

Transition	Power level
HP - LP	53.4 W
LP - BM	21.3 W
BM - LP	21.3 W
LP - HP	60.2 W

5.6 Output voltage ripple



(1) V_{out} (AC)

(2) I_{out}

Figure 12. Maximum output voltage ripple in burst mode at 50 % duty cycle

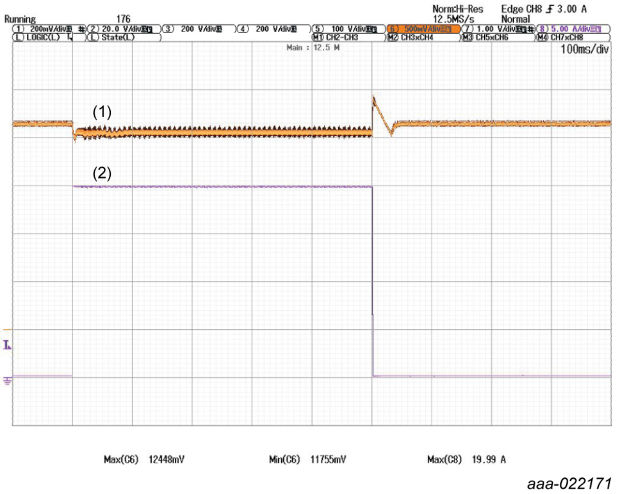
The maximum output voltage ripple is 114 mV (peak-to-peak).

5.7 Dynamic load response

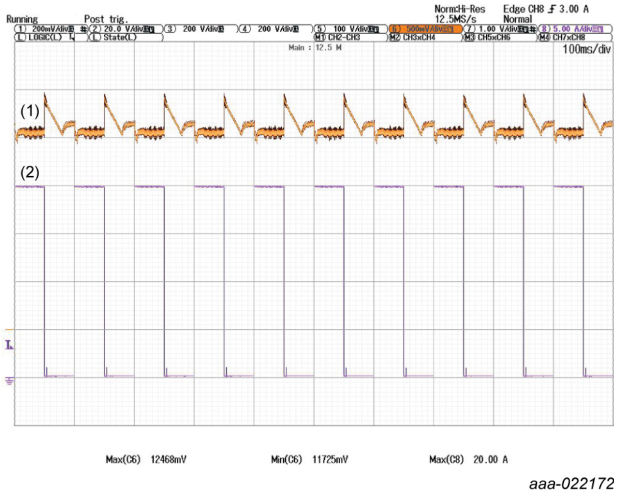
The dynamic load response test shows the result of constant load steps across the output. Output current of the converter is changed in steps of between 0 A and 20 A at a repetition frequency of 1 Hz, 10 Hz, 100 Hz, and 1000 Hz.

Table 9. Minimum and maximum output voltage at minimum-maximum load steps

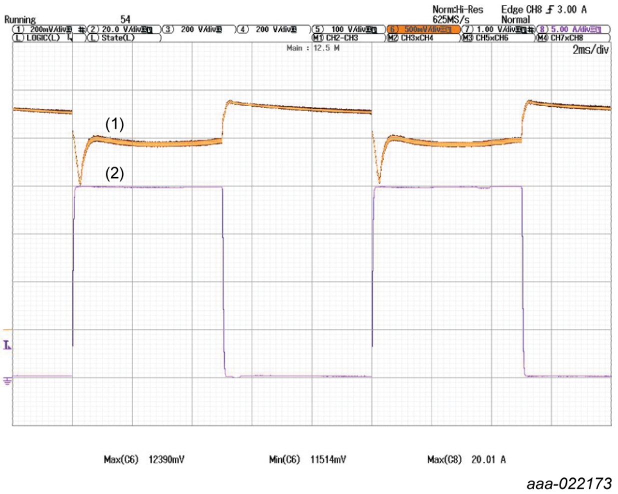
Condition	Load	Minimum to maximum output voltage
115 V/60 Hz	I_o: 0 % to 100 %	11.48 V to 12.47 V
230 V/50 Hz	I_o: 0 % to 100 %	11.48 V to 12.47 V



a. Basic sequential load step test is done at 1 Hz



b. Basic sequential load step test is done at 10 Hz



c. Basic sequential load step test is done at 100 Hz

d. Basic sequential load step test is done at 1 kHz

(1) V_{out}

(2) I_{out}

Figure 13. Output voltage during dynamic load test

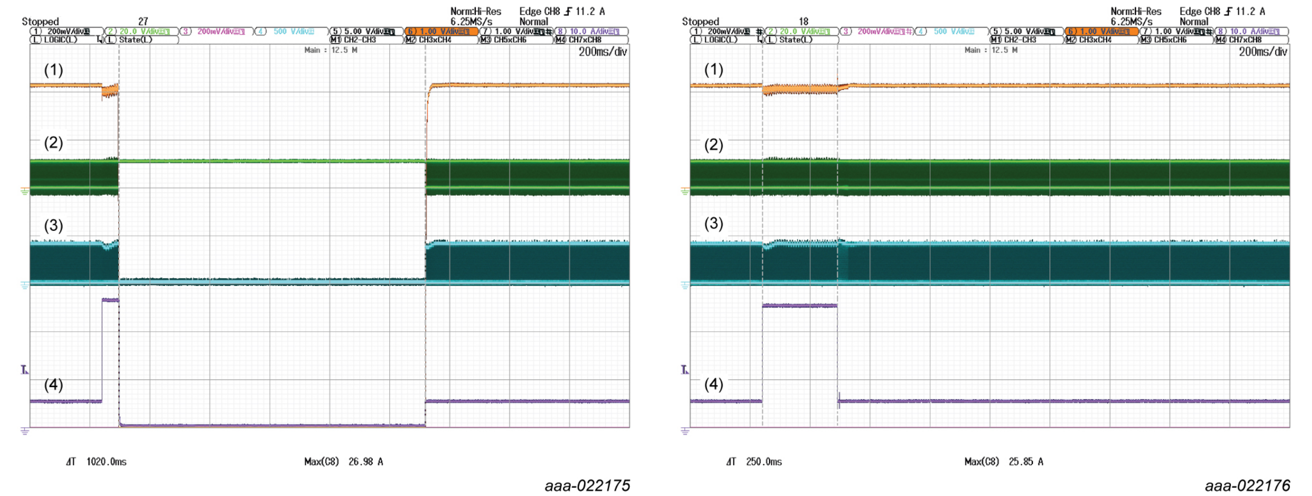
5.8 OverPower Protection (OPP)

Tested with a higher current (dynamic overload) on the output voltage, OPP is activated when the current exceeds 25 A (300 W). This current corresponds with a load condition that is 25 % higher than the rated power for continuous use.

OPP allows a typical continuously maximum output current of 25 A during 50 ms. Any higher current, intended to run longer than 50 ms, triggers an OPP. After the 50 ms, a safe restart follows (OPP protection is reset).

The SNSCAP function of the TEA19161 detects OPP. This function monitors the voltage across the series capacitor (C211) of the half bridge.

The power capability limitation protection limits the maximum power to 360 W as long as the time is shorter than 50 ms.



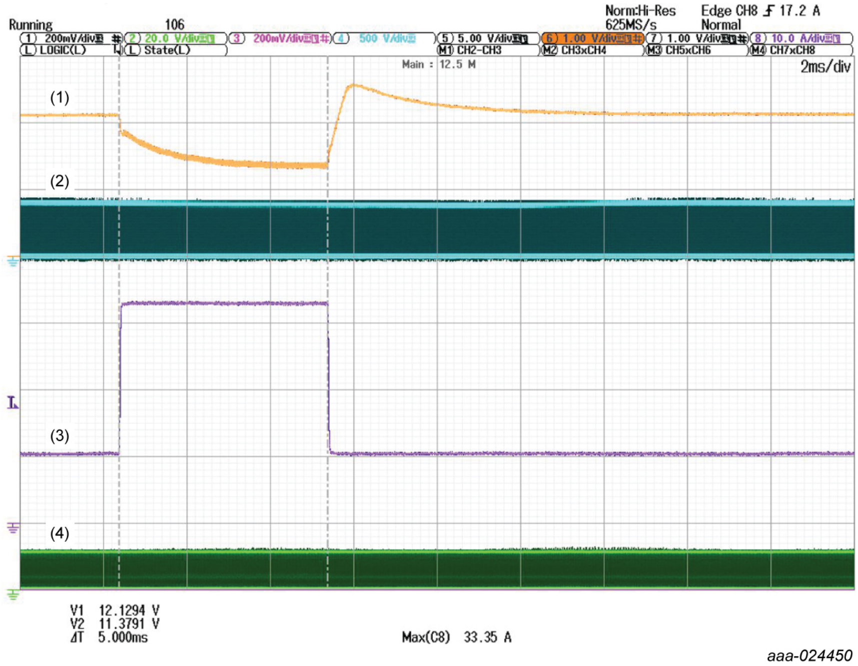
a. OPP protection is triggered at I_{out} ≈ 27 A (output power is lost during a safe restart)

b. OPP is not triggered at I_{out} ≈ 26 A

(1) V_{out}
(2) GATELS
(3) HBC
(4) I_{out}

Figure 14. Overpower protection

The power capability limitation level limits the maximum output power to typically 360 W as long as the time fits within the selected OPP timer. In this example, the time is shorter than 50 ms. So, when more output current is requested than accepted by the power capability limitation level, the output voltage drops.



(1) V_{out}

(2) HBC

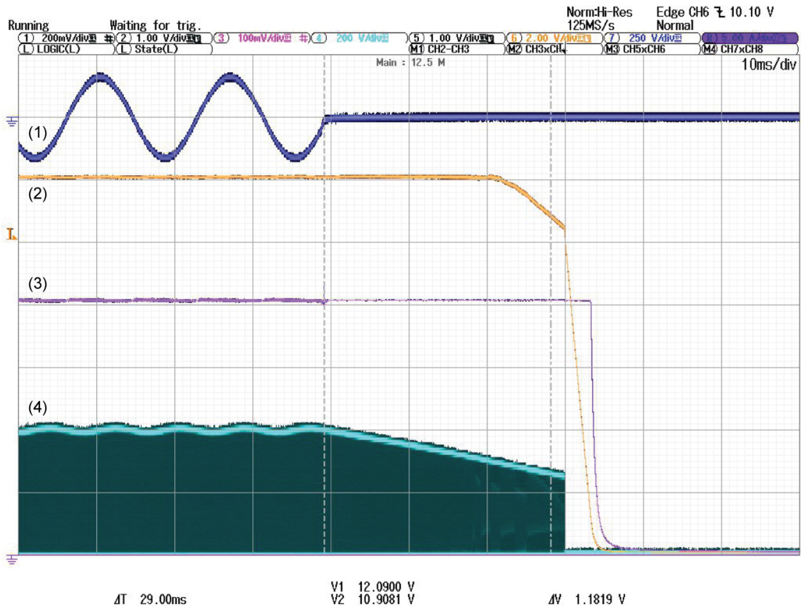
(3) I_{out}

(4) GATELS

Figure 15. Power capability level

5.9 Hold time

The output was set to full load and the mains supply voltage of 115 V disconnected. The time that passes before the output voltage falls below 90 % of its initial value was measured. The hold time is 29 ms.



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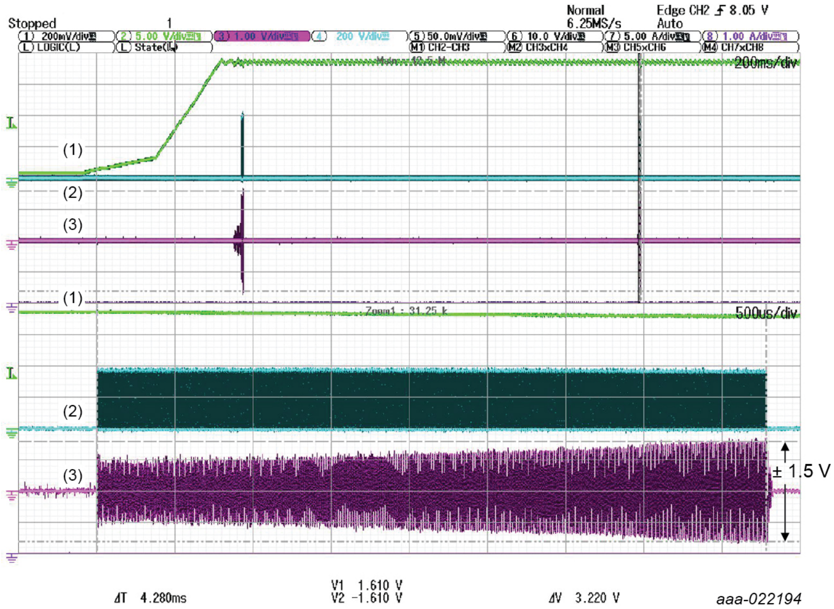
(1) V_{line}
(2) V_{out}
(3) I_{out}
(4) HBC

Figure 16. Hold time at V_{MAINS} = 115 V and nominal load

5.10 Short-Circuit Protection (SCP)

The output was shorted before the resonant converter was connected to the mains. A short circuit across the output of the resonant converter increases primary current. The SNSCUR pin detects the increase. When this voltage exceeds ±1.5 V, the safe-restart protection is triggered. Approximately 4 ms after the HBC is started, the protection level is reached. Removing the short across the output resets the protection.



(1) SUPIC
(2) HBC
(3) SNSCUR

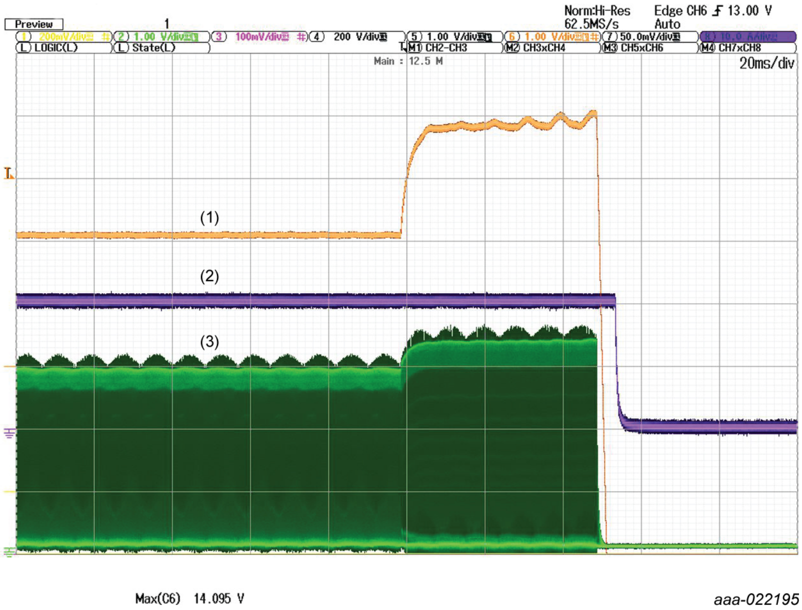
Figure 17. Safe-restart protection during shorted output

Table 10 shows the input power when the output is shorted.

Table 10. Input power when output power is shorted

Condition	P_{in} (W)
115 V; 60 Hz	1.75
230 V; 50 Hz	1.70

5.11 OverVoltage Protection (OVP)



(1) V_{out}
(2) I_{out}
(3) SNSOUT

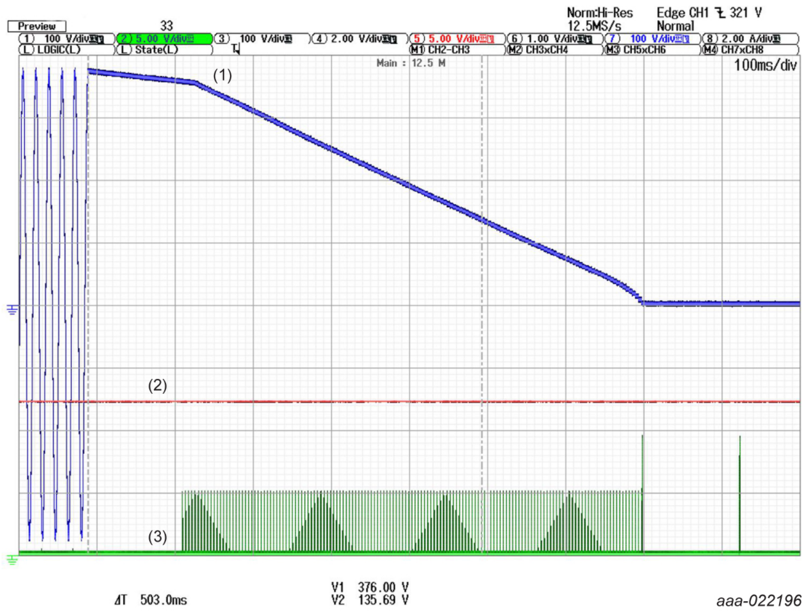
Figure 18. Overvoltage protection at V_{out} = 14.1 V (SNSOUT triggers latched protection)

5.12 X-capacitor discharge time

The power line was unplugged at no-load. The discharge time was measured at the X-capacitor (470 nF + 470 nF).

Table 11. X-capacitor discharge time test results

Condition	From 264 * √2 to 135 V
X-capacitor discharge time	505 ms



(1) V_{xcap}
(2) V_{out}
(3) GATEPFC

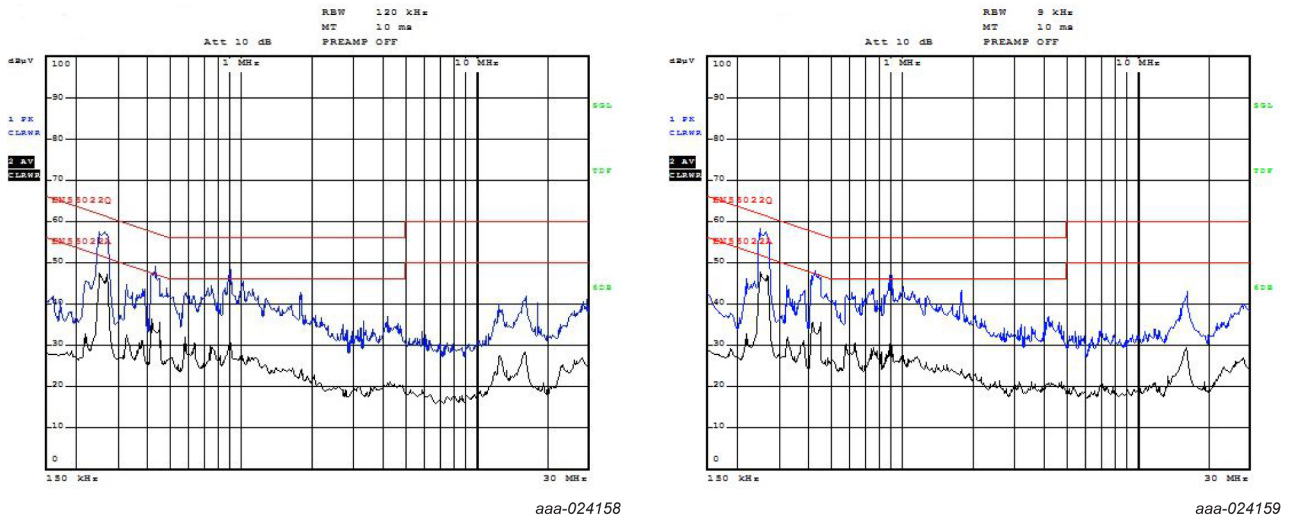
Figure 19. X-capacitor discharge at 264 V (RMS)/50 Hz and no load

5.13 ElectroMagnetic Compatibility (EMC)

The conducted ElectroMagnetic Interference (EMI) of the TEA1916DB1262 prototype demo board was measured under the following conditions:

- Load resistor: 0.6 Ω; V_{out} = 12.1 V; I_{out} =20.1 A
- V_{line} = 230 V/50 Hz or 120 V/50 Hz

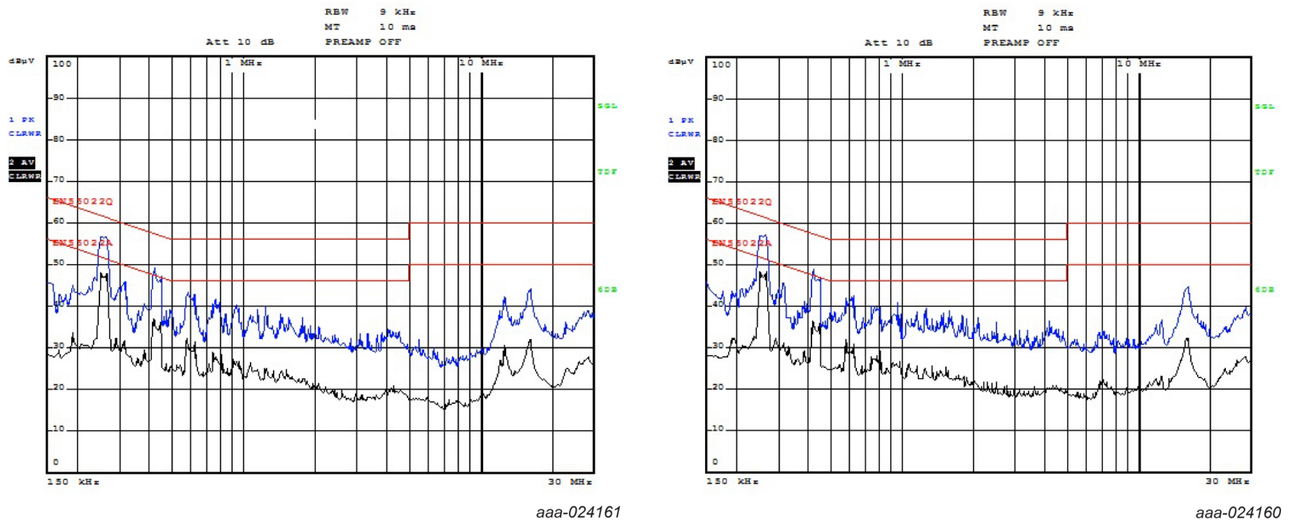
The conducted EMI was measured both in the Line and Neutral. The product complies with the EMC standard.



a. Line

b. Neutral

Figure 20. Conducted EMI at V_{line} = 230 V_{RMS}



a. Line

b. Neutral

Figure 21. Conducted EMI at V_{line} = 120 V_{RMS}

6 Schematic

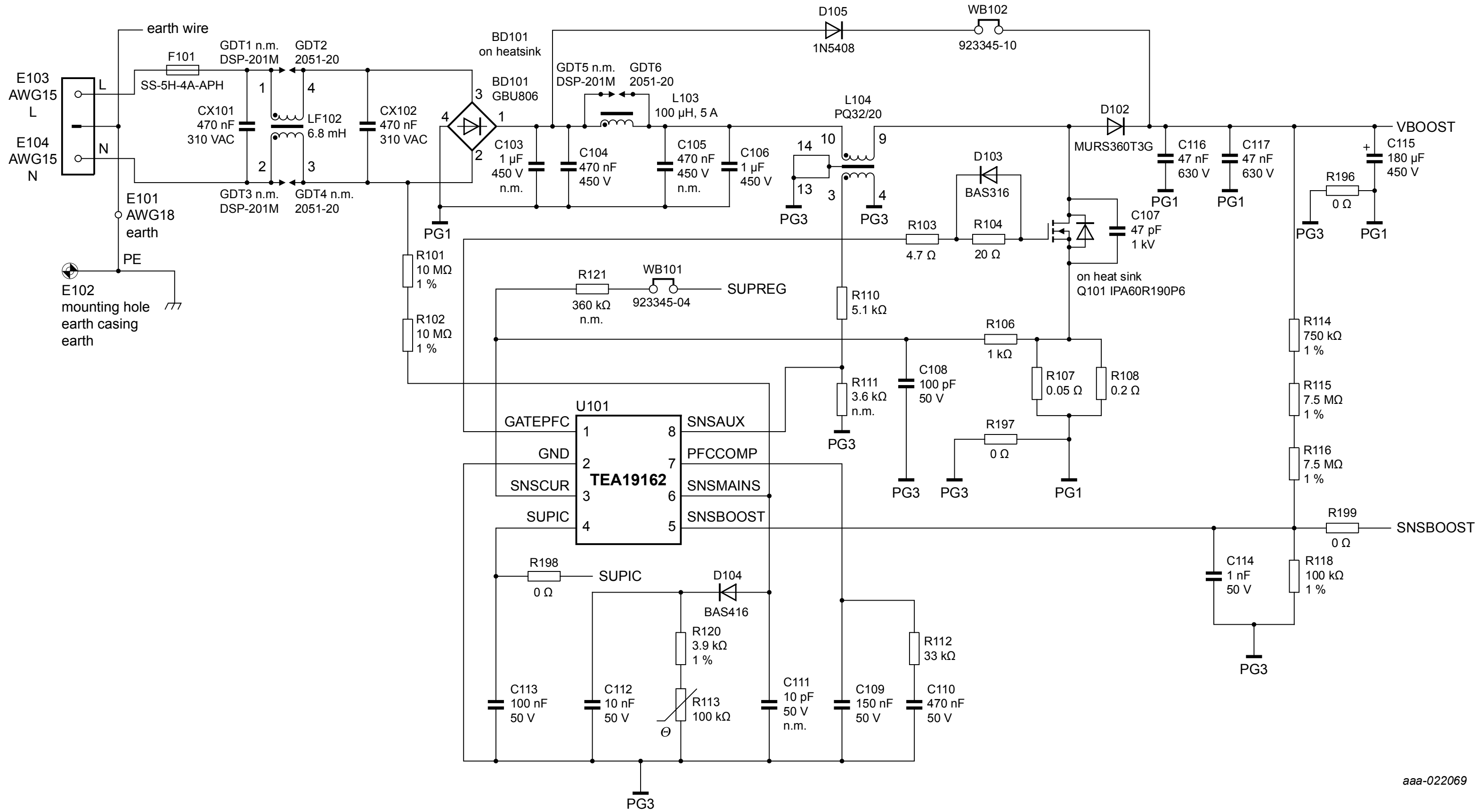


Figure 22. Schematic TEA1916DB1262 240 W prototype demo board (PFC)

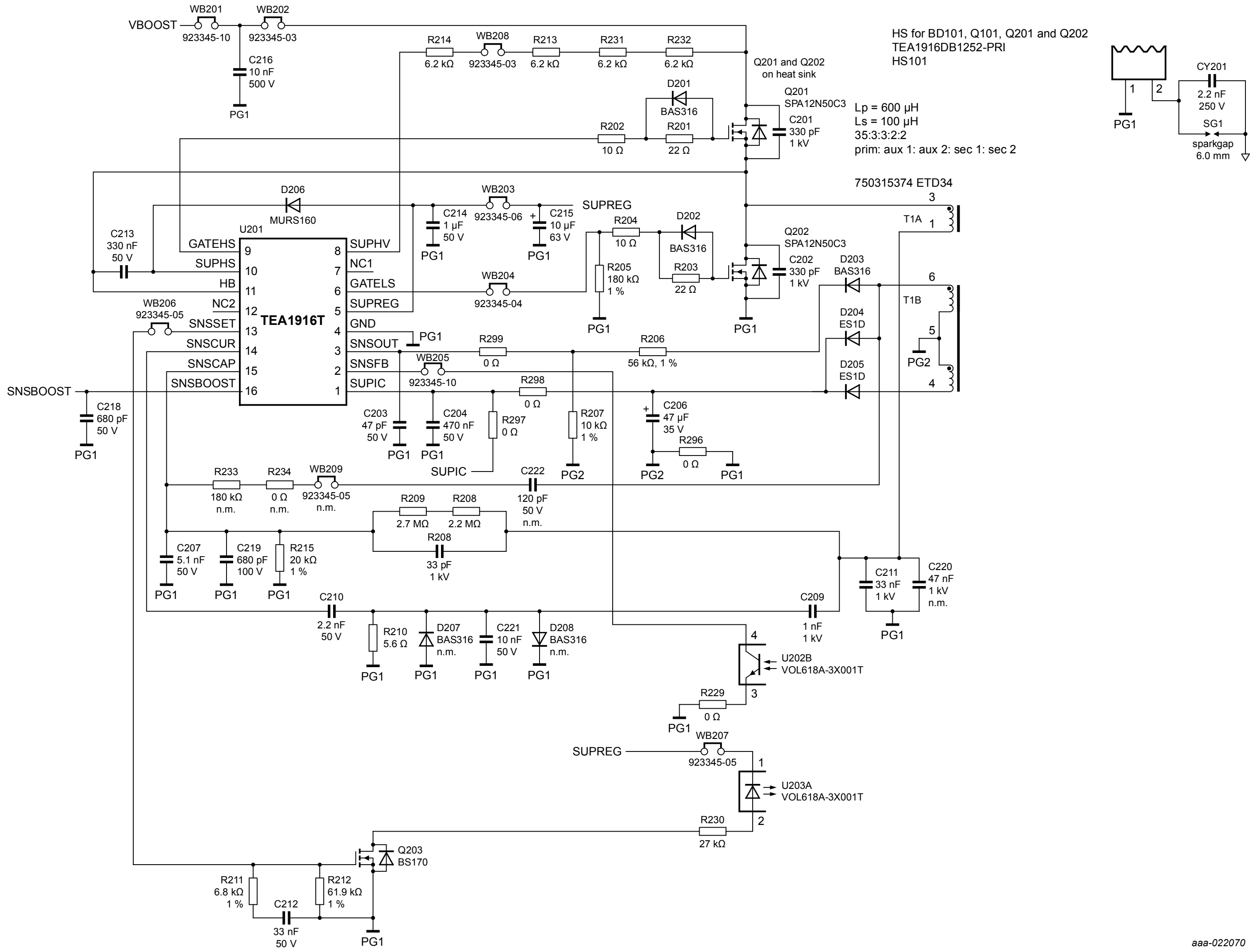


Figure 23. Schematic TEA1916DB1262 240 W prototype demo board (LLC)

