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ST-NXP Wireless

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As a result, the following changes are applicable to the attached document.

- **Company name - NXP B.V.** is replaced with **ST-NXP Wireless**.

- **Copyright** - the copyright notice at the bottom of each page "© NXP B.V. 200x. All rights reserved", shall now read: "© ST-NXP Wireless 200x - All rights reserved".

- **Web site** - http://www.nxp.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to salesaddresses@nxp.com , is now found at http://www.stnwireless.com under Contacts.

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ST-NXP Wireless

TEA5767HN

Low-power FM stereo radio for handheld applications

Rev. 05 — 26 January 2007 Product data sheet

1. General description

The TEA5767HN is a single-chip electronically tuned FM stereo radio for low-voltage applications with fully integrated Intermediate Frequency (IF) selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small and low cost external components. The radio can be tuned to the European, US, and Japanese FM bands.

2. Features

- High sensitivity due to integrated low-noise RF input amplifier
- FM mixer for conversion to IF of the US/Europe (87.5 MHz to 108 MHz) and Japanese (76 MHz to 91 MHz) FM band
- Preset tuning to receive Japanese TV audio up to 108 MHz
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- FM IF selectivity performed internally
- No external discriminator needed due to fully integrated FM demodulator
- Crystal reference frequency oscillator; the oscillator operates with a 32.768 kHz clock crystal or with a 13 MHz crystal and with an externally applied 6.5 MHz reference frequency
- Phase-locked loop (PLL) synthesizer tuning system
- I^2C-bus and 3-wire bus, selectable via pin BUSMODE
- 7-bit IF counter output via the bus
- 4-bit level information output via the bus
- Soft mute
- Signal dependent mono to stereo blend [Stereo Noise Cancelling (SNC)]
- Signal dependent High Cut Control (HCC)
- Soft mute, SNC and HCC can be switched off via the bus
- Adjustment-free stereo decoder
- Autonomous search tuning function
- Standby mode
- Two software programmable ports
- Bus enable line to switch the bus input and output lines into 3-state mode

3. Quick reference data

Table 1. Quick reference data

V_{CCA} = V_{CCD} = $V_{CC(VCO)}$ = 2.7 V; T_{amb} = 25 °C; AC values are given in RMS; for V_{RF} the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		[1]	2.5	3.0	5.0	V
$V_{CC(VCO)}$	Voltage-Controlled Oscillator (VCO) supply voltage		[1]	2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		[1]	2.5	3.0	5.0	V
I_{CCA}	analog supply current	operating; V_{CCA} = 3 V		6.0	8.4	10.5	mA
		Standby mode; V_{CCA} = 3 V		-	3	6	µA
$I_{CC(VCO)}$	VCO supply current	operating; $V_{CC(VCO)}$ = 3 V		560	750	940	µA
		Standby mode; $V_{CC(VCO)}$ = 3 V		-	1	2	µA
I_{CCD}	digital supply current	operating; V_{CCD} = 3 V		2.1	3.0	3.9	mA
		Standby mode; V_{CCD} = 3 V					
		bus enable line HIGH		30	56	80	µA
		bus enable line LOW		11	19	26	µA
$f_{FM(ant)}$	FM input frequency			76	-	108	MHz
T_{amb}	ambient temperature	V_{CCA} = $V_{CC(VCO)}$ = V_{CCD} = 2.5 V to 5 V		–10	-	+75	°C
FM overall system parameters; see Figure 13							
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 MHz to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 µs; L = R; B_{AF} = 300 Hz to 15 kHz		-	2	3.5	µV
S_{-200}	low side 200 kHz selectivity	Δf = –200 kHz; f_{tune} = 76 MHz to 108 MHz	[2]	32	36	-	dB
S_{+200}	high side 200 kHz selectivity	Δf = +200 kHz; f_{tune} = 76 MHz to 108 MHz	[2]	39	43	-	dB
V_{AFL}	left audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs		60	75	90	mV
V_{AFR}	right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs		60	75	90	mV

Table 1. Quick reference data *...continued*

V_{CCA} = V_{CCD} = $V_{CC(VCO)}$ = 2.7 V; T_{amb} = 25 °C; AC values are given in RMS; for V_{RF} the emf value is given; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	54	60	-	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9 % pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	-	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	-	0.4	1	%

[1] V_{CCA}, $V_{CC(VCO)}$ and V_{CCD} must not differ by more than 200 mV.

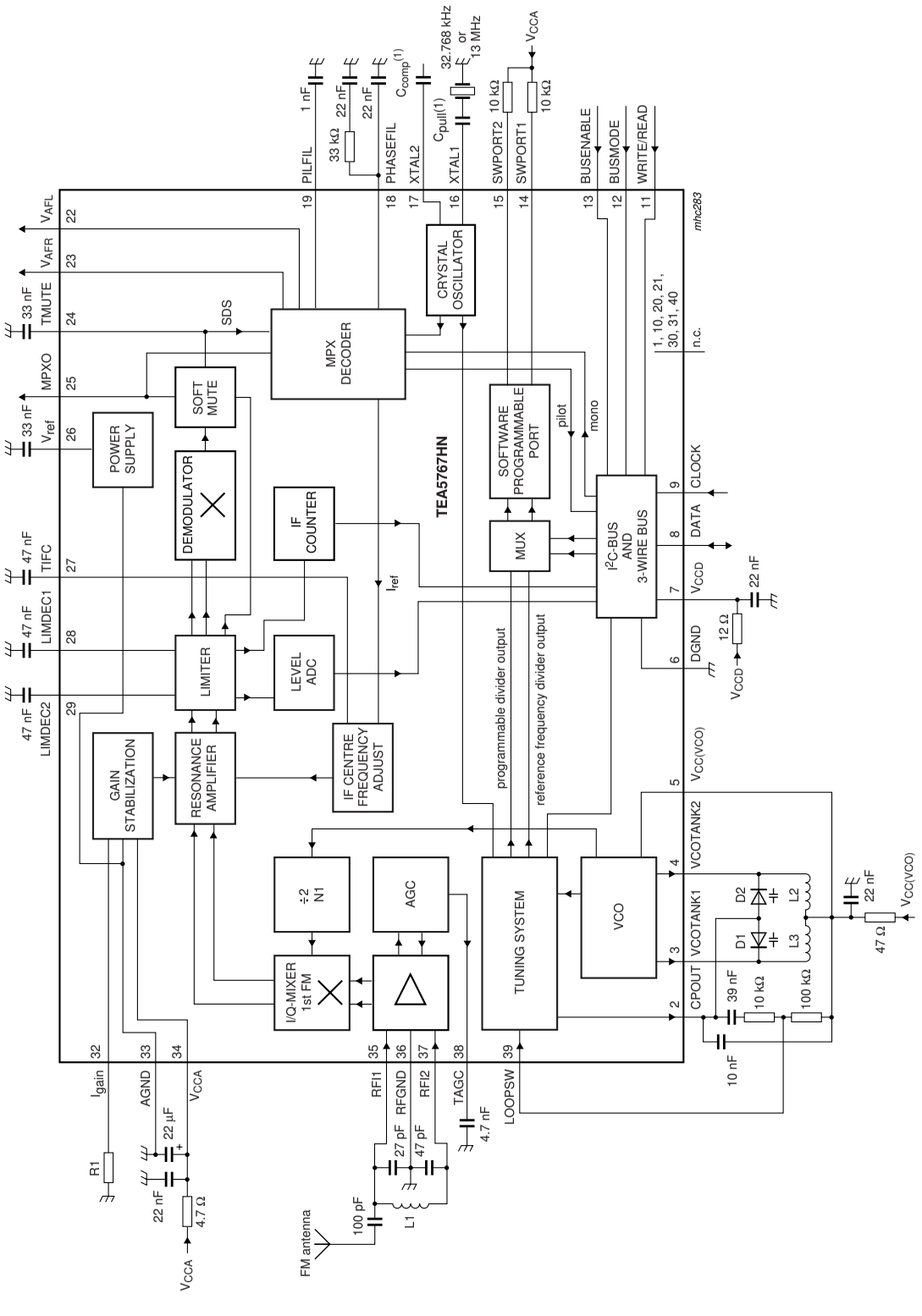
[2] Low side and high side selectivity can be switched by changing the mixer from high side to low side LO injection.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA5767HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

5. Block diagram



The component list is given in Section 16.

(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

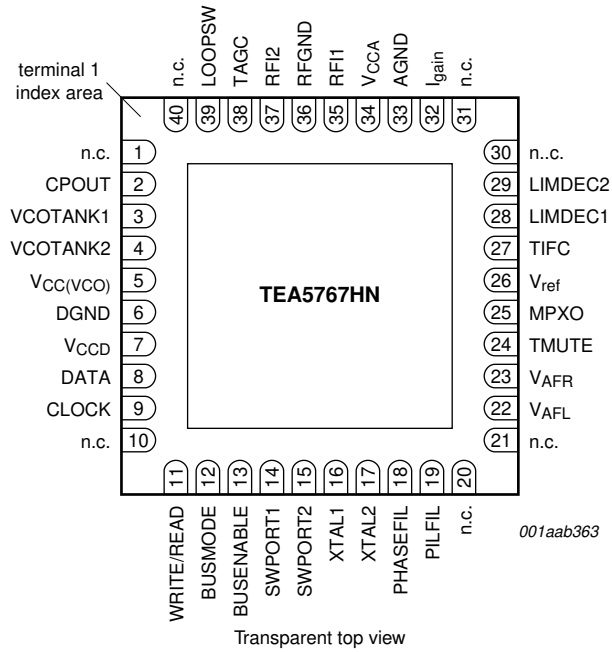


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
CPOUT	2	charge pump output of synthesizer PLL
VCOTANK1	3	VCO tuned circuit output 1
VCOTANK2	4	VCO tuned circuit output 2
$V_{CC(VCO)}$	5	VCO supply voltage
DGND	6	digital ground
V_{CCD}	7	digital supply voltage
DATA	8	bus data line input/output
CLOCK	9	bus clock line input
n.c.	10	not connected
WRITE/READ	11	write/read control input for the 3-wire bus
BUSMODE	12	bus mode select input
BUSENABLE	13	bus enable input
SWPORT1	14	software programmable port 1
SWPORT2	15	software programmable port 2
XTAL1	16	crystal oscillator input 1

Table 3. Pin description *...continued*

Symbol	Pin	Description
XTAL2	17	crystal oscillator input 2
PHASEFIL	18	phase detector loop filter
PILFIL	19	pilot detector low-pass filter
n.c.	20	not connected
n.c.	21	not connected
V_{AFL}	22	left audio frequency output voltage
V_{AFR}	23	right audio frequency output voltage
TMUTE	24	time constant for soft mute
MPXO	25	FM demodulator MPX signal output
V_{ref}	26	reference voltage
TIFC	27	time constant for IF center adjust
LIMDEC1	28	decoupling IF limiter 1
LIMDEC2	29	decoupling IF limiter 2
n.c.	30	not connected
n.c.	31	not connected
I_{gain}	32	gain control current for IF filter
AGND	33	analog ground
V_{CCA}	34	analog supply voltage
RFI1	35	RF input 1
RFGND	36	RF ground
RFI2	37	RF input 2
TAGC	38	time constant RF AGC
LOOPSW	39	switch output of synthesizer PLL loop filter
n.c.	40	not connected

7. Functional description

7.1 Low-noise RF amplifier

The Low Noise Amplifier (LNA) input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

7.2 FM mixer

The FM quadrature mixer converts the FM RF (76 MHz to 108 MHz) to an IF of 225 kHz.

7.3 VCO

The varactor tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 MHz to 217 MHz.

7.4 Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or a 13 MHz crystal. The temperature drift of standard 32.768 kHz clock crystals limits the operational temperature range from −10 °C to +60 °C.

The PLL synthesizer can be clocked externally with a 32.768 kHz, a 6.5 MHz or a 13 MHz signal via pin XTAL2.

The crystal oscillator generates the reference frequency for:

- The reference frequency divider for the synthesizer PLL
- The timing for the IF counter
- The free-running frequency adjustment of the stereo decoder VCO
- The center frequency adjustment of the IF filters

7.5 PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz or a 13 MHz reference frequency generated by the crystal oscillator or applied to the IC from an external source. The synthesizer can also be clocked via pin XTAL2 at 6.5 MHz. The PLL tuning system can perform an autonomous search tuning function.

7.6 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

7.7 IF filter

Fully integrated IF filter.

7.8 FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

7.9 Level voltage generator and analog-to-digital converter

The FM IF analog level voltage is converted to 4 bits digital data and output via the bus.

7.10 IF counter

The IF counter outputs a 7-bit count result via the bus.

7.11 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels. The soft mute function can be switched off via the bus.

7.12 MPX decoder

The PLL stereo decoder is adjustment-free. The stereo decoder can be switched to mono via the bus.

7.13 Signal dependent mono to stereo blend

With a decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono to stereo blend can also be programmed via the bus to an RF level depending switched mono to stereo transition. Stereo Noise Cancelling (SNC) can be switched off via the bus.

7.14 Signal dependent AF response

The audio bandwidth will be reduced with a decreasing RF input level. This function can be switched off via the bus.

7.15 Software programmable ports

Two software programmable ports (open-collector) can be addressed via the bus.

The port 1 (pin SWPORT1) function can be changed with write data byte 4 bit 0 (see Table 13). Pin SWPORT1 is then output for the ready flag of read byte 1.

7.16 I²C-bus and 3-wire bus

The 3-wire bus and the I²C-bus operate with a maximum clock frequency of 400 kHz.

Before any READ or WRITE operation the pin BUSENABLE has to be HIGH for at least 10 µs.

The I²C-bus mode is selected when pin BUSMODE is LOW, when pin BUSMODE is HIGH the 3-wire bus mode is selected.

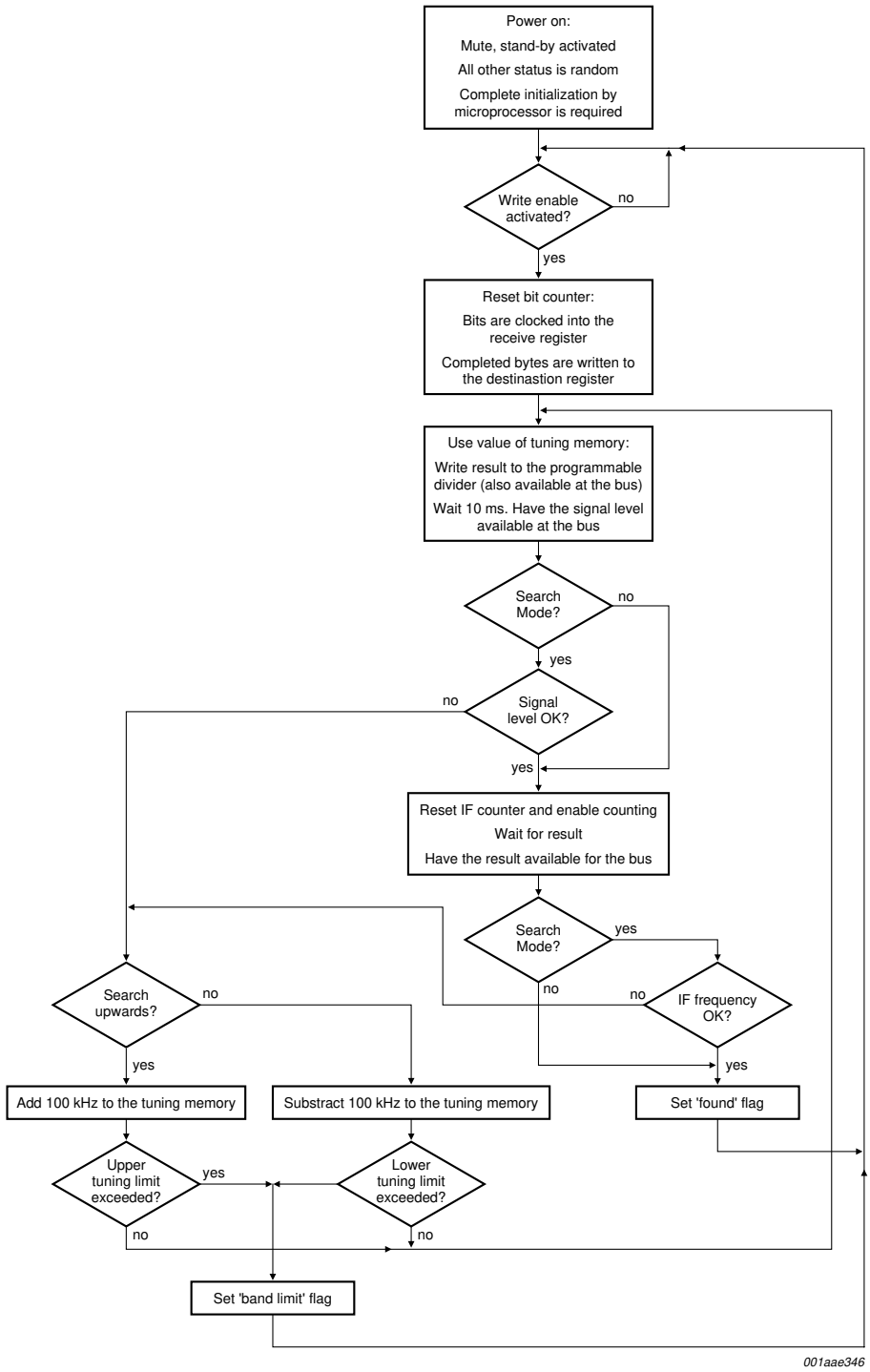


Fig 3. Flowchart auto search or preset

8. I²C-bus, 3-wire bus and bus-controlled functions

8.1 I²C-bus specification

Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it" (order number 9398 393 40011)*.

The standard I²C-bus specification is expanded by the following definitions:

IC address: 110 0000b

Structure of the I²C-bus logic: slave transceiver

Subaddresses are not used

The maximum LOW-level input and the minimum HIGH-level input are specified to $0.2V_{CCD}$ and $0.45V_{CCD}$ respectively.

The pin BUSMODE must be connected to ground to operate the IC with the I²C-bus.

Remark: The I²C-bus operates at a maximum clock frequency of 400 kHz. It is not allowed to connect the IC to an I²C-bus operating at a higher clock rate.

8.1.1 Data transfer

Data sequence: address, byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order). The Least Significant Bit (LSB) = 0 of the address indicates a WRITE operation to the TEA5767HN.

Bit 7 of each byte is considered as the Most Significant Bit (MSB) and has to be transferred as the first bit of the byte.

The data becomes valid bitwise at the appropriate falling edge of the clock. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started

The IC can be switched into a low current Standby mode with the standby bit; the bus is then still active. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the Standby mode being programmed, the IC maintains normal operation, but is isolated from the bus lines.

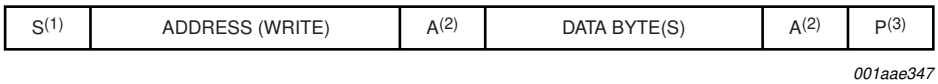
The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.1.2 Power-on reset

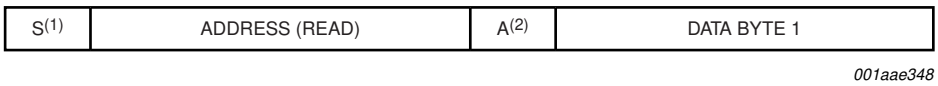
At Power-on reset the mute is set, all other bits are set to LOW. To initialize the IC all bytes have to be transferred.

8.2 I²C-bus protocol



(1) S = START condition.
(2) A = acknowledge.
(3) P = STOP condition.

Fig 4. Write mode



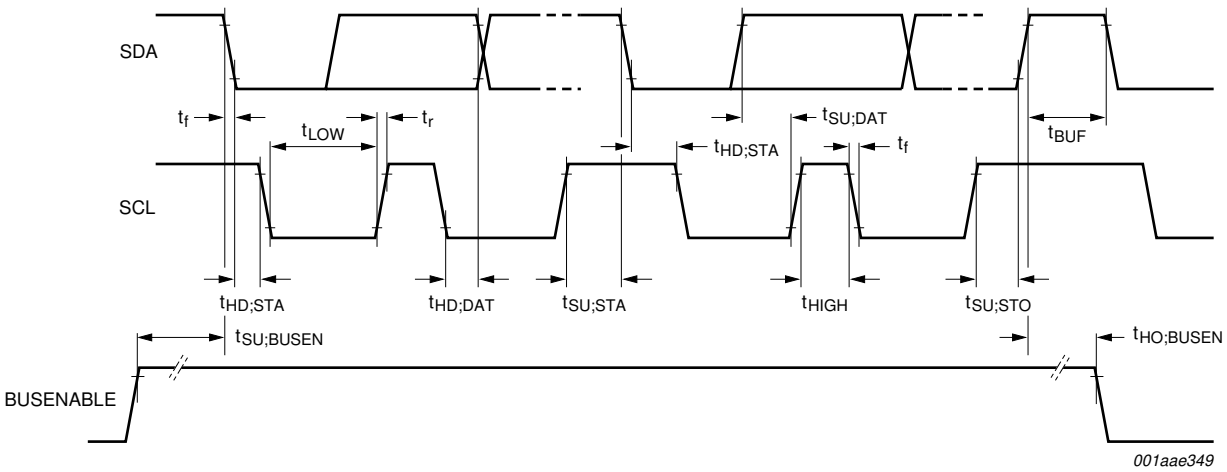
(1) S = START condition.
(2) A = acknowledge.

Fig 5. Read mode

Table 4. IC address byte

IC address							Mode
1	1	0	0	0	0	0	R/$\overline{W}$[1]

[1] Read or write mode:
a) 0 = write operation to the TEA5767HN.
b) 1 = read operation from the TEA5767HN.



t_f = fall time of both SDA and SCL signals: $20 + 0.1C_b < t_f < 300$ ns, where C_b = capacitive load on bus line in pF.

t_r = rise time of both SDA and SCL signals: $20 + 0.1C_b < t_f < 300$ ns, where C_b = capacitive load on bus line in pF.

$t_{HD;STA}$ = hold time (repeated) START condition. After this period, the first clock pulse is generated: > 600 ns.

t_{HIGH} = HIGH period of the SCL clock: > 600 ns.

t_{LOW} = LOW period of the SCL clock > 1300 ns.

$t_{SU;STA}$ = set-up time for a repeated START condition: > 600 ns.

$t_{HD;DAT}$ = data hold time: 300 ns < $t_{HD;DAT}$ < 900 ns.

Remark: 300 ns lower limit is added because the ASIC has no internal hold time for the SDA signal.

$t_{SU;DAT}$ = data set-up time: $t_{SU;DAT}$ > 100 ns. If ASIC is used in a standard mode I^2C-bus system, $t_{SU;DAT}$ > 250 ns.

$t_{SU;STO}$ = set-up time for STOP condition: > 600 ns.

t_{BUF} = bus free time between a STOP and a START condition: > 600 ns.

C_b = capacitive load of one bus line: < 400 pF.

$t_{SU;BUSEN}$ = bus enable set-up time: $t_{SU;BUSEN}$ > 10 µs.

$t_{HO;BUSEN}$ = bus enable hold time: $t_{HO;BUSEN}$ > 10 µs.

Remark: The terms SDA and SCL are the corresponding terms used by the I^2C-bus for the DATA and CLOCK signals respectively.

Fig 6. I^2C-bus timing diagram

8.3 3-wire bus specification

The 3-wire bus controls the write/read, clock and data lines and operates at a maximum clock frequency of 400 kHz.

Hint: By using the standby bit the IC can be switched into a low current Standby mode. In Standby mode the IC must be in the WRITE mode. When the IC is switched to READ mode, during standby, the IC will hold the data line down. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the Standby mode being programmed, the IC maintains normal operation, but is isolated from the clock and data line.

8.3.1 Data transfer

Data sequence: byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order).

A positive edge at pin WRITE/READ enables the data transfer into the IC. The data has to be stable at the positive edge of the clock. Data may change while the clock is LOW and is written into the IC on the positive edge of the clock. Data transfer can be stopped after the transmission of new tuning information with the first two bytes or after each following byte.

A negative edge at pin WRITE/READ enables the data transfer from the IC. The WRITE/READ pin changes while the clock is LOW. With the negative edge at pin WRITE/READ the MSB of the first byte occurs at pin DATA.

The bits are shifted on the negative clock edge to pin DATA and can be read on the positive edge.

To do two consecutive read or write actions, pin WRITE/READ has to be toggled for at least one clock period. When a search tuning request is sent, the IC autonomously starts searching the FM band; the search direction and search stop level can be selected. When a station with a field strength equal to or greater than the stop level is found, the tuning system stops and the ready flag bit is set to HIGH. When, during search, a band limit is reached, the tuning system stops at the band limit and the band limit flag bit is set to HIGH. The ready flag is also set to HIGH in this case.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.3.2 Power-on reset

At Power-on reset the mute is set, all other bits are random. To initialize the IC all bytes have to be transferred.

8.4 Writing data

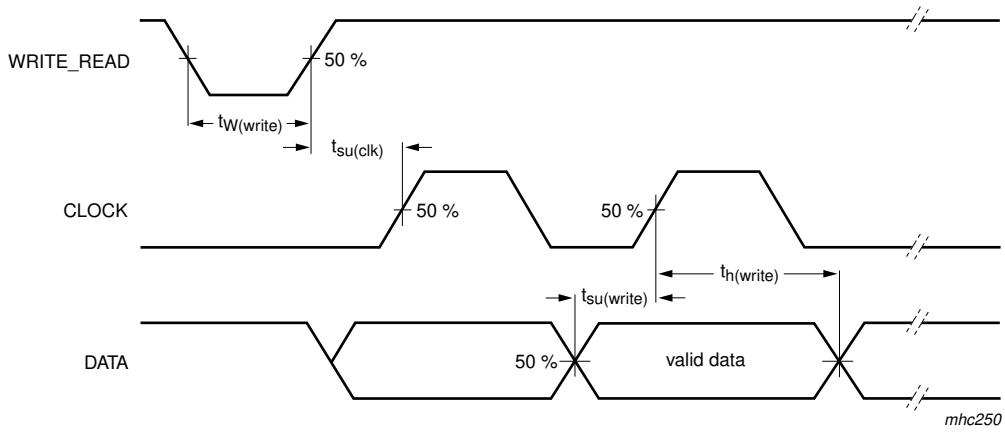


Fig 7. 3-wire bus write data

Fig 8. Write mode

Table 5. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6. Description of 1st data byte bits

Bit	Symbol	Description
7	MUTE	if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted
6	SM	**Search mode:** if SM = 1 then in search mode; if SM = 0 then not in search mode
5 to 0	PLL[13:8]	setting of synthesizer programmable counter for search or preset

Table 7. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter for search or preset

Table 9. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	MR	ML	SWP1

Table 10. Description of 3rd data byte bits

Bit	Symbol	Description
7	SUD	**Search Up/Down:** if SUD = 1 then search up; if SUD = 0 then search down
6 and 5	SSL[1:0]	**Search Stop Level:** see Table 11
4	HLSI	**High/Low Side Injection:** if HLSI = 1 then high side LO injection; if HLSI = 0 then low side LO injection
3	MS	**Mono to Stereo:** if MS = 1 then forced mono; if MS = 0 then stereo ON
2	MR	**Mute Right:** if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted
1	ML	**Mute Left:** if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted
0	SWP1	**Software programmable port 1:** if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW

Table 11. Search stop level setting

SSL1	SSL0	Search stop level
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

Table 12. Format of 4th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

Table 13. Description of 4th data byte bits

Bit	Symbol	Description
7	SWP2	**Software programmable port 2:** if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW
6	STBY	**Standby:** if STBY = 1 then in Standby mode; if STBY = 0 then not in Standby mode
5	BL	**Band Limits:** if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band
4	XTAL	**Clock frequency:** see Table 16
3	SMUTE	**Soft Mute:** if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF
2	HCC	**High Cut Control:** if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF
1	SNC	**Stereo Noise Cancelling:** if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF
0	SI	**Search Indicator:** if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1

Table 14. Format of 5th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLLREF	DTC	-	-	-	-	-	-

Table 15. Description of 5th data byte bits

Bit	Symbol	Description
7	PLLREF	if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled; see Table 16
6	DTC	if DTC = 1 then the de-emphasis time constant is 75 µs; if DTC = 0 then the de-emphasis time constant is 50 µs
5 to 0	-	not used; position is don't care

Table 16. Clock bits setting

PLLREF	XTAL	Clock frequency
0	0	13 MHz
0	1	32.768 kHz
1	0	6.5 MHz
1	1	not allowed

8.5 Reading data

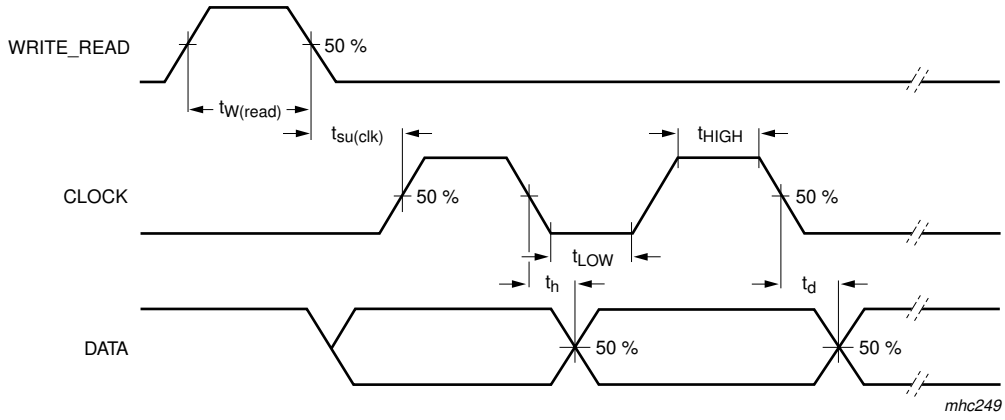


Fig 9. 3-wire bus read data

Fig 10. Read mode

Table 17. Format of 1st data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 18. Description of 1st data byte bits

Bit	Symbol	Description
7	RF	**Ready Flag:** if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found
6	BLF	**Band Limit Flag:** if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached
5 to 0	PLL[13:8]	setting of synthesizer programmable counter after search or preset

Table 19. Format of 2nd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 20. Description of 2nd data byte bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	setting of synthesizer programmable counter after search or preset

Table 21. Format of 3rd data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 22. Description of 3rd data byte bits

Bit	Symbol	Description
7	STEREO	**Stereo indication:** if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception
6 to 0	PLL[13:8]	IF counter result

Table 23. Format of 4th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 24. Description of 4th data byte bits

Bit	Symbol	Description
7 to 4	LEV[3:0]	level ADC output
3 to 1	CI[3:1]	**Chip Identification:** these bits have to be set to logic 0
0	-	this bit is internally set to logic 0

Table 25. Format of 5th data byte

7 (MSB)	6	5	4	3	2	1	0 (LSB)
0	0	0	0	0	0	0	0

Table 26. Description of 5th data byte bits

Bit	Symbol	Description
7 to 0	-	reserved for future extensions; these bits are internally set to logic 0

9. Internal circuitry

Table 27. Internal circuitry

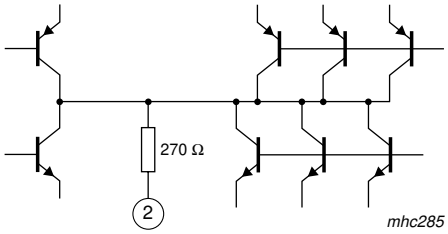
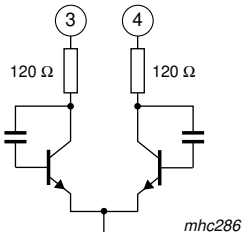
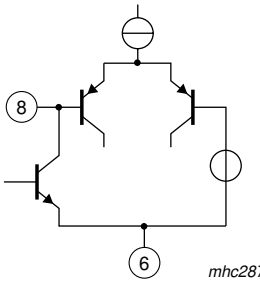
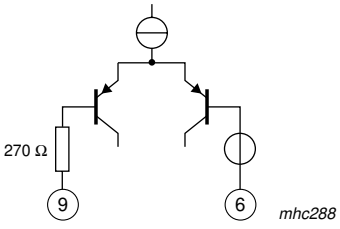
Pin	Symbol	Equivalent circuit
1	n.c.	
2	CPOUT	
3	$V_{COTANK1}$	
4	$V_{COTANK2}$	
5	$V_{CC(VCO)}$	
6	DGND	
7	V_{CCD}	
8	DATA	
9	CLOCK	
10	n.c.	

Table 27. Internal circuitry

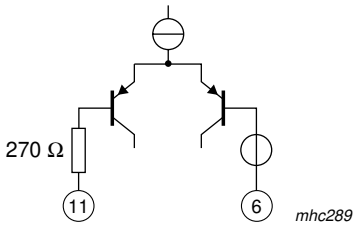
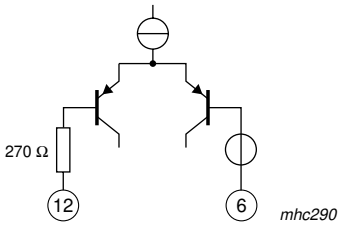
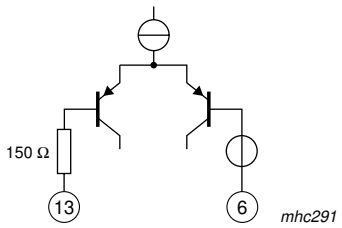
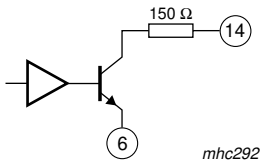
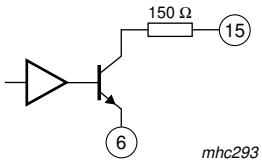
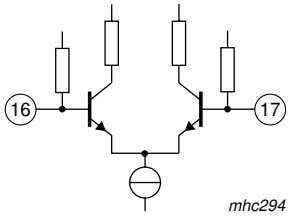
Pin	Symbol	Equivalent circuit
11	WRITE/READ	
12	BUSMODE	
13	BUSENABLE	
14	SWPORT1	
15	SWPORT2	
16	XTAL1	
17	XTAL2	

Table 27. Internal circuitry

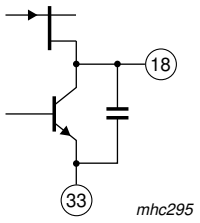
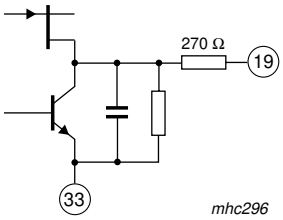
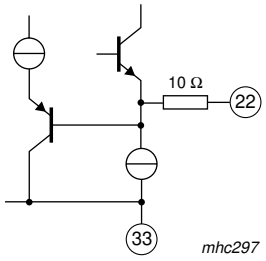
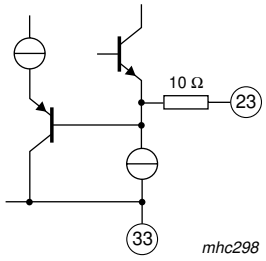
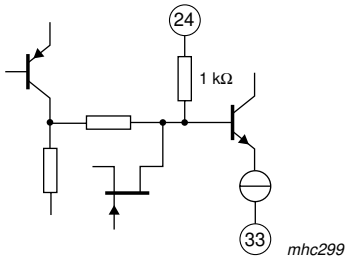
Pin	Symbol	Equivalent circuit
18	PHASEFIL	
19	PILFIL	
20	n.c.	
21	n.c.	
22	V_{AFL}	
23	V_{AFR}	
24	TMUTE	

Table 27. Internal circuitry

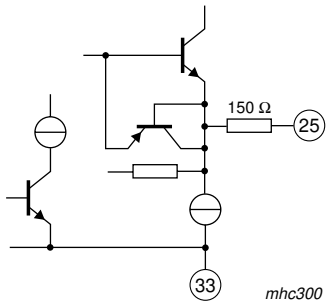
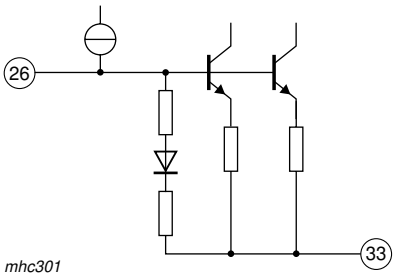
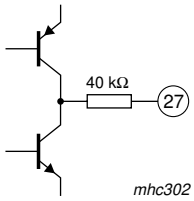
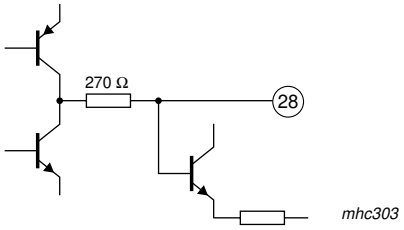
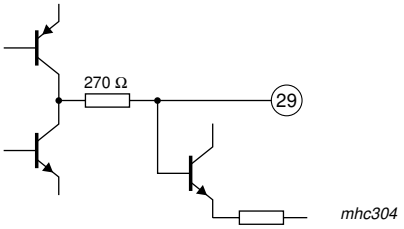
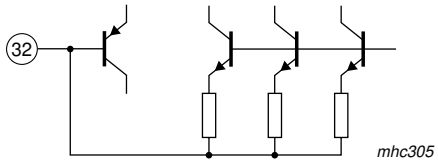
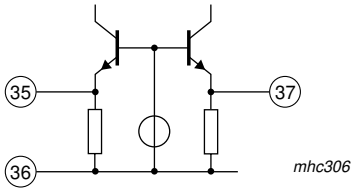
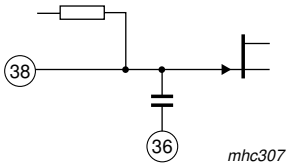
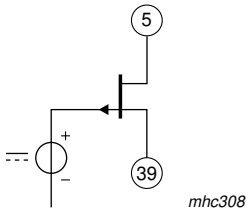
Pin	Symbol	Equivalent circuit
25	MPXO	
26	V_{ref}	
27	TIFC	
28	LIMDEC1	
29	LIMDEC2	
30	n.c.	
31	n.c.	

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
32	I_{gain}	
33	AGND	
34	V_{CCA}	
35	RFI1	
36	RFGND	
37	RFI2	
38	TAGC	
39	LOOPSW	
40	n.c.	

10. Limiting values

Table 28. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		−0.3	+8	V
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		−0.3	+8	V
V_{CCD}	digital supply voltage		−0.3	+5	V
V_{CCA}	analog supply voltage		−0.3	+8	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−10	+75	°C

Table 28. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{esd}	electrostatic discharge voltage	all pins except pin DATA	[1]	−200	+200	V
			[2]	−2000	+2000	V
		pin DATA	[1]	−150	+200	V
			[2]	−2000	+2000	V

[1] Machine model (R = 0 Ω, C = 200 pF).

[2] Human body model (R = 1.5 kΩ, C = 100 pF).

11. Thermal characteristics

Table 29. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	29	K/W

12. Static characteristics

Table 30. Static characteristics

V_{CCA} = $V_{CC(VCO)}$ = V_{CCD} = 2.7 V; T_{amb} = 25 °C; All AC values are given in RMS unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages[1]						
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	VCO supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
Supply currents						
I_{CCA}	analog supply current	operating				
		V_{CCA} = 3 V	6.0	8.4	10.5	mA
		V_{CCA} = 5 V	6.2	8.6	10.7	mA
		Standby mode				
		V_{CCA} = 3 V	-	3	6	µA
		V_{CCA} = 5 V	-	3.2	6.2	µA
$I_{CC(VCO)}$	VCO supply current	operating				
		$V_{CC(VCO)}$ = 3 V	560	750	940	µA
		$V_{CC(VCO)}$ = 5 V	570	760	950	µA
		Standby mode				
		$V_{CC(VCO)}$ = 3 V	-	1	2	µA
		$V_{CC(VCO)}$ = 5 V	-	1.2	2.2	µA

Table 30. Static characteristics *...continued*

V_{CCA} = $V_{CC(VCO)}$ = V_{CCD} = 2.7 V; T_{amb} = 25 °C; All AC values are given in RMS unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCD}	digital supply current	operating				
		V_{CCD} = 3 V	2.1	3.0	3.9	mA
		V_{CCD} = 5 V	2.25	3.15	4.05	mA
		Standby mode; V_{CCD} = 3 V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
		Standby mode; V_{CCD} = 5 V				
		bus enable line HIGH	50	78	105	µA
		bus enable line LOW	20	33	45	µA

[1] V_{CCA}, $V_{CC(VCO)}$ and V_{CCD} must not differ by more than 200 mV.

Table 31. DC operating points, unloaded DC voltage

V_{CCA} = $V_{CC(VCO)}$ = V_{CCD} = 2.7 V; T_{amb} = 25 °C; unless otherwise specified.

Operating point	Conditions	Min	Typ	Max	Unit
V_{CPOUT}		0.1	-	$V_{CC(VCO)}$ − 0.1	V
V_{XTAL2}	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
V_{XTAL2}	data byte 4 bit 4 = 1	1.64	1.72	1.8	V
	data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$		0.4	1.2	V_{CCA} − 0.4	V
V_{PILFIL}		0.65	0.9	1.3	V
V_{AFL}	f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{AFR}	f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{TMUTE}	V_{RF} = 0 V	1.5	1.65	1.8	V
V_{MPXO}	f_{RF} = 98 MHz; V_{RF} = 1 mV	680	815	950	mV
V_{ref}		1.45	1.55	1.65	V
V_{TIFC}		1.34	1.44	1.54	V
$V_{LIMDEC1}$		1.86	1.98	2.1	V
$V_{LIMDEC2}$		1.86	1.98	2.1	V
V_{Igain}		480	530	580	mV
V_{RFI1}		0.93	1.03	1.13	V
V_{RFI2}		0.93	1.03	1.13	V
V_{TAGC}	V_{RF} = 0 V	1	1.57	2	V