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TEA6848HL

New in car entertainment car radio tuner IC with precision adjacent channel suppression (NICE-PACS)

Rev. 04 — 29 January 2010 Product data sheet

1. General description

The TEA6848HL is a single IC with car radio tuner for AM, FM and Weather Band (WB) intended for microcontroller tuning with the I²C-bus. It provides the following functions:

- AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM double conversion receiver with integrated image rejection for IF1 and for IF2 capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands; fully integrated dynamic selectivity at 450 kHz FM IF2; FM demodulator with dynamic threshold extension; center frequency alignment of IF2 selectivity via the I²C-bus
- The tuning system includes VCO, crystal oscillator and PLL synthesizer on one chip

2. Features

- FM mixer 1 for conversion of FM RF (65 MHz to 108 MHz and US weather band) to IF of 10.7 MHz; the mixer provides inherent image rejection; for European and US FM band/WB (weather band) the mixer is driven with a ‘high’ injection Local Oscillator (LO); in Japan FM band and East Europe FM band the mixer is driven with a ‘low’ injection LO
- AM mixer 1 for conversion of AM RF to AM IF1 of 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 of 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and FM mixer 2 and reference for synthesizer PLL, IF count, timing for Radio Data System (RDS) update and reference frequency for car audio signal processor ICs
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx, TEF689x)
- Digital alignment circuit for bus controlled matching of oscillator tuning voltage to FM antenna tank circuit tuning voltage
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode drive can be activated by the I²C-bus as a local function for search tuning; AGC threshold is a programmable and keyed function switchable via the I²C-bus
- FM IF linear amplifier with high dynamic input range
- FM mixer 2 for conversion of FM IF1 to FM IF2 of 450 kHz with inherent image rejection

- Fully integrated dynamic selectivity and FM demodulator at IF2; improved sensitivity with dynamic threshold extension; center frequency of IF2 selectivity alignment via the I²C-bus
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I²C-bus
- AM cascode AGC stage and RF PIN diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold for detection at mixer 1 input is programmable via the I²C-bus
- AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with detection at IF1 and blanking at AM IF2
- Software controlled flag output
- Buffer output for weather band flag
- Adjacent channel detector, modulation detector and frequency offset for instantaneous bandwidth control of the integrated filter
- Flag and voltage output indicating the actual bandwidth
- I²C-bus alignment of center frequency and gain variation as functions of bandwidth of the IF2 filter and center frequency of the offset detector

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA(n)}$	analog supply voltages 1 to 4 and 6			8	8.5	9	V
$I_{DDA(tot)}$	total analog supply current	FM mode	[1]	45	56	67	mA
		AM mode	[1]	40	50	60	mA
V_{DDA5}	analog supply voltage 5			4.75	5	5.25	V
I_{DDA5}	analog supply current 5 for on-chip power supply	FM mode; Japan/East Europe band		-	7.4	-	mA
		AM mode		-	11	-	mA
V_{DDD}	digital supply voltage			4.75	5	5.25	V
I_{DDD}	digital supply current	FM mode; Europe/US band		21	26	31	mA
		AM mode		22	27	32	mA
T_{amb}	ambient temperature			−40	-	+85	°C
AM overall system parameters; see Figure 12 and Figure 13							
$f_{AM(ant)}$	AM input frequency	LW		0.144	-	0.288	MHz
		MW		0.522	-	1.710	MHz
		SW		5.730	-	9.99	MHz
(S+N)/N	signal plus noise-to-noise ratio	m = 0.3; B_{AF} = 2.15 kHz		-	59	-	dB
THD	total harmonic distortion	m = 0.8; f_{mod} = 1 kHz		-	0.3	-	%
$V_{sens(rms)}$	sensitivity (RMS value)	m = 0.3; f_{mod} = 1 kHz; (S+N)/N = 26 dB; with European dummy aerial 15 pF/60 pF; B_{AF} = 2.15 kHz		-	45	-	µV

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM overall system parameters; see Figure 12 and Figure 13						
$f_{FM(ant)}$	FM input frequency		65	-	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	-	162.55	MHz
(S+N)/N	signal plus noise-to-noise ratio	Δf = 22.5 kHz; de-emphasis = 50 μs; B_{AF} = 300 Hz to 15 kHz	-	63	-	dB
THD	total harmonic distortion	Δf = 75 kHz; with 2 × SFE10.7MS3	-	0.35	-	%
$V_{sens(rms)}$	sensitivity (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 50 μs; B_{AF} = 300 Hz to 15 kHz; with 75 Ω dummy antenna	-	1.4	2	μV

[1] Sum of analog supply currents 1 to 4 and 6.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEA6848HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

5. Block diagram

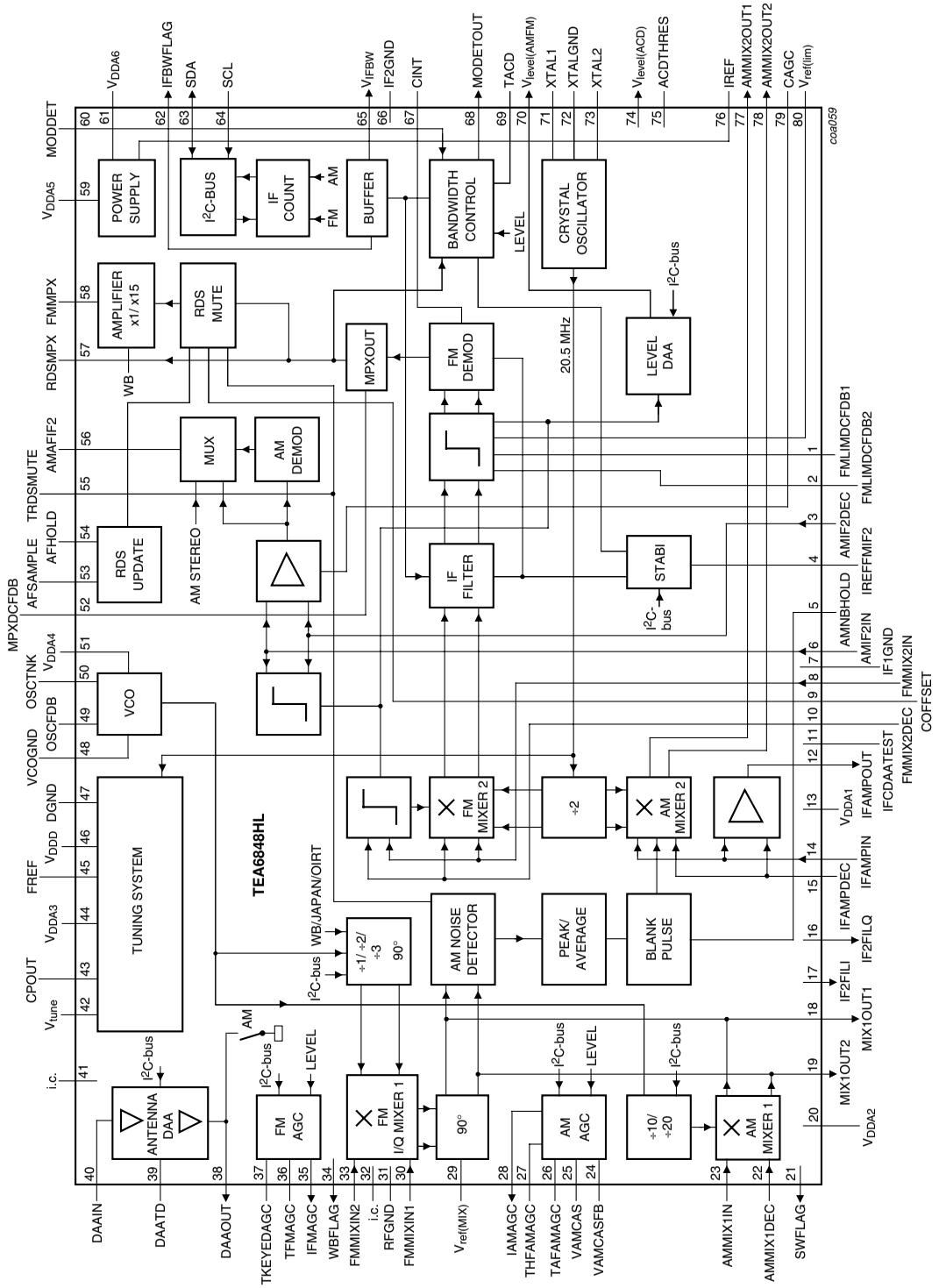


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

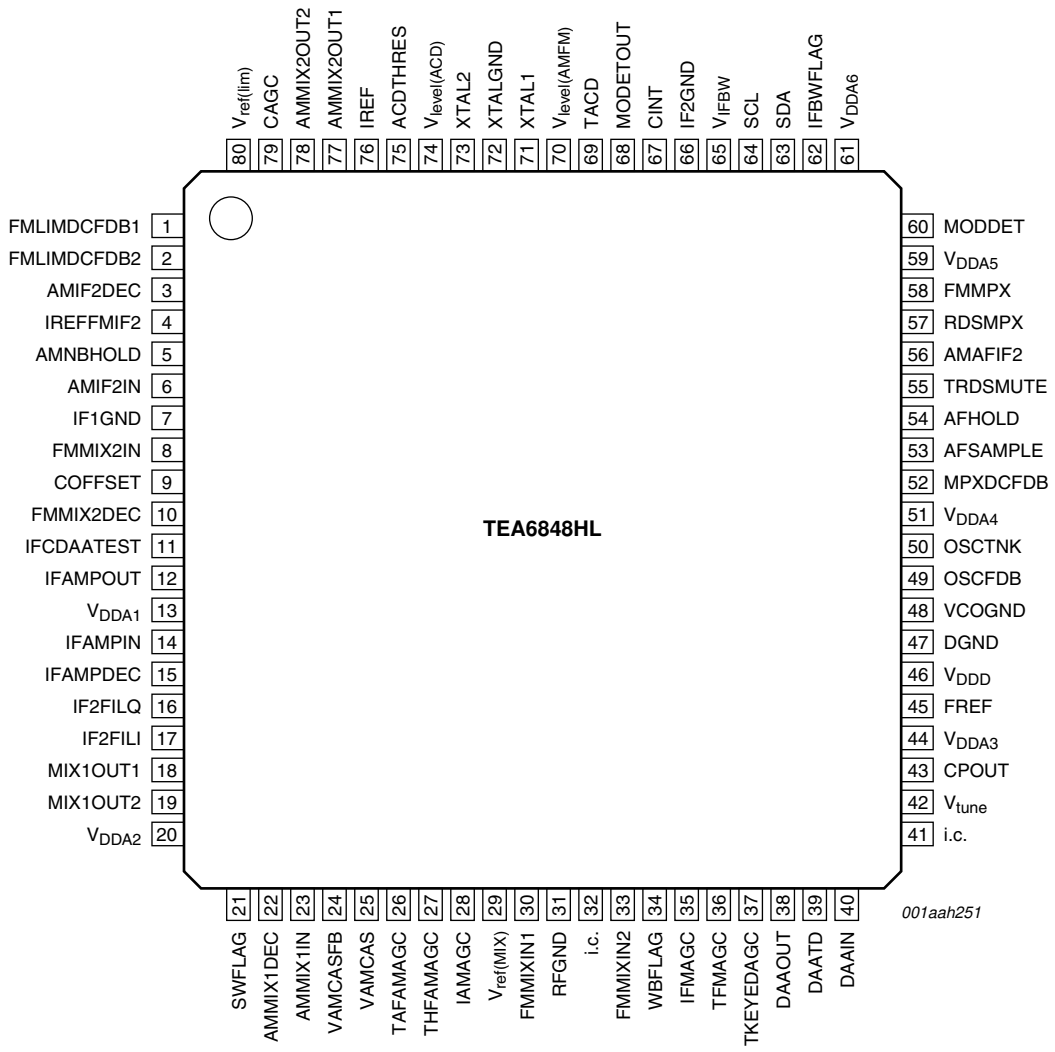


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
FMLIMDCFDB1	1	decoupling in-phase FM limiter
FMLIMDCFDB2	2	decoupling quadrature phase FM limiter
AMIF2DEC	3	decoupling for AM IF2 input
IREFFMIF2	4	reference current for FM IF2
AMNBHOLD	5	AM noise blanker threshold
AMIF2IN	6	AM IF2 input (450 kHz) for demodulator AGC and AM level detector

Table 3. Pin description *...continued*

Symbol	Pin	Description
IF1GND	7	AM IF1 ground
FMMIX2IN	8	FM mixer 2 input
COFFSET	9	DC feedback for offset compensation RDS mute
FMMIX2DEC	10	FM mixer 2 decoupling
IFCDAATEST	11	test pin for IF center DAA
IFAMPOUT	12	IF amplifier output (10.7 MHz)
V_{DDA1}	13	analog supply voltage 1 (8.5 V) for FM IF amplifier
IFAMPIN	14	FM IF amplifier and AM mixer 2 input (10.7 MHz)
IFAMPDEC	15	FM IF amplifier and AM mixer 2 decoupling
IF2FILQ	16	test output quadrature phase FM IF2 filter
IF2FILI	17	test output in-phase FM IF2 filter
MIX1OUT1	18	FM mixer and AM mixer 1 IF output 1 (10.7 MHz)
MIX1OUT2	19	FM mixer and AM mixer 1 IF output 2 (10.7 MHz)
V_{DDA2}	20	analog supply voltage 2 (8.5 V) for FM and AM RF
SWFLAG	21	output software programmable flag
AMMIX1DEC	22	AM mixer 1 decoupling
AMMIX1IN	23	AM mixer 1 input
VAMCASFB	24	feedback for cascode AM AGC
VAMCAS	25	cascode AM AGC
TAFAMAGC	26	AF time constant of AM front-end AGC
THFAMAGC	27	HF time constant of AM front-end AGC
IAMAGC	28	PIN diode drive current output of AM front-end AGC
$V_{ref(MIX)}$	29	reference voltage for FM RF mixer
FMMIXIN1	30	FM RF mixer input 1
RFGND	31	RF ground
i.c.	32	internal connection
FMMIXIN2	33	FM RF mixer input 2
WBFLAG	34	buffered weather band flag output
IFMAGC	35	PIN diode drive current output of FM front-end AGC
TFMAGC	36	time constant of FM front-end AGC
TKEYEDAGC	37	time constant of keyed FM front-end AGC
DAAOUT	38	output of digital auto alignment circuit for antenna tank circuit
DAATD	39	temperature compensation diode for digital auto alignment circuit for antenna tank circuit
DAAIN	40	input of digital auto alignment circuit for antenna tank circuit
i.c.	41	internal connection
V_{tune}	42	tuning voltage
CPOUT	43	charge pump output
V_{DDA3}	44	analog supply voltage 3 (8.5 V) for tuning PLL
FREF	45	reference frequency output for signal processor IC
V_{DDD}	46	digital supply voltage (5 V)
DGND	47	digital ground

Table 3. Pin description *...continued*

Symbol	Pin	Description
VCOGND	48	VCO ground
OSCFDB	49	VCO feedback
OSCTNK	50	VCO tank circuit
V_{DDA4}	51	analog supply voltage 4 (8.5 V) for VCO
MPXDCFDB	52	DC feedback for FM MPX signal path
AFSAMPLE	53	AF sample flag output for car audio signal processor IC
AFHOLD	54	AF hold flag output for car audio signal processor IC
TRDSMUTE	55	time constant for RDS update mute
AMAFIF2	56	AM demodulator AF output or IF2 output for AM stereo (multiplexed by I^2C-bus)
RDSMPX	57	MPX output for RDS decoder and signal processor (not muted)
FMMPX	58	FM demodulator MPX output
V_{DDA5}	59	analog supply voltage 5 (5 V) for on-chip power supply
MODDET	60	modulation detector input
V_{DDA6}	61	analog supply voltage 6 (8.5 V) for on-chip power supply
IFBWFLAG	62	FM IF2 bandwidth flag output
SDA	63	I^2C-bus data line input and output
SCL	64	I^2C-bus clock line input
V_{IFBW}	65	monitor voltage for FM IF2 bandwidth
IF2GND	66	AM IF2 ground
CINT	67	demodulator loop filter
MODETOUT	68	modulation detector output
TACD	69	adjacent channel detector time constant
$V_{level(AMFM)}$	70	level voltage output for AM and FM
XTAL1	71	crystal oscillator 1
XTALGND	72	crystal oscillator ground
XTAL2	73	crystal oscillator 2
$V_{level(ACD)}$	74	level voltage output for adjacent channel detector
ACDTHRES	75	adjacent channel detector threshold
IREF	76	reference current for power supply
AMMIX2OUT1	77	AM mixer 2 output 1 (450 kHz)
AMMIX2OUT2	78	AM mixer 2 output 2 (450 kHz)
CAGC	79	AM IF AGC capacitor/offset detector alignment (FM)
$V_{ref(lim)}$	80	limiter reference voltage

7. Functional description

7.1 Oscillators

7.1.1 VCO

The varactor tuned VCO provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range of 162.9 MHz to 248.2 MHz.

7.1.2 PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

7.1.3 Crystal oscillator

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2 and FM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.368 kHz) for the TEA688x (Car Audio Signal Processor - CASP) or TEF689x (Car Radio Integrated Signal Processor - CRISP)

7.2 DAA

To reduce the number of manual alignments in production the following I^2C-bus controlled Digital Auto Alignment (DAA) functions are included:

- FM RF DAA
  - 7-bit DAA circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit
- FM and AM level DAA
  - Level DAA circuitry for alignment of slope (3-bit) and starting point (5-bit) of the level curve
- IF2 center DAA
  - Center frequency alignment (7-bit) of integrated FM IF2 dynamic selectivity

7.3 FM signal channel

7.3.1 FM mixer 1

FM quadrature mixer converts FM RF (65 MHz to 108 MHz and weather band) to IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands:

- US FM = 87.9 MHz to 107.9 MHz
- US weather FM = 162.4 MHz to 162.55 MHz
- Europe FM = 87.5 MHz to 108 MHz
- Japan FM = 76 MHz to 91 MHz
- East Europe FM = 65 MHz to 74 MHz

7.3.2 Buffer output for weather band flag (pin WBFLAG)

The buffer output on pin WBFLAG is HIGH for weather band mode.

7.3.3 FM keyed AGC

The AGC threshold is programmable and the keyed AGC function is switchable via the I^2C-bus. AGC detection occurs at the input of the first FM mixer. If the keyed AGC function is activated, the AGC is keyed only by the narrow band level. The AGC PIN diode drive can be activated via the I^2C-bus as a local function for search tuning. The AGC sources a constant 10 mA current into the FM PIN diode in AM mode.

7.3.4 FM IF amplifier

The FM IF amplifier provides 18 dB amplification with high linearity over a wide dynamic range.

7.3.5 FM mixer 2

The FM mixer 2 converts 10.7 MHz FM IF1 to 450 kHz FM IF2 in I and Q phase to achieve image rejection in the demodulator.

7.3.6 FM IF2 dynamic selectivity

The IF bandwidth of the FM IF2 is automatically adjusted depending on modulation and reception conditions. The center frequency of the selectivity is adjusted by a 7-bit instruction via the I^2C-bus. The dynamic selectivity mode and three fixed bandwidths (60 kHz, 90 kHz and 130 kHz) can be selected via the I^2C-bus. The IF2 bandwidth is set to 13 kHz in weather band mode.

7.3.7 FM quadrature demodulator

The FM quadrature demodulator is adjustment free.

7.3.8 Adjacent channel detector and threshold extension

In the event of breakthrough of a strong neighboring transmitter, the IF2 bandwidth is reduced dynamically. At low RF input voltages and low modulation levels the IF2 bandwidth is reduced to achieve improved sensitivity by demodulator threshold extension.

7.3.9 Bandwidth control ‘active’ flag (pin IFBWFLAG)

Flag output IFBW = 1 from pin IFBWFLAG indicates that the IF2 bandwidth is reduced.

7.3.10 Bandwidth control monitor voltage (pin V_{IFBW})

The actual bandwidth is indicated by a voltage at pin V_{IFBW} that is proportional, not linear, to the IF bandwidth.

7.4 AM signal channel

7.4.1 AM tuner including mixer 1 and mixer 2

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to IF2 of 450 kHz:

- LW = 144 kHz to 288 kHz
- MW = 530 kHz to 1710 kHz (US AM band)
- SW = 5.73 MHz to 9.99 MHz (including the 31 m, 41 m and 49 m bands)

7.4.2 AM RF AGC

The AM wideband AGC in front of the first AM mixer is realized first by a cascaded NPN transistor, which controls the transconductance of the RF amplifier JFET with 10 dB of AGC range. Second, an AM PIN diode stage with antenna type and frequency dependent AGC range is available. The minimum JFET drain source voltage is controlled by a DC feedback loop (pin VAMCASFB) in order to limit the cascode AGC range to 10 dB. If the cascode AGC is not required, a simple RF AGC loop is possible by using only a PIN diode. In this event pins VAMCASFB and VAMCAS have to be open-circuit. In FM mode, the cascade switches off the JFET bias current to reduce total power consumption. The PIN diode is biased by 1 mA in FM mode.

The AGC detection points for AM AGC are at the first AM mixer input (threshold programmable via the I^2C-bus) and the IF2 AGC input (fixed threshold).

7.4.3 AM detector

The AM output provides either a detected AM AF or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing. Soft mute function is controlled by the I^2C-bus in AM mono mode.

7.4.4 AM noise blanker

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the mixer 2.

Trigger sensitivity can be modified by adding an external resistor at pin AMNBHOLD.

7.5 FM and AM level detector

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I^2C-bus.

7.6 IF2 filter gain alignment

The 4-bit filter gain alignment reduces the change in IF filter gain spread when the bandwidth is changed in dynamic mode from 155 kHz (maximum) to 25 kHz (minimum).

A frequency has to be chosen in the middle of European/US FM band, Japan band or OIRT band (for East Europe) and the IC has to be set into dynamic bandwidth mode (IF2 bandwidth is 155 kHz).

Setting and clearing the FMBW bit continuously allows the adjustment of the gain alignment to minimum change in AM/FM DC level.

7.7 Frequency offset detector/alignment

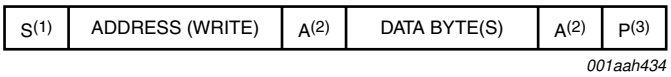
A very strong undesired neighboring signal causes offset in the demodulator in case of a weak desired input signal.

The frequency offset detector reduces the bandwidth of the IF2 filter when the detected offset in the demodulator is too large.

There are four bits available for frequency offset detector alignment. Every band has to be aligned separately. Tuning has to be set to middle of the band, input signal unmodulated, bit IFBW = 1 (alignment voltage will be given to pin IFBWFLAG). The DC voltage at pin IFBWFLAG has to be aligned to the minimum value.

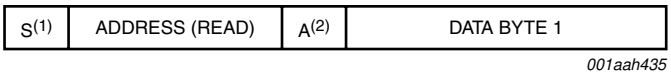
8. I²C-bus protocol

8.1 Data transfer mode and IC address



(1) S = START condition.
(2) A = acknowledge.
(3) P = STOP condition.

Fig 3. Write mode



(1) S = START condition.
(2) A = acknowledge.

Fig 4. Read mode

Table 4. IC address byte

IC address							Mode
1	1	0	0	0	0	0/1[1]	R/$\overline{W}$[2]

[1] Defined by address pin FREF:
a) 1 = 1st IC address
b) 0 = 2nd IC address

[2] Read or Write mode:
a) 0 = write operation to TEA6848HL
b) 1 = read operation from TEA6848HL

8.2 Write mode: data byte 0

Table 5. Format of data byte 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6. Description of data byte 0 bits

Bit	Symbol	Description
7	AF	**alternative frequency.** If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PLL[14:8]	**setting of programmable counter of synthesizer PLL.** Upper byte of PLL divider word.

8.3 Write mode: data byte 1

Table 7. Format of data byte 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8. Description of data byte 1 bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	**setting of programmable counter of synthesizer PLL.** Lower byte of PLL divider word.

8.4 Write mode: data byte 2

Table 9. Format of data byte 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUTE	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

Table 10. Description of data byte 2 bits

Bit	Symbol	Description
7	MUTE	**FM audio mute.** If MUTE = 0, then FM audio not muted. If MUTE = 1, then FM audio muted; writing to programmable divider and antenna DAA enabled.
6 to 0	DAA[6:0]	**setting of antenna digital auto alignment**

8.5 Write mode: data byte 3

Table 11. Format of data byte 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IFMT	FREF2	FREF1	FREF0	IFPR	BND1	BND0	AMFM

Table 12. Description of data byte 3 bits

Bit	Symbol	Description
7	IFMT	**IF measuring time.** If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms.
6 to 4	FREF[2:0]	**reference frequency for synthesizer.** These 3 bits determine the reference frequency, see Table 13.

Table 12. Description of data byte 3 bits *…continued*

Bit	Symbol	Description
3	IFPR	**IF counter prescaler ratio.** If IFPR = 0, then IF prescaler ratio is 40. If IFPR = 1, then IF prescaler ratio is 10.
2 and 1	BND[1:0]	**band switch.** These 2 bits select in FM mode band and local or distance, see Table 14; in AM mode band and AM stereo, see Table 15.
0	AMFM	**AM or FM switch.** If AMFM = 0, then FM mode. If AMFM = 1, then AM mode.

Table 13. Reference frequency setting

FREF2	FREF1	FREF0	f_{ref} (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

Table 14. FM mode

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	0	FM standard	2	130 μA + 3 mA
0	1	FM Japan	3	130 μA + 3 mA
1	0	FM East Europe	3	1 mA
1	1	FM weather	1	300 μA

Table 15. AM mode

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	0	AM SW mono	10	1 mA
0	1	AM SW stereo	10	1 mA
1	0	AM LW/MW mono	20	1 mA
1	1	AM LW/MW stereo	20	1 mA

8.6 Write mode: data byte 4

Table 16. Format of data byte 4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KAGC	AGC1	AGC0	AMSM/FMBW	LODX	FLAG	BW1	BW0

Table 17. Description of data byte 4 bits

Bit	Symbol	Description
7	KAGC	**keyed FM AGC.** If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	AGC[1:0]	**wideband AGC.** These 2 bits set the start value of wideband AGC. For AM, see Table 18 and for FM, see Table 19.
4	AMSM/FMBW	**AM soft mute or FM bandwidth.** AM mode: if AMSM/FMBW = 0, then AM soft mute is off; if AMSM/FMBW = 1, then AM soft mute is on. FM mode: see Table 20.
3	LODX	**local or distance.** If LODX = 0, then distance mode is on. If LODX = 1, then local mode is on.
2	FLAG	**software programmable flag.** If FLAG = 0, then flag output pin SWFLAG is HIGH. If FLAG = 1, then flag output pin SWFLAG is LOW.
1 and 0	BW[1:0]	**FM IF2 bandwidth setting.** See Table 20.

Table 18. Setting of wideband AGC for AM (m = 0.3)

AGC1	AGC0	AM mixer 1 input voltage (peak value) (mV)
0	0	150
0	1	275
1	0	400
1	1	525

Table 19. Setting of wideband AGC for FM

AGC1	AGC0	FM RF mixer input voltage (RMS value) (mV)
1	1	3
1	0	6
0	1	9
0	0	12

Table 20. FM IF2 bandwidth setting

FMBW	BW1	BW0	FM IF2 bandwidth B_{-3dB}
0	0	0	dynamic mode
0	0	1	130 kHz fixed
0	1	0	90 kHz fixed
0	1	1	60 kHz fixed
1	0	0	25 kHz frequency offset alignment mode; bandwidth flag output switched to frequency offset detector alignment voltage

8.7 Write mode: data byte 5

Table 21. Format of data byte 5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

Table 22. Description of data byte 5 bits

Bit	Symbol	Description
7 to 3	LST[4:0]	**setting of level DAA starting point.** These 5 bits determine the offset of the level detector output voltage.
2 to 0	LSL[2:0]	**setting of level DAA slope.** These 3 bits determine the steepness of the level detector output voltage.

Table 23. Standard setting of data byte 5 bits

Setting of level DAA starting point					Setting of level DAA slope		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

8.8 Write mode: data byte 6

Table 24. Format of data byte 6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TE	CF6	CF5	CF4	CF3	CF2	CF1	CF0

Table 25. Description of data byte 6 bits

Bit	Symbol	Description
7	TE	**threshold extension.** If TE = 0, then threshold extension is off. If TE = 1, then threshold extension is on.
6 to 0	CF[6:0]	**setting of FM IF2 center frequency DAA.** The content of CF6 to CF0 determines the center frequency of the 450 kHz filter.

8.9 Write mode: data byte 7

Table 26. Format of data byte 7

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FOF3	FOF2	FOF1	FOF0	FGN3	FGN2	FGN1	FGN0

Table 27. Description of data byte 7 bits

Bit	Symbol	Description
7 to 4	FOF[3:0]	**frequency offset gain alignment**
3 to 0	FGN[3:0]	**IF2 filter gain alignment**

8.10 Read mode: data byte 0

Table 28. Format of 1st data byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

Table 29. Description of data byte 0 bits

Bit	Symbol	Description
7 to 0	IFC[7:0]	**IF counter result.** These bits contain the least significant 8 bits of the IF counter result.

8.11 I²C-bus specification

Information about the I²C-bus can be found in the user manual *UM10204 "I²C-bus specification and user manual"*.

The standard I²C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2H: 1100 001R/$\overline{W}$
- 2nd IC address C0H: 1100 000R/$\overline{W}$

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

A second I²C-bus address can be selected by connecting pin FREF via a 68 kΩ resistor to GND.

8.11.1 Data transfer

Data sequence: address, byte 0, byte 1, byte 2, byte 3, byte 4, byte 5, byte 6, and byte 7. The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6848HL.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available

8.11.2 I²C-bus pull-up resistors

When the IC is used together with the TEA688x or TEF689x and both SCL and SDA lines are connected via the I²C-bus to the TEA688x or TEF689x, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA688x or TEF689x. Otherwise an I²C-bus pull-down can occur switching off the tuner IC supply when the I²C-bus buffer interface of the TEA688x or TEF689x is enabled for data transfer to the tuner IC.

8.11.3 Restriction of the I²C-bus characteristic

At −40 °C the start of the acknowledge bit after transmitting the slave address exceeds the general requirement of $t_{HD;DAT}$ < 3.45 μs. The start of acknowledge is $t_{ST;ACK}$ < 4.1 μs over the full temperature range from −40 °C to +85 °C. This will not influence the overall system performance, because the required set-up time $t_{SU;DAT}$ > 250 ns is fulfilled at any condition.

8.11.4 Frequency setting

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit MUTE = 1. To select an FM frequency, two I²C-bus transmissions are necessary:

- First: bit MUTE = 1
- Second: bit MUTE = 0

8.11.5 Default settings

No default settings at power-on reset. One I²C-bus transmission is required to program the IC.

8.11.6 Timing requirements

Table 30. Timing requirements of I²C-bus software

Function	Timing
Switching from FM to AM	400 ms (10 μF at pin CAGC)
Switching from AM to FM	100 ms (10 μF at pin CAGC; wideband position has to be set for at least 100 ms to activate speed-up circuitry)
Start-up in FM mode	wideband position has to be set for at least 100 ms to activate speed-up circuitry
Switching to dynamic mode	500 μs (18 nF at pin TACD; wideband position has to be set for at least 500 μs to activate clamping circuitry at pin TACD)

9. Internal circuitry

Table 31. Equivalent pin circuits

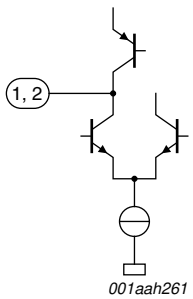
Pin	Symbol	Equivalent circuit
1	FMLIMDCFDB1	 001aah261
2	FMLIMDCFDB2	

Table 31. Equivalent pin circuits *…continued*

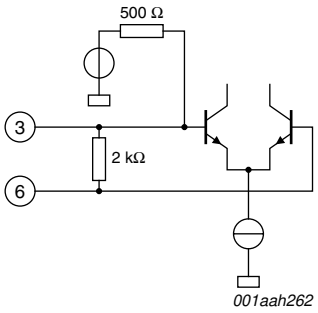
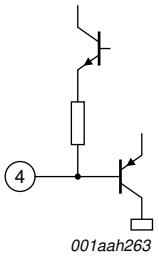
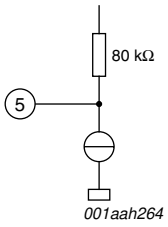
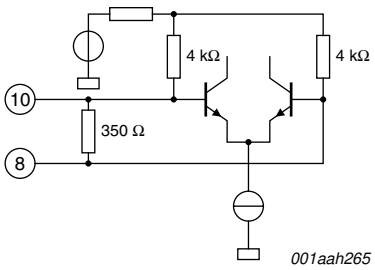
Pin	Symbol	Equivalent circuit
3	AMIF2DEC	
6	AMIF2IN	
4	IREFFMIF2	
5	AMNBHOLD	
7	IF1GND	
8	FMMIX2IN	
10	FMMIX2DEC	

Table 31. Equivalent pin circuits *…continued*

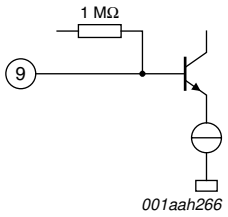
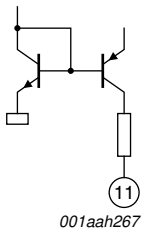
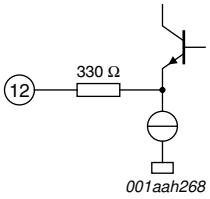
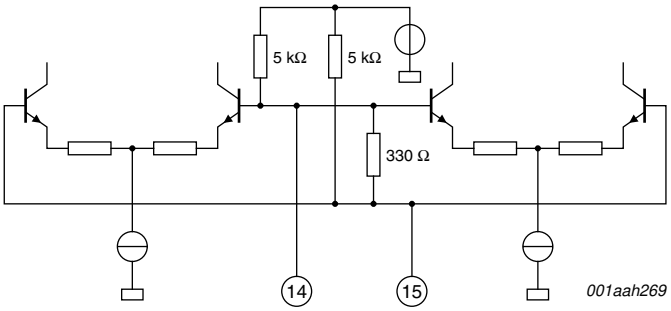
Pin	Symbol	Equivalent circuit
9	COFFSET	
11	IFCDAATEST	
12	IFAMPOUT	
13	V_{DDA1}	
14	IFAMPIN	
15	IFAMPDEC	

Table 31. Equivalent pin circuits *…continued*

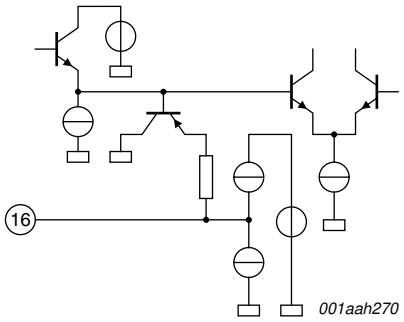
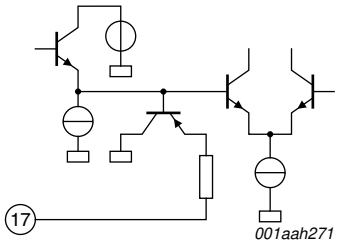
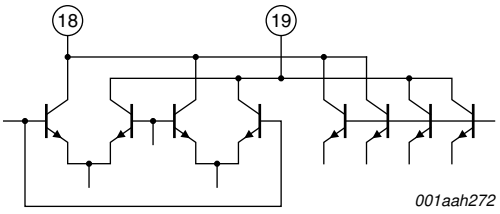
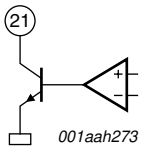
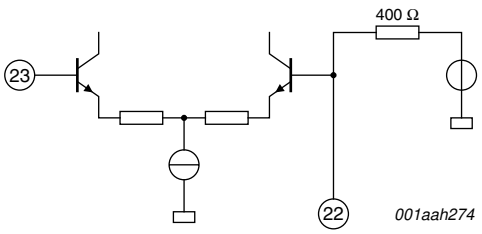
Pin	Symbol	Equivalent circuit
16	IF2FILQ	
17	IF2FILI	
18	MIX1OUT1	
19	MIX1OUT2	
20	V_{DDA2}	
21	SWFLAG	
22	AMMIX1DEC	
23	AMMIX1IN	

Table 31. Equivalent pin circuits *…continued*

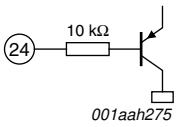
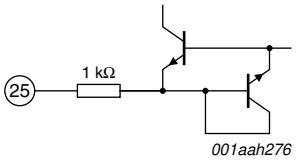
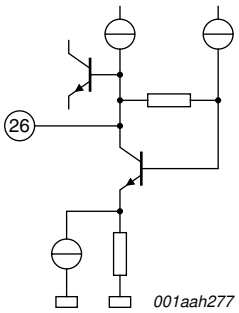
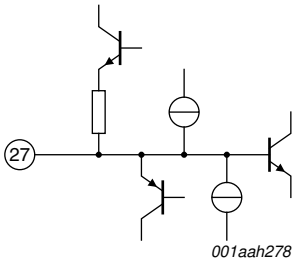
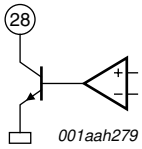
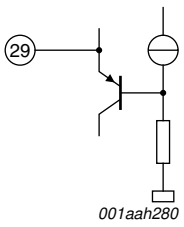
Pin	Symbol	Equivalent circuit
24	VAMCASFB	
25	VAMCAS	
26	TAFAMAGC	
27	THFAMAGC	
28	IAMAGC	
29	$V_{ref(MIX)}$	

Table 31. Equivalent pin circuits *…continued*

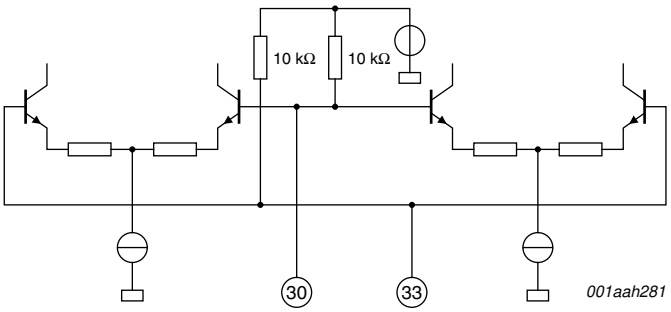
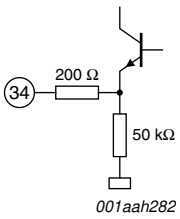
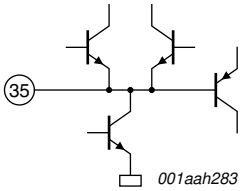
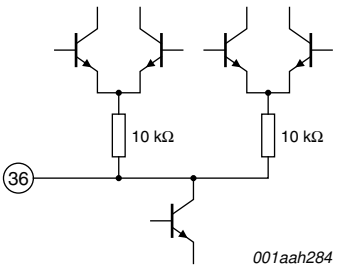
Pin	Symbol	Equivalent circuit
30	FMMIXIN1	
33	FMMIXIN2	
31	RFGND	
32	i.c.	
34	WBFLAG	
35	IFMAGC	
36	TFMAGC	

Table 31. Equivalent pin circuits *…continued*

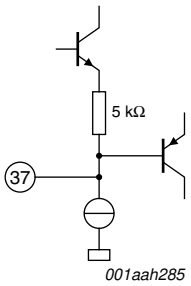
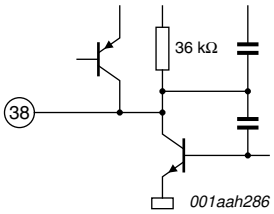
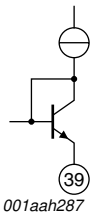
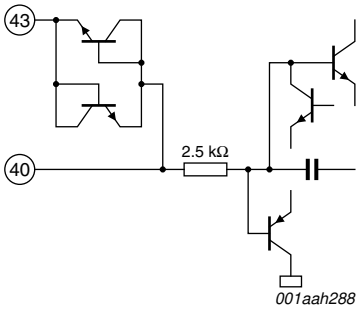
Pin	Symbol	Equivalent circuit
37	TKEYEDAGC	
38	DAAOUT	
39	DAATD	
40	DAAIN	
41	i.c.	

Table 31. Equivalent pin circuits *…continued*

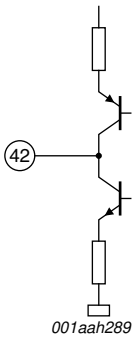
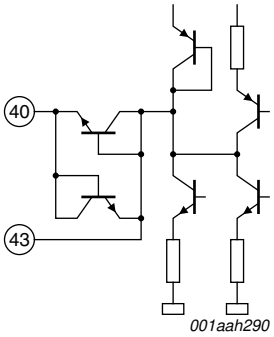
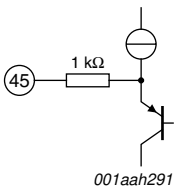
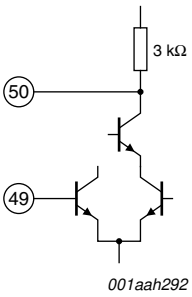
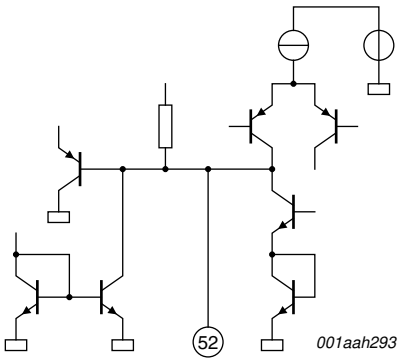
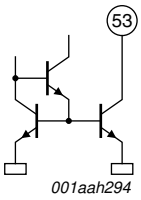
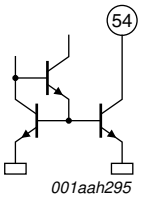
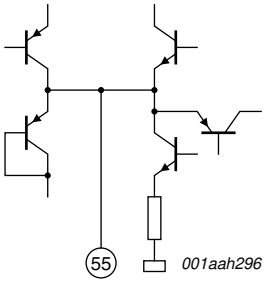
Pin	Symbol	Equivalent circuit
42	V_{tune}	
43	CPOUT	
44	V_{DDA3}	
45	FREF	
46	V_{DDD}	
47	DGND	
48	VCOGND	
49	OSCFDB	
50	OSCTNK	
51	V_{DDA4}	

Table 31. Equivalent pin circuits *…continued*

Pin	Symbol	Equivalent circuit
52	MPXDCFDB	
53	AFSAMPLE	
54	AFHOLD	
55	TRDSMUTE	
56	AMAFIF2