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# DATA SHEET



## **TEA6880H**

Up-level Car radio Analog Signal  
Processor (CASP)

Product specification  
Supersedes data of 2000 May 08

2003 Feb 04

# Up-level Car radio Analog Signal Processor (CASP)

## TEA6880H

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# Up-level Car radio Analog Signal Processor (CASP)

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## 1 FEATURES

### 1.1 General

- I<sup>2</sup>C-bus compatible
- Digital alignment/adjustment via I<sup>2</sup>C-bus:
  - FM noise blanker sensitivity
  - FM stereo noise canceller
  - FM High Cut Control (HCC)
  - FM stereo separation.
- FM audio processing hold for RDS updating; holds the detectors for the FM weak signal processing in their present state
- FM bandwidth limiting; limits the bandwidth of the FM audio signal with external capacitors
- AM stereo input; AM stereo audio can be fed in at the pins for the de-emphasis capacitors; this will provide 8 dB of gain to the AM audio.
- Volume 1 control from +20 to –56 dB in 1 dB steps; programmable 20 dB loudness control included
- Volume 2 control from 0 to –56 dB in 1 dB steps, –56, –58.5, –62, –68 dB and mute
- Programmable loudness control with bass boost as well as bass and treble boost
- Treble control from –14 to +14 dB in 2 dB steps
- Bass control from –18 to +18 dB in 2 dB steps with selectable characteristic
- Analog Step Interpolation (ASI) minimizes pops by smoothing out the transitions in the audio signal when a switch is made
- Audio Blend Control (ABC) minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings
- Rear Seat Audio (RSA) can select different sources for the front and rear speakers
- Chime input: can be sent to any audio output, at any volume level
- Chime adder circuit: chime input can also be summed with left front and/or right front audio, or be turned off



### 1.2 Stereo decoder and noise blanking

- FM stereo decoder
- Accepts FM multiplex signal and AM audio at input
- Pilot detector and pilot canceller
- De-emphasis selectable between 75 and 50  $\mu$ s
- AM noise blanker: impulse noise detector and an audio hold.

### 1.3 Weak signal processing

- FM weak signal processing: six signal condition detectors, soft mute, stereo noise canceller (blend) and high cut control (roll-off).

### 1.4 Audio pre-amplifier

- Source selector for 6 sources: 2 stereo inputs external (A and B), 1 symmetrical stereo input (C), 1 symmetrical mono input (D), 1 internal stereo input (AM or FM) and 1 chime/diagnostic mono input

## 2 GENERAL DESCRIPTION

The TEA6880H is a monolithic bipolar integrated circuit providing the stereo decoder function and ignition noise blanking facility combined with source selector and tone/volume control for AM/FM car radio applications. The device operates with a power supply voltage range from 7.8 to 9.2 V and a typical current consumption of 40 mA.

## 3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6880H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

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## 4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		7.8	8.5	9.2	V
$I_{CC}$	supply current		32	40	48	mA
<b>Stereo decoder path</b>						
S/N	signal-to-noise ratio		–	78	–	dB
THD	total harmonic distortion		–	0.1	–	%
$\alpha_{CS}$	channel separation		40	–	–	dB
$V_{o(rms)}$	output voltage level at pins ROPO and LOPO (RMS value)	FM: 91% modulation; AM: 100% modulation; $f_{mod} = 400$ Hz	840	950	1060	mV
<b>Tone/volume control</b>						
$V_{o(max)(rms)}$	maximum output voltage level at pins LF, LR, RF and RR (RMS value)	$V_{CC} = 8.5$ V; THD $\leq 0.1\%$	2000	–	–	mV
$G_V$	voltage gain	1 dB steps	–112	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
$G_{bass}$	bass control		–18	–	+18	dB
$G_{treble}$	treble control		–14	–	+14	dB
$G_{step(treble, bass)}$	step resolution (bass and treble)		–	2	–	dB
(S+N)/N	signal-plus-noise to noise ratio	$V_o = 2.0$ V; $G_V = 0$ dB; unweighted	–	107	–	dB
THD	total harmonic distortion	$V_{o(rms)} = 1.0$ V; $G_V = 0$ dB	–	0.01	–	%
RR <sub>100</sub>	ripple rejection	$V_{ripple(rms)} < 200$ mV; $f = 100$ Hz; $G_V = 0$ dB	–	70	–	dB
CMRR	common mode rejection ratio differential stereo input		48	53	–	dB

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### 5 BLOCK DIAGRAM

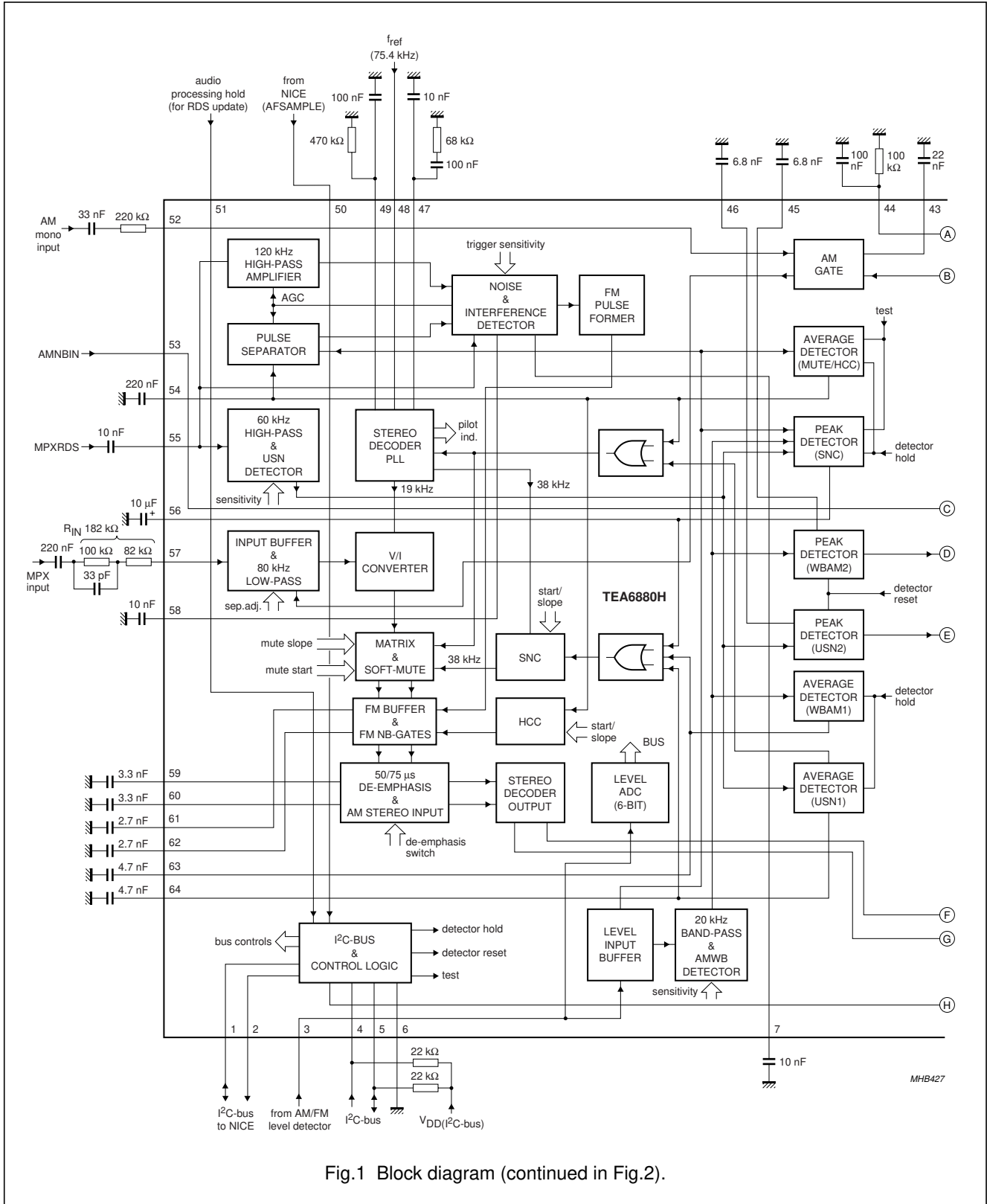


Fig.1 Block diagram (continued in Fig.2).

# Up-level Car radio Analog Signal Processor (CASP)

## TEA6880H

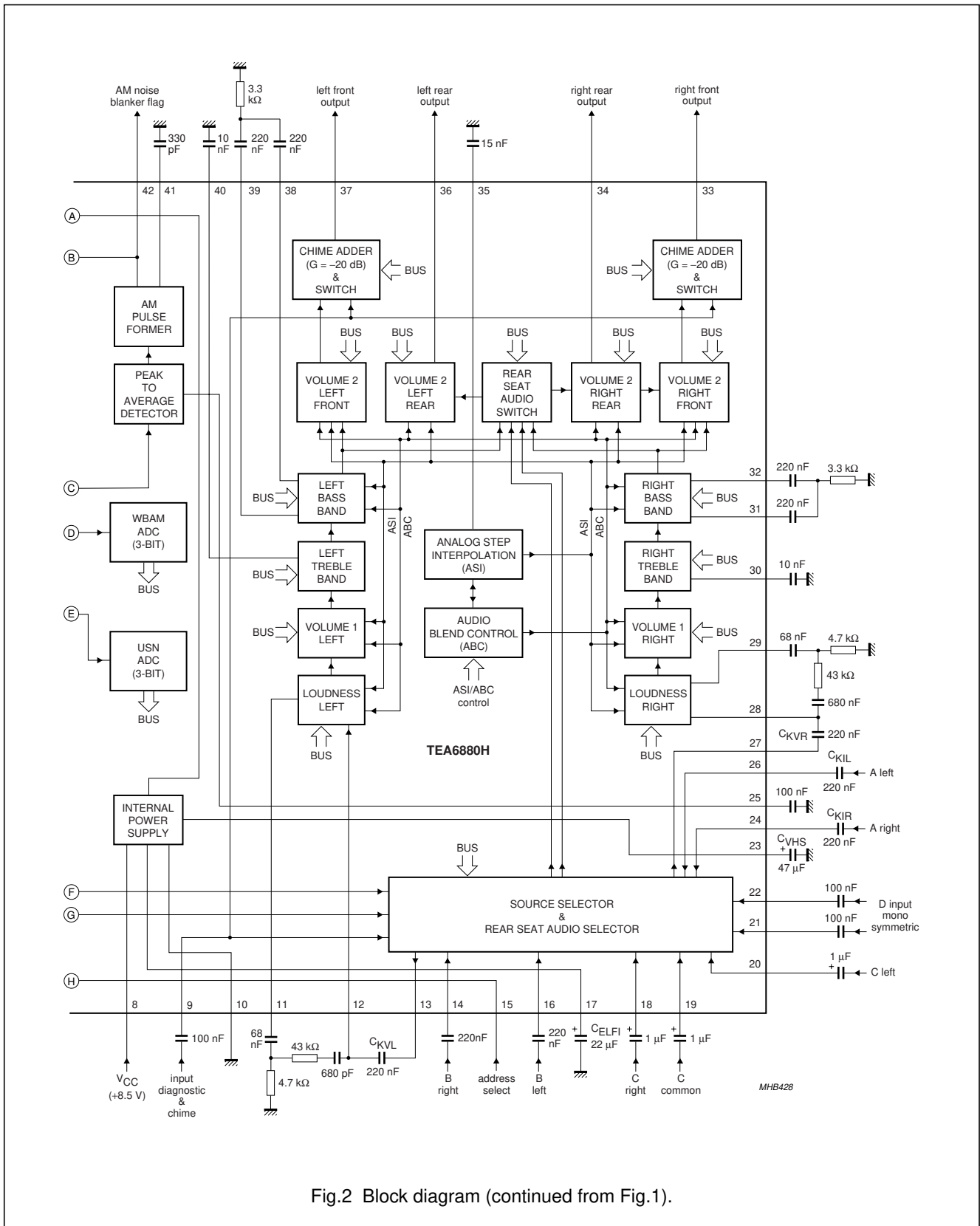


Fig.2 Block diagram (continued from Fig.1).

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## 6 PINNING

SYMBOL	PIN	DESCRIPTION
SDAQ	1	data output (to TEA6840H)
SCLQ	2	clock output (to TEA6840H)
LEVEL	3	FM and AM level input (from TEA6840H)
SCL	4	I <sup>2</sup> C-bus clock
SDA	5	I <sup>2</sup> C-bus data
DGND	6	digital ground
TBL	7	time constant for FM modulation detector
V <sub>CC</sub>	8	supply voltage
CHIME	9	chime tone input
AGND	10	analog ground
LLN	11	loudness left network
LOPI	12	left option port input (terminal impedance typical 100 k $\Omega$ )
LOPO	13	left option port output
BRI	14	channel B right stereo input (terminal impedance typical 100 k $\Omega$ )
ADR	15	address select
BLI	16	channel B left stereo input (terminal impedance typical 100 k $\Omega$ )
SCAP	17	supply filter capacitor
CRIP	18	channel C right symmetrical input (terminal impedance typical 30 k $\Omega$ )
CCOM	19	channel C common input (terminal impedance typical 30 k $\Omega$ )
CLIP	20	channel C left symmetrical input (terminal impedance typical 30 k $\Omega$ )
MONOC	21	mono common input (terminal impedance typical 30 k $\Omega$ )
MONOP	22	mono symmetrical input (terminal impedance typical 30 k $\Omega$ )
VHS	23	half supply filter capacitor
ARI	24	channel A right stereo input (terminal impedance typical 100 k $\Omega$ )
AMNCAP	25	peak-to-average detector capacitor for AM noise blanker
ALI	26	channel A left stereo input (terminal impedance typical 100 k $\Omega$ )
ROPO	27	right option port output
ROPI	28	right option port input (terminal impedance typical 100 k $\Omega$ )
RLN	29	loudness right network
RTC	30	right treble capacitor
RBI	31	right bass network input
RBO	32	right bass network output
RF	33	right front output
RR	34	right rear output
ASICAP	35	analog step interpolate capacitor
LR	36	left rear output
LF	37	left front output
LBO	38	left bass network output
LBI	39	left bass network input
LTC	40	left treble capacitor



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SYMBOL	PIN	DESCRIPTION
AMPCAP	41	AM blanking time capacitor
AMHOLD	42	AM noise blanker flag
AMHCAP	43	AM noise blanker hold capacitor
IREF	44	temperature independent reference current
TWBAM2	45	time constant for AM wideband peak detector
TUSN2	46	time constant for ultrasonic noise peak detector
PHASE	47	phase detector
FREF	48	frequency reference input (75.4 kHz from TEA6840H)
PILOT	49	pilot on/off output
AFSAMPLE	50	reset for multipath detector (from TEA6840H for RDS update)
FMHOLD	51	FM audio processing hold input (from TEA6840H for RDS update)
AMHIN	52	AM signal input (from TEA6840H)
AMNBIN	53	AM noise blanker input (from TEA6840H)
TMUTE	54	time constant for soft mute
MPXRDS	55	unmuted MPX input (from TEA6840H for RDS update)
TSNC	56	time constant for stereo noise canceller
MPXIN	57	MPX input (from TEA6840H)
FMNCAP	58	FM noise detector capacitor
DEEML	59	left de-emphasis capacitor
DEEMR	60	right de-emphasis capacitor
FMLBUF	61	left AM/FM audio buffer capacitor
FMRBUF	62	right AM/FM audio buffer capacitor
TWBAM1	63	time constant for AM wideband average detector
TUSN1	64	time constant for ultrasonic noise average detector

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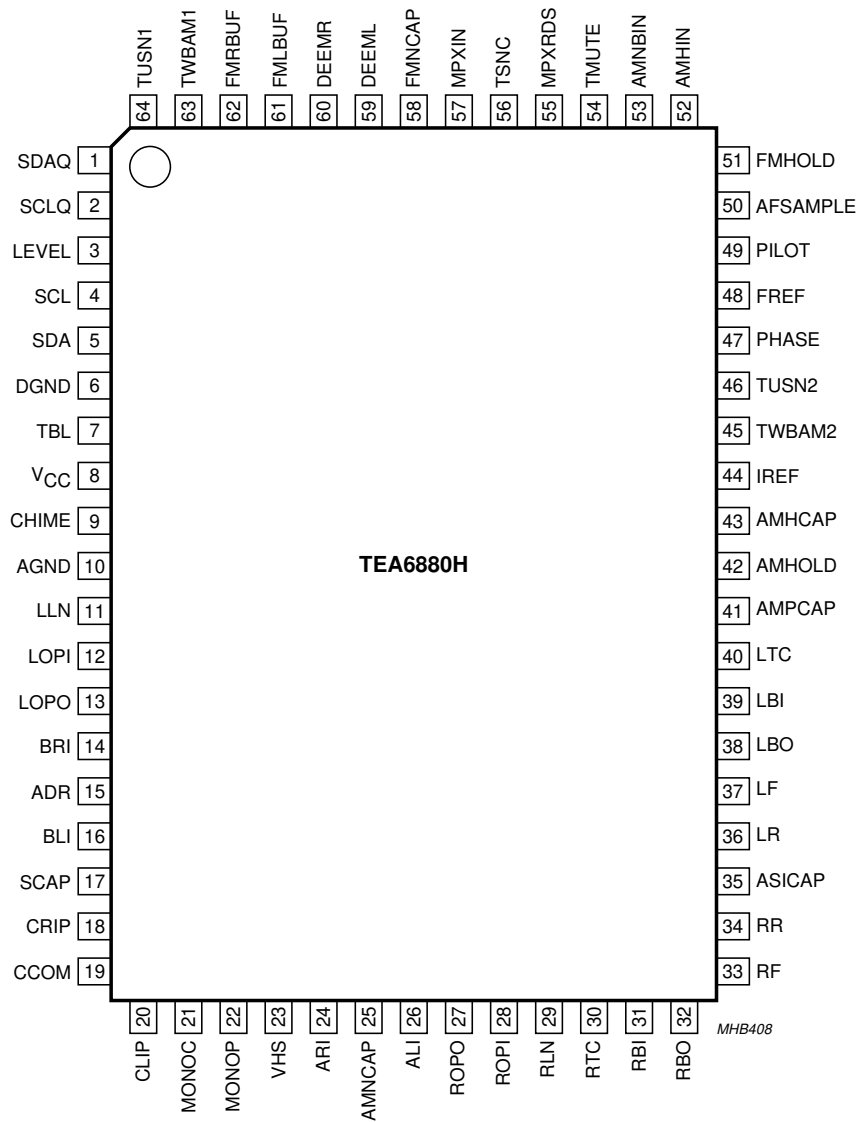


Fig.3 Pin configuration.

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### 7 FUNCTIONAL DESCRIPTION

#### 7.1 Stereo decoder

The MPX input is the null-node of an operational amplifier with internal feedback resistor. Adapting the stereo decoder input to the level of the MPX signal, coming from the FM demodulator output, is realized by the value of the input series resistor  $R_{IN}$ . To this input a second source (AM detector output) can be fed by current addition.

The input amplifier is followed by an integrated 4th order Bessel low-pass filter with a cut-off frequency of 80 kHz. It provides necessary signal delay for FM noise blanking and damping of high frequency interferences coming to the stereo decoder input.

Output of this filter is fed to the soft mute control circuitry, the output is voltage to current converted and then fed to phase detector, pilot detector and pilot canceller circuits, contained in the stereo decoder PLL block. For regeneration of the 38 kHz subcarrier, a PLL is used.

The fully integrated oscillator is adjusted by means of a digital auxiliary PLL into the capture range of the main PLL. The auxiliary PLL needs an external reference frequency (75.4 kHz) which is provided by the TEA6840H.

The required 19 and 38 kHz signals are generated by division of the oscillator output signal in a logical circuitry. The 19 kHz quadrature phase signal is fed to the 19 kHz phase detector, where it is compared with the incoming pilot tone. The DC output signal of the phase detector controls the oscillator (PLL).

The pilot presence detector is driven by an internally generated in-phase 19 kHz signal. Its pilot dependent DC output voltage is fed to a threshold switch, which activates the pilot indicator bit and turns the stereo decoder to stereo operation. The same DC voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. In the pilot canceller, the pilot tone is compensated by this anti-phase 19 kHz signal.

The pilot cancelled signal is fed to the matrix. There, the side signal is demodulated and combined with the main signal to left and right audio channel. Compensation for roll-off in the incoming MPX signal caused by IF filters and FM demodulator is typically realized by an external compensation network at pin MPXIN, individual alignment is achieved by I<sup>2</sup>C-bus controlled amplification of the side signal (DAA). A smooth mono to stereo takeover is achieved by controlling the efficiency of the matrix with help of the SNC peak detector.

The matrix is followed by the FM noise suppression gates, which are combined with FM single poles and High Cut Control (HCC).

The single pole is defined by internal resistors and external capacitors. From the gate circuits audio is fed to the switchable de-emphasis, where the demodulated AM stereo signal can be fed in. After de-emphasis the signal passes to the output buffers and is fed to the radio input of the source selector. For HCC, the time constant of the single pole contained in the output buffer can be changed to higher values. This function is controlled by an average detector contained in the multipath and fading detector.

#### 7.2 FM noise blanker

The input of the ignition noise blanker is coupled to the MPXRDS input signal and to the LEVEL input. Both signals are fed via separate 120 kHz filters and rectifiers to an adder circuit. The output signal of the adder circuit is fed in parallel to the noise detector and the interference detector. The noise detector is a negative peak detector. Its output controls the trigger sensitivity (prevention to false triggering at noisy input signals) and the gain of the MPX high-pass filter. The output of the interference detector, when receiving a steep pulse, fires a monoflop, contained in the pulse former circuitry. The time constant of the monoflop is defined by an internal capacitor and its output activates the blanking gates in the audio.

#### 7.3 AM noise blanker

The AM noise blanking pulse is derived from the AM audio signal which is fed into pin AMNBIN with the help of a peak-to-average comparator. The blanking time is set by a pulse former with external capacitor. The blanking pulse is fed to the gate in the AM audio path and out to pin AMHOLD to operate the gate built into the external AM stereo processor.

#### 7.4 Multipath/fading detection and weak signal control

For FM signal quality dependent controls there is built-in a combination of six detectors driven by the level information direct, by the AC components on the level via a 20 kHz band-pass filter (AM wideband) or the high notes present at the FM demodulator output via a 60 kHz high-pass filter (ultrasonic noise). The relation between DC level and the AC components is programmable by the I<sup>2</sup>C-bus (2 bits each). Output of level buffer, AM wideband detector and ultrasonic noise detector are analog-to-digital converted and readable by the I<sup>2</sup>C-bus.

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For the time of fast RDS updating soft mute, SNC and HCC can be put on hold and the AM wideband peak detector and the ultrasonic noise peak detector are put on reset by a switch signal delivered from the TEA6840H via pin FMHOLD.

The six separate detecting circuits are:

1. The AM wideband noise peak detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor at pin TWBAM2. The output voltage of the detector is analog-to-digital converted by 3-bit.
2. The AM wideband noise average detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor at pin TWBAM1. The output of the detector is connected to the Stereo Noise Control (SNC) circuit.
3. The ultrasonic noise peak detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor at pin TUSN2. The output voltage of the detector is analog-to-digital converted by 3-bit.
4. The ultrasonic noise average detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor at pin TUSN1. The output of the detector is connected to soft mute control and stereo noise control circuits.
5. For soft mute and high cut control purposes an average detector with externally defined time constant (TMUTE) is provided. The detector is driven by level output only. Soft mute as well as high cut control can be switched off by the I<sup>2</sup>C-bus.
6. The stereo noise control peak detector with externally defined time constant (TSNC) is driven by DC level output, AM wideband and ultrasonic noise outputs. It provides the stereo blend facility (SNC). Starting point and slope of stereo blend can be chosen by the I<sup>2</sup>C-bus controlled reference voltage.

### 7.5 Tone/volume control

The tone/volume control part consists of the following functions:

- Source selector
- Loudness
- Volume 1
- Treble
- Bass
- Volume 2
- Rear Seat Audio (RSA) selector
- Chime adder
- Analog step interpolation
- Audio blend control.

The stages loudness, volume 1, bass and volume 2 include the Analog Step Interpolation (ASI) function. This minimizes pops by smoothing out the transitions in the audio signal during switching. The transition time is I<sup>2</sup>C-bus programmable in a range of 1 : 24 in four steps.

The stages loudness, volume 1 and volume 2 also have the Audio Blend Control (ABC) function. This minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings. The speed of the ABC function is correlated with the transition time of the ASI function.

All stages are controlled via the I<sup>2</sup>C-bus.

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### 7.5.1 SOURCE SELECTOR

The source selector allows the selection between 6 sources:

- 2 external stereo inputs (ALI, ARI, BLI and BRI)
- 1 external symmetrical stereo input (CLIP, CRIP and CCOM)
- 1 external symmetrical mono input (MONOP and MONON)
- 1 internal stereo input (AM/FM)
- 1 chime/diagnostic mono input (CHIME).

Via the chime/diagnostic mono input a chime input signal can be sent to any audio output, at any volume level.

### 7.5.2 LOUDNESS

The output of the source selector is fed into the loudness circuit via the external capacitors  $C_{KVL}$  (pins LOPO and LOPI) and  $C_{KVR}$  (pins ROPO and ROPI). Depending on the external circuits for the left and the right channel only a bass boost or bass and treble boost is available. With the external circuits shown in Figs 13 and 15 the curves from Figs 14 and 16 will be obtained (without influence of  $C_{KVL}$  respectively  $C_{KVR}$ ).

### 7.5.3 VOLUME 1

The volume 1 control follows behind the loudness circuit. The control range of volume 1 is between +20 and -36 dB in steps of 1 dB.

### 7.5.4 TREBLE

The output signal of the volume 1 control is fed into the treble control stage. The control range is between +14 and -14 dB in steps of 2 dB. Fig.20 shows the control characteristic with external capacitors of 10 nF.

### 7.5.5 BASS

The bass control is the next stage. The characteristic of the bass curves depends upon the external circuits connected to pins LBO and LBI (left channel) and pins RBO and RBI (right channel) and also upon the setting of bit BSYM (MSB of the bass control byte). When BSYM = 1, an equalizer characteristic is obtained and when BSYM = 0, a shelving characteristic is obtained.

Figures 17 and 18 show the bass curves with an external circuit of  $2 \times 220$  nF capacitors and a resistor of 3.3 k $\Omega$  for each channel with different values for BSYM. Figure 19 shows the bass curves with an external capacitor of 47 nF for each channel and BSYM = 0, for boost and cut.

### 7.5.6 VOLUME 2

The four volume 2 blocks are located at the end of the tone/volume control. In addition to volume control (same settings as volume 2) also the balance and fader functions are performed by individual attenuation offsets for the four attenuators. The control range of these attenuators is 56 dB in steps of 1 dB and additional the steps -58.5 dB, -62 dB, -68 dB and a mute step.

### 7.5.7 RSA SELECTOR

The RSA selector provides the possibility to select an alternative source for the rear channels. In this event rear channels are only controlled by volume 2 function.

### 7.5.8 CHIME ADDER

With the chime adder circuit the chime input signal can be summed with the left front and/or right front audio, or be turned off.

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## 8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.3	+10	V
$V_i$	voltage at all pins (except SCL and SDA)	$V_{CC} \leq 10$ V	$V_{SS} - 0.3$	$V_{CC}$	V
	voltage at pins SCL and SDA		$V_{SS} - 0.3$	9.7	V
$P_{tot}$	total power dissipation		-	480	mW
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$V_{es}$	electrostatic handling voltage for all pins	note 1	-200	+200	V
		note 2	-2000	+2000	V

### Notes

1. Machine model ( $R = 0 \Omega$ ,  $C = 200$  pF).
2. Human body model ( $R = 1.5$  k $\Omega$ ,  $C = 100$  pF).

## 9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	48	K/W

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### 10 CHARACTERISTICS

FM part: input signal  $V_{i(\text{MPX})(\text{p-p})} = 1.89 \text{ V}$ ;  $m = 100\%$  ( $\Delta f = \pm 75 \text{ kHz}$ ,  $f_{\text{mod}} = 400 \text{ Hz}$ ); de-emphasis of  $75 \mu\text{s}$  and series resistor at input  $R_{\text{IN}} = 182 \text{ k}\Omega$ ; FM audio measurements are taken at pins LOPO and ROPO.

Tone part:  $R_{\text{S}} = 600 \Omega$ ;  $R_{\text{L}} = 10 \text{ k}\Omega$ , AC-coupled;  $C_{\text{L}} = 2.5 \text{ nF}$ ; CLK = square-wave (5 to 0 V) at 100 kHz; stereo source = A channel input; volume 1 attenuator = 0 dB; loudness = 0 dB, off; volume 2 attenuators = 0 dB; bass linear; treble linear; input voltage = 1 V,  $f = 1 \text{ kHz}$ . Tone part audio measurements are taken at pins RF and LF.  $V_{\text{CC}} = 8.3 \text{ to } 8.7 \text{ V}$ ;  $V_{\text{SS}} = 0 \text{ V}$ ;  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified.

This IC shall not radiate noise in the audio system such that it disturbs any other circuit. This IC shall also not be susceptible to the radiation of any other circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{CC}}$	supply voltage		7.8	8.5	9.2	V
$I_{\text{CC}}$	supply current	$V_{\text{CC}} = 8.5 \text{ V}$	32	40	48	mA
$V_{\text{HS}}$	half supply voltage	$V_{\text{CC}} = 8.5 \text{ V}$	3.75	4.25	4.75	V
$I_{\text{REF}}$	reference current	$V_{\text{CC}} = 8.5 \text{ V}$ ; $R_{\text{IREF}} = 100 \text{ k}\Omega$	35	37	39	$\mu\text{A}$
<b>FM signal path</b>						
$V_{i(\text{MPX})(\text{p-p})}$	MPX input signal (peak-to-peak value)	$R_{\text{i}} = 182 \text{ k}\Omega$	–	1.89	–	V
$\Delta V_{i(\text{MPX})}$	overdrive margin of MPX input signal	THD = 1%	6	–	–	dB
$I_{\text{i}}$	AF input current		–	3.66	–	$\mu\text{A}$
$I_{\text{i(max)}}$	maximum AF input current	THD = 1%	7.32	–	–	$\mu\text{A}$
$V_{\text{o(rms)}}$	AF mono output signal (RMS value)	91% modulation without pilot	890	1000	1110	mV
$\Delta V_{\text{out}}$	AF mono channel balance	without pilot; $V_{\text{LOPO}}/V_{\text{ROPO}}$	–1	–	+1	dB
$\alpha_{\text{cs}}$	channel separation	aligned setting of data byte 1, bit 0 to bit 3; $m = 30\%$ modulation plus 9% pilot				
		$L = 1$ ; $R = 0$	40	47	70	dB
		$L = 0$ ; $R = 1$	40	47	70	dB
THD	total harmonic distortion	$V_{i(\text{MPX})(\text{p-p})} = 1.89 \text{ V}$ ; $f_{\text{mod}} = 1 \text{ kHz}$ without pilot	–	0.1	0.3	%
		$V_{i(\text{MPX})(\text{p-p})} = 1.89 \text{ V}$ ; $f_{\text{mod}} = 5 \text{ kHz}$	–	0.1	0.3	%
		$L = 1$ ; $R = 0$	–	0.1	0.3	%
		$L = 0$ ; $R = 1$	–	0.1	0.3	%
S/N	signal-to-noise ratio	$f = 20 \text{ Hz to } 15 \text{ kHz}$	75	78	–	dB
$\alpha_{19}$	pilot signal suppression	$f = 19 \text{ kHz}$	40	50	–	dB
$\alpha_{38}$	subcarrier suppression	$f = 38 \text{ kHz}$	35	50	–	dB
$\alpha_{57}$		$f = 57 \text{ kHz}$	40	–	–	dB
$\alpha_{76}$		$f = 76 \text{ kHz}$	50	60	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IM2	second order intermodulation for $f_{\text{spur}} = 1 \text{ kHz}$	$f_{\text{mod}} = 10 \text{ kHz}$ ; note 1	–	60	–	dB
IM3	third order intermodulation for $f_{\text{spur}} = 1 \text{ kHz}$	$f_{\text{mod}} = 13 \text{ kHz}$ ; note 1	–	58	–	dB
$\alpha_{57(\text{RDS})}$	traffic radio (RDS)	$f = 57 \text{ kHz}$ ; note 2	–	70	–	dB
$\alpha_{67}$	Subsidiary Communication Authorization (SCA)	$f = 67 \text{ kHz}$ ; note 3	70	–	–	dB
$\alpha_{114}$	Adjacent Channel Interference (ACI)	$f = 114 \text{ kHz}$ ; note 4	–	80	–	dB
$\alpha_{190}$		$f = 190 \text{ kHz}$ ; note 4	–	70	–	dB
PSRR	power supply ripple rejection	$f = 100 \text{ Hz}$ ; $V_{\text{ripple(rms)}} = 100 \text{ mV}$	–	30	–	dB
$R_{\text{SDEEML}}$ ; $R_{\text{SDEEMR}}$	de-emphasis output source resistance	data byte 3, bit 5 = 1; $75 \mu\text{s}$	20	22.7	25.4	$\text{k}\Omega$
		data byte 3, bit 5 = 0; $50 \mu\text{s}$	13.4	15.2	17	$\text{k}\Omega$
$I_{\text{FMLBUF}}$ ; $I_{\text{FMRBUF}}$	current capacity of FM buffer	$V_{\text{FMLBUF,FMRBUF}} = 5.5 \pm 1 \text{ V}$	50	–	200	$\mu\text{A}$
<b>PLL VCO</b>						
$f_{\text{osc}}$	oscillator frequency		–	228	–	kHz
	frequency range of free running oscillator		190	–	270	kHz
$f_{\text{ref}}$	reference frequency at pin FREF		–	75.4	–	kHz
$V_{i(\text{FREF})}$	reference frequency input voltage		30	100	500	mV
$Z_{i(\text{FREF})}$	input impedance		100	–	–	$\text{k}\Omega$
<b>PLL pilot detector</b>						
$V_{i(\text{pilot})(\text{rms})}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)	stereo on; STIN = 1	–	27	37	mV
		stereo off; STIN = 0	9	22	–	mV
$h_{\text{YS}(\text{pilot})}$	hysteresis of pilot threshold voltage		–	2	–	dB
$V_{\text{PILOT}}$	switching voltage for external mono control (PILOT)		0.3	–	0.7	V
<b>AM signal path</b>						
$V_{\text{LOPO}}$ ; $V_{\text{ROPO}}$	AC output voltage at pins LOPO and ROPO	$\text{AMON} = 1$ and $\text{AMST} = 0$ ; $R_i = 220 \text{ k}\Omega$ ; $V_{i\text{AM}(\text{mono})} = 250 \text{ mV}$	195	245	295	mV
$G_{\text{V}}$	AM stereo audio buffer voltage gain	subaddress 0H: $\text{AMON} = 1$ and $\text{AMST} = 1$ ; input signal at pins DEEML or DEEMR; coupled with $220 \text{ nF}$ ; $V_{i(\text{DEEML,DEEMR})} = 200 \text{ mV}$ ; $f_i = 1 \text{ kHz}$ ; note 5	7	8	9	dB
$R_{i(\text{DEEML})}$ ; $R_{i(\text{DEEMR})}$	input resistance for AM stereo left and right	$\text{AMON} = 1$ and $\text{AMST} = 1$ ; note 6	80	100	120	$\text{k}\Omega$



## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Noise blanker</b>						
FM PART						
$t_{\text{sup}}$	interference suppression time		20	30	40	$\mu\text{s}$
$I_{\text{offset}}$	gate input offset current at pins during suppression pulse duration	during AF suppression time	–	20	50	nA
$I_{\text{ch}}(\text{FMNCAP})$	charge current (into 4 V)	no input signal; $V_{\text{FMNCAP}} = V_{\text{FMNCAP}(\text{int})} - 0.7 \text{ V}$	–16	–12.5	–9.5	$\mu\text{A}$
$I_{\text{dch}}(\text{FMNCAP})$	discharge current (from 5.5 V)	no input signal; $V_{\text{FMNCAP}} = V_{\text{FMNCAP}(\text{int})} + 0.7 \text{ V}$	45	70	100	$\mu\text{A}$
<i>Trigger Threshold Control (TTC), dependency on MPX signal at MPXRDS input</i>						
$V_{\text{FMNCAP}}$	trigger threshold variation voltage	$V_{i(\text{MPXRDS})} = 0 \text{ V}$	4.5	5	5.5	V
$\Delta V_{\text{FMNCAP}}$	trigger threshold voltage	$V_{i(\text{MPXRDS})} = 10 \text{ mV}; f = 120 \text{ kHz}$	15	40	60	mV
		$V_{i(\text{MPXRDS})} = 100 \text{ mV}; f = 120 \text{ kHz}$	75	100	200	mV
$\Delta V_{\text{TBL}}$	trigger threshold variation with audio frequency $f = 15 \text{ kHz}$	$V_{i(\text{MPXRDS})} = 670 \text{ mV}$	–	500	–	mV
<i>Trigger Threshold Control (TTC), dependency on level detector input signal</i>						
$V_{\text{FMNCAP}}$	trigger threshold voltage	$V_{\text{LEVEL}(\text{AC})} = 0 \text{ V}$	4.5	5	5.5	V
$\Delta V_{\text{FMNCAP}}$	trigger threshold voltage as a function of $V_{\text{LEVEL}(\text{AC})}$	$V_{\text{LEVEL}(\text{AC})} = 10 \text{ mV}; f = 120 \text{ kHz}$	–	0	–	mV
		$V_{\text{LEVEL}(\text{AC})} = 200 \text{ mV}; f = 120 \text{ kHz}$	–	40	–	mV
<i>Trigger sensitivity measurement with pulse (on MPX signal) at MPXRDS input</i>						
$V_{\text{pulse}}$	trigger sensitivity	$t_{\text{pulse}} = 10 \mu\text{s}$ ; write mode; data byte 3, bits 6 and 7: NBS1 = 0; NBS0 = 0	–	60	–	mV
		NBS1 = 0; NBS0 = 1	–	100	–	mV
		NBS1 = 1; NBS0 = 0	–	150	–	mV
		NBS1 = 1; NBS0 = 1	–	200	–	mV
<i>Trigger sensitivity measurement with pulse (on level signal) at AM/FM level input</i>						
$V_{\text{pulse}}$	trigger sensitivity	$t_{\text{pulse}} = 10 \mu\text{s}$ ; $V_{\text{LEVEL}} = 0.5 \text{ V}$ ; write mode; data byte 3, bits 6 and 7: NBS1 = 0; NBS0 = 0	–	250	–	mV
		NBS1 = 0; NBS0 = 1	–	275	–	mV
		NBS1 = 1; NBS0 = 0	–	300	–	mV
		NBS1 = 1; NBS0 = 1	–	320	–	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>AM PART</b>						
$m_{\text{mod}}$	trigger threshold		–	140	–	%
$V_{\text{AMPCAP(AC)}}$	AF voltage at AMHCAP	$V_{\text{iAM(mono)}} = 50 \text{ mV (RMS)}$ ; $f = 1 \text{ kHz}$	16	22	30	mV
$\alpha_{\text{AMGATE}}$	attenuation of blanking gate	$V_{\text{iAM(mono)}} = 50 \text{ mV (RMS)}$ ; gate open: internal voltage; gate closed: $V_{\text{AMHOLD(DC)}} = 4 \text{ V}$ ; note 7	–60	–70	–80	dB
$t_{\text{sup(AMHOLD)}}$	suppression time at AMHOLD	$t_{\text{pulse}} = 10 \text{ }\mu\text{s}$ ; repetition rate = 50 Hz; $V_{\text{pulse}} = 1.7 \text{ V}$ (AMNBIN); $V_{\text{LEVEL}} = 0.5 \text{ V}$	400	500	600	$\mu\text{s}$
$V_{\text{AMNCAP(DC)}}$	detector voltage; $V_{\text{ext(AMNBIN)DC}} - 0.7 \text{ V}$	$V_{\text{AMNBIN(AC)}} = 0 \text{ V}$ ; $V_{\text{LEVEL(DC)}} = 3.5 \text{ V}$	3.3	3.8	4.3	V
$f_{\text{AMHOLD}}$	trigger sensitivity	$t_{\text{pulse}} = 10 \text{ }\mu\text{s}$ ; repetition rate = 50 Hz; $V_{\text{pulse}} = 1.7 \text{ V}$ (AMNBIN); $V_{\text{LEVEL}} = 4 \text{ V}$	45	50	55	Hz
$I_{\text{offset}}$	gate input offset current at pins during suppression pulse duration	during AF suppression time	–50	0	+50	nA
<b>Muting average detector (TMUTE); see Fig.12</b>						
$V_{\text{i(LEVEL)}}$	input voltage on LEVEL		0.5	–	4	V
$G_{\text{v}}$	voltage gain LEVEL to TMUTE		–	0	–	dB
$\Delta V_{\text{TMUTE}}$	offset between TMUTE and LEVEL		–	1.5	–	V
$\Delta V_{\text{TMUTE/K}}$	temperature dependence at TMUTE		–	3.3	–	mV/K
<b>MUTING AVERAGE DETECTOR TIME CONSTANT</b>						
$I_{\text{ch(TMUTE)}}$	TMUTE charge current		–	–0.2	–	$\mu\text{A}$
$I_{\text{dch(TMUTE)}}$	TMUTE discharge current		–	0.2	–	$\mu\text{A}$
$V_{\text{O}}$	DC output voltage		2	–	5	V
<b>TEST CONDITION</b>						
$I_{\text{ch(test)}}$	capacitor charge current	data byte 6, bit 7 = 1	–	–12	–	$\mu\text{A}$
$I_{\text{dch(test)}}$	capacitor discharge current	data byte 6, bit 7 = 1	–	12	–	$\mu\text{A}$

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>AM wideband average detector (TWBAM1); see Fig.6</b>						
$V_{TWBAM1}$	DC voltage at TWBAM1 with respect to AGND	$V_{LEVEL(AC)} = 400 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 24 \text{ kHz}$ ; write mode; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
$V_{CTWBAM1}$	DC voltage coefficient	$V_{LEVEL(AC)} = 400 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 24 \text{ kHz}$ ; write mode; note 8; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
$V_O$	DC output voltage		1.5	–	5.5	V
<b>AM WIDEBAND AVERAGE DETECTOR TIME CONSTANT</b>						
$I_{ch(TWBAM1)}$	TWBAM1 charge current		–19.5	–15	–11.5	$\mu\text{A}$
$I_{dch(TWBAM1)}$	TWBAM1 discharge current		11.5	15	19.5	$\mu\text{A}$
<b>Ultrasonic noise average detector (TUSN1); see Fig.5</b>						
$V_{TUSN1}$	DC voltage at TUSN1 with respect to AGND	$V_{MPXRDS(AC)} = 350 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 80 \text{ kHz}$ ; write mode; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
$V_{CTUSN1}$	DC voltage coefficient	$V_{MPXRDS(AC)} = 350 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 80 \text{ kHz}$ ; write mode; note 9; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
$V_O$	DC output voltage		1.5	–	5.5	V

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ULTRASONIC NOISE AVERAGE DETECTOR TIME CONSTANT						
$I_{ch}(TUSN1)$	TUSN1 charge current		-19.5	-15	-11.5	$\mu\text{A}$
$I_{dch}(TUSN1)$	TUSN1 discharge current		11.5	15	19.5	$\mu\text{A}$
<b>Peak detector for stereo noise control (TSNC)</b>						
DEPENDENCY ON LEVEL VOLTAGE; see Fig.12						
$V_{LEVEL}$	input voltage		0.5	-	4.75	V
G	gain LEVEL to TSNC		-	0	-	dB
$V_{TSNC}$	DC voltage at TSNC referred to DC level voltage at LEVEL	without MPXRDS and LEVEL (AC) input $V_{LEVEL(DC)} = 0.5 \text{ V}$ $V_{LEVEL(DC)} = 3.5 \text{ V}$	1.75 4.50	2.00 5.00	2.25 5.50	V V
$\Delta V_{TSNC/K}$	temperature dependence at TSNC		-	3.3	-	mV/K
DEPENDENCY ON ULTRASONIC NOISE; see Fig.5						
$V_{TSNC}$	DC voltage at TSNC with respect to AGND	$V_{MPXRDS(AC)} = 350 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 80 \text{ kHz}$ ; write mode; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1 USS1 = 1; USS0 = 0 USS1 = 0; USS0 = 1 USS1 = 0; USS0 = 0	- - - -	4.25 4.00 3.50 2.60	- - - -	V V V V
$V_{C_{TSNC}}$	DC voltage coefficient	$V_{MPXRDS(AC)} = 350 \text{ mV}$ ; $V_{LEVEL(DC)} = 3.5 \text{ V}$ ; $f_i = 80 \text{ kHz}$ ; write mode; note 10; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1 USS1 = 1; USS0 = 0 USS1 = 0; USS0 = 1 USS1 = 0; USS0 = 0	0.71 0.67 0.60 0.44	0.85 0.80 0.70 0.52	1.00 0.95 0.85 0.62	
$V_O$	DC output voltage		2	-	5	V

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEPENDENCY ON AM WIDEBAND NOISE; see Fig.6						
V <sub>TSNC</sub>	DC voltage at TSNC	V <sub>LEVEL(AC)</sub> = 400 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 24 kHz; write mode; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
V <sub>C<sub>TSNC</sub></sub>	DC voltage coefficient	V <sub>LEVEL(AC)</sub> = 400 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 24 kHz; write mode; note 11; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V <sub>O</sub>	DC output voltage		1.5	–	5.5	V
DETECTOR TIME CONSTANT						
I <sub>ch(TSNC)</sub>	TSNC charge current		–	–2.3	–	μA
I <sub>dch(TSNC)</sub>	TSNC discharge current		–	65	–	μA
TEST CONDITION						
I <sub>ch(test)</sub>	charge current for testing	data byte 6, bit 7 = 1; V <sub>LEVEL(DC)</sub> = 2 V; V <sub>TSNC(DC)</sub> = 2.8 V	–	–1.5	–	mA
I <sub>dch(test)</sub>	discharge current for testing	data byte 6, bit 7 = 1; V <sub>LEVEL(DC)</sub> = 2 V; V <sub>TSNC(DC)</sub> = 4.2 V	–	200	–	μA

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Ultrasonic noise peak detector (TUSN2); see Fig.5</b>						
V <sub>TUSN2</sub>	DC voltage at TUSN2 with respect to AGND	V <sub>MPXRDS(AC)</sub> = 350 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 80 kHz; write mode; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
V <sub>CTUSN2</sub>	DC voltage coefficient	V <sub>MPXRDS(AC)</sub> = 350 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 80 kHz; write mode; note 12; data byte 1, bits 6 and 7: USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
V <sub>O</sub>	DC output voltage		1.5	–	5.5	V
<b>DETECTOR TIME CONSTANT</b>						
I <sub>ch(TUSN2)</sub>	TUSN2 charge current		–	–1.6	–	μA
I <sub>dch(TUSN2)</sub>	TUSN2 discharge current		–	21	–	μA
<b>AM wideband peak detector (TWBAM2); see Fig.6</b>						
V <sub>TWBAM2</sub>	DC voltage at TWBAM2 with respect to AGND	V <sub>LEVEL(AC)</sub> = 400 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 24 kHz; write mode; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
V <sub>CTWBAM2</sub>	DC voltage coefficient	V <sub>LEVEL(AC)</sub> = 400 mV; V <sub>LEVEL(DC)</sub> = 3.5 V; f <sub>i</sub> = 24 kHz; write mode; note 13; data byte 1, bits 4 and 5: AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V <sub>O</sub>	DC output voltage		2	–	5	V

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DETECTOR TIME CONSTANT						
$I_{ch(TWBAM2)}$	TWBAM2 charge current		–	–1.6	–	$\mu\text{A}$
$I_{dch(TWBAM2)}$	TWBAM2 discharge current		–	21	–	$\mu\text{A}$
<b>Soft mute;</b> see Figs 7 and 4						
$\alpha_{0\text{dB}}$	attenuation at LOPO and ROPO	$V_{\text{TMUTE}} = 3.5 \text{ V}; V_{\text{TUSN1}} = 3.5 \text{ V}$	–0.5	0	+0.5	dB
$\alpha_{6\text{dB}}$	start of muting; AC attenuation at LOPO and ROPO	see Fig.4; write mode; MSL0 = 1; MSL1 = 1				
		MST1 = 0; MST0 = 0; $V_{\text{TMUTE}} = 0.42V_{\text{TUSN1}}$ without AC	3	6	9	dB
		MST1 = 0; MST0 = 1; $V_{\text{TMUTE}} = 0.45V_{\text{TUSN1}}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 0; $V_{\text{TMUTE}} = 0.47V_{\text{TUSN1}}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 1; $V_{\text{TMUTE}} = 0.49V_{\text{TUSN1}}$ without AC	3	6	9	dB
$\alpha_{10\text{dB}}$	AC attenuation for setting of mute slope at LOPO and ROPO	MST1 = 0; MST0 = 0; see Fig.7				
		MSL1 = 0; MSL0 = 0; $V_{\text{TMUTE(DC)}} = 0.35V_{\text{TUSN1}}$ without AC	7	10	13	dB
		MSL1 = 0; MSL0 = 1; $V_{\text{TMUTE(DC)}} = 0.38V_{\text{TUSN1}}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 0; $V_{\text{TMUTE(DC)}} = 0.39V_{\text{TUSN1}}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 1; $V_{\text{TMUTE(DC)}} = 0.395V_{\text{TUSN1}}$ without AC	7	10	13	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Stereo Noise Control (SNC)</b>						
$\alpha_{cs(start)}$	start of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1111; $V_{TSNC}$ or $V_{TUSN1}$ or $V_{TWBAM1} = 0.63V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; $V_{TSNC}$ or $V_{TUSN1}$ or $V_{TWBAM1} = 0.70V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 0000; $V_{TSNC}$ or $V_{TUSN1}$ or $V_{TWBAM1} = 0.74V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
$\alpha_{cs(slope)}$	slope of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; $V_{TSNC} = 0.72V_{TUSN1}$ without AC; see note 15 and Fig.8; data byte 2, bits 4 and 5:				
		SSL1 = 0; SSL0 = 0	3	5	7	dB
		SSL1 = 0; SSL0 = 1	5	7	9	dB
		SSL1 = 1; SSL0 = 0	11	13	15	dB
		SSL1 = 1; SSL0 = 1 (not defined)				



## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>High Cut Control (HCC)</b>						
$\alpha_{\text{HCC(start)}}$	AC attenuation for start of HCC	AF = 10 kHz; $V_{\text{MPXIN}} = 200$ mV; HSL1 = 1; HSL0 = 0; data byte 0, SMUT = 0 and MONO = 1; write mode; see note 16 and Fig.10; data byte 3, bits 2 and 3: HST1 = 1; HST0 = 1; $V_{\text{LEVEL(DC)}} = 1.30$ V HST1 = 1; HST0 = 0; $V_{\text{LEVEL(DC)}} = 1.45$ V HST1 = 0; HST0 = 1; $V_{\text{LEVEL(DC)}} = 1.90$ V HST1 = 0; HST0 = 0; $V_{\text{LEVEL(DC)}} = 2.10$ V	1.5	3	4.5	dB
			1.5	3	4.5	dB
			1.5	3	4.5	dB
			1.5	3	4.5	dB
$\alpha_{\text{HCC(slope)}}$	AC attenuation for slope of HCC	AF = 10 kHz; $V_{\text{MPXIN}} = 200$ mV; $C_{\text{FMLBUF}}, C_{\text{FMRBUF}} = 2.7$ nF; HST1 = 1; HST0 = 1; data byte 0, SMUT = 0 and MONO = 1; see note 16 and Fig.11; data byte 3, bits 0 and 1: HSL1 = 1; HSL0 = 1 HSL1 = 1; HSL0 = 0 HSL1 = 0; HSL0 = 1 HSL1 = 0; HSL0 = 0	5.5	7.5	9.5	dB
			4	6	8	dB
			2	4	6	dB
			1	3	5	dB
$\alpha_{\text{HCC(max)}}$	maximum HCC attenuation	AF = 10 kHz; $V_{\text{TMUTE}} = 2$ V; data byte 0, SMUT = 0 and MONO = 1; data byte 3, bit 1 = bit 0 = 1 $C_{\text{FMLBUF}}, C_{\text{FMRBUF}} = 2.7$ nF; data byte 3, bit 4 = 1 $C_{\text{FMLBUF}}, C_{\text{FMRBUF}} = 680$ pF; data byte 3, bit 4 = 0	8	10	14.5	dB
			8	10	14.5	dB

## Up-level Car radio Analog Signal Processor (CASP)

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Analog-to-digital converters</b>						
LEVEL ANALOG-TO-DIGITAL CONVERTER (6-BIT)						
$V_{LEVEL(min)}$	lower limit of conversion range		600	720	840	mV
$V_{LEVEL(max)}$	upper limit of conversion range		3.2	3.4	3.6	V
$\Delta V_{LEVEL}$	bit resolution		–	44	–	mV
ULTRASONIC NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TUSN(min)}$	lower limit of conversion range		1.9	2.1	2.4	V
$V_{TUSN(max)}$	upper limit of conversion range		3.8	4.1	4.5	V
$\Delta V_{TUSN}$	bit resolution		280	330	380	mV
AM WIDEBAND NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TWBAM(min)}$	lower limit of conversion range		1.9	2.1	2.4	V
$V_{TWBAM(max)}$	upper limit of conversion range		3.8	4.1	4.5	V
$\Delta V_{TWBAM}$	bit resolution		280	330	380	mV
<b>Tone/volume control</b>						
$G_{v(max)}$	maximum voltage gain	$R_S \leq 10 \Omega$ ; $R_L \geq 10 M\Omega$	19	20	21	dB
$G_{v(signal)}$	signal voltage gain	$T_{amb} = 25 \text{ }^\circ\text{C}$	–0.75	0	+0.75	dB
		$T_{amb} = -40 \text{ to } +85 \text{ }^\circ\text{C}$	–1	0	+1	dB
$V_{o(rms)}$	output voltage level	THD $\leq 0.5\%$	–	2000	–	mV
		THD = 1%; $G_v = 3 \text{ dB}$	2300	–	–	mV
		$R_L = 2 \text{ k}\Omega$ ; $C_L = 10 \text{ nF}$ ; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	$V_o = 500 \text{ mV}$ ; $G_v = 20 \text{ dB}$	–	50	–	mV
$f_{ro}$	roll-off frequency	high frequency (–1 dB)	20000	–	–	Hz
		input A; $C_{KIL} = C_{KIR} = 100 \text{ nF}$ ; $C_{KVL} = C_{KVR} = 220 \text{ nF}$				
		low frequency (–1 dB)	–	35	45	Hz
		low frequency (–3 dB)	–	20	25	Hz
		input C; $C_{KICL} = C_{KICR} = 1 \text{ }\mu\text{F}$ ; $C_{KVL} = C_{KVR} = 220 \text{ nF}$				
low frequency (–1 dB)	–	18	23	Hz		
low frequency (–3 dB)	–	10	13	Hz		
$\alpha_{cs}$	channel separation	$V_i = 1 \text{ V}$ ; frequency range 250 Hz to 20 kHz	74	80	–	dB