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DATA SHEET

TEA6886HL
Up-level Car radio Analog Signal Processor (CASP)

Product specification
Supersedes data of 2000 Nov 21

2003 Feb 04

Philips
Semiconductors

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CONTENTS

Up-level Car radio Analog Signal Processor (CASP)

TEA6886HL

1 FEATURES

1.1 General

- I²C-bus compatible
- Digital alignment/adjustment via I²C-bus:
  - FM noise blanker sensitivity
  - FM stereo noise canceller
  - FM High Cut Control (HCC)
  - FM stereo separation.
- FM audio processing hold for RDS updating; holds the detectors for the FM weak signal processing in their present state
- FM bandwidth limiting; limits the bandwidth of the FM audio signal with external capacitors
- AM stereo input; AM stereo audio can be fed in at the pins for the de-emphasis capacitors; this will provide 8 dB of gain to the AM audio.

1.2 Stereo decoder and noise blanking

- FM stereo decoder
- Accepts FM multiplex signal and AM audio at input
- Pilot detector and pilot canceller
- De-emphasis selectable between 75 and 50 μs
- AM noise blanker: impulse noise detector and an audio hold.

1.3 Weak signal processing

- FM weak signal processing: six signal condition detectors, soft mute, stereo noise canceller (blend) and high cut control (roll-off).

1.4 Audio pre-amplifier

- Source selector for 6 sources: 2 stereo inputs external (A and B), 1 symmetrical stereo input (C), 1 symmetrical mono input (D), 1 internal stereo input (AM or FM) and 1 chime/diagnostic mono input
- Volume 1 control from +20 to −56 dB in 1 dB steps; programmable 20 dB loudness control included
- Volume 2 control from 0 to −56 dB in 1 dB steps, −56, −58.5, −62, −68 dB and mute
- Programmable loudness control with bass boost as well as bass and treble boost
- Treble control from −14 to +14 dB in 2 dB steps
- Bass control from −18 to +18 dB in 2 dB steps with selectable characteristic
- Analog Step Interpolation (ASI) minimizes pops by smoothing out the transitions in the audio signal when a switch is made
- Audio Blend Control (ABC) minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings
- Rear Seat Audio (RSA) can select different sources for the front and rear speakers
- Chime input: can be sent to any audio output, at any volume level
- Chime adder circuit: chime input can also be summed with left front and/or right front audio, or be turned off.

2 GENERAL DESCRIPTION

The TEA6886HL is a monolithic bipolar integrated circuit providing the stereo decoder function and ignition noise blanking facility combined with source selector and tone/volume control for AM/FM car radio applications. The device operates with a power supply voltage range from 7.8 to 9.2 V and a typical current consumption of 40 mA.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6886HL	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.8	8.5	9.2	V
I_{CC}	supply current		32	40	48	mA
Stereo decoder path						
S/N	signal-to-noise ratio		–	78	–	dB
THD	total harmonic distortion		–	0.1	–	%
α_{cs}	channel separation		40	–	–	dB
$V_{o(rms)}$	output voltage level at pins ROPO and LOPO (RMS value)	FM: 91% modulation; AM: 100% modulation; f_{mod} = 400 Hz	840	950	1060	mV
Tone/volume control						
$V_{o(max)(rms)}$	maximum output voltage level at pins LF, LR, RF and RR (RMS value)	V_{CC} = 8.5 V; THD ≤ 0.1%	2000	–	–	mV
G_v	voltage gain	1 dB steps	−112	–	+20	dB
$G_{step(vol)}$	step resolution (volume)		–	1	–	dB
G_{bass}	bass control		−18	–	+18	dB
G_{treble}	treble control		−14	–	+14	dB
$G_{step(treble, bass)}$	step resolution (bass and treble)		–	2	–	dB
(S+N)/N	signal-plus-noise to noise ratio	V_o = 2.0 V; G_v = 0 dB; unweighted	–	107	–	dB
THD	total harmonic distortion	$V_{o(rms)}$ = 1.0 V; G_v = 0 dB	–	0.01	–	%
RR_{100}	ripple rejection	$V_{ripple(rms)}$ < 200 mV; f = 100 Hz; G_v = 0 dB	–	70	–	dB
CMRR	common mode rejection ratio differential stereo input		48	53	–	dB

5 BLOCK DIAGRAM

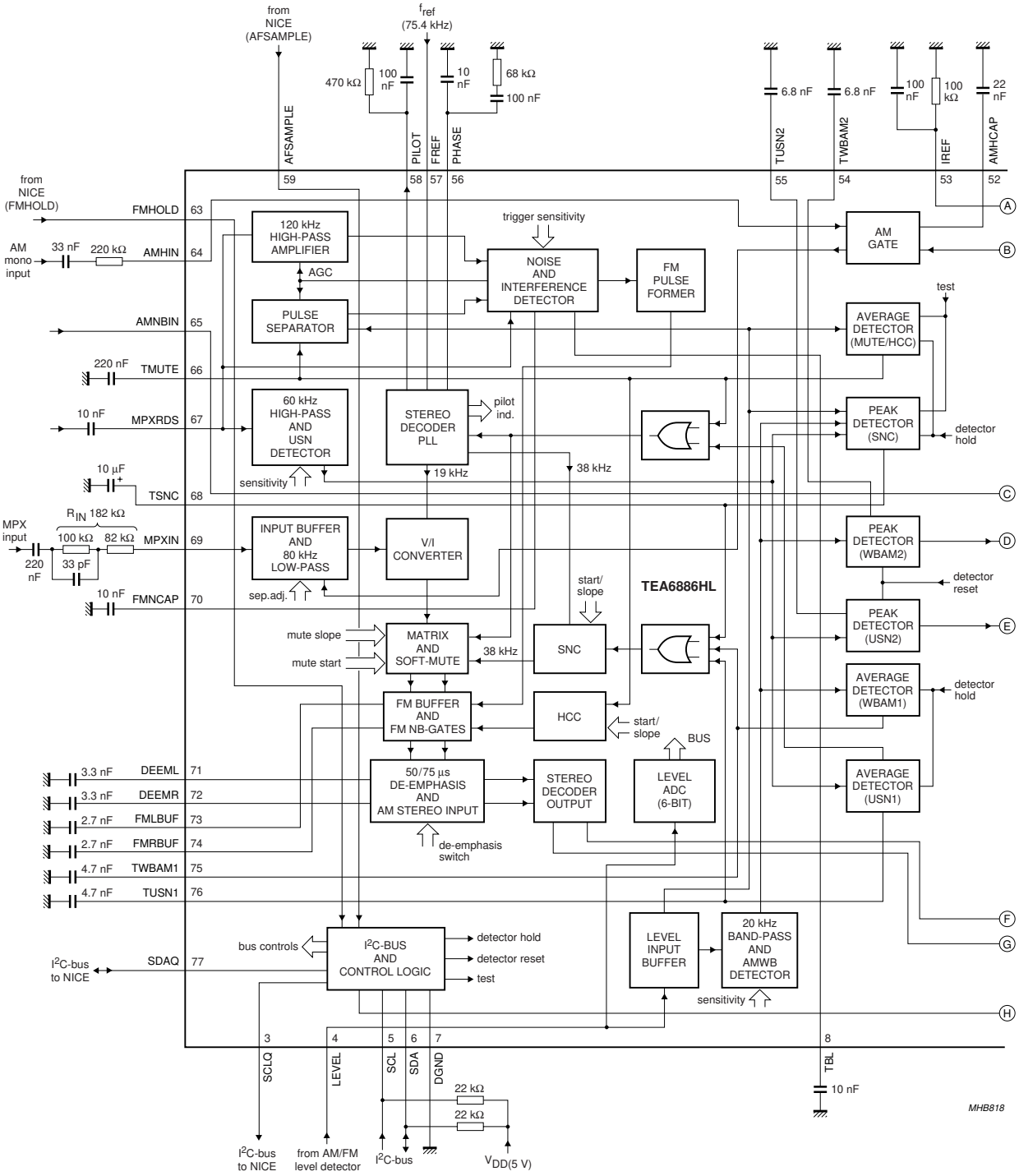

Fig.1 Block diagram (continued in Fig.2).

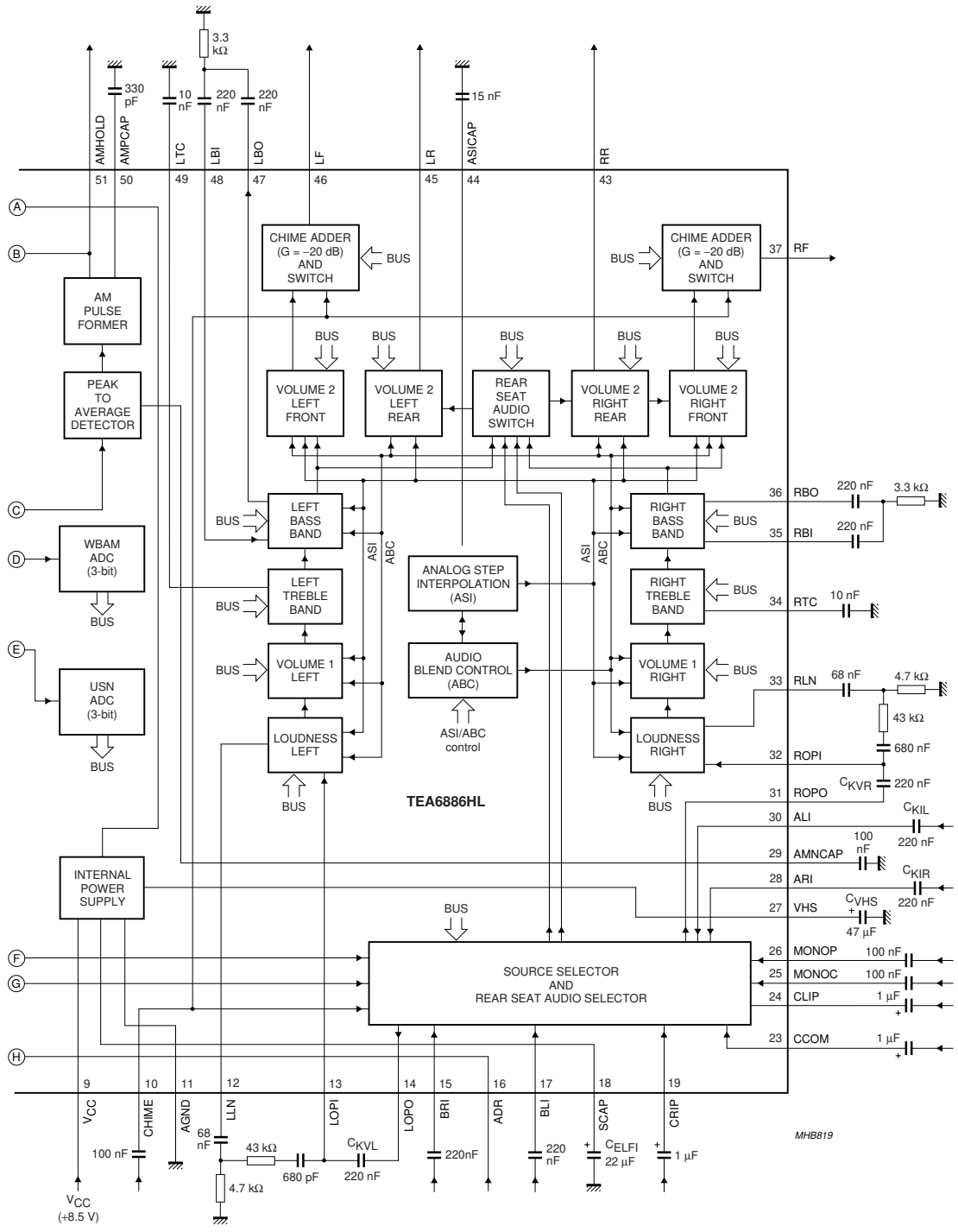

Fig.2 Block diagram (continued from Fig.1).

6 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
SCLQ	3	clock output (to TEA6840H)
LEVEL	4	FM and AM level input (from TEA6840H)
SCL	5	I^2C-bus clock input
SDA	6	I^2C-bus data input/output
DGND	7	digital ground
TBL	8	time constant for FM modulation detector
V_{CC}	9	supply voltage
CHIME	10	chime tone input
AGND	11	analog ground
LLN	12	loudness left network
LOPI	13	left option port input (terminal impedance typical 100 kΩ)
LOPO	14	left option port output
BRI	15	channel B right stereo input (terminal impedance typical 100 kΩ)
ADR	16	address select input
BLI	17	channel B left stereo input (terminal impedance typical 100 kΩ)
SCAP	18	supply filter capacitor
CRIP	19	channel C right symmetrical input (terminal impedance typical 30 kΩ)
n.c.	20	not connected
n.c.	21	not connected
n.c.	22	not connected
CCOM	23	channel C common input (terminal impedance typical 30 kΩ)
CLIP	24	channel C left symmetrical input (terminal impedance typical 30 kΩ)
MONOC	25	mono common input (terminal impedance typical 30 kΩ)
MONOP	26	mono symmetrical input (terminal impedance typical 30 kΩ)
VHS	27	half supply filter capacitor
ARI	28	channel A right stereo input (terminal impedance typical 100 kΩ)
AMNCAP	29	peak-to-average detector capacitor for AM noise blanker
ALI	30	channel A left stereo input (terminal impedance typical 100 kΩ)
ROPO	31	right option port output
ROPI	32	right option port input (terminal impedance typical 100 kΩ)
RLN	33	loudness right network
RTC	34	right treble capacitor
RBI	35	right bass network input
RBO	36	right bass network output
RF	37	right front output
n.c.	38	not connected
n.c.	39	not connected
n.c.	40	not connected

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
n.c.	42	not connected
RR	43	right rear output
ASICAP	44	analog step interpolate capacitor
LR	45	left rear output
LF	46	left front output
LBO	47	left bass network output
LBI	48	left bass network input
LTC	49	left treble capacitor
AMPCAP	50	AM blanking time capacitor
AMHOLD	51	AM noise blanker flag
AMHCAP	52	AM noise blanker hold capacitor
IREF	53	temperature independent reference current
TWBAM2	54	time constant for AM wideband peak detector
TUSN2	55	time constant for ultrasonic noise peak detector
PHASE	56	phase detector
FREF	57	frequency reference input (75.4 kHz from TEA6840H)
PILOT	58	pilot on/off output
AFSAMPLE	59	reset for multipath detector (from TEA6840H for RDS update)
n.c.	60	not connected
n.c.	61	not connected
n.c.	62	not connected
FMHOLD	63	FM audio processing hold input (from TEA6840H for RDS update)
AMHIN	64	AM signal input (from TEA6840H)
AMNBIN	65	AM noise blanker input (from TEA6840H)
TMUTE	66	time constant for soft mute
MPXRDS	67	unmuted MPX input (from TEA6840H for RDS update)
TSNC	68	time constant for stereo noise canceller
MPXIN	69	MPX input (from TEA6840H)
FMNCAP	70	FM noise detector capacitor
DEEML	71	left de-emphasis capacitor
DEEMR	72	right de-emphasis capacitor
FMLBUF	73	left AM/FM audio buffer capacitor
FMRBUF	74	right AM/FM audio buffer capacitor
TWBAM1	75	time constant for AM wideband average detector
TUSN1	76	time constant for ultrasonic noise average detector
SDAQ	77	data input/output (to TEA6840H)
n.c.	78	not connected
n.c.	79	not connected
n.c.	80	not connected

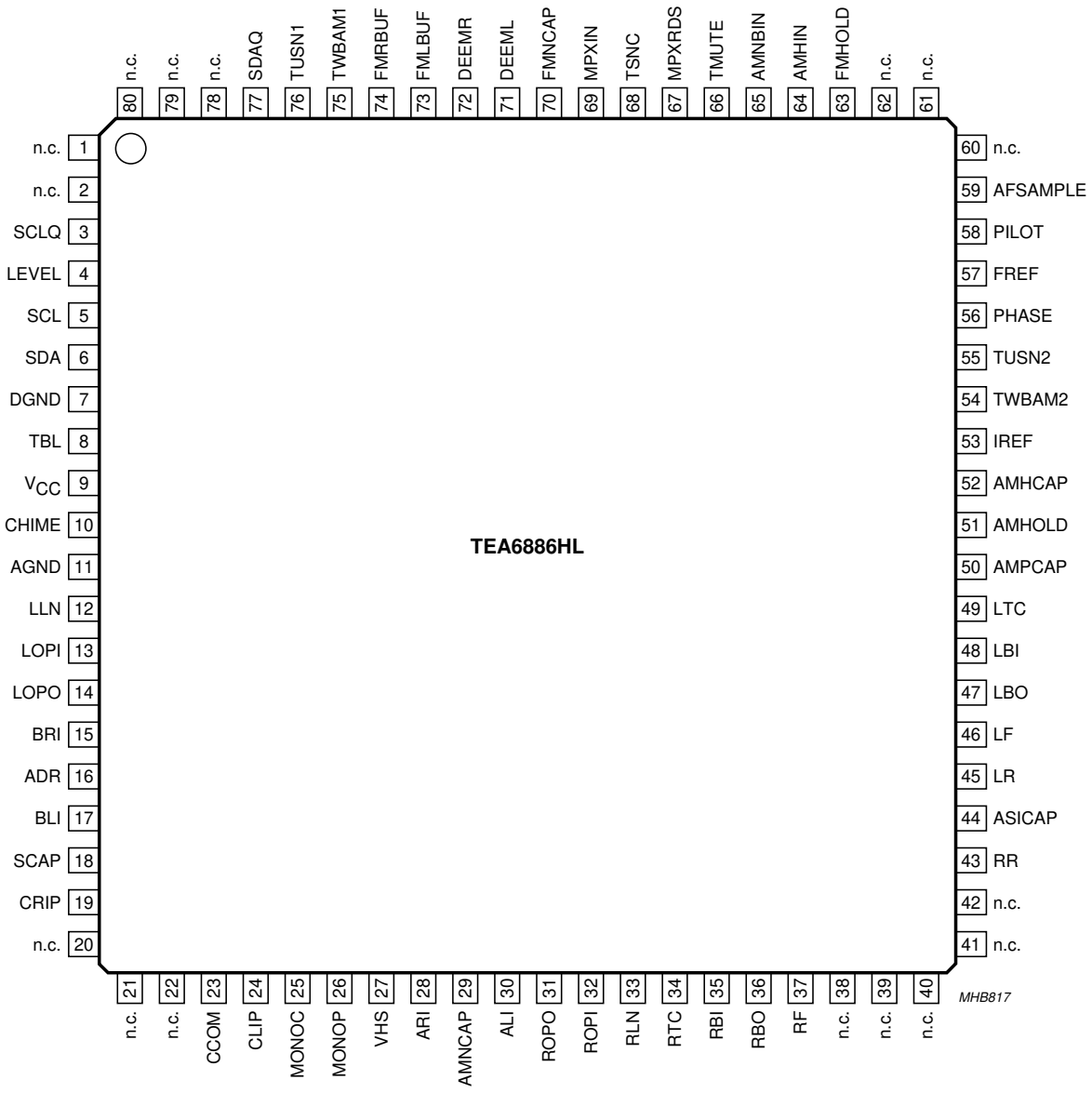

Fig.3 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Stereo decoder

The MPX input is the null-node of an operational amplifier with internal feedback resistor. Adapting the stereo decoder input to the level of the MPX signal, coming from the FM demodulator output, is realized by the value of the input series resistor R_{IN}. To this input a second source (AM detector output) can be fed by current addition.

The input amplifier is followed by an integrated 4th-order Bessel low-pass filter with a cut-off frequency of 80 kHz. It provides the necessary signal delay for FM noise blanking and damping of high frequency interference at the stereo decoder input.

The output signal of this filter is fed to the soft mute control circuitry, the output is voltage-to-current converted and then fed to the phase detector, pilot detector and pilot canceller circuits, contained in the stereo decoder PLL block. A PLL is used for regeneration of the 38 kHz subcarrier. The fully integrated oscillator is adjusted by means of a digital auxiliary PLL into the capture range of the main PLL. The auxiliary PLL needs an external reference frequency (75.4 kHz) which is provided by the TEA6840H. The required 19 and 38 kHz signals are generated by division of the oscillator output signal in a logic circuit. The 19 kHz quadrature phase signal is fed to the 19 kHz phase detector, where it is compared with the incoming pilot tone. The DC output signal of the phase detector controls the oscillator (PLL).

The pilot present detector is driven by an internally generated in-phase 19 kHz signal. Its pilot dependent DC output voltage is fed to a threshold switch, which activates the pilot indicator bit and switches the stereo decoder to stereo operation. The same DC voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. The pilot tone is compensated by this anti-phase 19 kHz signal in the pilot canceller.

The pilot cancelled signal is fed to the matrix. There, the side signal is demodulated and combined with the main signal to the left and right audio channels. Compensation for roll-off in the incoming MPX signal caused by the IF filters and the FM demodulator is typically realized by an external compensation network at pin MPXIN, individual alignment is achieved by I^2C-bus controlled amplification of the side signal (DAA). A smooth mono-to-stereo takeover is achieved by controlling the efficiency of the matrix with the help of the SNC peak detector.

The matrix is followed by the FM noise suppression gates, which are combined with FM single poles and High Cut Control (HCC).

The single pole is defined by internal resistors and external capacitors. Audio is fed from the gate circuits to the switchable de-emphasis, where the demodulated AM stereo signal can be fed in. After de-emphasis the signal passes to the output buffers and is fed to the radio input of the source selector. For HCC, the time constant of the single pole contained in the output buffer can be changed to higher values. This function is controlled by an average detector contained in the multipath and fading detector.

7.2 FM noise blanker

The input of the ignition noise blanker is coupled to the MPXRDS input signal and to the LEVEL input. Both signals are fed via separate 120 kHz filters and rectifiers to an adder circuit. The output signal of the adder circuit is fed in parallel to the noise detector and the interference detector. The noise detector is a negative peak detector. Its output controls the trigger sensitivity (prevention of false triggering at noisy input signals) and the gain of the MPX high-pass filter. The output of the interference detector, when receiving a steep pulse, fires a single-shot trigger circuit, contained in the pulse former circuitry. The time constant of the single-shot trigger circuit is defined by an internal capacitor, and its output activates the blanking gates in the audio.

7.3 AM noise blanker

The AM noise blanking pulse is derived from the AM audio signal which is fed into pin AMNBIN with the help of a peak-to-average comparator. The blanking time is set by a pulse former with external capacitor. The blanking pulse is fed to the gate in the AM audio path and out at pin AMHOLD to operate the gate built into the external AM stereo processor.

7.4 Multipath/fading detection and weak signal control

For FM signal quality dependent controls there is a built-in combination of six detectors. These detectors are driven by the level information direct, by the AC components on the level via a 20 kHz band-pass filter (AM wideband) or by the high notes present at the FM demodulator output via a 60 kHz high-pass filter (ultrasonic noise). The relationship between the DC level and the AC components is programmable by the I^2C-bus (2 bits each). The output of the level buffer, AM wideband detector and ultrasonic noise detector are analog-to-digital converted and readable by the I^2C-bus.

For the period of fast RDS updating soft mute, SNC and HCC can be put on hold. The AM wideband peak detector and the ultrasonic noise peak detector are reset by a switch signal delivered from the TEA6840H via pin FMHOLD.

The six separate detecting circuits are as follows:

1. The AM wideband noise peak detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor connected to pin TWBAM2. The output voltage of the detector is analog-to-digital converted by a 3-bit ADC.
2. The AM wideband noise average detector is driven from a 20 kHz band-pass filter connected to the level buffer output. The time constant is defined by an external capacitor connected to pin TWBAM1. The output of the detector is connected to the Stereo Noise Control (SNC) circuit.
3. The ultrasonic noise peak detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor connected to pin TUSN2. The output voltage of the detector is analog-to-digital converted by a 3-bit ADC.
4. The ultrasonic noise average detector is driven from a 60 kHz high-pass filter connected to the MPX signal from pin MPXRDS. The time constant is defined by an external capacitor connected to pin TUSN1. The output of the detector is connected to soft mute control and stereo noise control circuits.
5. For soft mute and high cut control purposes an average detector with an externally defined time constant (TMUTE) is provided. The detector is driven by level output only. Soft mute and high cut control can be switched off via the I^{2}C-bus.
6. The stereo noise control peak detector with an externally defined time constant (TSNC) is driven by DC level output, AM wideband and ultrasonic noise outputs. It provides the stereo blend facility (SNC). The starting point and slope of the stereo blend can be chosen via the I^{2}C-bus controlled reference voltage.

7.5 Tone/volume control

The tone/volume control part consists of the following functions:

- Source selector
- Loudness
- Volume 1
- Treble
- Bass
- Volume 2
- Rear Seat Audio (RSA) selector
- Chime adder
- Analog step interpolation
- Audio blend control.

The stages loudness, volume 1, bass and volume 2 include the Analog Step Interpolation (ASI) function. This minimizes pops by smoothing out the transitions in the audio signal during switching. The transition time is I^{2}C-bus programmable in a range of 1 : 24 in four steps.

The stages loudness, volume 1 and volume 2 also have the Audio Blend Control (ABC) function. This minimizes pops by automatically incrementing the volume and loudness controls through each step between their present settings and the new settings. The speed of the ABC function is correlated with the transition time of the ASI function.

All stages are controlled via the I^{2}C-bus.

7.5.1 SOURCE SELECTOR

The source selector allows the selection between 6 sources:

- 2 external stereo inputs (ALI, ARI, BLI and BRI)
- 1 external symmetrical stereo input (CLIP, CRIP and CCOM)
- 1 external symmetrical mono input (MONOP and MONON)
- 1 internal stereo input (AM/FM)
- 1 chime/diagnostic mono input (CHIME).

A chime input signal can be sent to any audio output, at any volume level, via the chime/diagnostic mono input.

7.5.2 LOUDNESS

The output of the source selector is fed into the loudness circuit via the external capacitor C_{KVL} (between pins LOPO and LOPI) and C_{KVR} (between pins ROPO and ROPI). Depending on the external circuits for the left and the right channel, only a bass boost or bass and treble boost is available. The external circuits illustrated in Figs 13 and 15 will produce the curves illustrated in Figs 14 and 16 (without the influence of C_{KVL} and C_{KVR} respectively).

7.5.3 VOLUME 1

The volume 1 control circuit follows the loudness circuit. The control range of volume 1 is between +20 and −36 dB in steps of 1 dB.

7.5.4 TREBLE

The output signal of the volume 1 control circuit is fed into the treble control stage. The control range is between +14 and −14 dB in steps of 2 dB. Fig.20 shows the control characteristic with external capacitors of 10 nF.

7.5.5 BASS

The bass control is the next stage. The characteristic of the bass curves depends upon the external circuits connected to pins LBO and LBI (left channel) and pins RBO and RBI (right channel) and also upon the setting of bit BSYM (MSB of the bass control byte). When BSYM = 1, an equalizer characteristic is obtained and when BSYM = 0, a shelving characteristic is obtained.

Figures 17 and 18 show the bass curves with an external circuit of 2×220 nF capacitors and a resistor of 3.3 kΩ for each channel with different values for BSYM. Figure 19 shows the bass curves with an external capacitor of 47 nF for each channel and BSYM = 0, for boost and cut.

7.5.6 VOLUME 2

The four volume 2 blocks are located at the end of the tone/volume control. In addition to volume control (same settings as volume 2) the balance and fader functions are also performed by individual attenuation offsets for the four attenuators. The control range of these attenuators is 56 dB in steps of 1 dB and the additional steps of −58.5 dB, −62 dB, −68 dB and a mute step.

7.5.7 RSA SELECTOR

The RSA selector provides the possibility to select an alternative source for the rear channels. In this event rear channels are only controlled by the volume 2 function.

7.5.8 CHIME ADDER

The chime adder circuit enables the chime input signal to be summed with the left front and/or right front audio, or be turned off.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.3	+10	V
V_i	voltage at all pins (except SCL and SDA)	$V_{CC} \leq 10$ V	$V_{SS} - 0.3$	V_{CC}	V
	voltage at pins SCL and SDA		$V_{SS} - 0.3$	9.7	V
P_{tot}	total power dissipation		−	480	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{es}	electrostatic handling voltage for all pins	note 1	−200	+200	V
		note 2	−2000	+2000	V

Notes

1. Machine model (R = 0 Ω, C = 200 pF).
2. Human body model (R = 1.5 kΩ, C = 100 pF).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	54	K/W

10 CHARACTERISTICS

FM part: input signal $V_{i(MPX)(p-p)}$ = 1.89 V; m = 100% ($\Delta f = \pm 75$ kHz, f_{mod} = 400 Hz); de-emphasis of 75 µs and series resistor at input R_{IN} = 182 kΩ; FM audio measurements are taken at pins LOPO and ROPO.

Tone part: R_S = 600 Ω; R_L = 10 kΩ, AC-coupled; C_L = 2.5 nF; CLK = square wave (5 to 0 V) at 100 kHz; stereo source = A channel input; volume 1 attenuator = 0 dB; loudness = 0 dB, off; volume 2 attenuators = 0 dB; bass linear; treble linear; input voltage = 1 V, f = 1 kHz. Tone part audio measurements are taken at pins RF and LF. V_{CC} = 8.3 to 8.7 V; V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified.

This IC shall not radiate noise in the audio system such that it disturbs any other circuit. This IC shall also not be susceptible to the radiation of any other circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.8	8.5	9.2	V
I_{CC}	supply current	V_{CC} = 8.5 V	32	40	48	mA
V_{HS}	half supply voltage	V_{CC} = 8.5 V	3.75	4.25	4.75	V
I_{IREF}	reference current	V_{CC} = 8.5 V; R_{IREF} = 100 kΩ	35	37	39	µA
FM signal path						
$V_{i(MPX)(p-p)}$	MPX input signal (peak-to-peak value)	R_i = 182 kΩ	–	1.89	–	V
$\Delta V_{i(MPX)}$	overdrive margin of MPX input signal	THD = 1%	6	–	–	dB
I_i	AF input current		–	3.66	–	µA
$I_{i(max)}$	maximum AF input current	THD = 1%	7.32	–	–	µA
$V_{o(rms)}$	AF mono output signal (RMS value)	91% modulation without pilot	890	1000	1110	mV
ΔV_{out}	AF mono channel balance	without pilot; V_{LOPO}/V_{ROPO}	–1	–	+1	dB
α_{cs}	channel separation	aligned setting of data byte 1, bit 0 to bit 3; m = 30% modulation plus 9% pilot				
		L = 1; R = 0	40	47	70	dB
		L = 0; R = 1	40	47	70	dB
THD	total harmonic distortion	$V_{i(MPX)(p-p)}$ = 1.89 V; f_{mod} = 1 kHz without pilot	–	0.1	0.3	%
		$V_{i(MPX)(p-p)}$ = 1.89 V; f_{mod} = 5 kHz				
		L = 1; R = 0	–	0.1	0.3	%
		L = 0; R = 1	–	0.1	0.3	%
S/N	signal-to-noise ratio	f = 20 Hz to 15 kHz	75	78	–	dB
α_{19}	pilot signal suppression	f = 19 kHz	40	50	–	dB
α_{38}	subcarrier suppression	f = 38 kHz	35	50	–	dB
α_{57}		f = 57 kHz	40	–	–	dB
α_{76}		f = 76 kHz	50	60	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IM2	second order intermodulation for f_{spur} = 1 kHz	f_{mod} = 10 kHz; note 1	–	60	–	dB
IM3	third order intermodulation for f_{spur} = 1 kHz	f_{mod} = 13 kHz; note 1	–	58	–	dB
$\alpha_{57(RDS)}$	traffic radio (RDS)	f = 57 kHz; note 2	–	70	–	dB
α_{67}	Subsidiary Communication Authorization (SCA)	f = 67 kHz; note 3	70	–	–	dB
α_{114}	Adjacent Channel Interference (ACI)	f = 114 kHz; note 4	–	80	–	dB
α_{190}		f = 190 kHz; note 4	–	70	–	dB
PSRR	power supply ripple rejection	f = 100 Hz; $V_{ripple(rms)}$ = 100 mV	–	30	–	dB
R_{SDEEML}; R_{SDEEMR}	de-emphasis output source resistance	data byte 3, bit 5 = 1; 75 µs	20	22.7	25.4	kΩ
		data byte 3, bit 5 = 0; 50 µs	13.4	15.2	17	kΩ
I_{FMLBUF}; I_{FMRBUF}	current capacity of FM buffer	$V_{FMLBUF,FMRBUF}$ = 5.5 ±1 V	50	–	200	µA
PLL VCO						
f_{osc}	oscillator frequency		–	228	–	kHz
	frequency range of free running oscillator		190	–	270	kHz
f_{ref}	reference frequency at pin FREF		–	75.4	–	kHz
$V_{i(FREF)}$	reference frequency input voltage		30	100	500	mV
$Z_{i(FREF)}$	input impedance		100	–	–	kΩ
PLL pilot detector						
$V_{i(pilot)(rms)}$	pilot threshold voltage for automatic switching by pilot input voltage (RMS value)	stereo on; STIN = 1	–	27	37	mV
		stereo off; STIN = 0	9	22	–	mV
$hys_{(pilot)}$	hysteresis of pilot threshold voltage		–	2	–	dB
V_{PILOT}	switching voltage for external mono control (PILOT)		0.3	–	0.7	V
AM signal path						
V_{LOPO}; V_{ROPO}	AC output voltage at pins LOPO and ROPO	AMON = 1 and AMST = 0; R_i = 220 kΩ; $V_{iAM(mono)}$ = 250 mV	195	245	295	mV
G_v	AM stereo audio buffer voltage gain	subaddress 0H: AMON = 1 and AMST = 1; input signal at pins DEEML or DEEMR; coupled with 220 nF; $V_{i(DEEML,DEEMR)}$ = 200 mV; f_i = 1 kHz; note 5	7	8	9	dB
$R_{i(DEEML)}$; $R_{i(DEEMR)}$	input resistance for AM stereo left and right	AMON = 1 and AMST = 1; note 6	80	100	120	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Noise blanker						
FM PART						
t_{sup}	interference suppression time		20	30	40	µs
I_{offset}	gate input offset current at pins during suppression pulse duration	during AF suppression time	–	20	50	nA
$I_{ch(FMNCAP)}$	charge current (into 4 V)	no input signal; $V_{FMNCAP} = V_{FMNCAP(int)} - 0.7$ V	−16	−12.5	−9.5	µA
$I_{dch(FMNCAP)}$	discharge current (from 5.5 V)	no input signal; $V_{FMNCAP} = V_{FMNCAP(int)} + 0.7$ V	45	70	100	µA
Trigger Threshold Control (TTC), dependency on MPX signal at MPXRDS input						
V_{FMNCAP}	trigger threshold variation voltage	$V_{i(MPXRDS)}$ = 0 V	4.5	5	5.5	V
ΔV_{FMNCAP}	trigger threshold voltage	$V_{i(MPXRDS)}$ = 10 mV; f = 120 kHz	15	40	80	mV
		$V_{i(MPXRDS)}$ = 100 mV; f = 120 kHz	75	100	200	mV
ΔV_{TBL}	trigger threshold variation with audio frequency f = 15 kHz	$V_{i(MPXRDS)}$ = 670 mV	–	500	–	mV
Trigger Threshold Control (TTC), dependency on level detector input signal						
V_{FMNCAP}	trigger threshold voltage	$V_{LEVEL(AC)}$ = 0 V	4.5	5	5.5	V
ΔV_{FMNCAP}	trigger threshold voltage as a function of $V_{LEVEL(AC)}$	$V_{LEVEL(AC)}$ = 10 mV; f = 120 kHz	–	0	–	mV
		$V_{LEVEL(AC)}$ = 200 mV; f = 120 kHz	–	40	–	mV
Trigger sensitivity measurement with pulse (on MPX signal) at MPXRDS input						
V_{pulse}	trigger sensitivity	t_{pulse} = 10 µs; write mode; data byte 3, bits 6 and 7:				
		NBS1 = 0; NBS0 = 0	–	60	–	mV
		NBS1 = 0; NBS0 = 1	–	100	–	mV
		NBS1 = 1; NBS0 = 0	–	150	–	mV
		NBS1 = 1; NBS0 = 1	–	200	–	mV
Trigger sensitivity measurement with pulse (on level signal) at AM/FM level input						
V_{pulse}	trigger sensitivity	t_{pulse} = 10 µs; V_{LEVEL} = 0.5 V; write mode; data byte 3, bits 6 and 7:				
		NBS1 = 0; NBS0 = 0	–	250	–	mV
		NBS1 = 0; NBS0 = 1	–	275	–	mV
		NBS1 = 1; NBS0 = 0	–	300	–	mV
		NBS1 = 1; NBS0 = 1	–	320	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM PART						
m_{mod}	trigger threshold		–	140	–	%
$V_{AMPCAP(AC)}$	AF voltage at AMHCAP	$V_{iAM(mono)}$ = 50 mV (RMS); f = 1 kHz	16	22	30	mV
α_{AMGATE}	attenuation of blanking gate	$V_{iAM(mono)}$ = 50 mV (RMS); gate open: internal voltage; gate closed: $V_{AMHOLD(DC)}$ = 4 V; note 7	–60	–70	–80	dB
$t_{sup(AMHOLD)}$	suppression time at AMHOLD	t_{pulse} = 10 µs; repetition rate = 50 Hz; V_{pulse} = 1.7 V (AMNBIN); V_{LEVEL} = 0.5 V	400	500	600	µs
$V_{AMNCAP(DC)}$	detector voltage; $V_{ext(AMNBIN)DC}$ − 0.7 V	$V_{AMNBIN(AC)}$ = 0 V; $V_{LEVEL(DC)}$ = 3.5 V	3	3.5	4	V
f_{AMHOLD}	trigger sensitivity	t_{pulse} = 10 µs; repetition rate = 50 Hz; V_{pulse} = 1.7 V (AMNBIN); V_{LEVEL} = 4 V	45	50	55	Hz
I_{offset}	gate input offset current at pins during suppression pulse duration	during AF suppression time	–50	0	+50	nA
Muting average detector (TMUTE); see Fig.12						
$V_{i(LEVEL)}$	input voltage on LEVEL		0.5	–	4	V
G_v	voltage gain LEVEL to TMUTE		–	0	–	dB
ΔV_{TMUTE}	offset between TMUTE and LEVEL		–	1.5	–	V
$\Delta V_{TMUTE/K}$	temperature dependence at TMUTE		–	3.3	–	mV/K
MUTING AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TMUTE)}$	TMUTE charge current		–	–0.2	–	µA
$I_{dch(TMUTE)}$	TMUTE discharge current		–	0.2	–	µA
V_O	DC output voltage		2	–	5	V
TEST CONDITION						
$I_{ch(test)}$	capacitor charge current	data byte 6, bit 7 = 1	–	–12	–	µA
$I_{dch(test)}$	capacitor discharge current	data byte 6, bit 7 = 1	–	12	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM wideband average detector (TWBAM1); see Fig.6						
V_{TWBAM1}	DC voltage at TWBAM1 with respect to AGND	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
VC_{TWBAM1}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 8; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V_O	DC output voltage		1.5	–	5.5	V
AM WIDEBAND AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TWBAM1)}$	TWBAM1 charge current		–19.5	–15	–11.5	µA
$I_{dch(TWBAM1)}$	TWBAM1 discharge current		11.5	15	19.5	µA
Ultrasonic noise average detector (TUSN1); see Fig.5						
V_{TUSN1}	DC voltage at TUSN1 with respect to AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TUSN1}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; note 9; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
V_O	DC output voltage		1.5	–	5.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ULTRASONIC NOISE AVERAGE DETECTOR TIME CONSTANT						
$I_{ch(TUSN1)}$	TUSN1 charge current		−19.5	−15	−11.5	μA
$I_{dch(TUSN1)}$	TUSN1 discharge current		11.5	15	19.5	μA
Peak detector for stereo noise control (TSNC)						
DEPENDENCY ON LEVEL VOLTAGE; see Fig.12						
V_{LEVEL}	input voltage		0.5	–	4.75	V
G	gain LEVEL to TSNC		–	0	–	dB
V_{TSNC}	DC voltage at TSNC referred to DC level voltage at LEVEL	without MPXRDS and LEVEL (AC) input				
		$V_{LEVEL(DC)}$ = 0.5 V	1.75	2.00	2.25	V
		$V_{LEVEL(DC)}$ = 3.5 V	4.50	5.00	5.50	V
$\Delta V_{TSNC/K}$	temperature dependence at TSNC		–	3.3	–	mV/K
DEPENDENCY ON ULTRASONIC NOISE; see Fig.5						
V_{TSNC}	DC voltage at TSNC with respect to AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TSNC}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; note 10; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
V_O	DC output voltage		2	–	5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DEPENDENCY ON AM WIDEBAND NOISE; see Fig.6						
V_{TSNC}	DC voltage at TSNC	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
VC_{TSNC}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 11; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V_O	DC output voltage		1.5	–	5.5	V
DETECTOR TIME CONSTANT						
$I_{ch(TSNC)}$	TSNC charge current		–	–2.5	–	µA
$I_{dch(TSNC)}$	TSNC discharge current		–	65	–	µA
TEST CONDITION						
$I_{ch(test)}$	charge current for testing	data byte 6, bit 7 = 1; $V_{LEVEL(DC)}$ = 2 V; $V_{TSNC(DC)}$ = 2.8 V	–	–1.5	–	mA
$I_{dch(test)}$	discharge current for testing	data byte 6, bit 7 = 1; $V_{LEVEL(DC)}$ = 2 V; $V_{TSNC(DC)}$ = 4.2 V	–	200	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ultrasonic noise peak detector (TUSN2); see Fig.5						
V_{TUSN2}	DC voltage at TUSN2 with respect to AGND	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	–	4.25	–	V
		USS1 = 1; USS0 = 0	–	4.00	–	V
		USS1 = 0; USS0 = 1	–	3.50	–	V
		USS1 = 0; USS0 = 0	–	2.60	–	V
VC_{TUSN2}	DC voltage coefficient	$V_{MPXRDS(AC)}$ = 350 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 80 kHz; write mode; note 12; data byte 1, bits 6 and 7:				
		USS1 = 1; USS0 = 1	0.71	0.85	1.00	
		USS1 = 1; USS0 = 0	0.67	0.80	0.95	
		USS1 = 0; USS0 = 1	0.60	0.70	0.85	
		USS1 = 0; USS0 = 0	0.44	0.52	0.62	
V_O	DC output voltage		1.5	–	5.5	V
DETECTOR TIME CONSTANT						
$I_{ch(TUSN2)}$	TUSN2 charge current		–	–1.6	–	μA
$I_{dch(TUSN2)}$	TUSN2 discharge current		–	21	–	μA
AM wideband peak detector (TWBAM2); see Fig.6						
V_{TWBAM2}	DC voltage at TWBAM2 with respect to AGND	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	–	4.10	–	V
		AWS1 = 1; AWS0 = 0	–	3.60	–	V
		AWS1 = 0; AWS0 = 1	–	3.00	–	V
		AWS1 = 0; AWS0 = 0	–	2.35	–	V
VC_{TWBAM2}	DC voltage coefficient	$V_{LEVEL(AC)}$ = 400 mV; $V_{LEVEL(DC)}$ = 3.5 V; f_i = 24 kHz; write mode; note 13; data byte 1, bits 4 and 5:				
		AWS1 = 1; AWS0 = 1	0.69	0.82	0.98	
		AWS1 = 1; AWS0 = 0	0.60	0.72	0.86	
		AWS1 = 0; AWS0 = 1	0.50	0.60	0.71	
		AWS1 = 0; AWS0 = 0	0.40	0.47	0.56	
V_O	DC output voltage		2	–	5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DETECTOR TIME CONSTANT						
$I_{ch(TWBAM2)}$	TWBAM2 charge current		–	–1.6	–	μA
$I_{dch(TWBAM2)}$	TWBAM2 discharge current		–	21	–	μA
Soft mute; see Figs 7 and 4						
α_{0dB}	attenuation at LOPO and ROPO	V_{TMUTE} = 3.5 V; V_{TUSN1} = 3.5 V	–0.5	0	+0.5	dB
α_{6dB}	start of muting; AC attenuation at LOPO and ROPO	see Fig.4; write mode; MSL0 = 1; MSL1 = 1				
		MST1 = 0; MST0 = 0; $V_{TMUTE} = 0.42V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 0; MST0 = 1; $V_{TMUTE} = 0.45V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 0; $V_{TMUTE} = 0.47V_{TUSN1}$ without AC	3	6	9	dB
		MST1 = 1; MST0 = 1; $V_{TMUTE} = 0.49V_{TUSN1}$ without AC	3	6	9	dB
α_{10dB}	AC attenuation for setting of mute slope at LOPO and ROPO	MST1 = 0; MST0 = 0; see Fig.7				
		MSL1 = 0; MSL0 = 0; $V_{TMUTE(DC)} = 0.35V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 0; MSL0 = 1; $V_{TMUTE(DC)} = 0.38V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 0; $V_{TMUTE(DC)} = 0.39V_{TUSN1}$ without AC	7	10	13	dB
		MSL1 = 1; MSL0 = 1; $V_{TMUTE(DC)} = 0.395V_{TUSN1}$ without AC	7	10	13	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo Noise Control (SNC)						
$\alpha_{cs(start)}$	start of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1111; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.63V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.70V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
		aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 0000; V_{TSNC} or V_{TUSN1} or $V_{TWBAM1} = 0.74V_{TUSN1}$ without AC; see note 14 and Fig.9	4.5	6	7.5	dB
$\alpha_{cs(slope)}$	slope of channel separation	aligned at L = 1 and R = 0; data byte 2, SST[3:0] = 1000; $V_{TSNC} = 0.72V_{TUSN1}$ without AC; see note 15 and Fig.8; data byte 2, bits 4 and 5:				
		SSL1 = 0; SSL0 = 0	3	5	7	dB
		SSL1 = 0; SSL0 = 1	5	7	9	dB
		SSL1 = 1; SSL0 = 0	11	13	15	dB
		SSL1 = 1; SSL0 = 1 (not defined)				

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
High Cut Control (HCC)						
$\alpha_{HCC(start)}$	AC attenuation for start of HCC	AF = 10 kHz; V_{MPXIN} = 200 mV; HSL1 = 1; HSL0 = 0; data byte 0, SMUT = 0 and MONO = 1; write mode; see note 16 and Fig.10; data byte 3, bits 2 and 3:				
		HST1 = 1; HST0 = 1; $V_{LEVEL(DC)}$ = 1.00 V	1.5	3	4.5	dB
		HST1 = 1; HST0 = 0; $V_{LEVEL(DC)}$ = 1.25 V	1.5	3	4.5	dB
		HST1 = 0; HST0 = 1; $V_{LEVEL(DC)}$ = 1.50 V	1.5	3	4.5	dB
		HST1 = 0; HST0 = 0; $V_{LEVEL(DC)}$ = 1.75 V	1.5	3	4.5	dB
$\alpha_{HCC(slope)}$	AC attenuation for slope of HCC	AF = 10 kHz; V_{MPXIN} = 200 mV; C_{FMLBUF}, C_{FMRBUF} = 2.7 nF; HST1 = 1; HST0 = 1; data byte 0, SMUT = 0 and MONO = 1; see note 16 and Fig.11; data byte 3, bits 0 and 1:				
		HSL1 = 1; HSL0 = 1	5.5	7.5	9.5	dB
		HSL1 = 1; HSL0 = 0	4	6	8	dB
		HSL1 = 0; HSL0 = 1	2	4	6	dB
		HSL1 = 0; HSL0 = 0	1	3	5	dB
$\alpha_{HCC(max)}$	maximum HCC attenuation	AF = 10 kHz; V_{TMUTE} = 2 V; data byte 0, SMUT = 0 and MONO = 1; data byte 3, bit 1 = bit 0 = 1				
		C_{FMLBUF}, C_{FMRBUF} = 2.7 nF; data byte 3, bit 4 = 1	8	10	14.5	dB
		C_{FMLBUF}, C_{FMRBUF} = 680 pF; data byte 3, bit 4 = 0	8	10	14.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converters						
LEVEL ANALOG-TO-DIGITAL CONVERTER (6-BIT)						
$V_{LEVEL(min)}$	lower limit of conversion range		–	740	–	mV
$V_{LEVEL(max)}$	upper limit of conversion range		–	3.4	–	V
ΔV_{LEVEL}	bit resolution		–	42.5	–	mV
ULTRASONIC NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TUSN(min)}$	lower limit of conversion range		–	2.1	–	V
$V_{TUSN(max)}$	upper limit of conversion range		–	4	–	V
ΔV_{TUSN}	bit resolution		–	320	–	mV
AM WIDEBAND NOISE ANALOG-TO-DIGITAL CONVERTER (3-BIT)						
$V_{TWBAM(min)}$	lower limit of conversion range		–	2.1	–	V
$V_{TWBAM(max)}$	upper limit of conversion range		–	4	–	V
ΔV_{TWBAM}	bit resolution		–	320	–	mV
Tone/volume control						
$G_{v(max)}$	maximum voltage gain	$R_S \leq 10\ \Omega$; $R_L \geq 10\ M\Omega$	19	20	21	dB
$G_{v(signal)}$	signal voltage gain	T_{amb} = 25 °C	–0.75	0	+0.75	dB
		T_{amb} = –40 to +85 °C	–1	0	+1	dB
$V_{o(rms)}$	output voltage level	THD ≤ 0.5%	–	2000	–	mV
		THD = 1%; G_v = 3 dB	2300	–	–	mV
		R_L = 2 kΩ; C_L = 10 nF; THD = 1%	2000	–	–	mV
$V_{i(rms)}$	input sensitivity	V_o = 500 mV; G_v = 20 dB	–	50	–	mV
f_{ro}	roll-off frequency	high frequency (–1 dB)	20000	–	–	Hz
		input A; $C_{KIL} = C_{KIR}$ = 100 nF; $C_{KVL} = C_{KVR}$ = 220 nF				
		low frequency (–1 dB)	–	35	45	Hz
		low frequency (–3 dB)	–	20	25	Hz
		input C; $C_{KICL} = C_{KICR}$ = 1 μF; $C_{KVL} = C_{KVR}$ = 220 nF				
		low frequency (–1 dB)	–	18	23	Hz
		low frequency (–3 dB)	–	10	13	Hz
α_{cs}	channel separation	V_i = 1 V; frequency range 250 Hz to 20 kHz	74	80	–	dB