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TEBF0808 TRM

Revision: v.93

Exported on: 08/13/2018

1 Table of Contents

2 Overview

Refer to http://trenz.org/tebf0808-info for the current online version of this manual and other available documentation.The Trenz Electronic TEBF0808 carrier board is a baseboard for the Xilinx Zynq Ultrascale+ MPSoC modules TE0808 and TE0803, which exposes the module's B2B connector pins to accessible connectors and provides a whole range of on-board components to test and evaluate the Zynq Ultrascale+ SoMs and for developing purposes. The carrier board has a Mini-ITX form factor making it capable to be fitted into a PC enclosure. On the PC enclosure's rear and front panel, MGT interfaces and connectors are accessible, for the front panel elements there are also Intel-PC compatible headers available.

2.1 Key Features

- Mini-ITX form factor, PC enclosure compatible
- ATX-24 power supply connector
- Optional 12V standard power plug
- Headers
  - Intel 10-pin HDA Audio
  - Intel 9-pin Power-/Reset-Button, Power-/HD-LED
  - PC-BEEPER
- On-board Power- / Reset-Switches
- 2x Configuration 4-bit DIP-switches
- 2x Optional 4-wire PWM fan connectors
- PCIe Slot - one PCIe lane (16 lane connector)
- CAN FD Transceiver (10 Pin IDC connector and 6-pin header)
- 4x On-board configuration EEPROMs (1x Microchip 24LC128-I/ST, 3x Microchip 24AA025E48T-I/OT)
- Dual SFP+ Connector (2x1 Cage)
- 1x DisplayPort (single lane)
- 1x SATA Connector
- 2x USB3.0 A Connector (Superspeed Host Port (Highspeed at USB2.0))
- 1x USB3.0 on-board connector with two ports
- FMC HPC Slot (FMC_VADJ max. VCCIO)
- FMC Fan
- Gigabit Ethernet RGMII PHY with RJ45 MagJack
- All carrier board peripherals' I^2C interfaces muxed to MPSoC's I^2C interface
- Quad programmable PLL clock generator SI5338A
- 2x SMA coaxial connectors for clock signals
- MicroSD- / MMC-Card Socket (bootable)
- 32 Gbit (4 GByte) on-board eMMC flash (8 banks a 4 Gbit)
- 2x System Controller CPLDs Lattice MachXO2 1200 HC
- 1x Samtec FireFly (4 GT lanes bidirectional)
- 1x Samtec FireFly connector for reverse loopback
- 2x JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for programming MPSoC and SC CPLDs
- 20-pin ARM JTAG Connector (PS JTAG0)
- 3x PMOD connector (GPIO's and I^2C interface to SC CPLDs and MPSoC module)
- On-board DC-DC PowerSoCs

Additional assembly options are available for cost or performance optimization upon request.

2.2 Block Diagram

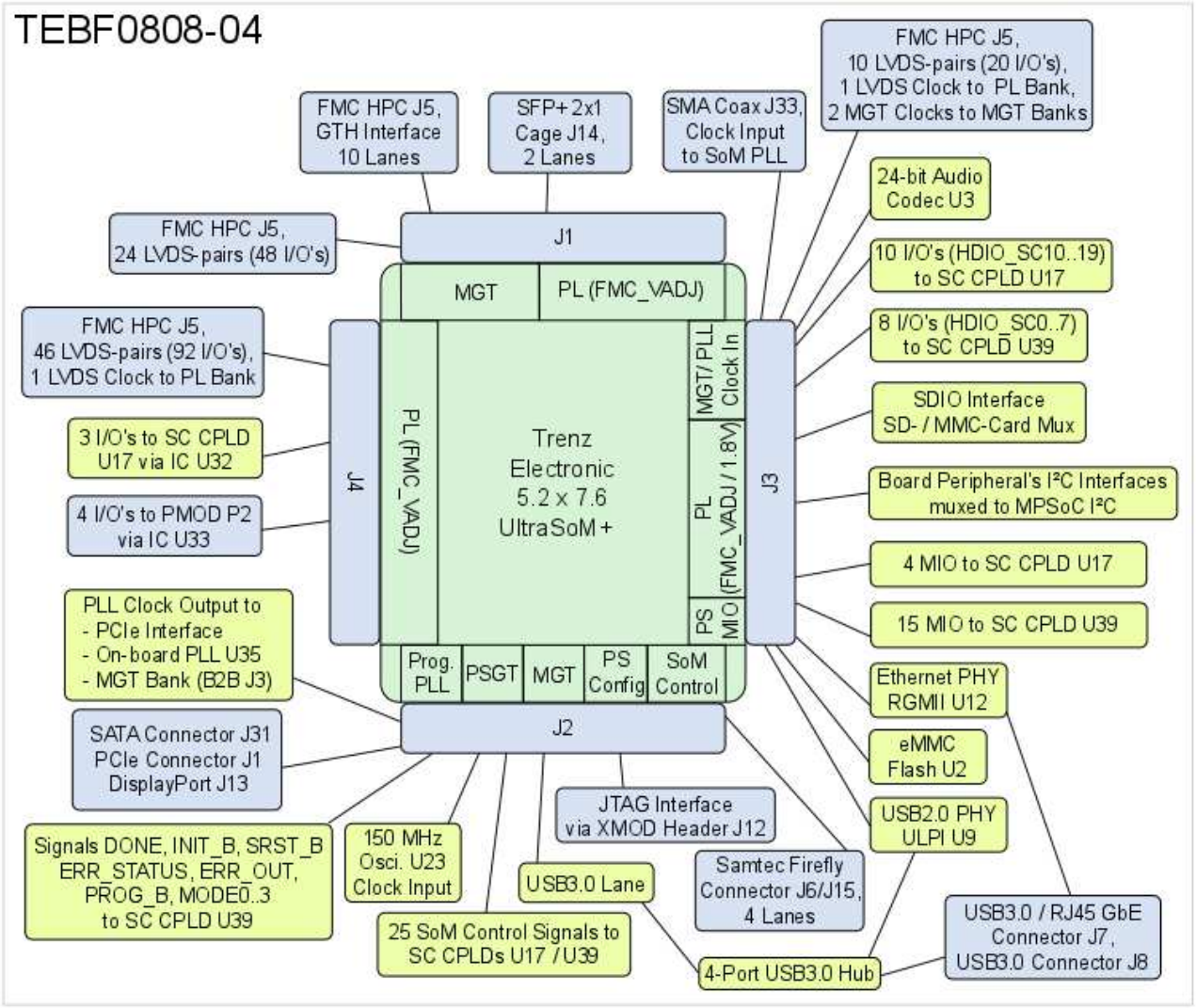

Figure 1: TEBF0808-04 Block Diagram

Block Diagram description of depicted on-board peripherals

On-board Peripheral	B2B	MPSoC Unit / SoM peripheral	Description	TRM Section
FMC HPC J5, 24 LVDS pairs (48 I/O's)	J1	PL Bank (FMC_VADJ)	PL I/O-bank pins, differential pairs	FMC HPC Connector
FMC HPC J5, GTH Interface	J1	MGT Bank	10 MGT Lanes	FMC HPC Connector
SFP+ 2x1 Cage J14	J1	MGT Bank	2 MGT Lanes to dual SFP+ Connector	MGT Interfaces SFP+ and FireFly

On-board Peripheral	B2B	MPSoC Unit / SoM peripheral	Description	TRM Section
SMA Coax J33	J1	On-module PLL	SMA Coaxial Connector to on-module PLL Clock Input pin	Programmable PLL Clock Generator
FMC HPC J5 ▪ 10 LVDS pairs (20 I/O's) ▪ 1 LVDS Clock to PL Bank ▪ 2 MGT Clocks to MGT Banks	J2	PL Bank (FMC_VADJ) MGT Bank	PL I/O-bank pins, differential pairs 1 clock capable PL bank pin-pair 2 MGT clock input pin-pairs	FMC HPC Connector Programmable PLL Clock Generator
24-bit Audio Codec U3	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board 24-bit Audio Codec	Intel-PC Compatible Headers and FAN Connectors 24-bit Audio Codec
10 I/O's to SC CPLD U17	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board System Controller CPLD U17	System Controller CPDLs
8 I/O's to SC CPLD U39	J3	PL Bank (1.8 V)	PL I/O-bank pins to on-board System Controller CPLD U39	System Controller CPDLs
SDIO Interface, SD- / MMC-Card Mux	J3	PS MIO	SDIO interface connected to SD- / MMC-Card socket	MIO Bank Interfaces SDIO Port Expander
Board Peripheral's I^2C Interfaces muxed to MPSoC I^2C	J3	PS MIO	MPSoC I^2C interface configured as master connected to on-board slaves	MIO Bank Interfaces 8-Channel I^2C Switches
4 MIO to SC CPLD U17	J3	PS MIO	Functionality depending on MPSoC and CPLD firmware	System Controller CPDLs
15 MIO to SC CPLD U39	J3	PS MIO	Functionality depending on MPSoC and CPLD firmware	System Controller CPDLs
Ethernet PHY RGMII	J3	PS MIO	Ethernet PHY U12 connected per RGMII	MIO Bank Interfaces Gigabit Ethernet PHY
eMMC Flash	J3	PS MIO	eMMC Flash memory interface on PS bank	MIO Bank Interfaces eMMC Memory

On-board Peripheral	B2B	MPSoC Unit / SoM peripheral	Description	TRM Section
USB2.0 PHY ULPI	J2	PS MIO	USB2.0 PHY U9 connected per ULPI	MIO Bank Interfaces High-speed USB ULPI PHY
SAMTEC FireFly Connector J6/J15	J2	MGT Bank	MGT Lanes to Samtec FireFly connector	MGT Interfaces SFP+ and FireFly
JTAG Interface via XMOD Header J12	J2	PS Config	MPSoC USB programmable JTAG interface	MIO Bank Interfaces JTAG Interface
USB3.0 Lane	J2	PSGT	USB3.0 PS MGT Lane	MIO Bank Interfaces PS GT Bank Interfaces
4-port USB3.0 Hub	-	-	USB3.0 (2.0 compatible) Hub with 4 ports	MIO Bank Interfaces 4-port USB3.0 Hub
USB3.0 / RJ45 GbE Connector J7, USB3.0 Connector J8	-	-	2-port USB3.0 / RJ45 GbE Connector (stacked)	MIO Bank Interfaces
25 SoM Control Signals to SC CPLDs U17 / U39	J2	On-module DC-DC converter, PLL clock generator	Control Signals, e.g. "Enable"- / "Power Good"- signals of DC-DC-converter and further on-module peripherals	Power-On Sequence Diagram Programmable PLL Clock Generator
150 MHz Osci Clock Input	J2	-	150 MHz SATA interface MGT clock	Oscillators
Signals DONE, INIT_B, SRST_B, ... to SC CPLD U39	J2	PS Config	MPSoC control signal for PS- / PL configuration	System Controller CPDLs
SATA Connector J31 PCIe Connector J1 DisplayPort J13	J2	PSGT	Connectors of the MGT based data interfaces	PS GT Bank Interfaces
PLL Clock Output to ▪ PCIe Interface ▪ On-board PLL U35 ▪ MGT Bank (B2B J3)	J2	On-module PLL clock generator	Reference clock signals of the on-module programmable PLL clock generator	Programmable PLL Clock Generator
4 I/O's to PMOD P2 via IC U33	J4	PL Bank (FMC_VADJ)	PL user I/O's accessible on PMOD connector P2	CAN FD Interface and PMOD Connectors
3 I/O's to SC CPLD U17 via IC U32	J4	PL Bank (FMC_VADJ)	PL user I/O's routed to System Controller CPLD U17	System Controller CPDLs

On-board Peripheral	B2B	MPSoC Unit / SoM peripheral	Description	TRM Section
FMC HPC J5 • 46 LVDS pairs (92 I/O's) • 1 LVDS Clock to PL Bank	J4	PL Bank (FMC_VADJ)	PL I/O-bank pins, differential pairs 1 clock capable PL bank pin-pair	FMC HPC Connector Programmable PLL Clock Generator

Table 1: Description of depicted on-board peripherals

2.3 Main Components

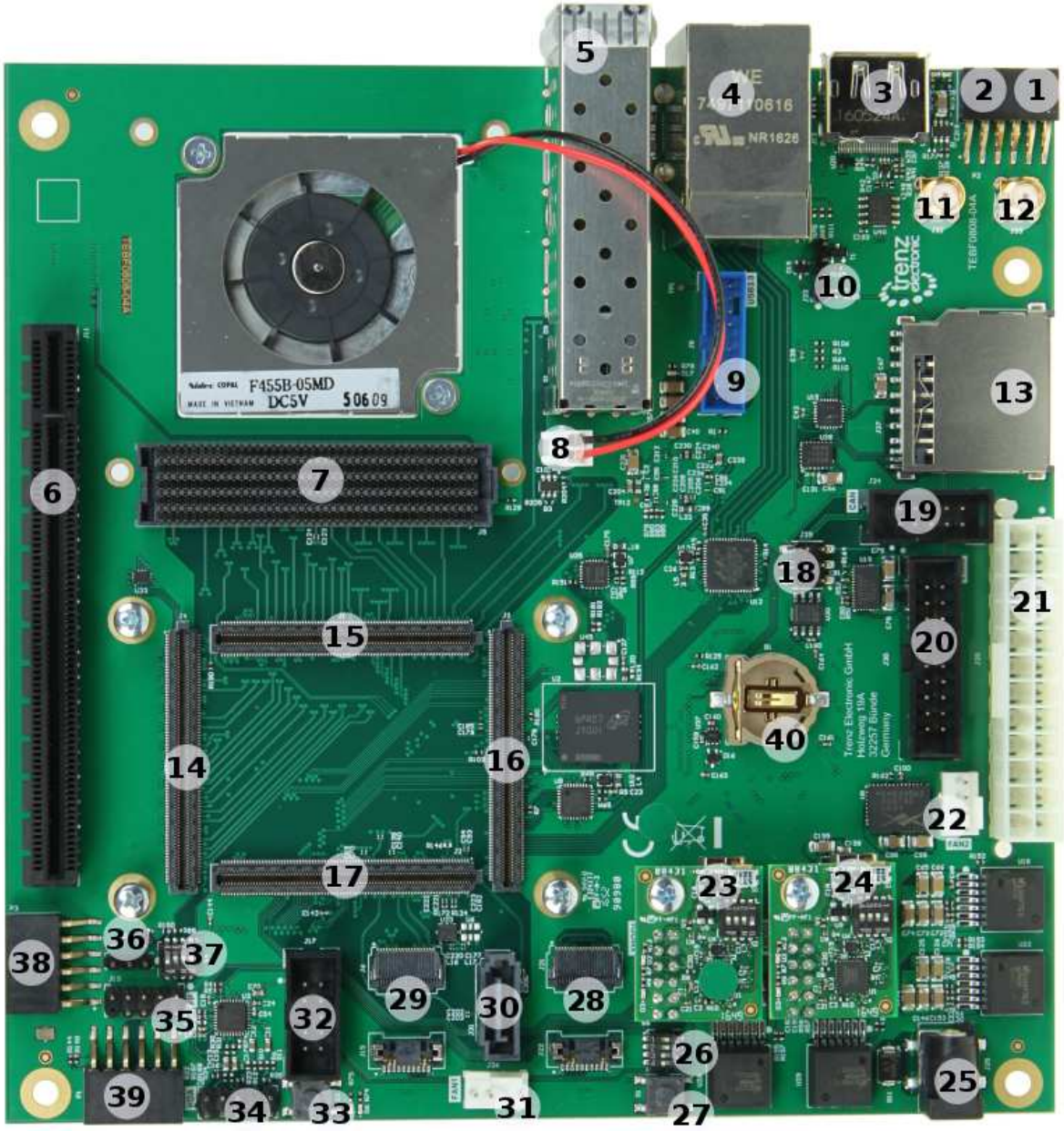

Figure 2: TEBF0808-04 Carrier Board

1. PMOD connector, P2
2. MicroSD Card socket (on bottom side), J16
3. DisplayPort connector, J13
4. USB3.0 A 2x , RJ45 1x (stacked), J7
5. SFP+ 2x1 cage, J14
6. PCIe x16 connector (one PCIe lane connected), J11
7. FMC HPC connector, J5
8. FMC-Fan connector 5V, J19
9. USB3.0 connector, J8
10. PC-BEEPER 4-pin header, J23
11. SMA coaxial connector (SI5338A clock output), J32
12. SMA coaxial connector (clock input to MPSoC module), J33
13. MMC Card socket, J27
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
17. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
18. CAN bus 6-pin header, J29
19. CAN bus 10-pin connector, J24
20. ARM JTAG 20-pin connector, J30
21. ATX-24 power supply connector, J20
22. 4-Wire PWM fan connector, J35
23. JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to MPSoC module, J12
24. JTAG/UART header ('XMOD FTDI JTAG Adapter'-compatible) for access to System Controller CPLDs, J28
25. Power Jack 2.1mm 12V, J25
26. 4-bit DIP-switch, S5
27. Power Button, S1
28. Samtec FireFly connector for reverse loopback, J21/J22
29. Samtec FireFly connector (4 GT lanes bidirectional), J6/J15
30. SATA header, J31
31. 4-Wire PWM fan connector, J26
32. I^2C interface of programmable on-module PLL (10-pin header), J17
33. Reset Button, S2
34. INTEL HDA 9-pin header, J9
35. Intel front panel (PWR-/RST-Button, HD-/PWR-LED) 9-pin header, J10
36. Samtec FireFly connector J6/J15 I^2C interface (3-pin header), J34
37. 4-bit DIP-switch, S4
38. PMOD connector, P3
39. PMOD connector, P1
40. Battery Holder CR1220, B1

2.4 Initial Delivery State

Storage device name	Content	Notes
User configuration EEPROMs (1x Microchip 24LC128-I/ST, 3x Microchip 24AA025E48T-I/OT)	Not programmed	-
USB3.0 HUB Configuration EEPROM (Microchip 24LC128-I/ST)	Not programmed	-
Si5338A programmable PLL NVM OTP	Not programmed	-

Table 2: Initial Delivery State of the flash memories

3 Signals, Interfaces and Pins

3.1 FMC HPC Connector

The FMC (FPGA Mezzanine Card) connector J5 with high pin count (HPC) provides as an ANSI/VITA 57.1 standard a modular interface to the MPSoCs FPGA and exposes numerous of its I/O pins for use by other mezzanine modules and expansion cards.

The connector supports single ended (VCCIO: FMC_VADJ) and differential signaling as the I/O's are routed from the FPGA banks as LVDS-pairs to the FMC connector.

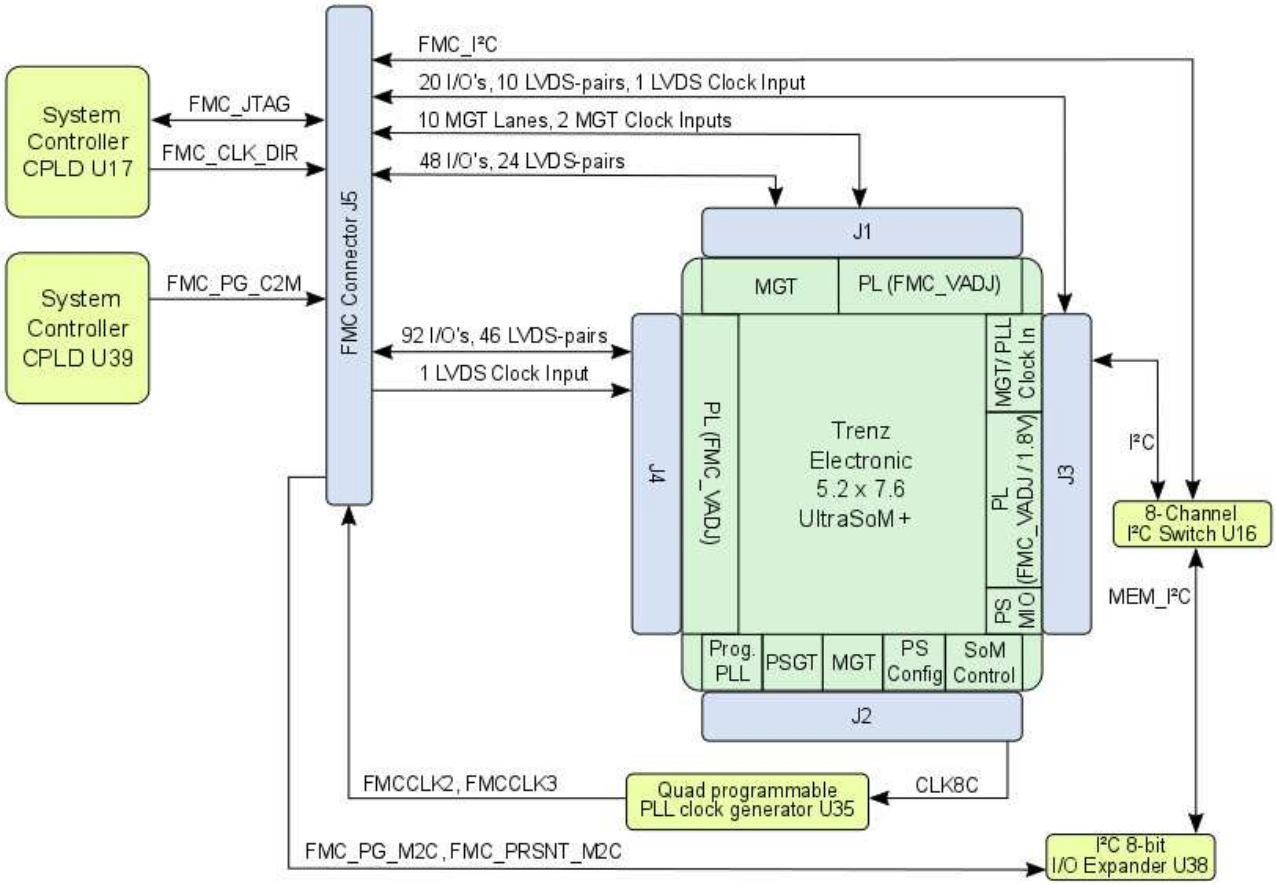

Figure 3: FMC HPC Connector

B2B	I/O Signal Count	LVDS-pairs count	VCCO bank Voltage	Reference Clock Input from FMC Connector	Notes
J1	48	24	FMC_VADJ	-	bank's VREF-pin connected to FMC connector pin J5-H1 (VREF_A_M2C)

B2B	I/O Signal Count	LVDS-pairs count	VCCO bank Voltage	Reference Clock Input from FMC Connector	Notes
J3	20	10	FMC_VADJ	1 LVDS clock from FMC-connector J5 (pins J5-G2, J5-G3) to clock capable PL bank pin-pair	
J4	92	46	FMC_VADJ	1 LVDS clock from FMC connectorJ5 (pins J5-H4, J5-H5) to clock capable PL bank pin-pair	bank's VREF-pin connected to FMC connector pin J5-H1 (VREF_A_M2C)

Table 3: FMC connector pin-outs of available logic banks of the MPSoC

The MGT-banks have also clock input-pins which are exposed to the FMC connector. Following MGT-lanes are available on the FMC connectors J5:

Schematic Names of the MGT Signals	B2B Connector Pins	FMC Connector Pins
B228_RX3_P, B228_RX3_N	pins J1-51, J1-53	pins J5-A10, J5-A11
B228_TX3_P, B228_TX3_N	pins J1-50, J1-52	pins J5-A30, J5-A31
B228_RX2_P, B228_RX2_N	pins J1-57, J1-59	pins J5-A6, J5-A7
B228_TX2_P, B228_TX2_N	pins J1-56, J1-58	pins J5-A26, J5-A27
B228_RX1_P, B228_RX1_N	pins J1-63, J1-65	pins J5-A2, J5-A3
B228_TX1_P, B228_TX1_N	pins J1-62, J1-64	pins J5-A22, J5-A23
B228_RX0_P, B228_RX0_N	pins J1-69, J1-71	pins J5-C6, J5-C7
B228_TX0_P, B228_TX0_N	pins J1-68, J1-70	pins J5-C2, J5-C3
B229_RX3_P, B229_RX3_N	pins J1-27, J1-29	pins J5-B12, J5-B13
B229_TX3_P, B229_TX3_N	pins J1-26, J1-28	pins J5-B32, J5-B33
B229_RX2_P, B229_RX2_N	pins J1-33, J1-35	pins J5-B16, J5-B17
B229_TX2_P, B229_TX2_N	pins J1-32, J1-34	pins J5-B36, J5-B37
B229_RX1_P, B229_RX1_N	pins J1-39, J1-41	pins J5-A18, J5-A19
B229_TX1_P, B229_TX1_N	pins J1-38, J1-40	pins J5-A38, J5-A39
B229_RX0_P, B229_RX0_N	pins J1-45, J1-47	pins J5-A14, J5-A15
B229_TX0_P, B229_TX0_N	pins J1-44, J1-46	pins J5-A34, J5-A35
B230_RX1_P, B230_RX1_N	pins J1-15, J1-17	pins J5-B4, J5-B5
B230_TX1_P, B230_TX1_N	pins J1-14, J1-16	pins J5-B24, J5-B25
B230_RX0_P, B230_RX0_N	pins J1-21, J1-23	pins J5-B8, J5-B9
B230_TX0_P, B230_TX0_N	pins J1-20, J1-22	pins J5-B28, J5-B29

Table 4: FMC connector pin-outs of available MGT lanes of the MPSoC

The FMC connector provides pins for reference clock output to the Mezzanine module and clock input to PL banks of the MPSoC:

Clock Signal Schematic Name	FMC Connector Pins	Direction	Clock Source	Notes
B228_CLK0	J5-D4 / J5-D5	in	FMC Connector J5	Extern MGT clock
B229_CLK0	J5-B20 / J5-B21	in	FMC Connector J5	Extern MGT clock
FMCCLK2	J5-K4 / J5-K5	out	Carrier Board PLL SI5338A U35, CLK2	Clock signal to Mezzanine module
FMCCLK3	J5-J2 / J5-J3	out	Carrier Board PLL SI5338A U35, CLK3	Clock signal to Mezzanine module
B64_L14_P / B64_L14_N	J5-H4 / J5-H5	in	FMC Connector J5	Extern LVDS clock to PL bank
B48_L6_P / B48_L6_N	J5-G2 / J5-G3	in	FMC Connector J5	Extern LVDS clock to PL bank

Table 5: FMC connector pin-outs for reference clock output

The FMC connector provides further interfaces like JTAG and I^2C interfaces:

Interfaces	I/O Signal Count	Pin schematic Names / FMC Pins	Connected to	Notes
JTAG	5	FMC_TCK, pin J5-D29 FMC_TMS, pin J5-D33 FMC_TDI, pin J5-D30 FMC_TDO, pin J5- D31	SC CPLD U17, bank 1	VCCIO: 3V3SB TRST_L, pin J5-D34 pulled-up to 3V3_PER
I^2C	2	FMC_SCL, pin J5-C30 FMC_SDA, pin J5-C31	I^2C Switch U16	I^2C-lines pulled-up to 3V3_PER
Control Lines	4	FMC_PRSNT_M2C, pin J5-H2	I^2C I/O Expander U38	'PG' = 'Power Good'-signal
		FMC_PG_C2M, pin J5-D1 (3V3_PER pull-up)	SC CPLD U39, bank 0	'C2M' = carrier to (Mezzanine) module
		FMC_PG_M2C, pin J5-F1 (3V3_PER pull-up)	I^2C I/O Expander U38	'M2C' = (Mezzanine) module to carrier
		FMC_CLK_DIR, pin J5-B1 (pulled-down to GND)	SC CPLD U17, bank 1	

Table 6: FMC connector pin-outs of available interfaces to the System Controller CPLD

Several VCCIO voltages are available on the FMC connector to operate the I/O's on different voltage levels:

VCCIO Schematic Name	FMC Connector J5 Pins	Notes
12V	C35/C37	extern 12V power supply
3V3_PER	D32/D36/D38/D40/C39	3.3V peripheral supply voltage
FMC_VADJ	H40/G39/F40/E39	adjustable FMC VCCIO voltage, supplied by DC-DC converter U8

Table 7: Available VCCIO voltages on FMC connector

3.2 MIO Bank Interfaces

The TEBF0808 carrier board provides several interfaces, which are configured on the MIO banks 500 .. 503 of the Zynq Ultrascale+ MPSoC.

Following table contains the assignment of the MIO pins to the configured interfaces:

MIO	Configured as	System Controller CPLD	Notes
0..12	Dual QSPI	-	Dual Flash Memory on TE0808 / TE0803 SoM; Bootable
13..23	SD0: eMMC	-	eMMC Memory U2; Bootable
24, 25	-	CPLD (U39) MUXED	-
26..29	-	CPLD (U17 MUXED	Bootable JTAG (PJTAG0)
30	force reboot after FSBL-PLL config for PCIe	CPLD (U39) MUXED	-
31	PCIe reset	CPLD (U39) MUXED	-
32	-	CPLD (U39) MUXED	-
33	-	CPLD (U39) MUXED	-
34..37	-	CPLD (U39) MUXED	-
38, 39	I2C0	-	-
40	forwarded to PWRLED_P / LED_P	CPLD (U39) MUXED	-
41	-	-	-
42, 43	UART0	CPLD (U39) MUXED	-
44	SD_WP to FPGA	CPLD (U39) MUXED	-
45..51	SD1: SD	-	Bootable MikroSD / MMC Card
52..63	USB0	-	-
64..75	GEM3	-	Ethernet RGMII
76, 77	MDC / MDIO	-	Ethernet RGMII

Table 8: MIO Assignment

Following interfaces are provided by the MIO bank of the Zynq Ultrascale+ MPSoC:

- 4x USB3.0 Superspeed ports (downward compatible to USB2.0 Highspeed)
- SDIO port with muxed MikroSD and MMC Card socket
- Gigabit Ethernet interface connected per RGMII

- eMMC interface
- Master I²C interface to on-board peripherals

The block-diagram below visualizes the interfaces of the MIO bank at the Zynq Ultrascale+ MPSoC and their associated on-board peripherals.

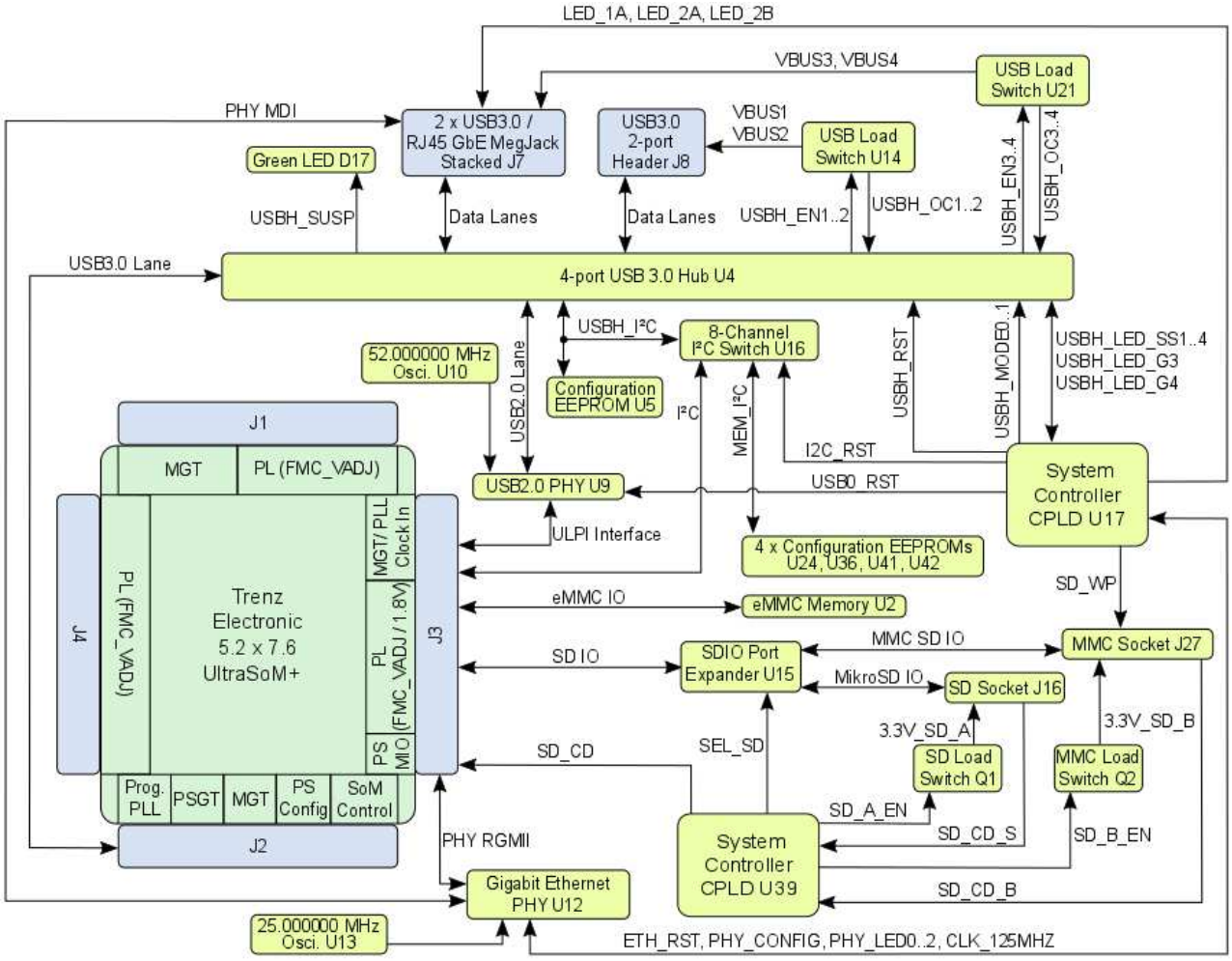

Figure 4: TEBF0808 MIO Interfaces

3.3 PS GT Bank Interfaces

The PS GT Bank 505 provides beside the USB3.0 Lane also following interfaces:

- SATA (PS GT bank, MGT2 Lane)
- DisplayPort (PS GT bank, MGT3 Lane, only TX-pair routed)
- PCI Express (PS GT bank, MGT0 Lane)

Function	MGT Lane	Schematic Names / B2B pins	Required Ref Clock	Clock Source	Comment
PCIe	PS 0	PCI_TX_N, pin J2-67 PCI_TX_P, pin J2-69 PCI_RX_N, pin J2-70 PCI_RX_P, pin J2-72	100 MHz	clock signal of SoM's prog. PLL	single lane PCIe connector clock signal routed on carrier board to PCIe connector J1
USB3	PS 1	USB3_TXUP_N, pin J2-61 USB3_TXUP_P, pin J2-63 USB3_RXUP_N, pin J2-64 USB3_RXUP_P, pin J2-66	100 MHz	clock signal of SoM's prog. PLL	clock signal routed on-module, Optional (not equipped) 100 MHz osci. U6 is possible (Configurable on Zynq PS).
SATA	PS 2	SATA_TX_N, pin J2-55 SATA_TX_P, pin J2-57 SATA_RX_N, pin J2-58 SATA_RX_P, pin J2-60	150 MHz	On-board oscillator U23	optional: clock signal of SoM's prog. PLL
DP.0	PS 3	DP0_TX_N, pin J2-49 DP0_TX_P, pin J2-51	27 MHz	clock signal of SoM's prog. PLL	DisplayPort GT SERDES clock signal, routed on-module to MGT bank

Table 9: PS GT Lane Assignment

Following block diagram shows the wiring of the MGT Lanes of the PS GT bank 505 to the particular high speed data interfaces:

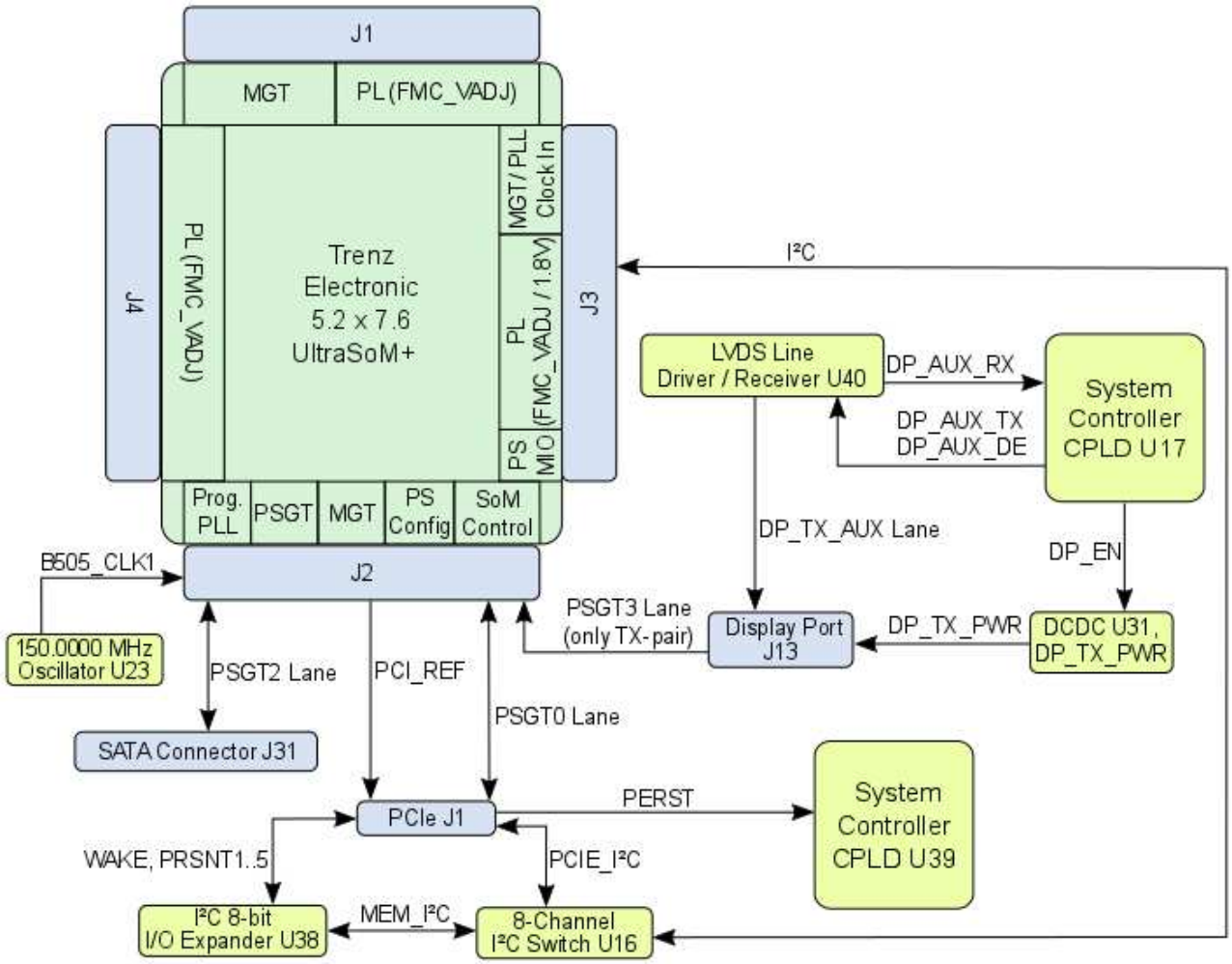

Figure 5: TEBF0808 PS GT Bank 505 Interface

Follwowing table contains a brief description of the control and status signals of PCIe interface:

Signal Schematic Name	FPGA Direction	Description	Logic
WAKE	Input	Link reactivation	Low active
PERST	Input	PCI Express reset input	Low active
PRSNT1	Input	Reference pin for PCIe card lane size	-
PRSNT2	Input	PCI Express ×1 cards	connect to PRSNT1
PRSNT3	Input	PCI Express ×4 cards	connect to PRSNT1
PRSNT4	Input	PCI Express ×8 cards	connect to PRSNT1
PRSNT5	Input	PCI Express ×16 cards	connect to PRSNT1
PCIE_I^{2}C	BiDir	2-wire PCIE System Management Bus	-

Table 10: Description of MGT Connectors Control and Status Signals

3.4 MGT Interfaces SFP+ and FireFly

The TEBF0808 carrier board provides the high speed MGT interface connectors "SFP+" (Enhanced small form-factor pluggable) and Samtec "FireFly". This connectors are capable of data transmission rates up to 10 Gbit/s with SFP+ and 28 Gbit/s with FireFly.

Function	MGT Lane	Schematic Names / B2B pins	Required Ref Clock	Clock Source	Comment
FireFly	MGT Lanes 0..3	B128_RX3_N, B128_RX3_P, pins J2-28, J2-30 B128_TX3_N, B128_TX3_P, pins J2-25, J2-27 B128_RX2_N, B128_RX2_P, pins J2-34, J2-36 B128_TX2_N, B128_TX2_P, pins J2-31, J2-33 B128_RX1_N, B128_RX1_P, pins J2-40, J2-42 B128_TX1_N, B128_TX1_P, pins J2-37, J2-39 B128_RX0_N, B128_RX0_P, pins J2-46, J2-48 B128_TX0_N, B128_TX0_P, pins J2-43, J2-45	-	clock signal of SoM's prog. PLL	clock signal on-module routed to MGT bank
SFP	MGT Lane 2	B230_RX2_P, pin J1-9 B230_RX2_N, pin J1-11 B230_TX2_P, pin J1-8 B230_TX2_N, pin J1-10	125 / 156.25 MHz	clock signal of SoM's prog. PLL	clock signal routed on carrier board to MGT bank
SFP	MGT Lane 3	B230_RX3_P, pin J1-3 B230_RX3_N, pin J1-5 B230_TX3_P, pin J1-2 B230_TX3_N, pin J1-4	125 / 156.25 MHz	clock signal of SoM's prog. PLL	clock signal routed on carrier board to MGT bank

Table 11: MGT Lane Assignment

Following block diagram show the wiring of the MGT lanes to the particular interface connectors:

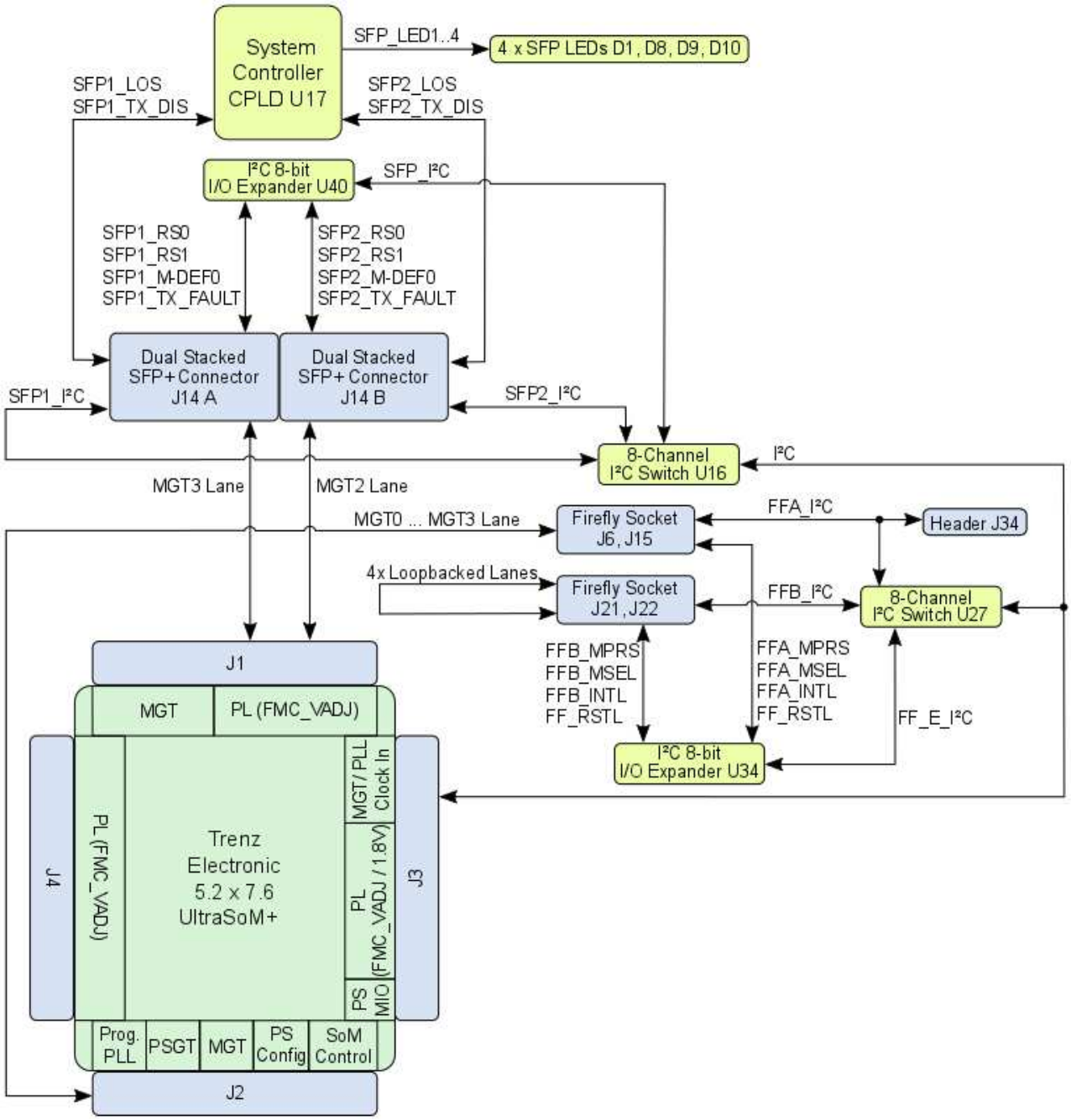

Figure 6: TEBF0808 MGT Interfaces

As shown on the block diagram, the FireFly connector pair J21, J22 provides four reversed looped back MGT lanes. To test any of the on-board MGT lanes or of an extern device, 4 RX/TX differential pairs are bridged on the connector, hence the transmitted data on these MGT lanes flows back to their sources in a loop-back circuit without intentional processing or modification.

Follwowing table contains a brief description of the control and status signals of the MGT lanes incorporating SFP+ and Samtec FireFly connectors:

Signal Schematic Name	Connector Type	FPGA Direction	Description	Logic
SFPx_TX_DISABLE	SFP+	Output	SFP Enabled / Disabled	Low active

Signal Schematic Name	Connector Type	FPGA Direction	Description	Logic
SFPx_LOS	SFP+	Input	Loss of receiver signal	High active
SFPx_RS0	SFP+	Output	Full RX bandwidth	Low active
SFPx_RS1	SFP+	Output	Reduced RX bandwidth	Low active
SFPx_M-DEF0	SFP+	Input	Module present / not present	Low active
SFPx_TX_FAULT	SFP+	Input	Fault / Normal Operation	High active
SFPx_I^{2}C	SFP+	BiDir	2-wire Serial Interface	-
FFx_MPRS	FireFly	Output	depending on connected module	-
FFx_MSEL	FireFly	Output	depending on connected module	-
FFx_INTL	FireFly	Input	Module interrupt line	-
FFx_RSTL	FireFly	Output	Module reset line	-
FFx_I^{2}C	FireFly	BiDir	2-wire Serial Interface	-

Table 12: Description of MGT Connectors Control and Status Signals

3.5 CAN FD Interface and PMOD Connectors

On the carrier board there is a CAN FD (CAN with Flexible Data-Rate) interface available which is accessible on the CAN headers J24 (10-pin IDC connector) or J29 (6-pin header), which are connected to the CAN FD transceiver U30.

Additionally the carrier board provides PMOD connectors with GPIO and I^{2}C interface:

PMOD	Interface	Connected to	Notes
P1	I^{2}C	8-channel I^{2}C Switch U27	Accessible on MPSoC's I^{2}C interface through I^{2}C switch U27
P2	GPIO	HP Bank of MPSoC (4 I/O's, B65_T0 ... B65_T3), System Controller CPLD U17 (4 I/O's, EX_IO1 ... EX_IO4)	Voltage translation via IC U33 with direction control, only singled-ended signaling possible
P3	I^{2}C	8-channel I^{2}C Switch U27	Accessible on MPSoC's I^{2}C interface through I^{2}C switch U27

Table 13: PMOD Pin Assignment

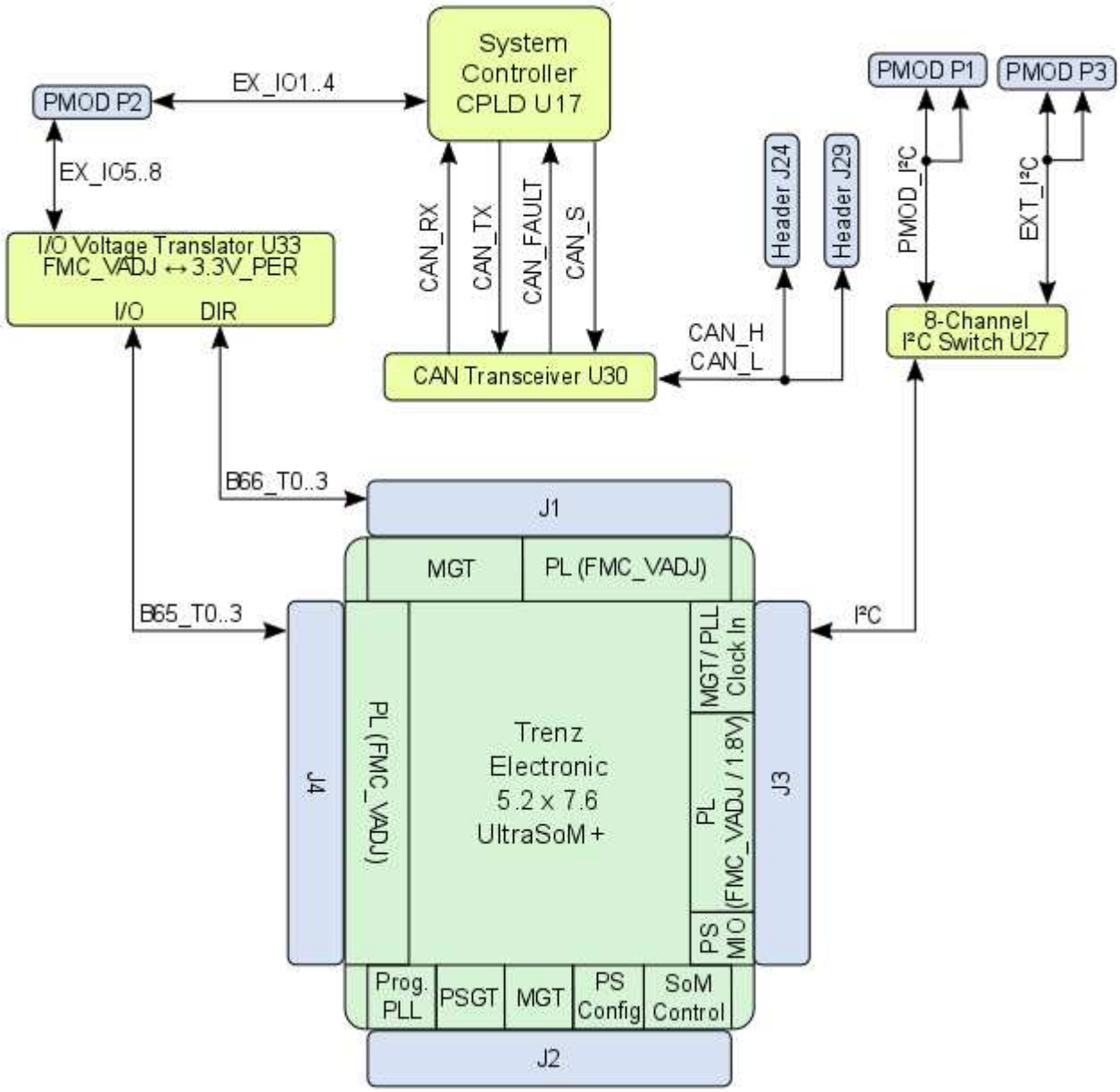

Figure 7: TEBF0808 CAN Interfaces, PMOD

3.6 Intel-PC Compatible Headers and FAN Connectors

The TEBF0808 carrier board provides with its Mini-ITX form factor the possibility to encase the boa rd in a PC Enclosure. For this purpose, the board is equipped with several Intel-PC compatible headers to connect them to the PC Enclosure.

Headers are available for following PC front panel elements

- Reset Button
- Power Button
- Power LED
- Hard Disc (HD) LED
- Intel High Definition Audio (HDA) Jacks

Following table gives an overview about the particular headers and a description about their functionalities:

Header	Pin Name	Functionality	Connected to	Notes
J10	Pin 1, HD LED+ Pin 3, HD LED- Pin 2, PWRLED+ Pin 4, PWRLED- Pin 5, GND Pin 7, RSTSW Pin 6, PWRSW Pin 8, GND Pin 9, +5V DC	HD LED Anode HD LED Cathode Power LED Anode Power LED Cathode Ground Reset Switch Power Switch Ground 5V DC Supply	SC CPLD U39	Reset and Power switch-pins are also connected to switch buttons S1 and S2
J9	Pin 1, PORT1L Pin 3, PORT1R Pin 9, PORT2L Pin 5, PORT2R Pin 7, SENS_SEND Pin 2, GND	Microphone Jack Left Microphone Jack Right Audio Out Jack Left Audio Out Jack Right Jack Detect / Mic in Ground	24-bit Audio Codec U3	-
J23	Pin 1, 3V3SB Pin 4, S1	3.3V DC Supply PC compatible Beeper	SC CPLD U39	-
J26	Pin 1, GND Pin 2, 12V Pin 3, F1SENSE Pin 4, F1PWM	Ground 12V DC Supply RPM PWM	SC CPLD U39	4-wire PWM FAN connector
J35	Pin 1, GND Pin 2, 12V Pin 3, F2SENSE Pin 4, F2PWM	Ground 12V DC Supply RPM PWM	SC CPLD U39	4-wire PWM FAN connector optional load switch U48 to turn off/on FAN with pin F2_EN
J19	Pin 1, GND Pin 2, 5V	Ground 5V DC Supply	Load Switch Q3 (5V DC)	2-wire FAN connector Fan off/on switchable by signal 'FAN_FMC_EN' on SC CPLD U39

Table 14: PC compatible Headers

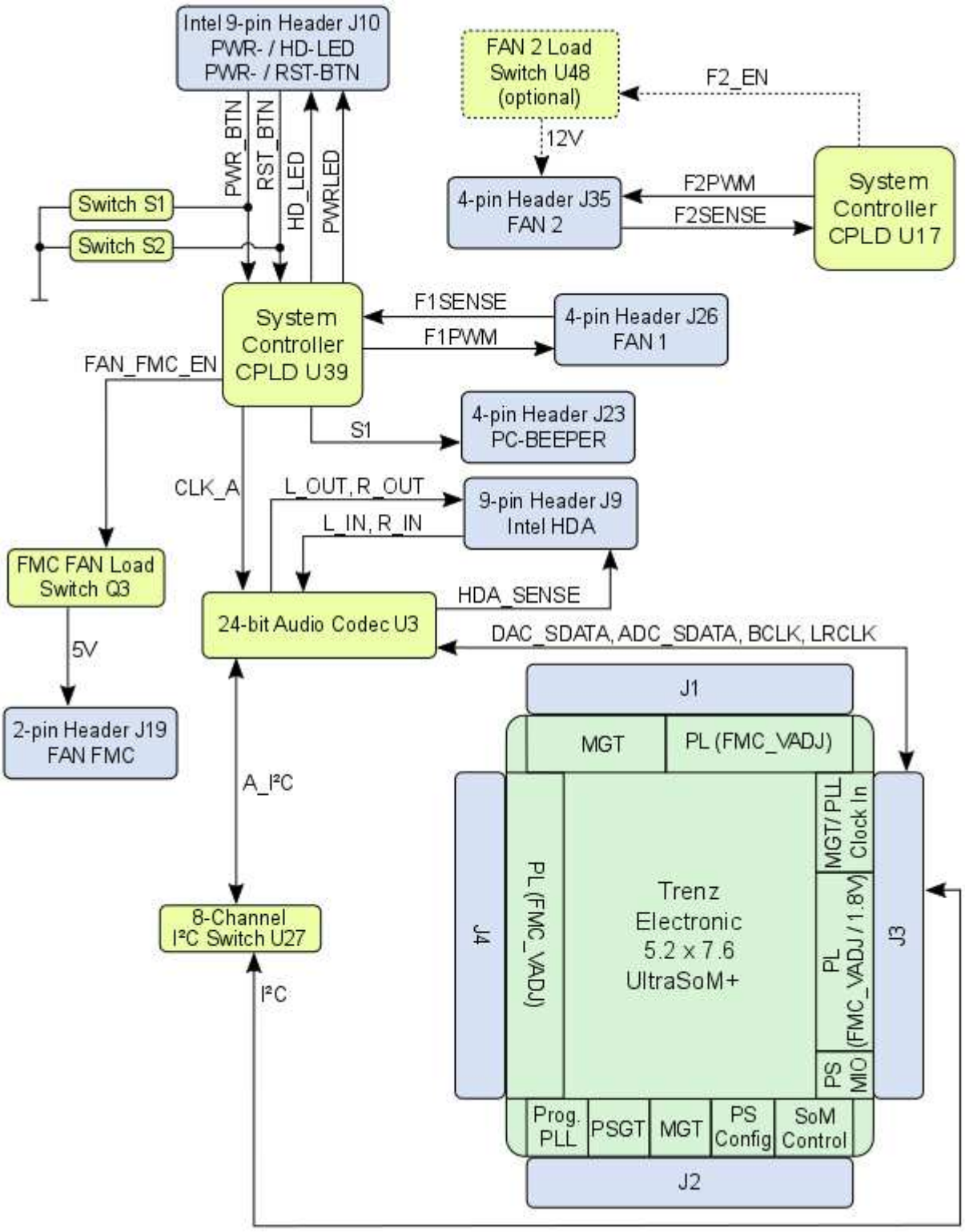

Figure 8: TEBF0808 PC Compatible Headers

3.7 JTAG Interface

The TEBF0808 carrier board provides several JTAG interfaces to program both the System Controller CPLDs and the Zynq Ultrascale+ MPSoC.

Therefore, the board is equipped with two JTAG/UART headers, which have 'XMOD FTDI JTAG Adapter'-compatible pin-assignment. So in use with the XMOD-FT2232H adapter-board TE0790 the mounted SoM and the System Controller CPLDs can be programmed via USB interface.

The System Controller CPLDs will be programmed by the XMOD-Header J28 in a cascaded JTAG chain as visualized in Figure 8. To program the System Controller CPLDs, the JTAG interface of these devices have to be activated by DIP-switch S4-3.
The 4 GPIO/UART pins (XMOD1_A/B/E/G) of the XMOD-Header J28 are routed to the System Controller CPLD U17.

XMOD-Header J12 is designated to program the Zynq Ultrascale+ MPSoC via USB interface, the 4 GPIO/UART pins (XMOD2_A/B/E/G) of this header are routed to the System Controller CPLD U39.

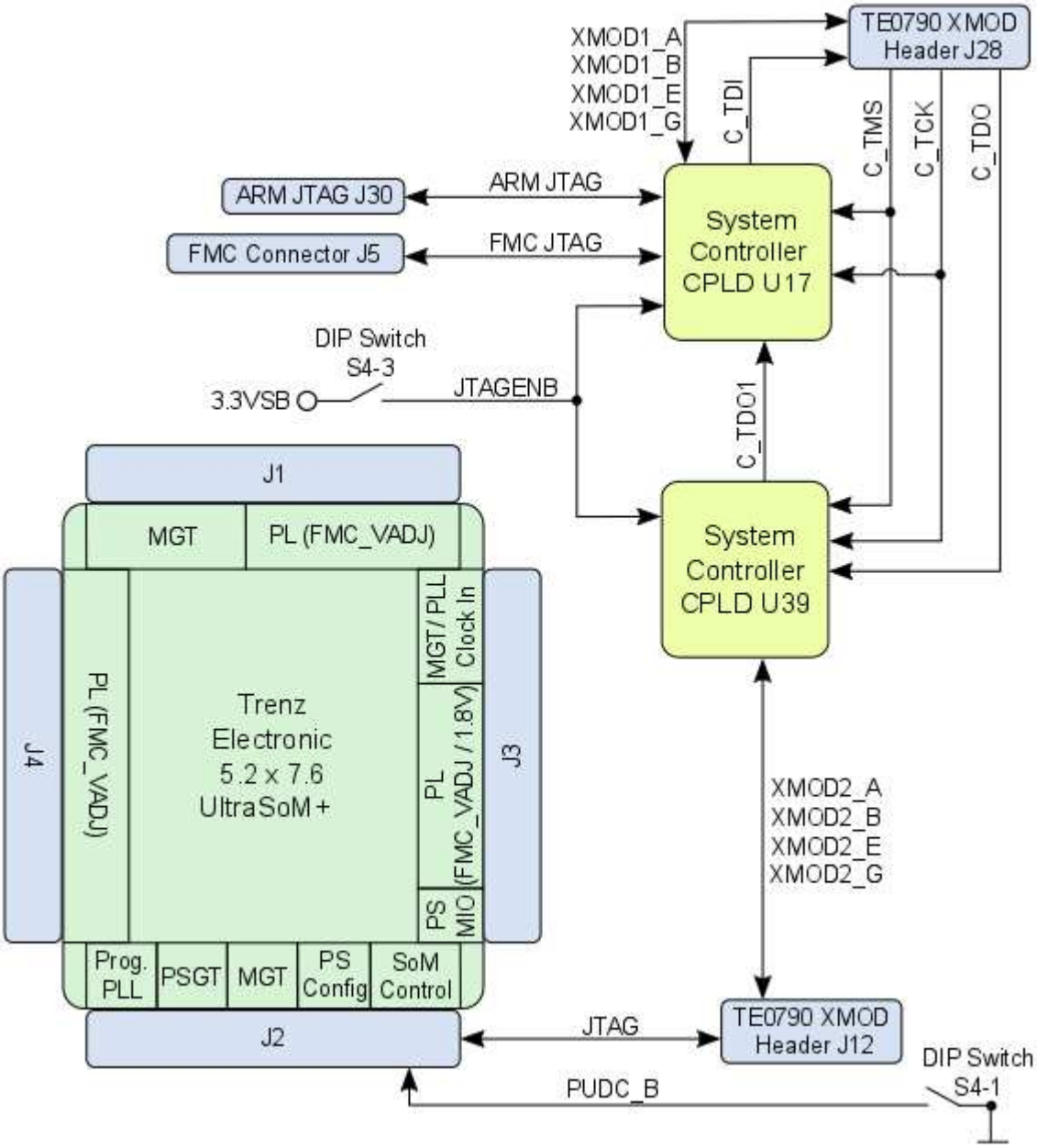

Figure 9: TEBF0808 JTAG interfaces

Further JTAG interfaces of the TEBF0808 carrier board are the ARM JTAG 20-pin IDC connector J30 and on the FMC Connector J5. This JTAG interfaces are connected to the System Controller CPLD U17, hence the logical processing and forwarding of the JTAG signals depend on the SC CPLD firmware. The documentation of the firmware of the SC CPLD U17 contains detailed information on this matter.

4 On-board Peripherals

4.1 System Controller CPLDs

The TEBF0808 is equipped with two System Controller CPLDs - Lattice Semiconductor LCMXO2-1200HC (MachXO2 Product Family) - with the schematic designators U17 and U39.

The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic of the CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA-module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

Both System Controller CPLDs are connected to the Zynq Ultrascale+ MPSoC through MIO, PL IO-bank pins and I^2C interface. The CPLDs are connected with each other through the IO pins SC_IO0 ... SC_IO8.

The functionalities and configuration of the pins depend on the CPLDs' firmware. The documentations of the firmware of SC CPLD U17 and SC CPLD U39 contains detailed information on this matter.

Following block diagram visualizes the connection of the SC CPLDs with the Zynq Ultrascale+ MPSoC via PS (MIO), PL bank pins and I^2C interface.

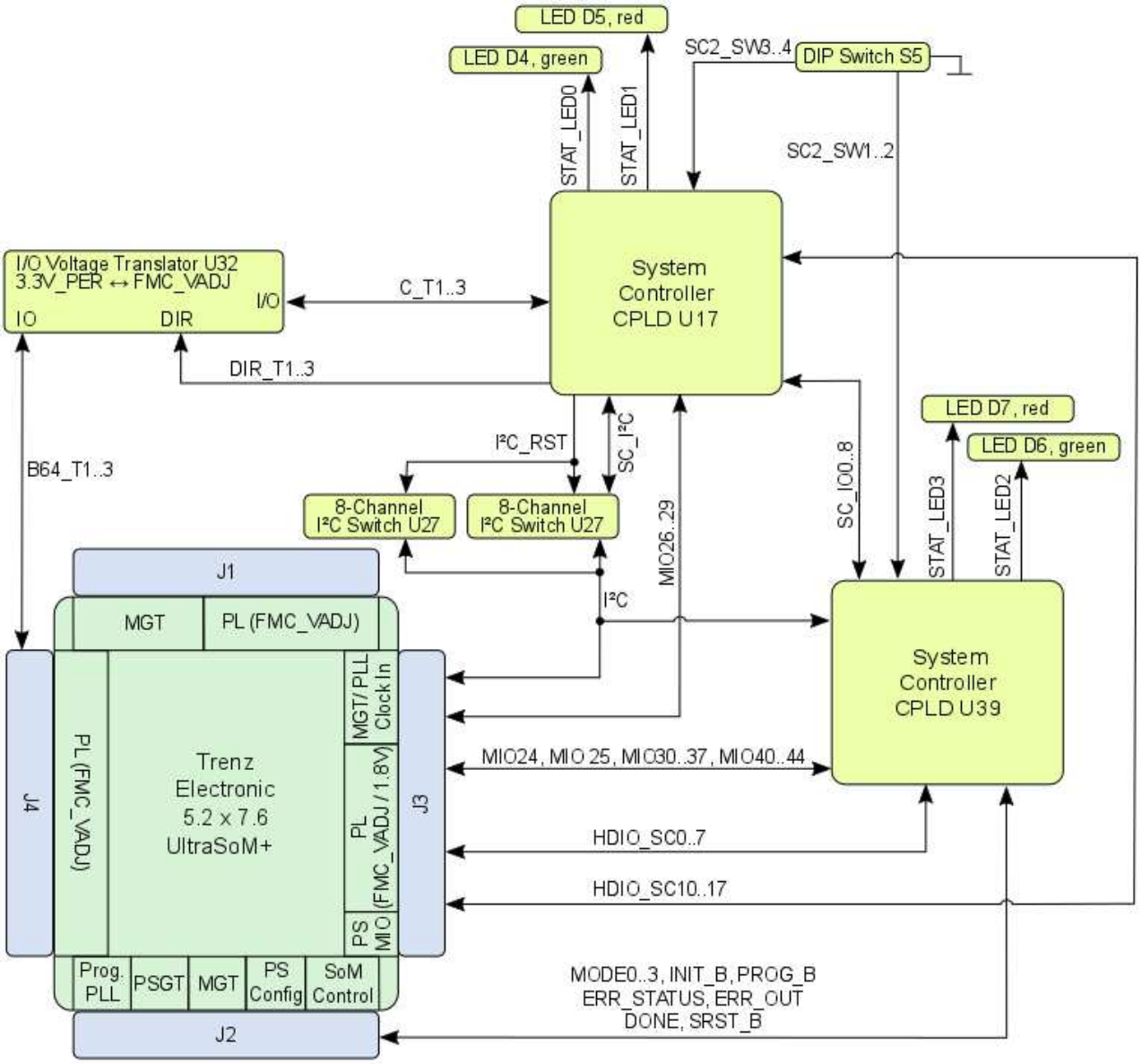

Figure 10: TEBF0808 System Controller CPLDs

4.2 Programmable PLL Clock Generator

The TEBF0808 carrier board is equipped with a Silicon Labs I²C programmable quad PLL clock generator Si5338A (U35). It's output frequencies can be programmed by using the I²C bus with address 0x70.

A 25 MHz (U7) oscillator is connected to pin 3 (IN3) and is used to generate the output clocks.

Once running, the frequency and other parameters can be changed by programming the device using the I²C-bus connected through I²C switch U16 between the Zynq module (master) and reference clock signal generator (slave).

Si5338A (U35) Input	Signal Schematic Name	Note
IN1/IN2	CLK8C_P, CLK8C_N	Clock signal of SoM's prog. PLL