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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





TEF6730

Front-end for digital-IF car radio

Rev. 01 — 10 July 2006

Product data sheet

1. General description

The TEF6730 is a car radio tuner front-end for digital-IF reception, especially designed for co-operation with digital-IF DSP back-ends of the SAF773x and SAF778x families.

The FM tuner features single conversion to IF = 10.7 MHz and integrated image rejection; capable for FM 65 MHz to 108 MHz and weather band reception. The AM tuner features single conversion to IF = 10.7 MHz with an integrated AM front-end, capable for LW, MW and full SW reception. A combined AM/FM IF AGC amplifier provides a suitable IF signal to the ADC in IF DSP.

The device can be controlled via the fast-mode I²C-bus (400 kHz) and includes autonomous tuning functions for easy control. No manual alignments are required.

2. Features

- FM mixer for conversion of FM RF to IF 10.7 MHz with large dynamic range, high image rejection and selectable mixer gain
- Selectable high or low injection of LO
- AGC PIN diode drive circuit for FM RF AGC with detection at RF and IF, including keyed AGC function
- RF input for weather band applications
- Integrated AM front-end LNA
- Integrated AM RF AGC for low desensitization and AGC PIN diode drive circuit with detection at RF and IF
- AM mixer for conversion of AM RF to IF 10.7 MHz
- AM/FM IF AGC amplifier with large dynamic range, gain controlled from IF DSP
- AM and FM front-end AGC information is available via the I²C-bus
- Low phase noise local oscillator with reliable start-up behavior
- In-lock detection for optimized adaptive PLL tuning speed
- Programmable divider and mixer dividers for reception of FM (65 MHz to 108 MHz), weather band, AM LW, MW and full SW
- Two antenna DAAs
- Sequential state machine supporting all tuning actions including AFU for RDS
- Interfacing signals for IF AGC, FM keyed AGC, AFU and reference frequency to IF DSP for optimum system performance
- Software controlled flag outputs
- Selection of four I²C-bus addresses

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3. Quick reference data

Table 1. Quick reference data

$V_{CCA} = 8.5 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; see [Figure 25](#); all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CCA}	analog supply voltage	on pins V_{CC} , $V_{CC(PLL)}$, $V_{CC(VCO)}$, $V_{CC(RF)}$, $V_{CC(IF)}$, FMMIXOUT1, FMMIXOUT2, AMMIXOUT1 and AMMIXOUT2	8	8.5	9	V
Current in FM mode						
$I_{CC(tot)}$	total supply current		-	85.3	-	mA
Current in AM mode						
$I_{CC(tot)}$	total supply current		-	114.7	-	mA
Antenna Digital Auto Alignment (DAA)						
DAA1: pin DAAOUT1 ^[1]						
$G_{conv(DAA)}$	DAA conversion gain		0.1	-	2	
DAA2: pin DAAOUT2 ^[2]						
$G_{conv(DAA)}$	DAA conversion gain		0.7	-	1.35	
Reference frequency						
External reference frequency, circuit inputs: pins FREF1 and FREF2						
f_{ext}	external frequency		-	100	-	kHz
Tuning system; see Table 28, Table 29, Table 30 and Table 31						
Voltage controlled oscillator						
$f_{VCO(min)}$	minimum VCO frequency		^[3] -	-	130	MHz
		application according to Figure 25	^[3] -	-	159.9	MHz
$f_{VCO(max)}$	maximum VCO frequency		^[3] 256	-	-	MHz
C/N	carrier-to-noise ratio	$f_{VCO} = 200 \text{ MHz}$; $\Delta f = 10 \text{ kHz}$; $Q = 30$	94	98	-	dBc/√Hz
Timings						
t_{tune}	tuning time	Europe FM/US FM band; $f_{ref} = 100 \text{ kHz}$; $f_{RF} = 87.5 \text{ MHz}$ to 108 MHz	-	0.75	1	ms
		AM MW band; $f_{ref} = 20 \text{ kHz}$; $f_{RF} = 0.53 \text{ MHz}$ to 1.7 MHz	-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time	-	6	6.5	ms
AM overall system parameters^[4]						
$f_{i(RF)}$	RF input frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
f_{IF}	IF frequency		-	10.7	-	MHz
V_{sens}	sensitivity voltage	$(S+N)/N = 26 \text{ dB}$	-	50	-	μV

Table 1. Quick reference data ...continued $V_{CCA} = 8.5 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; see [Figure 25](#); all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{i(RF)}$	RF input voltage	start level of wideband AGC					
		data byte AGC bits WBAGC[1:0] = 00	-	125	-	mV	
		data byte AGC bits WBAGC[1:0] = 01	-	100	-	mV	
		data byte AGC bits WBAGC[1:0] = 10	-	75	-	mV	
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0					
		data byte AGC bits NBAGC[1:0] = 00	-	200	-	mV	
		data byte AGC bits NBAGC[1:0] = 01	-	170	-	mV	
		data byte AGC bits NBAGC[1:0] = 10	-	140	-	mV	
IP2	second-order intercept point	referenced to receiver input	-	152	-	dB μ V	
		third-order intercept point	$\Delta f = 40 \text{ kHz}$	-	130	-	dB μ V
			$\Delta f = 100 \text{ kHz}$	-	133	-	dB μ V
			ripple rejection	$V_{CC(ripple)}/V_{audio}$; $f_{ripple} = 100 \text{ Hz}$; $V_{CC(ripple)} = 10 \text{ mV (RMS)}$; $V_{i(RF)} = 1 \text{ mV to } 1 \text{ V}$	-	40	-
FM overall system parameters^[5]							
$f_{i(RF)}$	RF input frequency	FM standard	65	-	108	MHz	
		weather band	162.4	-	162.55	MHz	
f_{IF}	IF frequency		-	10.7	-	MHz	
V_{sens}	sensitivity voltage	$B_{IF} = 170 \text{ kHz}$	-	2	-	μ V	
		threshold extension enabled; weak signal handling enabled (SAF7730 N231)	-	1.1	-	μ V	
$V_{i(RF)}$	RF input voltage	start level of wideband AGC					
		data byte AGC bits WBAGC[1:0] = 00	-	19	-	mV	
		data byte AGC bits WBAGC[1:0] = 01	-	14	-	mV	
		data byte AGC bits WBAGC[1:0] = 10	-	10	-	mV	
$V_{i(RF)M}$	peak RF input voltage	start level of narrow-band AGC; m = 0					
		data byte AGC bits NBAGC[1:0] = 00	-	17	-	mV	
		data byte AGC bits NBAGC[1:0] = 01	-	14	-	mV	
		data byte AGC bits NBAGC[1:0] = 10	-	11	-	mV	
IP3	third-order intercept point	$\Delta f = 400 \text{ kHz}$	-	123	-	dB μ V	
		ripple rejection	$V_{CC(ripple)}/V_{audio}$; $f_{ripple} = 100 \text{ Hz}$; $V_{CC(ripple)} = 10 \text{ mV (RMS)}$; $V_{i(RF)} = 500 \text{ } \mu\text{V}$	-	64	-	dB

[1] Conversion gain formula of DAA1: $V_{DAAOUT1} = \left(1.915 \times \frac{n}{128} + 0.1\right) \times V_{tune}$ where n = 0 to 127.

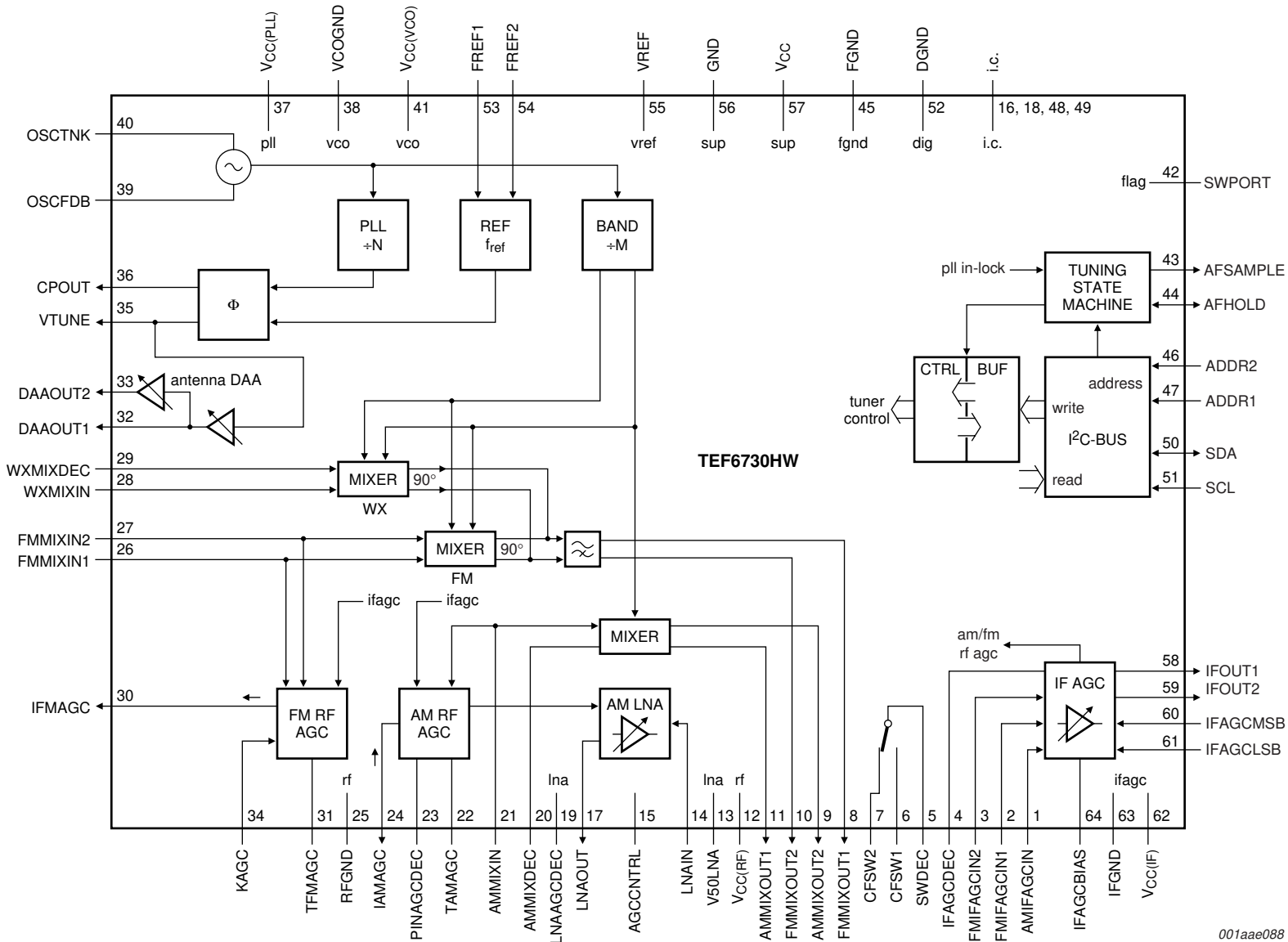
- [2] Conversion gain formula of DAA2: $V_{DAAOUT2} = \left(0.693 \times \frac{n}{16} + 0.7\right) \times V_{DAAOUT1}$ where $n = 0$ to 15.
- [3] The VCO frequency is determined by the external circuit at pins OSCFDB and OSCTNK.
- [4] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, $f_{mod} = 400$ Hz, 2.5 kHz audio bandwidth, $f_{i(RF)} = 990$ kHz, $m = 0.3$ and nominal maximum IF AGC gain, unless otherwise specified.
- [5] Based on 75 Ω dummy aerial, voltages at dummy aerial input, $f_{mod} = 400$ Hz, de-emphasis = 50 μ s, $f_{i(RF)} = 97.1$ MHz, $\Delta f = 22.5$ kHz, nominal mixer gain and nominal maximum IF AGC gain, unless otherwise specified.

4. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
TEF6730HW	HTQFP64	plastic thermal enhanced thin quad flat package; 64 leads; body 10 x 10 x 1 mm; exposed die pad	SOT855-1

5. Block diagram



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Fig 1. Block diagram of TEF6730HW

6. Pinning information

6.1 Pinning

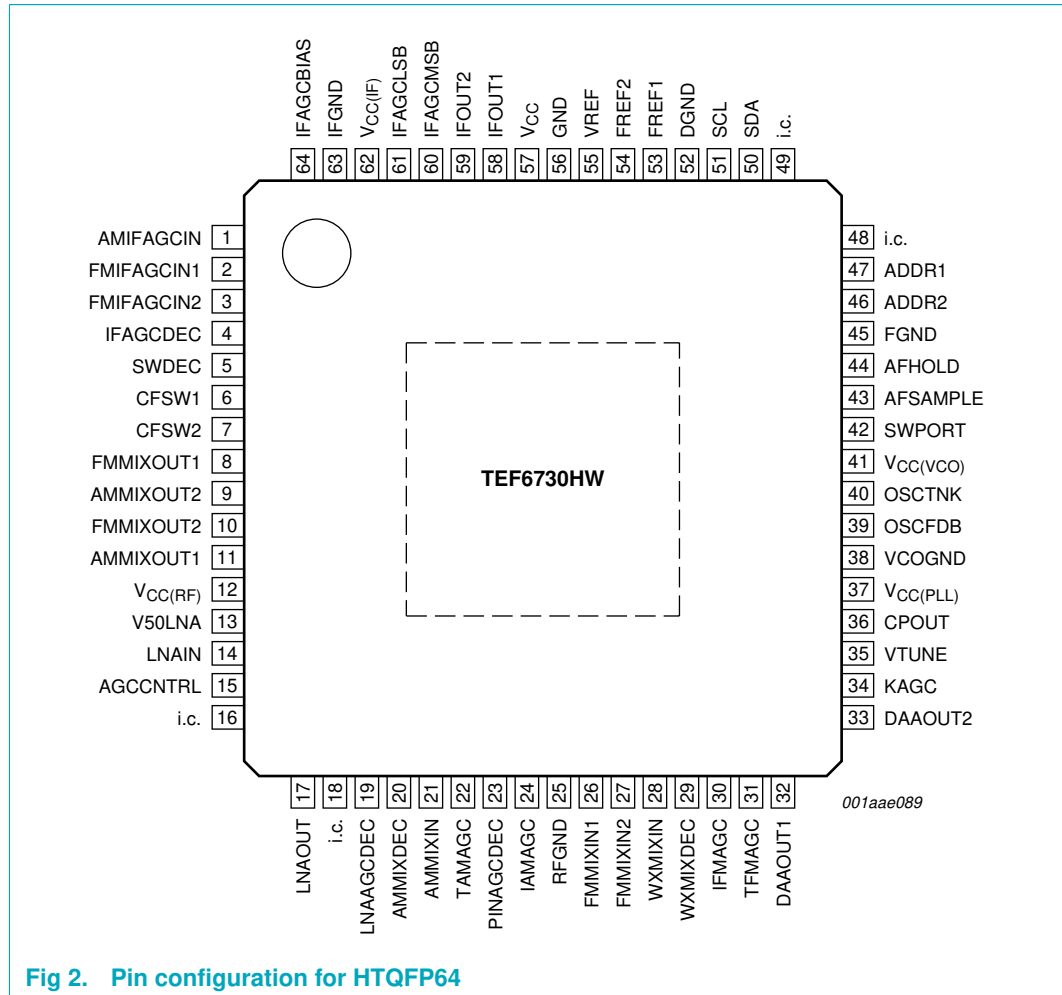


Fig 2. Pin configuration for HTQFP64

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
AMIFAGCIN	1	IF AGC amplifier AM input (10.7 MHz)
FMIFAGCIN1	2	IF AGC amplifier FM input 1 (10.7 MHz)
FMIFAGCIN2	3	IF AGC amplifier FM input 2 (10.7 MHz)
IFAGCDEC	4	IF AGC amplifier AM and FM decoupling
SWDEC	5	ceramic filter switch decoupling
CFSW1	6	ceramic filter switch 1
CFSW2	7	ceramic filter switch 2
FMMIXOUT1	8	FM mixer IF output 1 (10.7 MHz)
AMMIXOUT2	9	AM mixer IF output 2 (10.7 MHz)

Table 3. Pin description ...continued

Symbol	Pin	Description
FMMIXOUT2	10	FM mixer IF output 2 (10.7 MHz)
AMMIXOUT1	11	AM mixer IF output 1 (10.7 MHz)
V _{CC(RF)}	12	AM/FM RF supply voltage
V50LNA	13	AM LNA supply voltage decoupling
LNAIN	14	AM LNA input
AGCCNTRL	15	AM LNA AGC pin
i.c.	16	internally connected; leave open
LNAOUT	17	AM LNA output
i.c.	18	internally connected; leave open
LNAAGCDEC	19	AM LNA AGC decoupling
AMMIXDEC	20	AM mixer decoupling
AMMIXIN	21	AM mixer input
TAMAGC	22	AM RF AGC time constant
PINAGCDEC	23	AM PIN diode AGC decoupling
IAMAGC	24	AGC current for AM PIN diode
RFGND	25	RF ground
FMMIXIN1	26	FM mixer input 1
FMMIXIN2	27	FM mixer input 2
WXMIXIN	28	weather band mixer input
WXMIXDEC	29	weather band mixer decoupling
IFMAGC	30	AGC current for FM PIN diode
TFMAGC	31	FM RF AGC time constant
DAAOUT1	32	antenna DAA output 1
DAAOUT2	33	antenna DAA output 2
KAGC	34	level input for FM keyed AGC function
VTUNE	35	tuning voltage input antenna DAA
CPOUT	36	charge pump output
V _{CC(PLL)}	37	tuning PLL supply voltage
VCOGND	38	VCO ground
OSCFDB	39	VCO feedback
OSCTNK	40	VCO tank circuit
V _{CC(VCO)}	41	VCO supply voltage
SWPORT	42	software controllable port output
AFSAMPLE	43	AF sample flag output
AFHOLD	44	AF hold flag output and input
FGND	45	reference frequency ground
ADDR2	46	address select input 2
ADDR1	47	address select input 1
i.c.	48	internally connected; leave open
i.c.	49	internally connected; leave open
SDA	50	I ² C-bus data line input and output

Table 3. Pin description ...continued

Symbol	Pin	Description
SCL	51	I ² C-bus clock line input
DGND	52	digital ground
FREF1	53	reference frequency input 1
FREF2	54	reference frequency input 2
VREF	55	reference voltage noise decoupling
GND	56	ground
V _{CC}	57	supply voltage (8.5 V)
IFOUT1	58	IF AGC amplifier output 1
IFOUT2	59	IF AGC amplifier output 2
IFAGCMSB	60	MSB input for IF AGC amplifier gain setting
IFAGCLSB	61	LSB input for IF AGC amplifier gain setting
V _{CC(IF)}	62	IF AGC amplifier supply voltage
IFGND	63	IF AGC amplifier ground
IFAGCBIAS	64	bias voltage decoupling for IF AGC amplifier

7. Functional description

7.1 FM mixer 1

The FM quadrature mixer converts FM RF (65 MHz to 108 MHz) to an IF frequency of 10.7 MHz. The FM mixer provides high image rejection, a large dynamic range and selectable mixer gain. The image rejection can be selected between low injection of LO and high injection of LO via the I²C-bus independently of the band selection. A separate RF input for weather band is available.

7.2 FM RF AGC

AGC detection at the FM front-end mixer input and the AM/FM IF AGC amplifier input, both with programmable AGC thresholds. When the threshold is exceeded, the PIN diode drive circuit sources a current to an external PIN diode circuit, keeping the RF signal level constant.

Keyed AGC function is selectable via the I²C-bus and uses the in-band level information from the IF DSP.

The AGC PIN diode drive circuit can optionally deliver a fixed current as a local function. In AM mode, the AGC PIN diode drive circuit can be set to generate a fixed source current into the external FM PIN diode circuitry.

7.3 Antenna DAA1 and DAA2

The antenna DAA1 measures the VCO tuning voltage and multiplies it with a factor defined by the 7-bit DAA1 setting to generate a tuning voltage for the FM antenna tank circuit. If a second FM tank circuit is applied, the tuning voltage can be derived from the antenna DAA2 output. The antenna DAA2 measures the output voltage of the antenna DAA1 and multiplies it with a factor defined by the 4-bit DAA2 setting.

7.4 AM LNA

The AM low noise amplifier is fully integrated.

7.5 AM RF AGC

The AM RF AGC is partially integrated. Detection is at the output of the AM LNA and at the input of the AM/FM IF AGC amplifier, both with programmable thresholds. First the integrated AGC reduces the gain of the LNA. After the LNA AGC, the PIN diode AGC takes over by sinking a current via an external PIN diode.

In FM mode, the AM AGC can be set to a fixed attenuation.

7.6 AM mixer

The large dynamic range AM mixer converts AM RF (144 kHz to 26.1 MHz) to an IF frequency of 10.7 MHz.

7.7 VCO and dividers

The varactor tuned LC oscillator together with the dividers provides the LO signal for both AM and FM front-end mixers. The VCO has an operating frequency of approximately 160 MHz to 256 MHz. In FM mode the LO frequency is divided by 2 or 3. These dividers generate in-phase and quadrature-phase output signals used in the FM front-end mixer for image rejection. In weather band mode the LO signal is directly phase shifted to generate the in-phase and quadrature-phase signals. In AM mode the LO frequency is divided by 6, 8, 10, 16 or 20 depending on the selected AM band.

7.8 Tuning PLL

The tuning PLL locks the VCO frequency divided by the programmable divider ratio to the reference frequency. Due to the combination of different charge pump signals in the PLL loop filter, the loop parameters are adapted dynamically. Tuning to different RF frequencies is done by changing the programmable divider ratio. The tuning step size is selected with the reference frequency divider setting.

7.9 AM/FM IF AGC amplifier

The combined AM/FM IF AGC amplifier delivers a suitable IF signal for the ADC in the IF DSP. The maximum gain of the IF AGC amplifier can be selected via the I²C-bus. The gain of this amplifier is automatically adapted via interfacing signals from the IF DSP. The IF AGC amplifier has three signal inputs, two for FM and one for AM. This allows the application of multiple external filters, e.g. with different bandwidths.

8. I²C-bus protocol

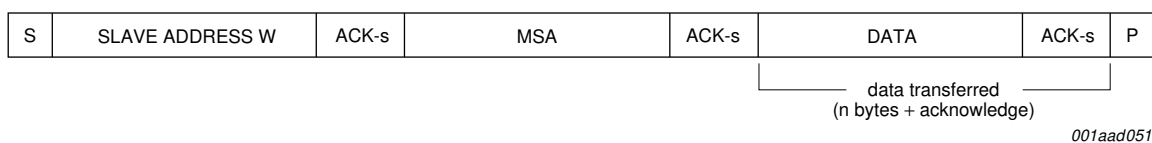


Fig 3. Write mode

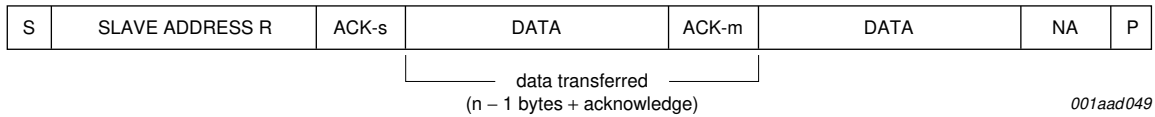


Fig 4. Read mode

Table 4. Description of I²C-bus format

Code	Description
S	START condition
Slave address W	1100 0000b for pin ADDR2 and pin ADDR1 grounded 1100 0010b for pin ADDR2 grounded and pin ADDR1 floating 1100 0100b for pin ADDR2 floating and pin ADDR1 grounded 1100 0110b for pin ADDR2 and pin ADDR1 floating
Slave address R	1100 0001b for pin ADDR2 and pin ADDR1 grounded 1100 0011b for pin ADDR2 grounded and pin ADDR1 floating 1100 0101b for pin ADDR2 floating and pin ADDR1 grounded 1100 0111b for pin ADDR2 and pin ADDR1 floating
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge
MSA	mode and subaddress byte
Data	data byte
P	STOP condition

8.1 Read mode

Read data is loaded into the I²C-bus register at the preceding acknowledge clock pulse.

Table 5. Read register overview

Data byte	Name	Reference
0h	TUNER	Section 8.1.1
1h	ID	Section 8.1.2

8.1.1 Read mode: data byte TUNER

Table 6. TUNER - data byte 0h bit allocation

7	6	5	4	3	2	1	0
RAGC1	RAGC0	TAS1	TAS0	-	-	-	POR

Table 7. TUNER - data byte 0h bit description

Bit	Symbol	Description
7 and 6	RAGC[1:0]	RF AGC attenuation indicator, PIN diode current on pin IFMAGC AM mode: 00 = no AGC 01 = LNA AGC 10 = $I_{AGC} < 1$ mA 11 = $I_{AGC} > 1$ mA FM mode: 00 = < 0.1 mA 01 = 0.1 mA to 0.5 mA 10 = 0.5 mA to 2.5 mA 11 = > 2.5 mA
5 and 4	TAS[1:0]	tuning action state; the signal TAS informs about internal control functions of the tuner action state machine; this way the progress of tuner actions can be monitored by the microcontroller; see Figure 8 to Figure 18 00 = no current action 01 = mute started and in progress at DSP 10 = PLL tuning in progress and mute activated at DSP 11 = PLL tuning ready and mute activated at DSP
3 to 1	-	not used
0	POR	power-on reset 0 = normal operation 1 = I ² C-bus data is reset to default POR state; POR is reset to logic 0 after the TEF6730 has been read out and written to via I ² C-bus at least once

8.1.2 Read mode: data byte ID

Table 8. ID - data byte 1h bit allocation

7	6	5	4	3	2	1	0
-	-	-	-	-	ID2	ID1	ID0

Table 9. ID - data byte 1h bit description

Bit	Symbol	Description
7 to 3	-	not used
2 to 0	ID[2:0]	device type identification 110 = TEF6730

8.2 Write mode

The tuner is controlled by the I²C-bus. After the IC address the MSA byte contains the control of the tuning action via the bits MODE[2:0] and REGC and subaddressing via bits SA[3:0] (see [Figure 5](#)).

The tuner circuit is controlled by the CONTROL register. Any data change in the CONTROL register has immediate effect and will change the operation of the tuner circuit accordingly. Transmitted I²C-bus data is not loaded into the CONTROL register directly but loaded into a BUFFER register instead. This allows the IC to take care of tuning actions freeing the microcontroller from cumbersome controls and timings.

Controlled by a state machine, the BUFFER data will be loaded into the CONTROL register for new settings. However, at the same time the CONTROL data is loaded into the BUFFER register. This register swap action allows a fast return to the previous setting because the previous data remains available in the BUFFER register (see [Figure 6](#) and [Figure 7](#)).

Via MODE several operational modes can be selected for the state machine. MODE offers all standard tuning actions as well as generic control for flexibility. The state machine controls the tuner by controlling the internal I²C-bus data. Action progress is monitored by the accompanying IF DSP via the AFSAMPLE and AFHOLD lines. This way, functions like tuning mute and weak signal processing can be controlled complementary to the tuner action.

The state machine operation starts at the end of transmission (P = STOP). In case a previous action is still active, this is ignored and the new action defined by MODE is started immediately. When only the address byte is transmitted, no action is started at all (device presence test).

To minimize the I²C-bus transmission time, only bytes that include data changes need to be written. Following the MSA byte the transmission can start at any given data byte defined by the subaddress (SA) bits.

Furthermore, when writing the buffered range either the current BUFFER data or the current CONTROL data can be used as default, controlled by the REGC bit:

- With REGC = 0, any BUFFER data that is not newly written via I²C-bus remains unchanged. In general, the BUFFER register will contain the previous tuner setting, so this becomes default for the new setting. When only the MSA byte is transmitted defining a tuning MODE with REGC = 0, the tuner will return to its previous settings (see [Figure 6](#)).
- With REGC = 1, the BUFFER register is loaded with data from the CONTROL register first. This way, not written BUFFER data equals the CONTROL data. Since the CONTROL register contains the current tuner setting with REGC = 1, the current tuner setting is default for the new setting. When a tuning MODE action is defined with REGC = 1, the tuner will keep its current settings (CONTROL = current) for all data that is not newly written during the transmission (see [Figure 7](#)).

After power-on reset, all registers are in their default settings. The control signals for the IF DSP are set to AFSAMPLE = HIGH and AFHOLD = HIGH (i.e. mute state). Any action of the state machine will change this setting to a new one as defined by the bits MODE[2:0].

Table 10. Write mode subaddress overview

Subaddress	Name	Default	Reference
0h	CONTROL	0000 0100b	Section 8.2.2
1h	PLLM	0000 1000b	Section 8.2.3
2h	PLLL	0111 1110b	Section 8.2.4
3h	DAA	0100 0000b	Section 8.2.5
4h	AGC	1000 0000b	Section 8.2.6
5h	BAND	0010 0000b	Section 8.2.7
Fh	TEST	0000 0000b	Section 8.2.8

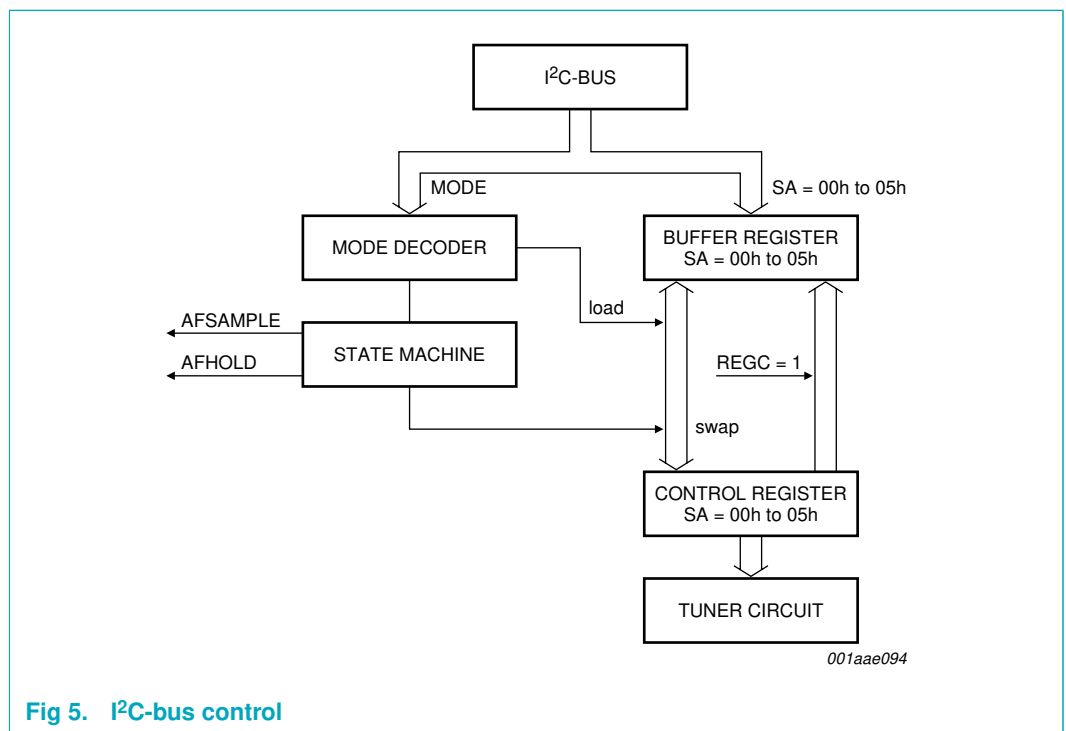


Fig 5. I2C-bus control

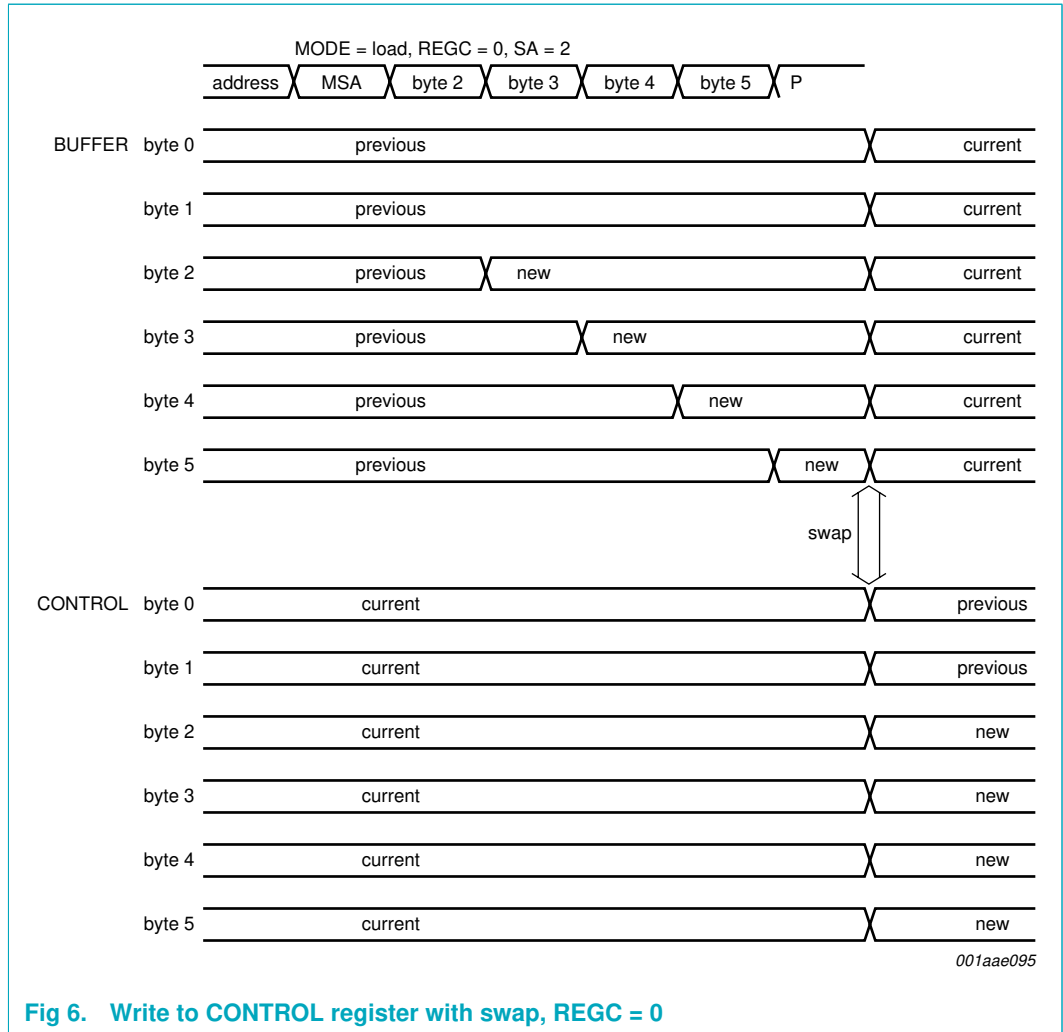


Fig 6. Write to CONTROL register with swap, REGC = 0

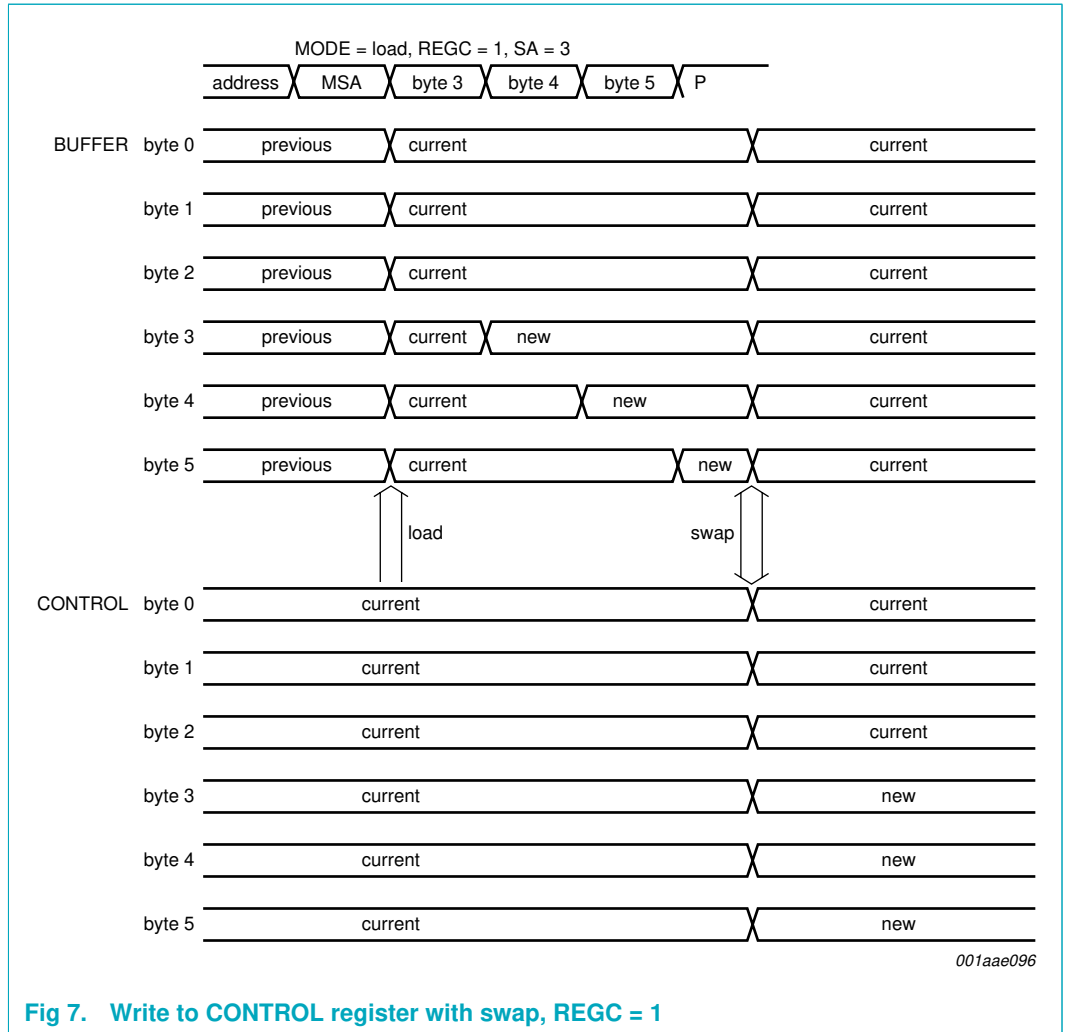


Fig 7. Write to CONTROL register with swap, REGC = 1

8.2.1 Mode and subaddress byte for write

Table 11. MSA - mode and subaddress byte bit allocation

7	6	5	4	3	2	1	0
MODE2	MODE1	MODE0	REGC	SA3	SA2	SA1	SA0

Table 12. MSA - mode and subaddress byte bit description

Bit	Symbol	Description
7 to 5	MODE[2:0]	mode; see Table 13
4	REGC	register mode 0 = buffer mode or back mode: previous tuning data is default for new I ² C-bus write (data of the BUFFER register is not changed before I ² C-bus write); see Figure 6 1 = control mode or current mode: current tuning data is default for new I ² C-bus write (the BUFFER register is loaded with CONTROL register data before I ² C-bus write); see Figure 7
3 to 0	SA[3:0]	subaddress; write data byte subaddress 0 to 15. The subaddress value is auto-incremented and will revert from SA = 15 to SA = 0. The auto-increment function cannot be switched off.

Table 13. Tuning action modes^[1]

MODE2	MODE1	MODE0	Symbol	Description ^[2]
0	0	0	buffer	write BUFFER register, no state machine action, no swap
0	0	1	preset	tune to new program with 60 ms mute control; swap ^[3] ; see Figure 8 and Figure 9
0	1	0	search	tune to new program and stay muted (for release use end mode); swap ^[3] ; see Figure 10 and Figure 11
0	1	1	AF update	tune to AF program; check AF quality and tune back to main program; two swap operations ^[4] ; see Figure 12 and Figure 13
1	0	0	jump	tune to AF program in minimum time; swap; see Figure 14 and Figure 15
1	0	1	check	tune to AF program and stay muted (for release use end mode); swap; see Figure 16 and Figure 17
1	1	0	load	write CONTROL register via BUFFER; no state machine action; immediate swap; see Figure 6 and Figure 7
1	1	1	end	end action; release mute; no swap; see Figure 18

[1] When the write transmission of a state machine command starts during a mute state of the state machine, the sequences of the state machine start immediately with the actions which follow the mute period in the standard sequence (see [Figure 9](#), [Figure 11](#), [Figure 13](#), [Figure 15](#) and [Figure 17](#)).

[2] References to mute are only used for better understanding. Muting is performed in the IF DSP controlled by the tuner AFHOLD and AFSAMPLE lines.

[3] In the modes preset and search the AM AGC time constant is set to fast during the period of complete mute.

[4] The AF update sequence can also be started by pulling the AFHOLD pin LOW. In this case the AF information should be loaded into the BUFFER before. LOW period for a correct AF update timing: $t_{LOW} > 20 \mu s$. Between the end of the I²C-bus transmission and the falling edge of the AFHOLD pulse a delay of $\geq 20 \mu s$ is necessary.

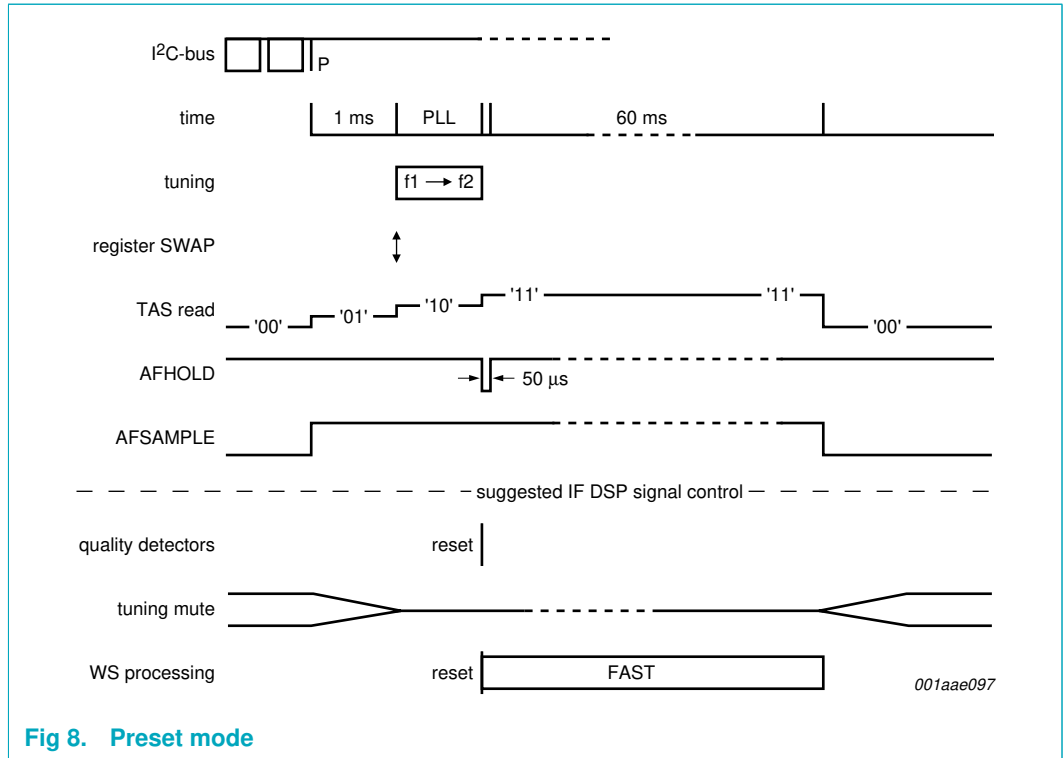


Fig 8. Preset mode

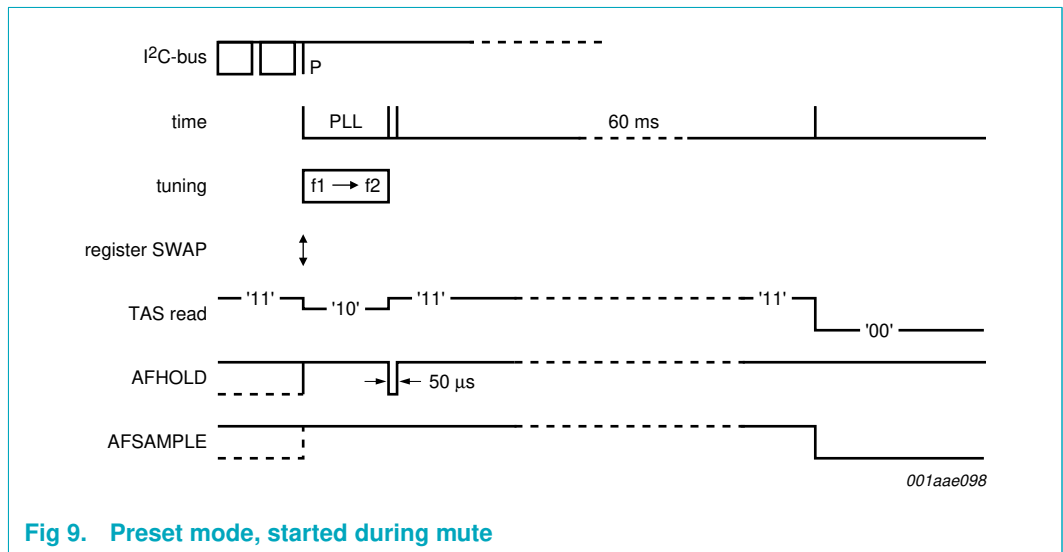


Fig 9. Preset mode, started during mute

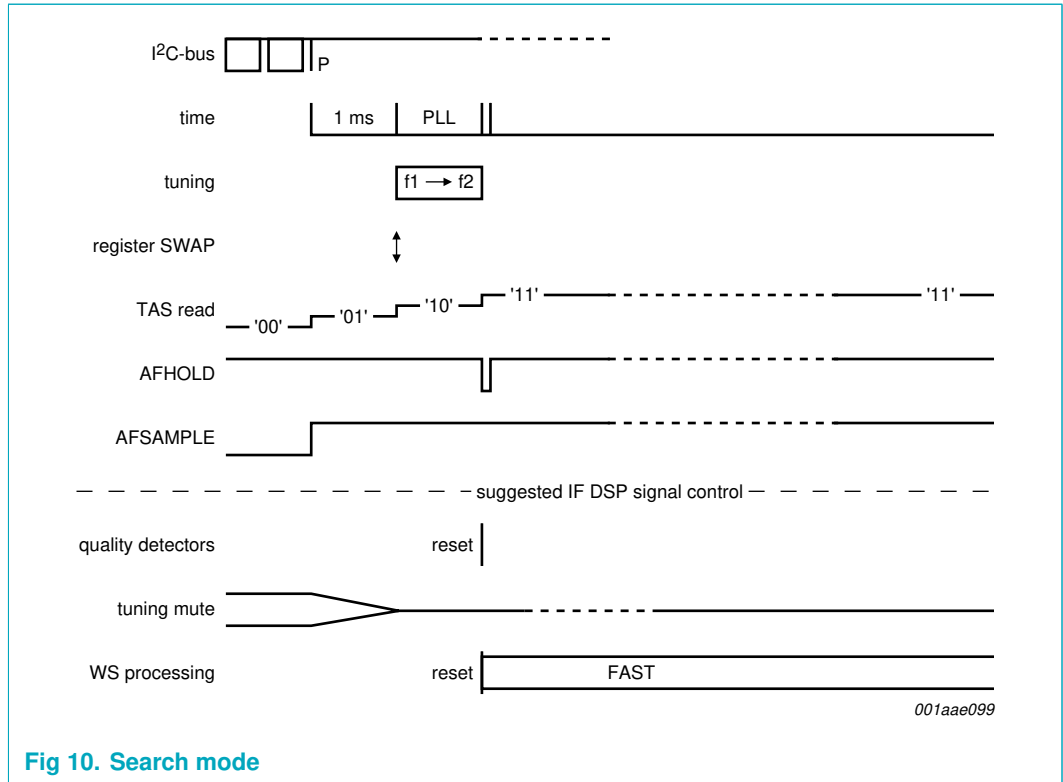


Fig 10. Search mode

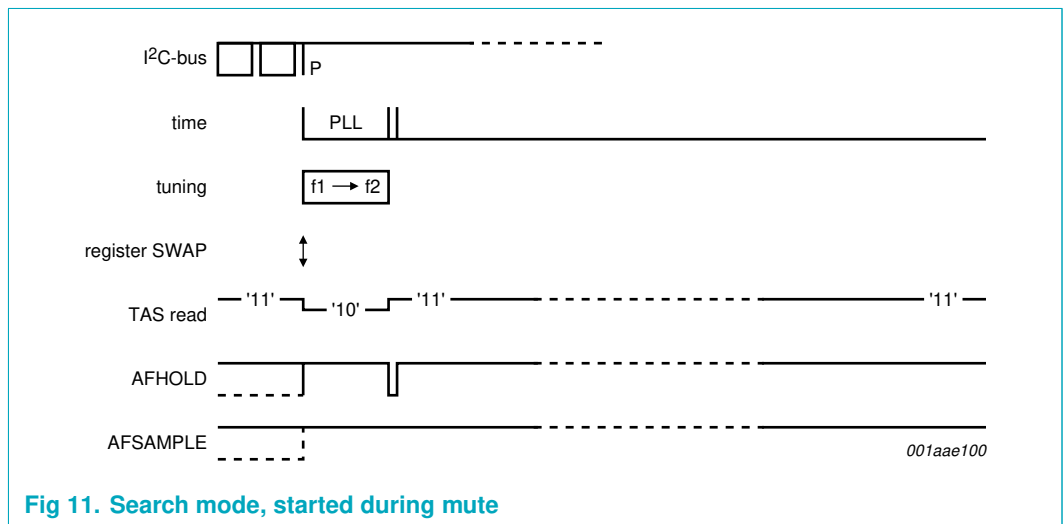


Fig 11. Search mode, started during mute

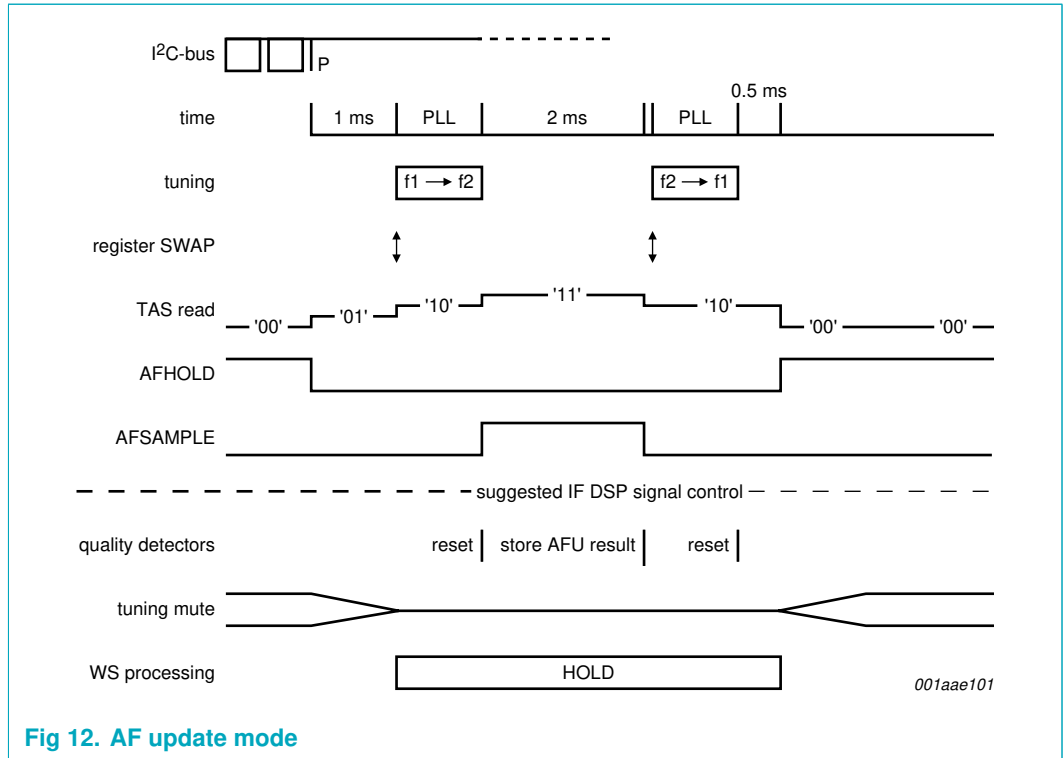


Fig 12. AF update mode

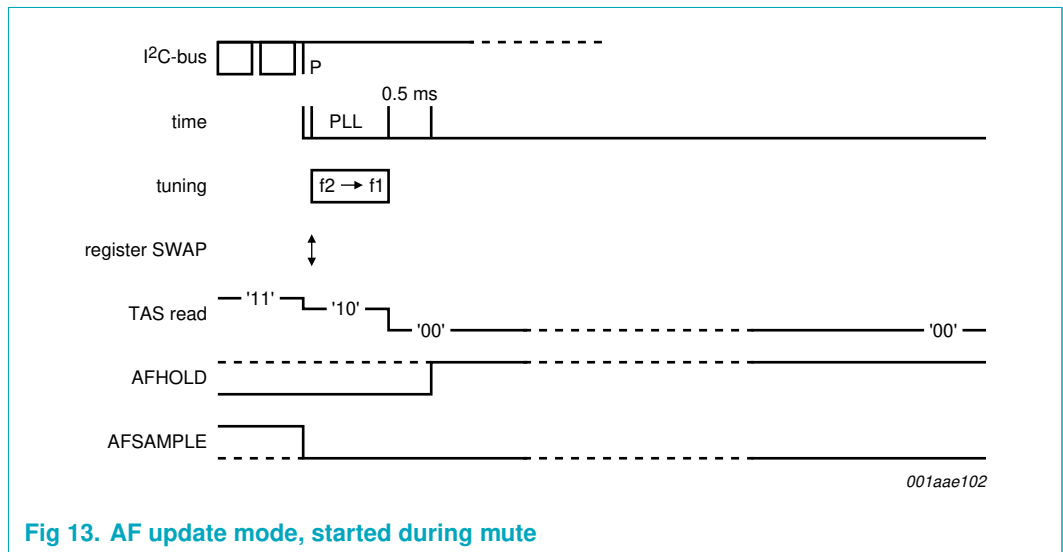


Fig 13. AF update mode, started during mute

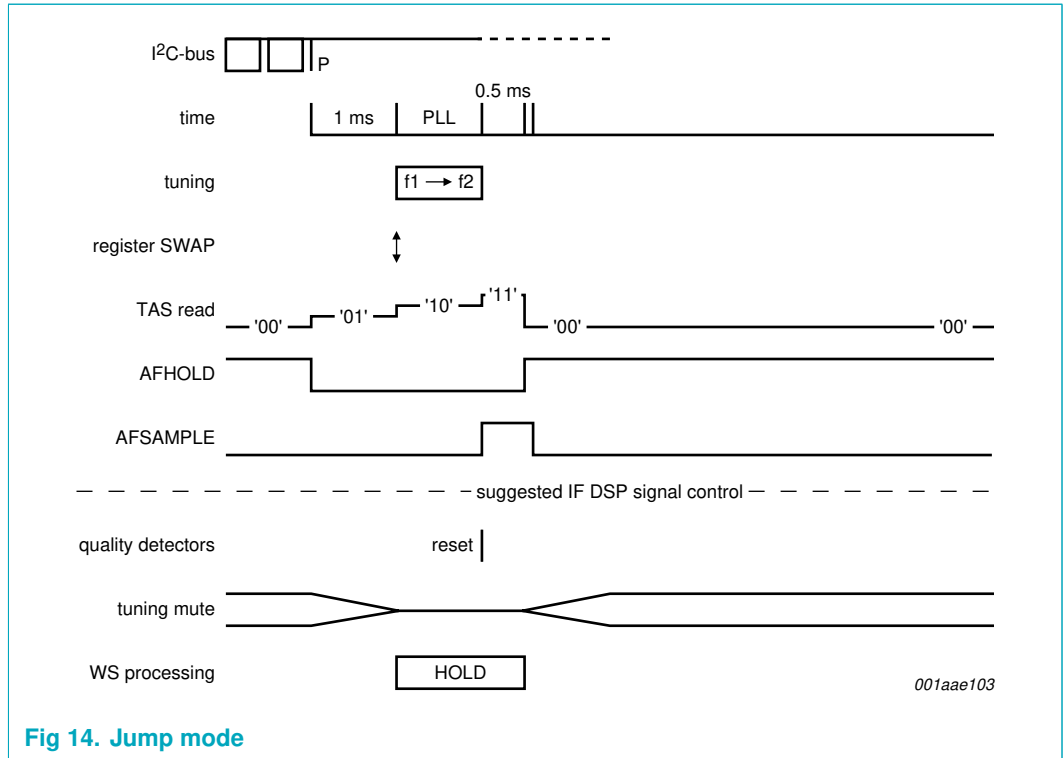


Fig 14. Jump mode

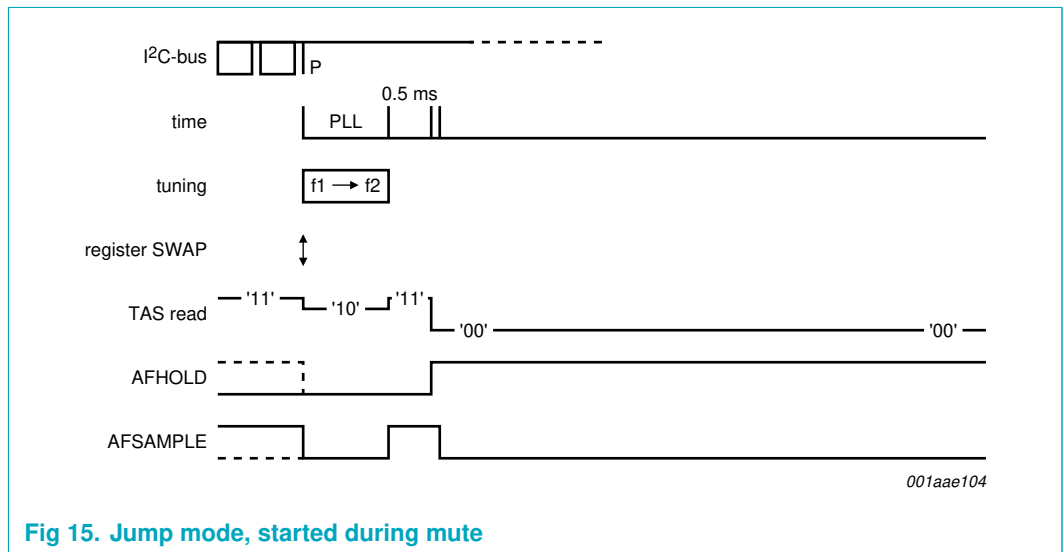


Fig 15. Jump mode, started during mute

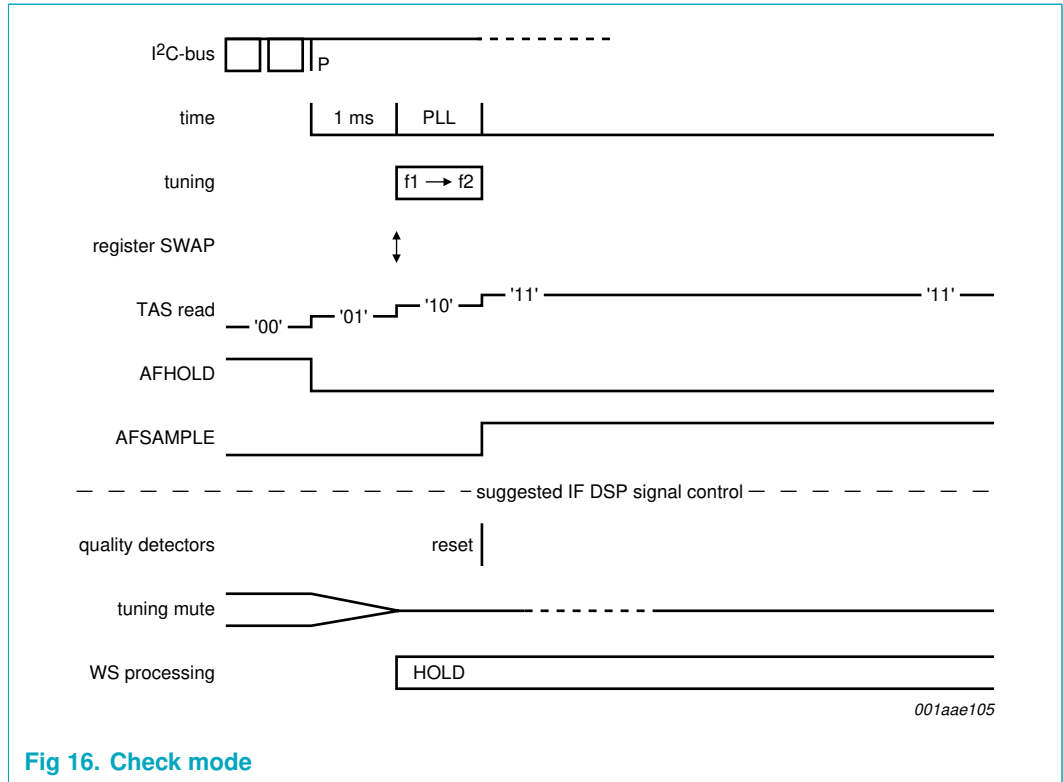


Fig 16. Check mode

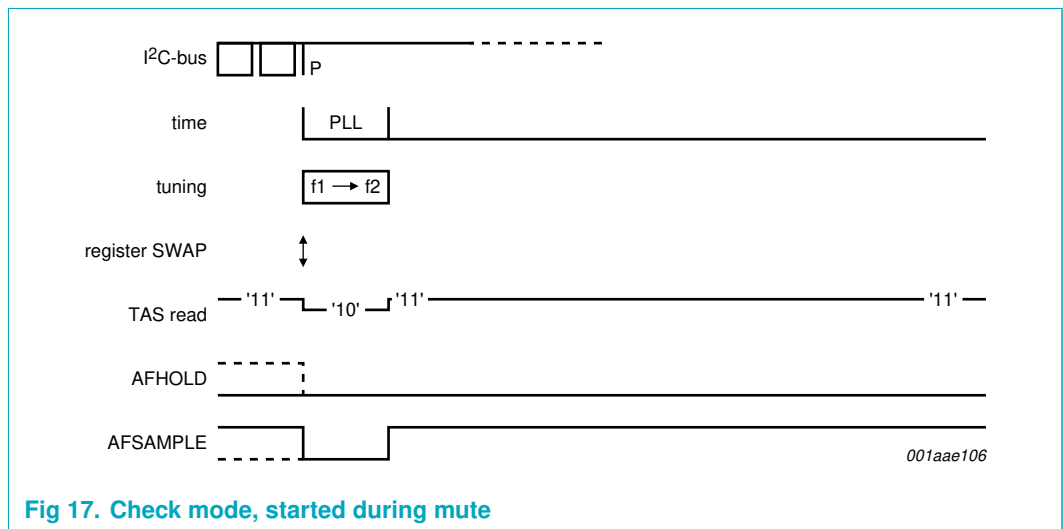


Fig 17. Check mode, started during mute

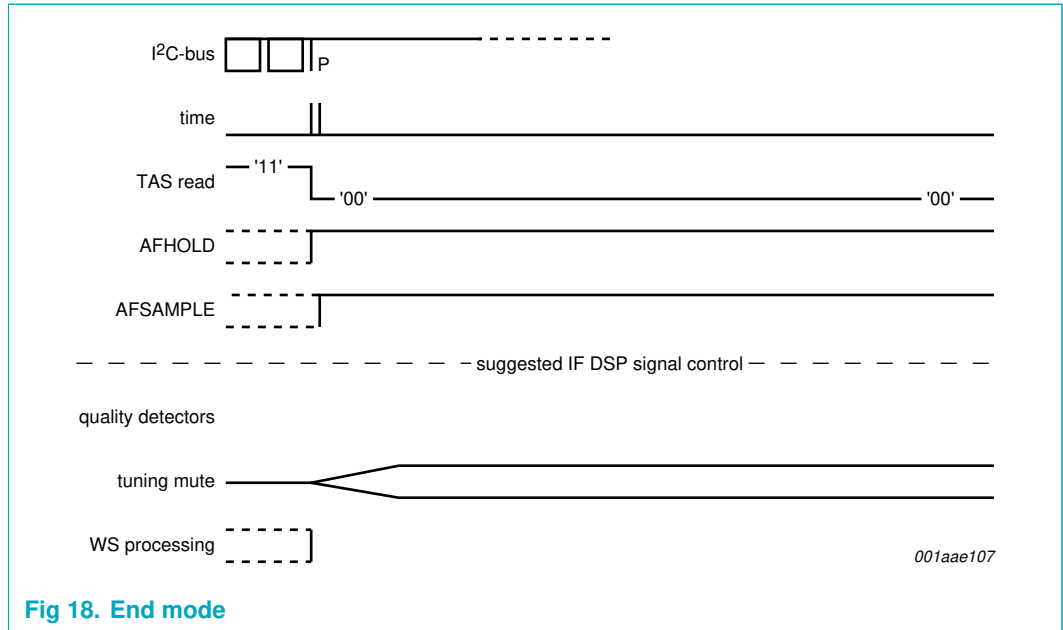


Fig 18. End mode

8.2.2 Write mode: data byte CONTROL

Table 14. CONTROL - data byte 0h bit allocation with default setting

7	6	5	4	3	2	1	0
RFGAIN	0	FLAG	IFGAIN	NBAGC1	NBAGC0	DAASW	CFSW
0		0	0	0	1	0	0

Table 15. CONTROL - data byte 0h bit description

Bit	Symbol	Description
7	RFGAIN	FM RF gain 0 = standard gain 1 = +6 dB added gain
6	-	not used, must be set to logic 0
5	FLAG	software port output open-collector 0 = SWPORT pin inactive (high-impedance) 1 = SWPORT pin active (pull-down to ground)
4	IFGAIN	IF gain 0 = standard IF gain 1 = increased IF gain (6 dB)
3 and 2	NBAGC[1:0]	RF AGC start level; setting of narrow band (IF) detection 00 = 700 mV (peak value) 01 = 560 mV (peak value) 10 = 450 mV (peak value) 11 = 350 mV (peak value)

Table 15. CONTROL - data byte 0h bit description ...continued

Bit	Symbol	Description
1	DAASW	antenna DAA mode in FM 0 = standard; DAA output voltage is controlled by V_{tune} 1 = DAA output voltage is a fixed temperature stable voltage controlled by the DAA setting (independent of V_{tune})
0	CFSW	ceramic filter switch 0 = CFSW1 pin active (low-impedance) and CFSW2 pin inactive (high-impedance) 1 = CFSW2 pin active (low-impedance) and CFSW1 pin inactive (high-impedance)

8.2.3 Write mode: data byte PLLM

Table 16. PLLM - data byte 1h bit allocation with default setting

7	6	5	4	3	2	1	0
CPOFF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8
0	0	0	0	1	0	0	0

Table 17. PLLM - data byte 1h bit description

Bit	Symbol	Description
7	CPOFF	charge pump off 0 = standard operation 1 = charge pump deactivated
6 to 0	PLL[14:8]	upper byte of PLL divider word

8.2.4 Write mode: data byte PLLL

Table 18. PLLL - data byte 2h bit allocation with default setting

7	6	5	4	3	2	1	0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0
0	1	1	1	1	1	1	0

Table 19. PLLL - data byte 2h bit description

Bit	Symbol	Description
7 to 0	PLL[7:0]	lower byte of PLL divider word; PLL[14:0] is the divider ratio N of the VCO programmable divider; N = 1024 to 32767

8.2.5 Write mode: data byte DAA

Table 20. DAA - data byte 3h bit allocation with default setting

7	6	5	4	3	2	1	0
AGCSW	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0
0	1	0	0	0	0	0	0

Table 21. DAA - data byte 3h bit description

Bit	Symbol	Description
7	AGCSW	RF AGC switch 0 = no drive of unused RF AGC PIN diode (FM PIN diode in AM mode or AM PIN diode in FM mode) 1 = unused PIN diode supplied with constant current
6 to 0	DAA[6:0]	alignment of antenna circuit tuning voltage in FM mode (0.1V _{tune} to 2.0V _{tune})

8.2.6 Write mode: data byte AGC

Table 22. AGC - data byte 4h bit allocation with default setting

7	6	5	4	3	2	1	0
SDAA3	SDAA2	SDAA1	SDAA0	WBAGC1	WBAGC0	KAGC	LODX
1	0	0	0	0	0	0	0

Table 23. AGC - data byte 4h bit description

Bit	Symbol	Description
7 to 4	SDAA[3:0]	alignment of second antenna circuit tuning voltage in FM mode (0.7V _{DAAOUT1} to 1.35V _{DAAOUT1})
3 and 2	WBAGC[1:0]	RF AGC start level; setting of wideband (RF) detection; for AM, see Table 24 and for FM, see Table 25
1	KAGC	FM keyed AGC 0 = keyed AGC off 1 = keyed AGC on
0	LODX	local switch 0 = standard operation (DX) 1 = forced FM RF AGC attenuation (LOCAL)

Table 24. Setting of RF AGC threshold voltage for AM

WBAGC1	WBAGC0	AM output (RMS value) at LNAOUT
0	0	250 mV
0	1	200 mV
1	0	150 mV
1	1	70 mV

Table 25. Setting of RF AGC threshold voltage for FM

WBAGC1	WBAGC0	FM mixer input voltage (RMS value) at FMMIXIN
0	0	24 mV
0	1	17 mV
1	0	12 mV
1	1	9 mV

8.2.7 Write mode: data byte BAND

Table 26. BAND - data byte 5h bit allocation with default setting

7	6	5	4	3	2	1	0
BAND2	BAND1	BAND0	FREF2	FREF1	FREF0	LOINJ	FMIFIN
0	0	1	0	0	0	0	0

Table 27. BAND - data byte 5h bit description

Bit	Symbol	Description
7 to 5	BAND[2:0]	see Table 28
4 to 2	FREF[2:0]	PLL reference frequency; see Table 29
1	LOINJ	0 = high injection image suppression 1 = low injection image suppression
0	FMIFIN	0 = FMIFAGCIN1 input is selected 1 = FMIFAGCIN2 input is selected

Table 28. Decoding of BAND bits

BAND2	BAND1	BAND0	Divider ratio M	Receiver band
0	0	0	1	WB
0	0	1	2	FM
0	1	0	3	FM
0	1	1	6	AM
1	0	0	8	AM
1	0	1	10	AM
1	1	0	16	AM
1	1	1	20	AM

Table 29. Reference frequencies

FREF2	FREF1	FREF0	f _{ref}
0	0	0	100 kHz
0	0	1	50 kHz
0	1	0	25 kHz
0	1	1	20 kHz
1	0	0	10 kHz
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

The correct charge pump current for each reference frequency is selected automatically, see [Table 30](#).