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TEF6862

Car Radio Enhanced Selectivity Tuner (CREST)

Rev. 01 — 14 September 2006 Product data sheet

1. General description

The TEF6862 is a single-chip car radio tuner for AM, FM and weather band reception providing AM double conversion for LW, MW and full range SW (11 m to 120 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz.

FM double conversion to IF1 = 10.7 MHz and IF2 = 450 kHz with integrated image rejection for both IF1 and IF2; integrated IF filter with variable bandwidth and automatic bandwidth control algorithm with flexibility via the I^{2}C-bus; capable of US FM, Europe FM, Japan FM, East Europe FM and weather band reception; all FM bands can be selected using high injection LO or low injection LO in the FM mixer 1.

Tuning system including crystal oscillator, VCO, PLL synthesizer and state machine for timing uncritical control of search, preset change and AF check via microcontroller.

2. Features

- High dynamic range FM front-end mixer for conversion of FM RF (65 MHz to 108 MHz and USA weather band) to an IF frequency of 10.7 MHz; mixer provides inherent image rejection which can be switched from low injection LO to high injection LO via the I^{2}C-bus
- FM front-end AGC PIN diode drive circuit; AGC detection at the FM font-end mixer input and the IF filter input; AGC threshold for detection at the mixer input is programmable and keyed AGC function can be selected via the I^{2}C-bus; the AGC PIN diode drive can be activated by the I^{2}C-bus for a search tuning in local mode; in AM mode the AGC PIN diode drive can be activated by the I^{2}C-bus if required; information on amount of PIN diode AGC is available via the I^{2}C-bus
- FM front-end mixer includes +6 dB gain setting via the I^{2}C-bus
- FM second mixer for conversion of IF1 10.7 MHz to IF2 450 kHz including inherent image rejection; the gain can be controlled via the I^{2}C-bus
- Integrated FM channel selection filter with continuous variable bandwidth providing simultaneous low distortion and high selectivity with only one external ceramic filter; improved sensitivity with dynamic threshold extension can be enabled via the I^{2}C-bus
- Fully integrated FM demodulator with very low distortion
- Digital bandwidth control algorithm with detection on adjacent channel information, deviation, detuning and level with customer flexibility via the I^{2}C-bus
- Digital alignment circuit for bus controlled adjustment of oscillator tuning voltage to two FM antenna tank circuit tuning voltages; AM and FM level start and slope alignment; IF filter and demodulator center frequency alignment
- AM and FM level detection (signal strength indication)
- Separate RF input to FM front-end mixer for weather band
- Flag or voltage output indicators for actual IF bandwidth information

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- AM front-end mixer for conversion of AM RF to an IF frequency of 10.7 MHz
- AM RF AGC circuit for external cascode AGC and PIN diode AGC
- AM noise blanker with detection at IF1 and blanking at IF2
- AM second mixer for conversion of IF1 10.7 MHz to IF2 450 kHz; IF2 AGC amplifier and AM demodulator with low distortion
- For AM stereo applications the gain controlled AM IF2 output voltage can be switched to MPXAM output pin via the I^2C-bus
- Crystal oscillator providing frequency for second conversion, references for synthesizer PLL and analog signal processor and timing for tuning action
- LC tuning oscillator with low phase noise and oscillator dividers with selectable divider ratios for worldwide tuner reception without band switching in application
- Fast synthesizer PLL tuning system with dynamically adapting loop parameters combining fast PLL frequency jumps for inaudible RDS updating with low spurious responses for large signal-to-noise ratios
- Sequential state machine for preset change, search and inaudible AFU allowing a timing uncritical microcontroller operation; the state machine generates timing signals for the internal inaudible tuning mute and analog or digital signal processor
- An alternative frequency check can be initiated by the signal processor for audio correlation algorithms directly without involvement of the microcontroller
- Audio soft slope tuning mute circuit allowing inaudible AFU
- Two hardware programmable I^2C-bus addresses
- Two software controlled flag outputs
- Several test modes for fast IC and system tests

3. Quick reference data

Table 1. Quick reference data

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CCA}	analog supply voltage	on pins VCC, VCCPLL, VCCVCO, VCCRF, AMMIX2OUT1, AMMIX2OUT2, MIX1OUT1 and MIX1OUT2	8	8.5	9	V
Current in FM mode						
$I_{CC(tot)}$	total supply current		-	101.9	-	mA
Current in AM mode						
$I_{CC(tot)}$	total supply current		-	84.4	-	mA
Tuning system; see Table 37, Table 38 and Table 39						
Timings						
t_{tune}	tuning time	Europe FM and US FM band; f_{ref} = 100 kHz; f_{RF} = 87.5 MHz to 108 MHz	-	0.75	1	ms
		AM MW band; f_{ref} = 20 kHz; f_{RF} = 0.53 MHz to 1.7 MHz	-	-	10	ms
$t_{upd(AF)}$	AF update time	cycle time for inaudible AF update including 1 ms mute start and 1 ms mute release time	-	6	6.5	ms

Table 1. Quick reference data *...continued*

V_{CCA} = 8.5 V; T_{amb} = 25 °C; see Figure 25 and Figure 26; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM overall system parameters[1]						
$f_{i(RF)}$	RF input frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB	-	45	-	µV
(S+N)/N	signal plus noise-to-noise ratio		54	58	-	dB
THD	total harmonic distortion	200 µV < $V_{i(RF)}$ < 1 V; m = 0.8	-	0.5	1	%
IP3	third-order intercept point		-	130	-	dBµV
FM overall system parameters[2]						
$f_{i(RF)}$	RF input frequency		65	-	108	MHz
V_{sens}	sensitivity voltage	(S+N)/N = 26 dB				
		IF bandwidth wide	-	2	-	µV
		IF bandwidth dynamic; threshold extension off	-	1.8	-	µV
		IF bandwidth dynamic; threshold extension on	-	1.6	-	µV
(S+N)/N	signal plus noise-to-noise ratio	V_i = 3 mV; IF bandwidth wide	-	63	-	dB
THD	total harmonic distortion	Δf = 75 kHz	-	0.2	0.7	%
IP3	third-order intercept point		-	123	-	dBµV
Weatherband overall system parameters[2]; see Figure 27						
$f_{i(RF)}$	RF input frequency		162.4	-	162.55	MHz
(S+N)/N	signal plus noise-to-noise ratio	Δf = 1.5 kHz; $V_{i(RF)}$ = 10 mV; de-emphasis = 120 µs	-	45	-	dB
THD	total harmonic distortion	Δf = 5 kHz	-	0.7	-	%

[1] Based on 15 pF/60 pF dummy aerial, voltages at dummy aerial input, f_{mod} = 400 Hz, 2.15 kHz audio bandwidth, $f_{i(RF)}$ = 990 kHz, m = 0.3, unless otherwise specified.

[2] Based on 75 Ω dummy aerial, voltages at dummy aerial input, f_{mod} = 1 kHz, de-emphasis = 50 µs, B = 300 Hz to 22 kHz, Δf = 22.5 kHz, unless otherwise specified.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6862HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5. Block diagram

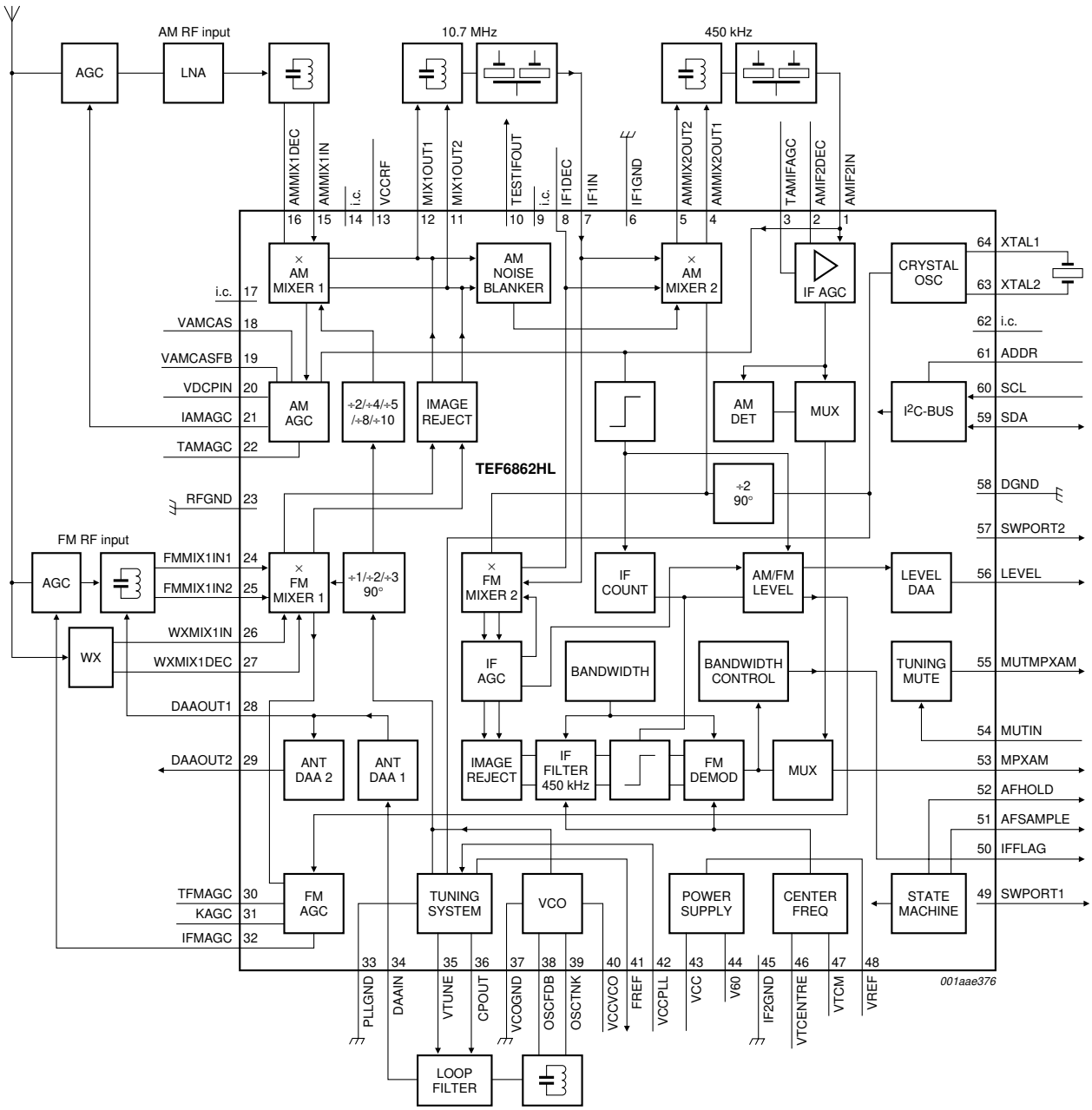

Fig 1. Block diagram of TEF6862HL

6. Pinning information

6.1 Pinning

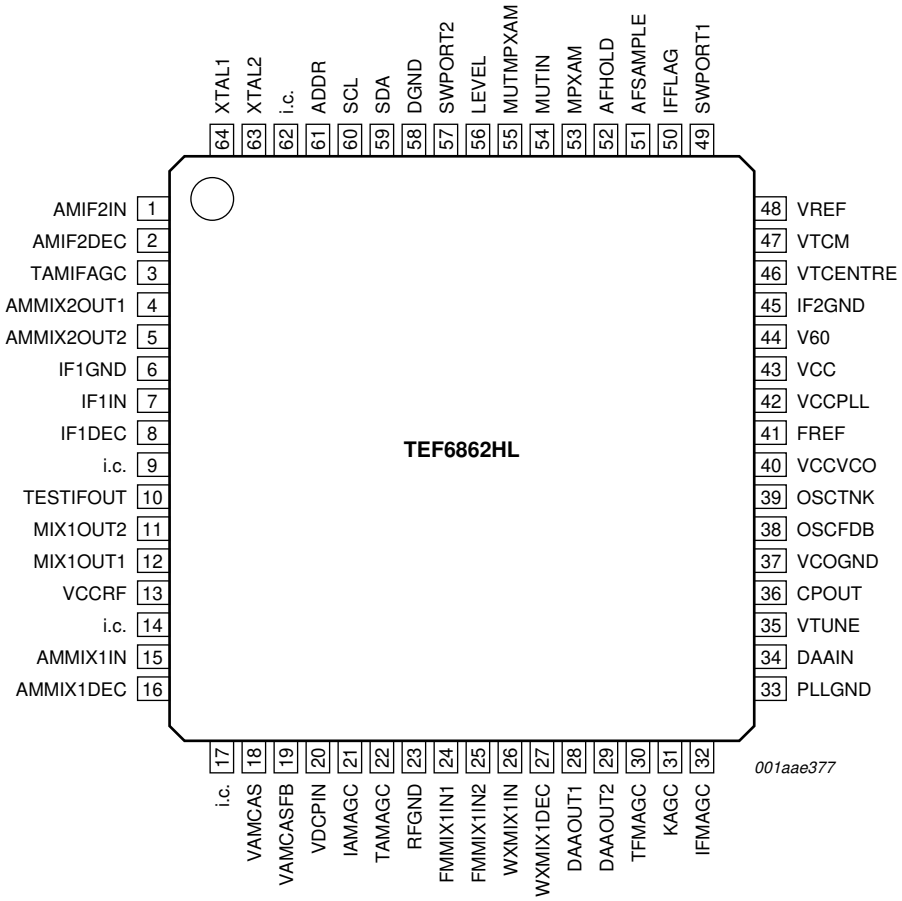

Fig 2. Pin configuration for LQFP64

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
AMIF2IN	1	AM IF2 input
AMIF2DEC	2	decoupling for AM IF2 input
TAMIFAGC	3	time constant of AM IF AGC
AMMIX2OUT1	4	AM mixer 2 output 1
AMMIX2OUT2	5	AM mixer 2 output 2
IF1GND	6	IF1 ground
IF1IN	7	AM and FM mixer 2 input
IF1DEC	8	AM and FM mixer 2 decoupling
i.c.	9	internally connected; leave open

Table 3. Pin description *...continued*

Symbol	Pin	Description
TESTIFOUT	10	test pin IF filter output
MIX1OUT2	11	AM and FM mixer 1 output 2 at IF1
MIX1OUT1	12	AM and FM mixer 1 output 1 at IF1
VCCRF	13	supply voltage for AM and FM RF
i.c.	14	internally connected; leave open
AMMIX1IN	15	AM mixer 1 input
AMMIX1DEC	16	AM mixer 1 decoupling
i.c.	17	internally connected; leave open
VAMCAS	18	cascode AM AGC
VAMCASFB	19	feedback for cascode AM AGC
VDCPIN	20	5 V bias voltage for AM PIN diode
IAMAGC	21	AGC current for AM PIN diode
TAMAGC	22	time constant of AM RF AGC
RFGND	23	RF ground
FMMIX1IN1	24	FM mixer 1 input 1
FMMIX1IN2	25	FM mixer 1 input 2
WXMIX1IN	26	weather band mixer input
WXMIX1DEC	27	weather band mixer decoupling
DAAOUT1	28	antenna DAA output 1
DAAOUT2	29	antenna DAA output 2
TFMAGC	30	time constant of FM RF AGC
KAGC	31	time constant of keyed FM front-end AGC
IFMAGC	32	PIN diode drive current output of FM front-end AGC
PLLGND	33	ground for tuning PLL
DAAIN	34	input of DAA circuit for antenna tank circuit
VTUNE	35	tuning voltage; 3 mA charge pump output
CPOUT	36	charge pump output
VCOGND	37	VCO ground
OSCFDB	38	VCO feedback
OSCTNK	39	VCO tank circuit
VCCVCO	40	VCO supply voltage
FREF	41	reference frequency output
VCCPLL	42	supply voltage for tuning PLL
VCC	43	supply voltage (8.5 V)
V60	44	input for FM filter and demodulator supply current
IF2GND	45	FM IF2 ground
VTCENTRE	46	filtering of tuning voltage of center frequency
VTCM	47	reference for filtering of tuning voltage of center frequency
VREF	48	reference voltage for noise decoupling
SWPORT1	49	software port output 1
IFFLAG	50	FM IF2 bandwidth voltage flag

Table 3. Pin description *...continued*

Symbol	Pin	Description
AFSAMPLE	51	AF sample flag output
AFHOLD	52	AF hold flag output and input
MPXAM	53	not muted FM or AM demodulator output and IF output for AM stereo
MUTIN	54	input of tuning mute circuit
MUTMPXAM	55	FM MPX output or AM output from tuning mute
LEVEL	56	level voltage output for AM and FM
SWPORT2	57	software port output 2
DGND	58	digital ground
SDA	59	I²C-bus data line input and output
SCL	60	I²C-bus clock line input
ADDR	61	address select
i.c.	62	internally connected
XTAL2	63	crystal oscillator 2
XTAL1	64	crystal oscillator 1

7. Functional description

7.1 FM mixer 1

The FM quadrature mixer converts FM RF (65 MHz to 108 MHz and 162.4 MHz to 162.55 MHz) to an IF of 10.7 MHz. The FM mixer provides inherent image rejection and a large dynamic range. The image rejection can be switched from low injection LO to high injection LO via the I²C-bus independently of the band selection. The gain can be increased by 6 dB via the I²C-bus.

7.2 FM RF AGC

AGC detection at the FM front-end mixer input with programmable threshold. When the threshold is exceeded, the PIN diode drive circuit sources a current to an external PIN diode circuit, keeping the mixer input signal level constant.

Keyed AGC function is selectable via the I²C-bus and uses the in-band level information derived from the limiter level detector.

The AGC PIN diode drive circuit can be forced via the I²C-bus to deliver a fixed current as a local function for search tuning. In AM mode, the AGC PIN diode drive circuit can also be forced via the I²C-bus to deliver the maximum source current into the external FM PIN diode circuitry. AGC information is available via the I²C-bus.

7.3 FM mixer 2

The FM quadrature mixer converts 10.7 MHz FM IF1 to 450 kHz FM IF2 and includes inherent image rejection. The gain can be selected via I²C-bus to compensate for different ceramic filter insertion loss.

7.4 FM IF2 channel filter

The order and dynamic range of the filter is designed for operation with only one external ceramic filter in the application. The filter characteristic is optimized to combine high selectivity with low distortion from maximum to minimum IF bandwidth settings. The bandwidth of the filter can be selected directly with 5 bits via the I^2C-bus or automatically via the bandwidth control algorithm. When the automatic mode is selected the bandwidth depends on the signal conditions: the amount of adjacent channel, the deviation of the desired signal, detuning and signal strength.

The filter center frequency is I^2C-bus aligned with 6 bits.

7.5 FM limiter and level detection

The limiter amplifies the IF filter output signal, removes AM modulations from the IF signal and supplies a well defined signal for the FM demodulator. From the limiter also the RSSI is derived which is converted to a suitable level voltage with minimum temperature drift.

7.6 FM demodulator

The fully integrated FM demodulator converts the IF signal from the limiter to the FM MPX output signal with very low distortion. The center frequency of the filter in the demodulator is aligned together with the IF2 filter center frequency.

7.7 Audio output buffer

The output buffer for AM and FM amplifies the demodulated signal and includes low-pass filtering to attenuate any IF residual signals. The gain is increased in weather band reception to compensate for the low frequency deviation.

7.8 Tuning mute

The audio soft slope tuning mute circuit is controlled by the sequential machine for different tuning actions to eliminate audible effects. Control signals are generated to control the muting and the weak signal processing in the signal processor.

7.9 Weather band input

A separate RF input to the FM front-end mixer for weather band makes the weather band application easier.

7.10 IF filter and demodulator tuning

The center frequency as well as the bandwidth of both the IF filter and demodulator are coupled to the stable crystal reference frequency. Fine adjustment is achieved with a 6-bit DAA.

7.11 VCO and dividers

The varactor tuned LC oscillator together with the dividers provides the local oscillator signal for both AM and FM front-end mixers. The VCO has an operating frequency of approximately 160 MHz to 256 MHz. In FM mode the LO frequency is divided by 1, 2 or 3.

These dividers generate in-phase and quadrature-phase output signals used in the FM front-end mixer for image rejection. In AM mode the LO frequency is divided by 6, 8, 10, 16 or 20 depending on the selected AM band.

7.12 Crystal oscillator

The linear crystal oscillator provides a 20.5 MHz signal. A divider-by-two generates in-phase and quadrature-phase mixer frequencies for the conversion from IF1 to IF2 including image rejection. The reference divider generates from the crystal frequency various reference frequencies for the tuning PLL. Also the different timing signals for the sequential machine as well as the analog signal processor reference frequency are derived from the crystal reference.

7.13 Tuning PLL

The tuning PLL locks the VCO frequency divided by the programmable divider ratio to the reference frequency. Due to the combination of different charge pump signals in the PLL loop filter, the loop parameters are adapted dynamically. Tuning to different radio frequencies is done by changing the programmable divider ratio. The tuning step size is selected with the reference frequency divider setting.

7.14 Antenna DAA

The antenna DAA measures the VCO tuning voltage and multiplies it with a factor defined by the 7-bit DAA1 setting to generate a tuning voltage for the FM antenna tank circuit. A second tuning voltage (DAA output 2) for an optional second FM tank circuit is derived from the first tuning voltage with 4 bits.

7.15 AM RF AGC

The AM front-end is designed for the application of an external JFET low noise amplifier with cascode AGC and PIN diode AGC both controlled by an integrated AGC circuit. Four AGC thresholds of the detector at the first mixer input are selectable via I^2C-bus. A further detector at the IF AGC input prevents undesired overload (see Figure 21). AGC information can be read out via I^2C-bus. The PIN diode current drive circuit includes a pull-up current source for reverse biasing of the PIN diode, when the AGC is not active to achieve a low parasitic capacitance.

7.16 AM mixer

The large dynamic range AM mixer converts AM RF (144 kHz to 26.1 MHz) to an IF of 10.7 MHz.

7.17 AM IF noise blanker

The spike detection for the AM noise blanker is at the output of the AM front-end mixer. Blanking is realized at the output of the second AM mixer. The sensitivity of the noise blanker can be set in three settings and switched off via I^2C-bus.

7.18 AM IF AGC amplifier and demodulator

The 450 kHz IF2 signal after the ceramic channel selection filter is amplified by the IF AGC amplifier and demodulated. Instead of the demodulated AM audio signal, also the IF2 signal can be selected on the MPXAM output pin. This IF2 signal can be used for an external AM stereo decoder. To avoid overdrive of the input stage a detector at the input drives the RF AGC.

7.19 AM level detection

The IF2 signal used for AM IF AGC and demodulation is also used in the limiter circuit for in-band level detection to generate a level voltage.

7.20 AM and FM level DAA

The start and slope of the level detector output are programmable with 5 bits and 3 bits respectively to achieve level information independent on gain variations in the signal channel.

7.21 AM and FM IF counter

The output signal from the limiters is used for IF counting in both AM and FM. The IF count time is automatically controlled to achieve the optimum counting accuracy. The minimum count time is 2 ms.

8. I²C-bus protocol

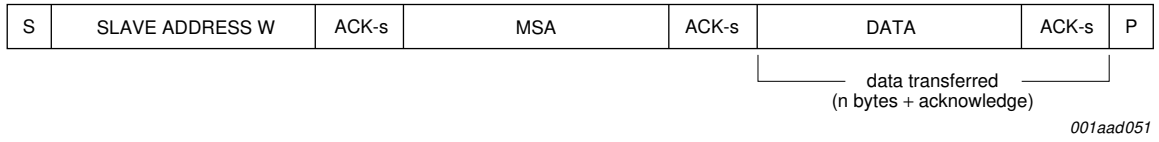

Fig 3. Write mode

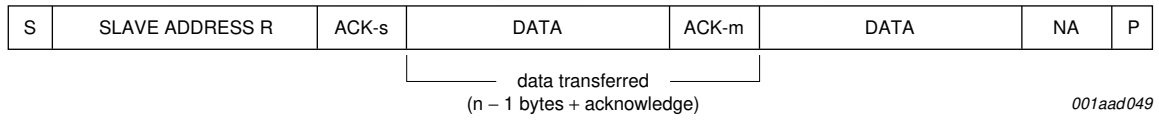

Fig 4. Read mode

Table 4. Description of I²C-bus format

Code	Description
S	START condition
Slave address W	1100 0000b for pin ADDR grounded
	1100 0010b for pin ADDR floating
Slave address R	1100 0001b for pin ADDR grounded
	1100 0011b for pin ADDR floating

Table 4. Description of I²C-bus format *…continued*

Code	Description
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge
MSA	mode and subaddress byte
Data	data byte
P	STOP condition

8.1 Read mode

Read data is loaded into the output register at the preceding acknowledge clock pulse.

Table 5. Read register overview

Data byte	Name	Reference
0h	IFCOUNTER	Section 8.1.1
1h	TUNER	Section 8.1.2
2h	ACDREAD	Section 8.1.3
3h	LEVEL	Section 8.1.4
4h	ID	Section 8.1.5
5h	TEMP	Section 8.1.6

8.1.1 Read mode: data byte IFCOUNTER

Table 6. IFCOUNTER - data byte 0h bit allocation

7	6	5	4	3	2	1	0
IFCM1	IFCM0	IFCS	IFCA	IFC3	IFC2	IFC1	IFC0

Table 7. IFCOUNTER - data byte 0h bit description

Bit	Symbol	Description
7 and 6	IFCM[1:0]	IF counter mode
		00 = no new counter result available (IF counter value is last result or reset state)
		01 = new counter result available (IF counter value is new result)
		10 = counter result from AFU (IF counter value is AF result)
		11 = POR is detected, the I²C-bus data is reset to POR state
5	IFCS	IF counter sign
		0 = the IF counter result indicates a positive **RF** frequency
		1 = the IF counter result indicates a negative **RF** frequency
4	IFCA	IF counter accuracy
		0 = IF counter result with 1 kHz resolution in FM mode and 0.5 kHz resolution in AM mode
		1 = IF counter result with 8 kHz resolution in FM mode and 4 kHz resolution in AM mode
3 to 0	IFC[3:0]	IF counter result; see Table 8

Table 8. IF counter result

IFC3	IFC2	IFC1	IFC0	FM deviation from nominal value		AM deviation from nominal value	
				IFCA = 0	IFCA = 1	IFCA = 0	IFCA = 1
0	0	0	0	0 kHz to 1 kHz	reset state	0 kHz to 0.5 kHz	reset state
0	0	0	1	1 kHz to 2 kHz	-	0.5 kHz to 1 kHz	-
0	0	1	0	2 kHz to 3 kHz	16 kHz to 24 kHz	1 kHz to 1.5 kHz	8 kHz to 12 kHz
0	0	1	1	3 kHz to 4 kHz	24 kHz to 32 kHz	1.5 kHz to 2 kHz	12 kHz to 16 kHz
0	1	0	0	4 kHz to 5 kHz	32 kHz to 40 kHz	2 kHz to 2.5 kHz	16 kHz to 20 kHz
0	1	0	1	5 kHz to 6 kHz	40 kHz to 48 kHz	2.5 kHz to 3 kHz	20 kHz to 24 kHz
0	1	1	0	6 kHz to 7 kHz	48 kHz to 56 kHz	3 kHz to 3.5 kHz	24 kHz to 28 kHz
0	1	1	1	7 kHz to 8 kHz	56 kHz to 64 kHz	3.5 kHz to 4 kHz	28 kHz to 32 kHz
1	0	0	0	8 kHz to 9 kHz	64 kHz to 72 kHz	4 kHz to 4.5 kHz	32 kHz to 36 kHz
1	0	0	1	9 kHz to 10 kHz	72 kHz to 80 kHz	4.5 kHz to 5 kHz	36 kHz to 40 kHz
1	0	1	0	10 kHz to 11 kHz	80 kHz to 88 kHz	5 kHz to 5.5 kHz	40 kHz to 44 kHz
1	0	1	1	11 kHz to 12 kHz	88 kHz to 96 kHz	5.5 kHz to 6 kHz	44 kHz to 48 kHz
1	1	0	0	12 kHz to 13 kHz	96 kHz to 104 kHz	6 kHz to 6.5 kHz	48 kHz to 52 kHz
1	1	0	1	13 kHz to 14 kHz	104 kHz to 112 kHz	6.5 kHz to 7 kHz	52 kHz to 56 kHz
1	1	1	0	14 kHz to 15 kHz	112 kHz to 120 kHz	7 kHz to 7.5 kHz	56 kHz to 60 kHz
1	1	1	1	15 kHz to 16 kHz	≥ 120 kHz	7.5 kHz to 8 kHz	≥ 60 kHz

After a tuning action, which is activated by the state machine, the IF counter is reset at that moment when tuning is established (PLL in-lock). Reset is also possible via bit IFCR. The first counter result is available from 2 ms after reset. For FM further results can be obtained from 4 ms, 8 ms, 16 ms and 32 ms after reset, the increasing count time attenuates influence of FM modulation on the counter result. After this, the counter continues at the maximum count time of 32 ms (see Figure 5).

After AFU sampling the IF counter read value is held (IFCM = 10); see Figure 6, Figure 14 and Figure 15. The counter itself remains active in the background in raw mode (2 ms count time). The IF counter hold is disabled after I^2C-bus read.

For AM mode the count time is fixed to 2 ms and results are available every 2 ms.

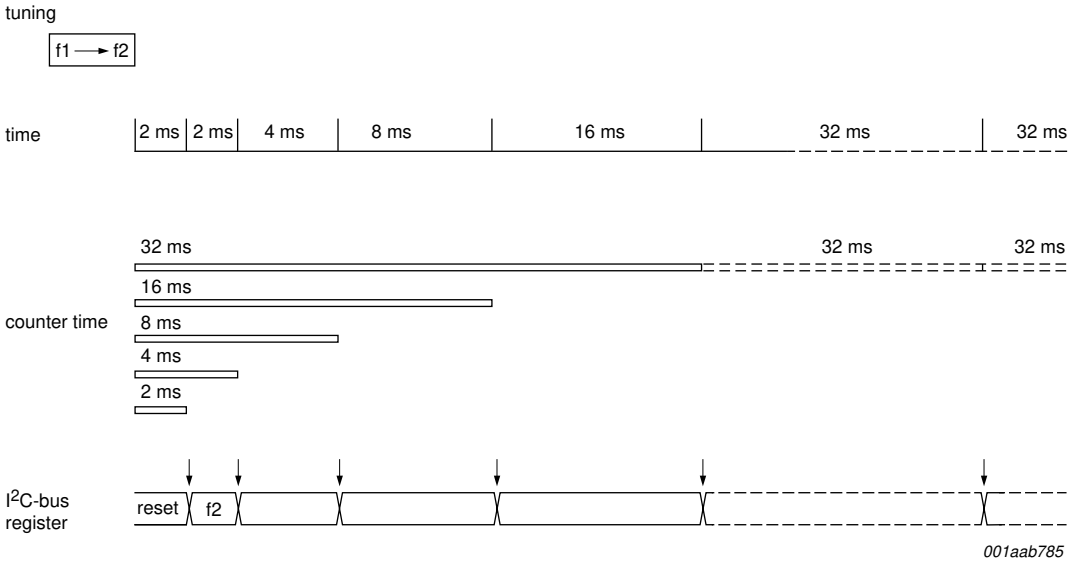

Fig 5. IF counter in FM mode after tuning

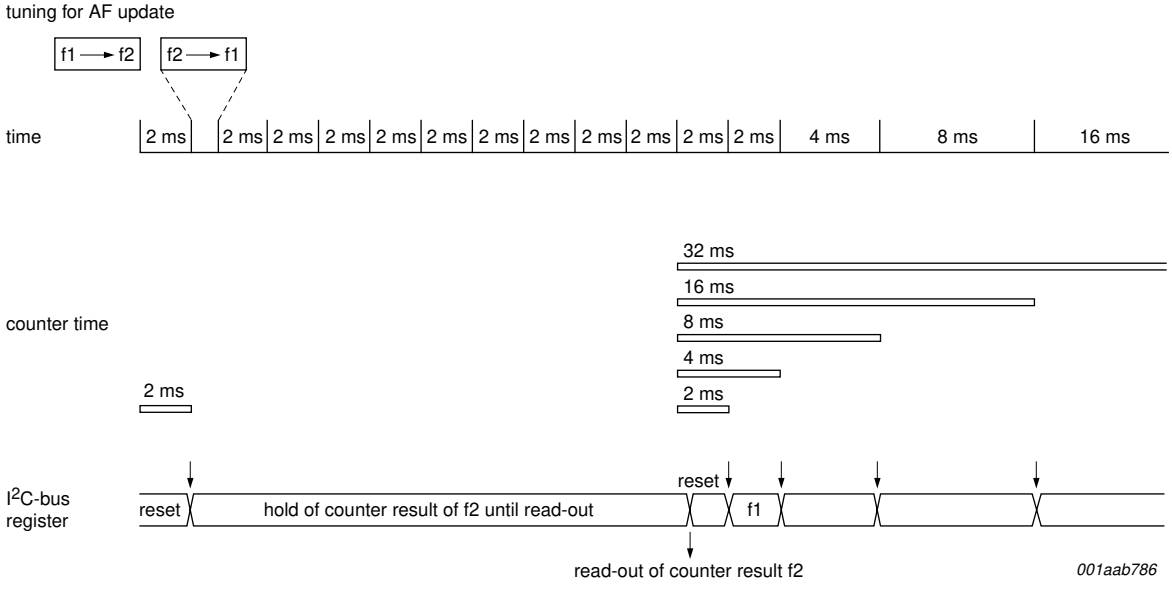

Fig 6. IF counter in FM mode during and after AF update

8.1.2 Read mode: data byte TUNER

Table 9. TUNER - data byte 1h bit allocation

7	6	5	4	3	2	1	0
RAGC1	RAGC0	-	IFBW4	IFBW3	IFBW2	IFBW1	IFBW0

Table 10. TUNER - data byte 1h bit description

Bit	Symbol	Description
7 and 6	RAGC[1:0]	RF AGC attenuation indicator, PIN diode current on pins IAMAGC or IFMAGC
		00 = < 0.1 mA
		01 = 0.1 mA to 0.5 mA
		10 = 0.5 mA to 2.5 mA
		11 = > 2.5 mA
5	-	not used
4 to 0	IFBW[4:0]	FM IF filter bandwidth control 45 kHz to 130 kHz

8.1.3 Read mode: data byte ACDREAD

Table 11. ACDREAD - data byte 2h bit allocation

7	6	5	4	3	2	1	0
ACD2	ACD1	ACD0	MOD2	MOD1	MOD0	OFFS	WAM

Table 12. ACDREAD - data byte 2h bit description

Bit	Symbol	Description
7 to 5	ACD[2:0]	adjacent channel detector value
4 to 2	MOD[2:0]	modulation detector value
1	OFFS	offset detector result
		0 = no offset detected
		1 = offset detected (adjacent channel breakthrough)
0	WAM	wideband AM detector result
		0 = no WAM detected
		1 = WAM detected (multipath or co-channel)

After AFU sampling the content of the byte ACDREAD is held until the next I^2C-bus read. The values ACD and MOD and the WAM bit can be used as quality indicators of the alternate frequency. The OFFS bit cannot be used because of too slow attack time. See Figure 14 and Figure 15.

8.1.4 Read mode: data byte LEVEL

Table 13. LEVEL - data byte 3h bit allocation

7	6	5	4	3	2	1	0
LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 14. LEVEL - data byte 3h bit description

Bit	Symbol	Description
7 to 0	LEV[7:0]	level detector output value V_{level} [V] = $^1/_{64}$LEV[7:0] + 0.25

8.1.5 Read mode: data byte ID

Table 15. ID - data byte 4h bit allocation

7	6	5	4	3	2	1	0
IFCAPG	-	-	-	-	ID2	ID1	ID0

Table 16. ID - data byte 4h bit description

Bit	Symbol	Description
7	IFCAPG	IF filter gear; value is used for IFCAP adjustment (byte IFCAP); see Table 47 and Table 48
6 to 3	-	not used
2 to 0	ID[2:0]	device type identification 010 = TEF6862

8.1.6 Read mode: data byte TEMP

Table 17. TEMP - data byte 5h bit allocation

7	6	5	4	3	2	1	0
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 18. TEMP - data byte 5h bit description

Bit	Symbol	Description
7 to 0	TEMP[7:0]	chip temperature; 1 step ≈ 1 K; relative indication

8.2 Write mode

The tuner is controlled by the I²C-bus. After the IC address the MSA byte contains the control of the tuning action via the bits MODE[2:0] and REGC and subaddressing via bits SA[3:0] (see Figure 7).

The tuner circuit is controlled by the CONTROL register. Any data change in the CONTROL register has immediate effect and will change the operation of the tuner circuit accordingly. The subaddress range 00h to 05h includes data that may lead to audible disturbance when changed. Therefore the subaddress range 00h to 05h is not loaded in the CONTROL register directly but loaded in a BUFFER register instead. This allows the IC to take care of tuning actions and mute control, freeing the microcontroller from cumbersome controls and timings. The subaddress range of 06h to 0Fh does not contain such critical data. I²C-bus information in the range 06h to 0Fh will be loaded in the CONTROL register directly (at acknowledge of each byte).

Controlled by a state machine the BUFFER data will be loaded in the CONTROL register for new settings. However at the same time the CONTROL data is loaded in the BUFFER register. This register swap action allows a fast return to the previous setting because the previous data remains available in the BUFFER register (see Figure 8 and Figure 9).

Via MODE several operational modes can be selected for the state machine. MODE offers all standard tuning actions as well as generic control for flexibility. The state machine controls the tuner by controlling I²C-bus data and internal circuits like the IF counter and mute. Action progress is monitored by the accompanying signal processor via the AFSAMPLE and AFHOLD lines, this way functions like weak signal processing can be controlled complementary to the tuner action.

The state machine operation starts at the end of transmission (P = STOP). In case a previous action is still active this is ignored and the new action defined by MODE is started immediately. When only the address byte is transmitted no action is started however (device presence test).

To minimize the I²C-bus transmission time only bytes that include data changes need to be written. Following the MSA byte the transmission can start at any given data byte defined by the subaddress (SA) bits.

Furthermore when writing the buffered range either the current BUFFER data or the current CONTROL data can be used as default, controlled by the REGC bit: with REGC = 0 any BUFFER data that is not newly written via I²C-bus remains unchanged. In general the BUFFER register will contain the previous tuner setting so this becomes default for the new setting. When only the MSA byte is transmitted defining a tuning MODE with REGC = 0 the tuner will return to its previous settings (see Figure 8). Instead with REGC = 1 the BUFFER register is loaded with data from the CONTROL register first, this way not written BUFFER data equals the CONTROL data. Since the CONTROL register contains the current tuner setting with REGC = 1 the current tuner setting is default for the new setting. When a tuning MODE action is defined with REGC = 1 the tuner will keep its current settings (CONTROL = current) for all data that is not newly written during the transmission (see Figure 9).

After power-on reset, all registers are in their default settings. The tuning mute circuit is muted. The control signals for the signal processors are set to AFSAMPLE = HIGH and AFHOLD = HIGH. An action of the state machine de-mutes the circuit.

Table 19. Write mode subaddress overview

Subaddress	Name	Default	Reference
0h	BANDWIDTH	1111 1110b	Section 8.2.2
1h	PLLM	0000 1000b	Section 8.2.3
2h	PLLL	0111 1110b	Section 8.2.4
3h	DAA	0100 0000b	Section 8.2.5
4h	AGC	1000 0000b	Section 8.2.6
5h	BAND	0010 0000b	Section 8.2.7
6h	CONTROL	1001 1000b	Section 8.2.8
7h	LEVEL	1000 0100b	Section 8.2.9
8h	IFCF	0010 0000b	Section 8.2.10
9h	IFCAP	0000 1000b	Section 8.2.11
Ah	ACD	0100 1010b	Section 8.2.12
Fh	TEST	0000 0000b	Section 8.2.13

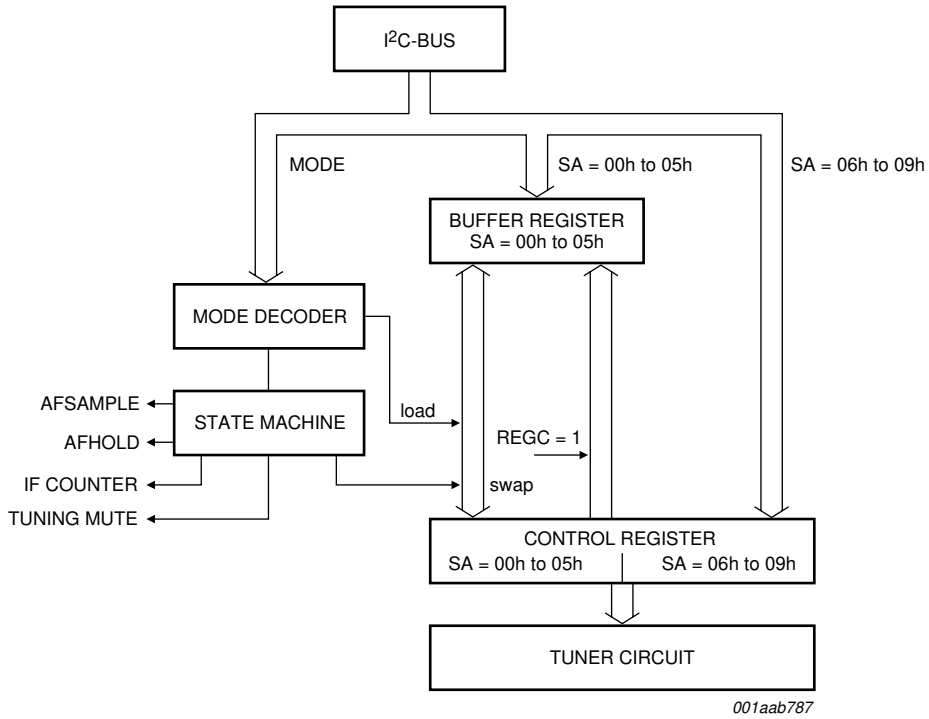

Fig 7. I²C-bus control

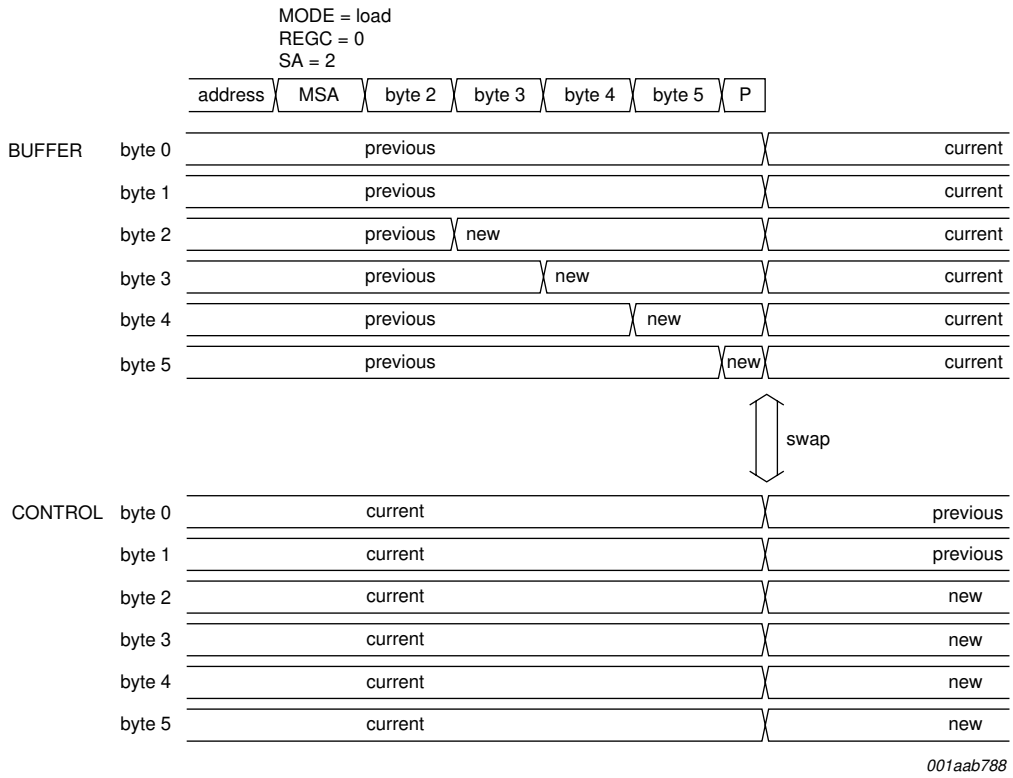

Fig 8. Write to CONTROL register with swap, REGC = 0

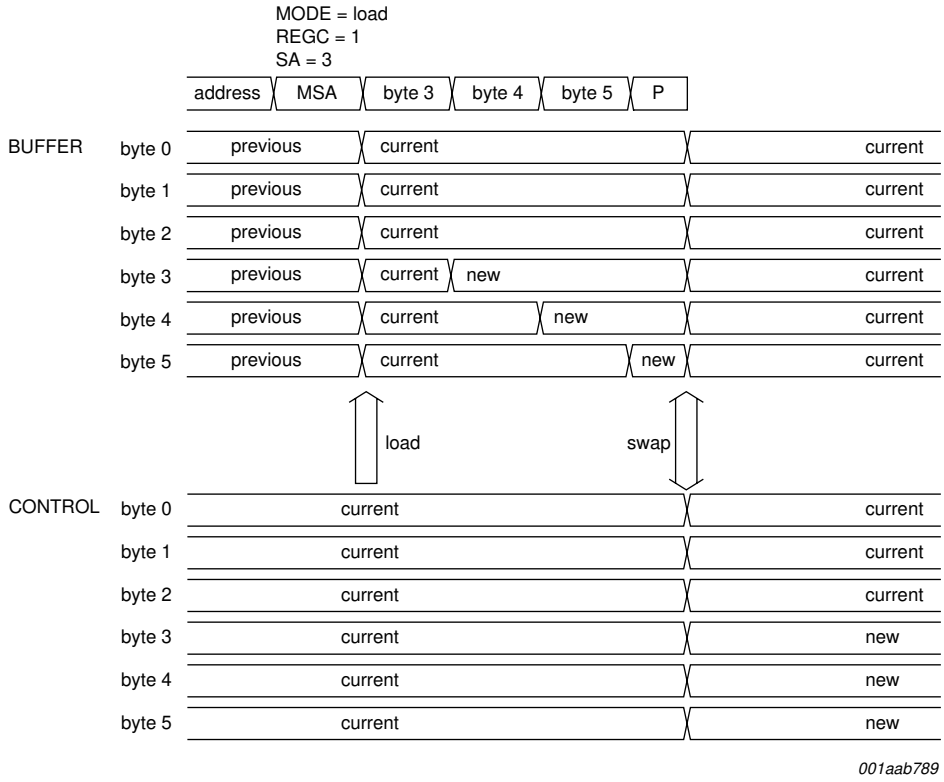

Fig 9. Write to CONTROL register with swap, REGC = 1

8.2.1 Mode and subaddress byte for write

Table 20. MSA - mode and subaddress byte bit allocation

7	6	5	4	3	2	1	0
MODE2	MODE1	MODE0	REGC	SA3	SA2	SA1	SA0

Table 21. MSA - mode and subaddress byte bit description

Bit	Symbol	Description
7 to 5	MODE[2:0]	mode; see Table 22
4	REGC	register mode
		0 = buffer mode or back mode: previous tuning data is default for new I²C-bus write (data of the BUFFER register is not changed before I²C-bus write); see Figure 8
		1 = control mode or current mode: current tuning data is default for new I²C-bus write (the BUFFER register is loaded with CONTROL register data before I²C-bus write); see Figure 9
3 to 0	SA[3:0]	subaddress; write data byte subaddress 0 to 15. The subaddress value is auto-incremented and will revert from SA = 15 to SA = 0. The auto-increment function cannot be switched off.

Table 22. Tuning action modes[1]

MODE2	MODE1	MODE0	Symbol	Description
0	0	0	buffer	write BUFFER register, no state machine action, no swap
0	0	1	preset	tune to new program with 60 ms mute control; swap[2]; see Figure 10 and Figure 11
0	1	0	search	tune to new program and stay muted (for release use end mode); swap[2]; see Figure 12 and Figure 13
0	1	1	AF update	tune to AF program; check AF quality and tune back to main program; two swap operations[3]; see Figure 14 and Figure 15
1	0	0	jump	tune to AF program in minimum time; swap; see Figure 16 and Figure 17
1	0	1	check	tune to AF program and stay muted (for release use end mode); swap; see Figure 18 and Figure 19
1	1	0	load	write CONTROL register via BUFFER; no state machine action; immediate swap; see Figure 8 and Figure 9
1	1	1	end	end action; release mute; no swap; see Figure 20

[1] When the write transmission of a state machine command starts during a mute state of the state machine, the sequences of the state machine start immediately with the actions which follow the mute period in the standard sequence (see Figure 11, Figure 13, Figure 15, Figure 17 and Figure 19).

[2] In the modes preset and search the AM AGC time constant is set to fast during the period of complete mute.

[3] The AF update sequence can also be started by pulling the AFHOLD pin LOW. In this case the AF information should be loaded into the BUFFER before. LOW period for a correct AF update timing: $t_{LOW} > 20\ \mu s$. Between the end of the I²C-bus transmission and the falling edge of the AFHOLD pulse a delay of $\geq 20\ \mu s$ is necessary.

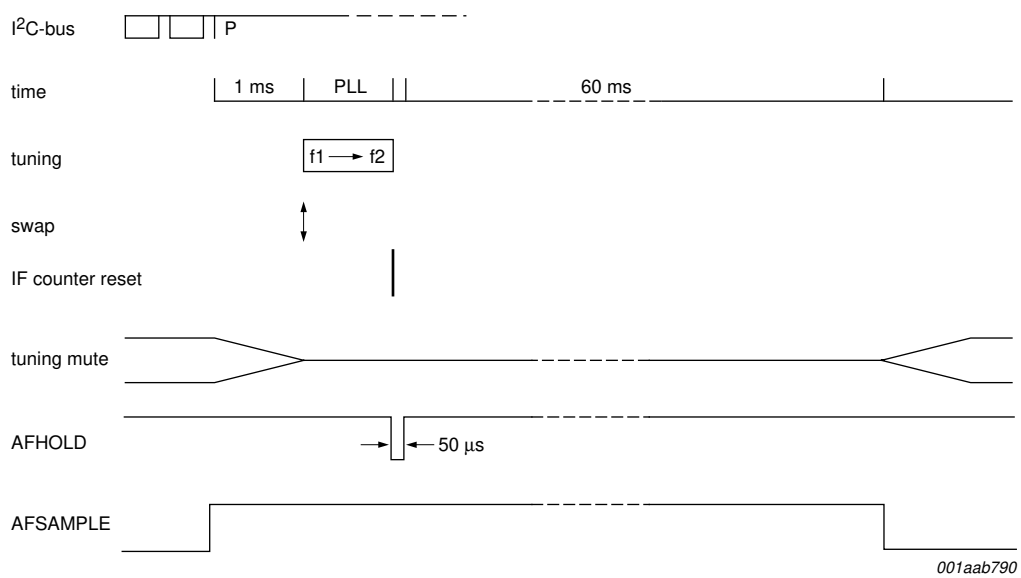

Fig 10. Preset mode

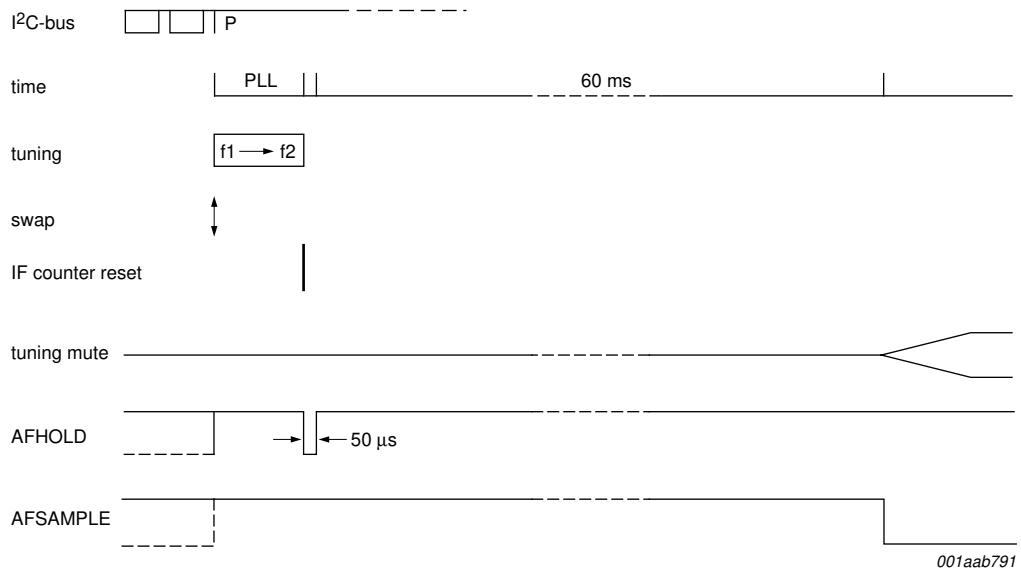

Fig 11. Preset mode, started during mute

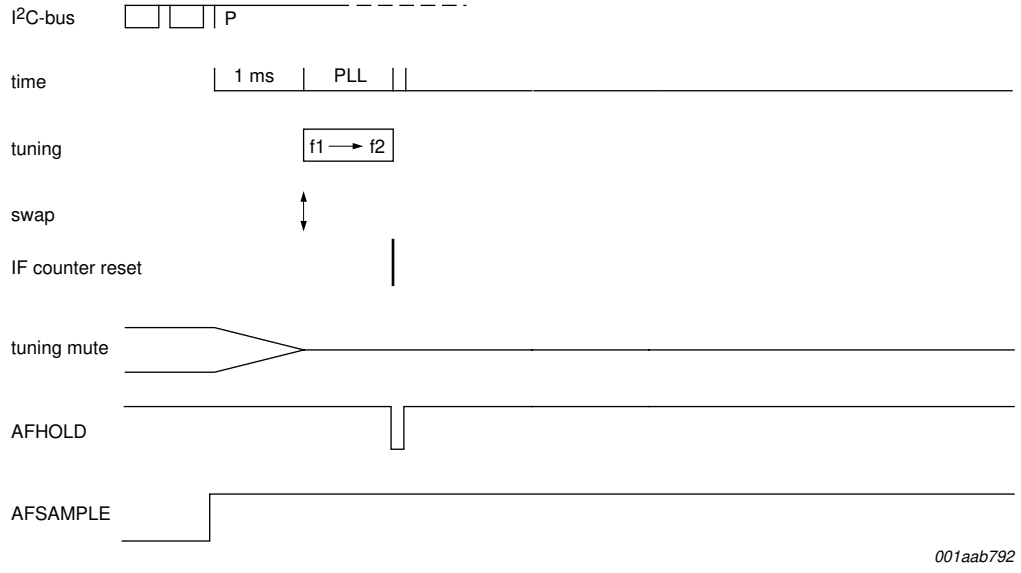

Fig 12. Search mode

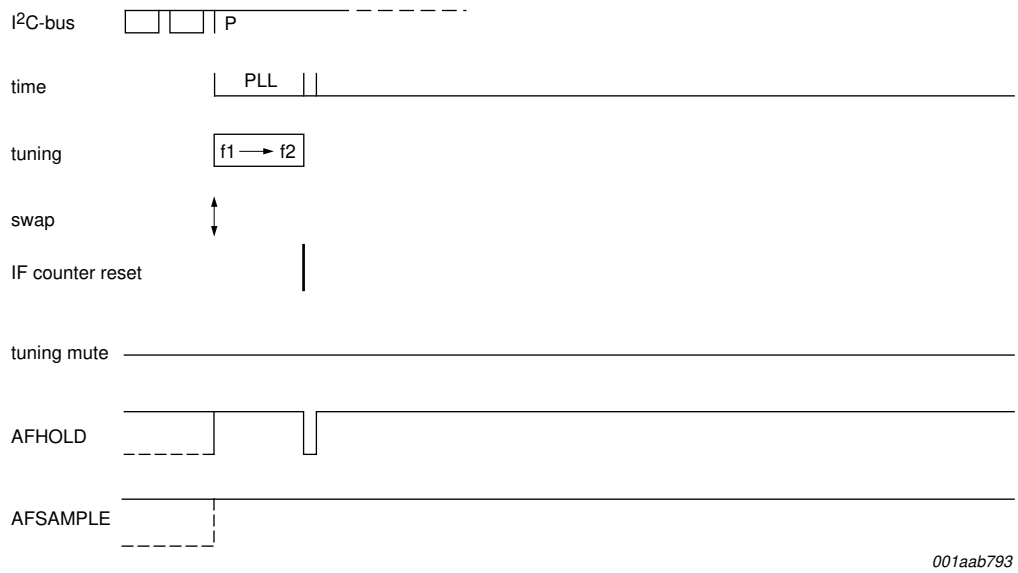

Fig 13. Search mode, started during mute

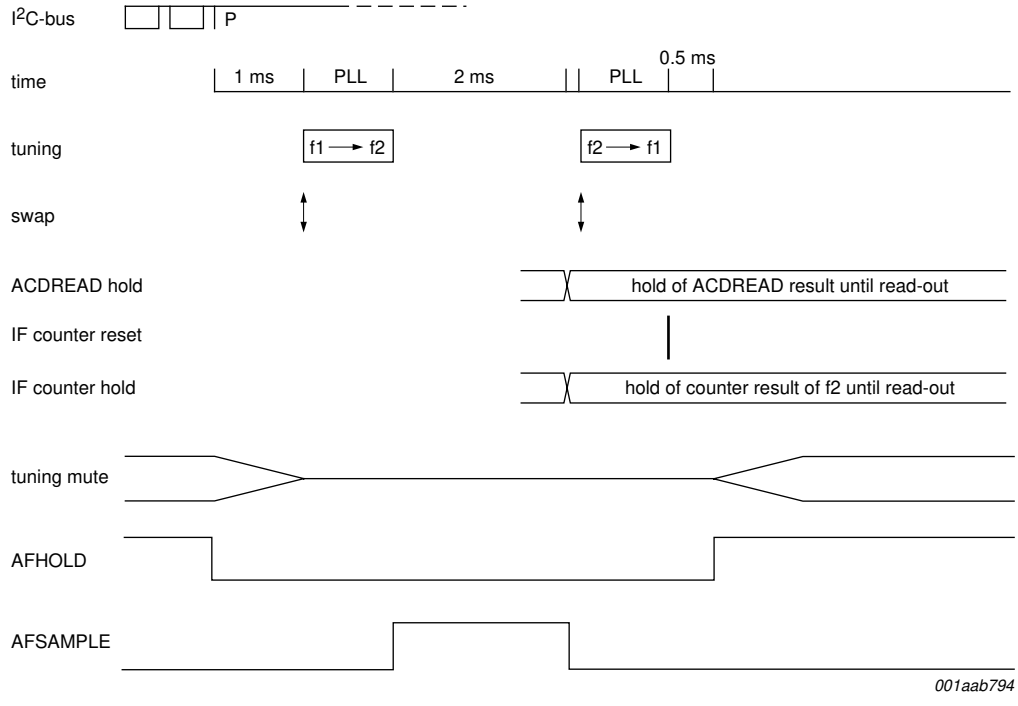

Fig 14. AF update mode

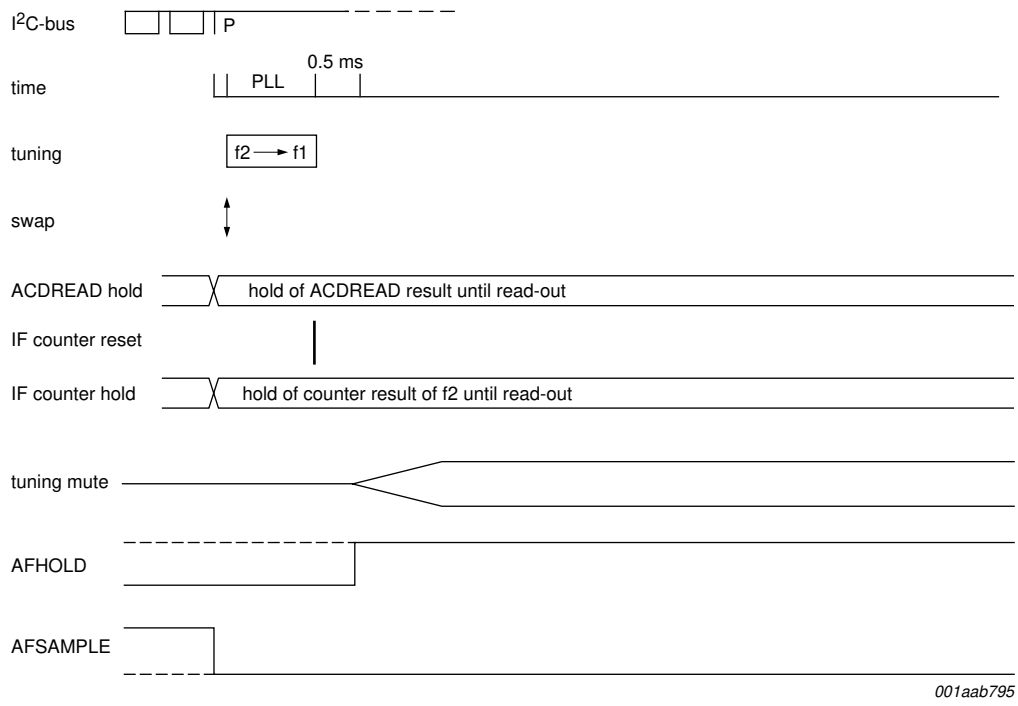

Fig 15. AF update mode, started during mute

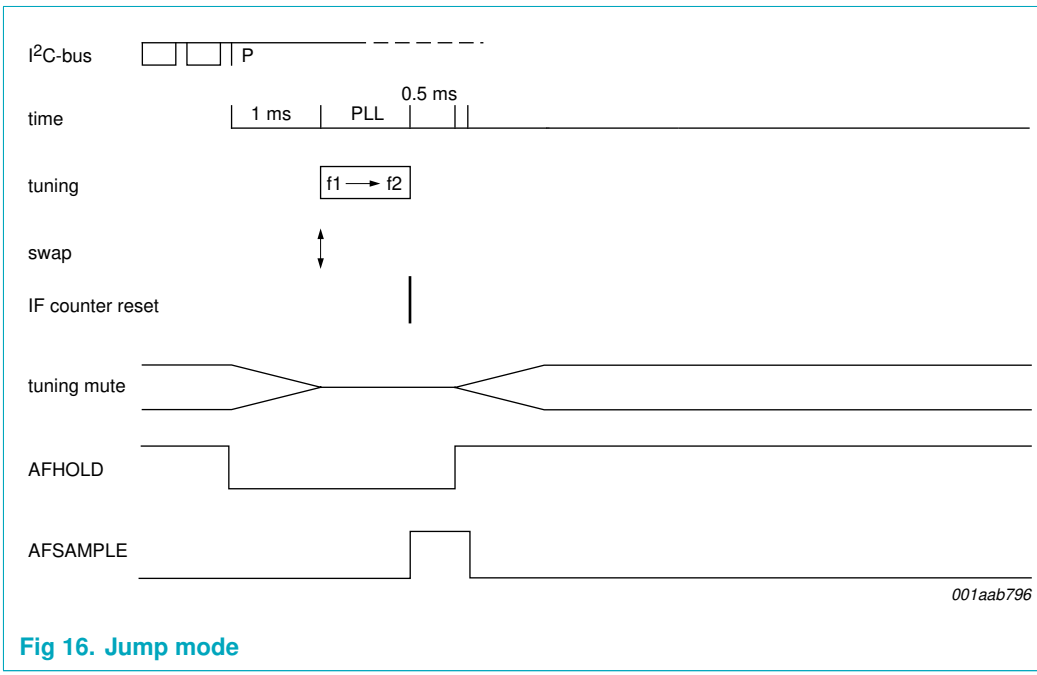

Fig 16. Jump mode

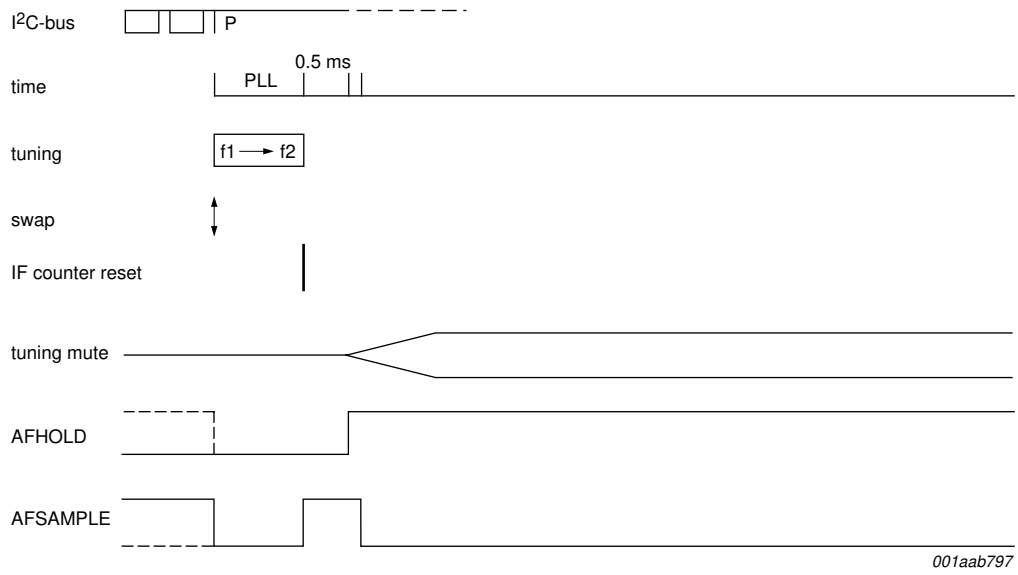

Fig 17. Jump mode, started during mute

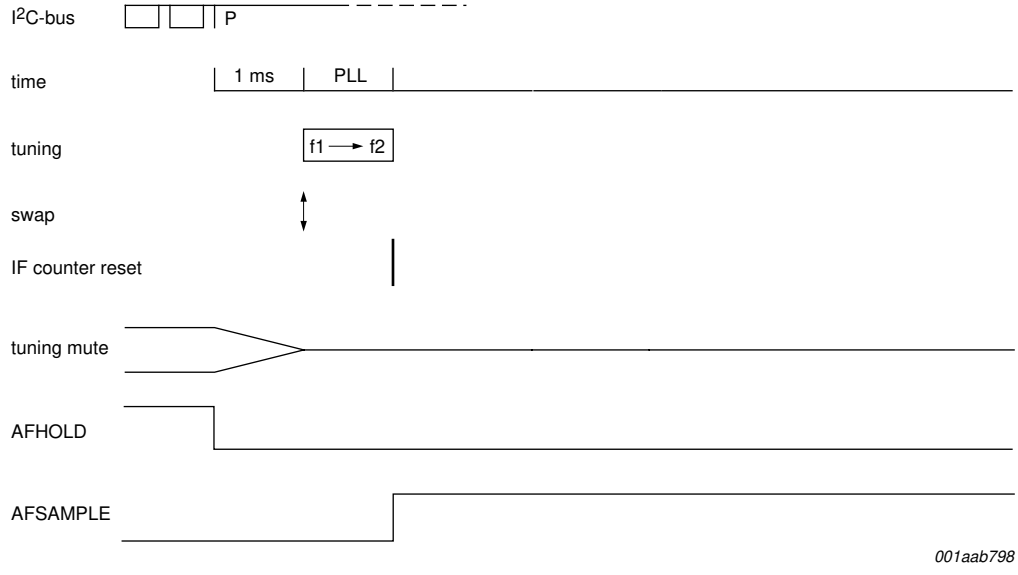

Fig 18. Check mode

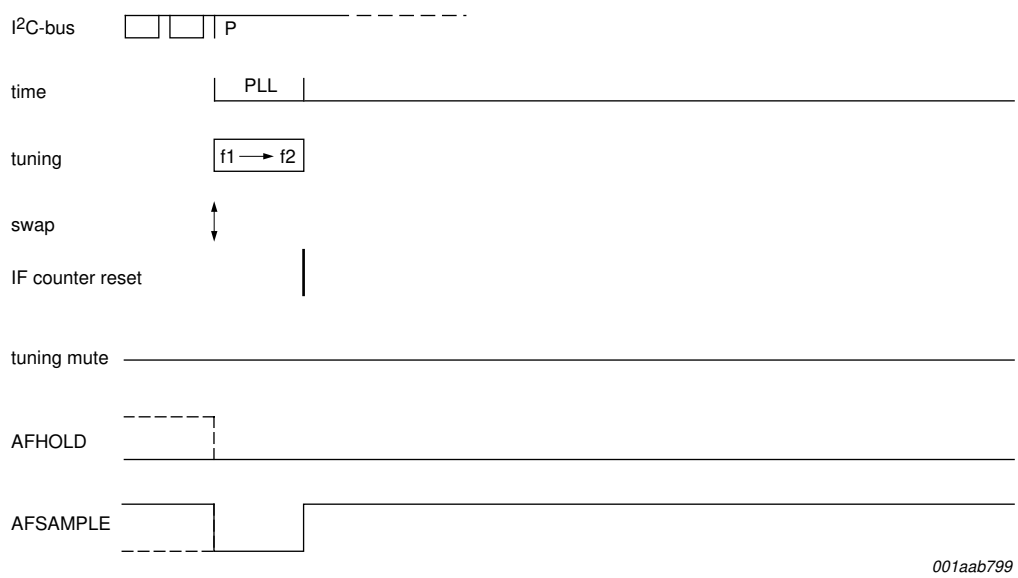

Fig 19. Check mode, started during mute

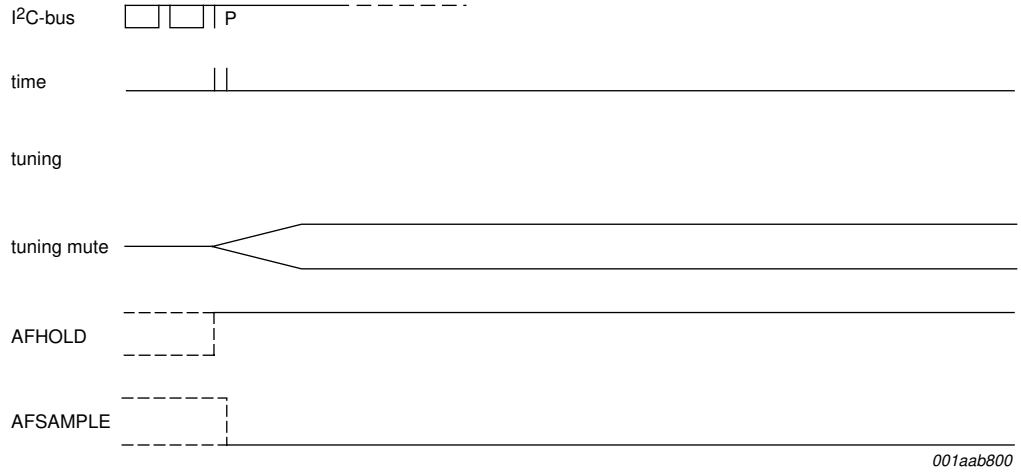

Fig 20. End mode

8.2.2 Write mode: data byte BANDWIDTH

Table 23. BANDWIDTH - data byte 0h bit allocation with default setting (buffered)

7	6	5	4	3	2	1	0
DYN	BW4	BW3	BW2	BW1	BW0	TE1	FLAG
1	1	1	1	1	1	1	0