



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



DATA SHEET



TEF6892H

Car radio integrated signal
processor

Product specification

2003 Oct 21

Car radio integrated signal processor

TEF6892H

CONTENTS

1	FEATURES	11.1.4	Data byte 4; RDS STATUS
1.1	General	11.1.5	Data byte 5; RDS LDATM
1.2	I ² C-bus	11.1.6	Data byte 6; RDS LDATL
1.3	Stereo decoder	11.1.7	Data byte 7; RDS PDATM
1.4	Noise blanking	11.1.8	Data byte 8; RDS PDATL
1.5	Weak signal processing	11.1.9	Data byte 9; RDS COUNT
1.6	RDS demodulator and decoder	11.1.10	Data byte 10; RDS PBIN
1.7	Tone/volume part	11.2	Write mode
2	GENERAL DESCRIPTION	11.2.1	Subaddress 0H; RDS SET A
3	ORDERING INFORMATION	11.2.2	Subaddress 1H; RDS SET B
4	QUICK REFERENCE DATA	11.2.3	Subaddress 2H; RDSCLK
5	BLOCK DIAGRAM	11.2.4	Subaddress 3H; RDS CONTROL
6	PINNING	11.2.5	Subaddress 4H; CONTROL
7	FUNCTIONAL DESCRIPTION	11.2.6	Subaddress 5H; CSALIGN
7.1	Stereo decoder	11.2.7	Subaddress 6H; MULTIPATH
7.2	FM and AM noise blanker	11.2.8	Subaddress 7H; SNC
7.3	High cut control and de-emphasis	11.2.9	Subaddress 8H; HIGHCUT
7.4	Noise detector	11.2.10	Subaddress 9H; SOFTMUTE
7.4.1	FM noise detector	11.2.11	Subaddress AH; RADIO
7.4.2	AM noise detector	11.2.12	Subaddress BH; INPUT and ASI
7.5	Multipath/weak signal processing	11.2.13	Subaddress CH; LOUDNESS
7.6	Tone/volume control	11.2.14	Subaddress DH; VOLUME
7.6.1	Input selector	11.2.15	Subaddress EH; TREBLE
7.6.2	Loudness	11.2.16	Subaddress FH; BASS
7.6.3	Volume/balance	11.2.17	Subaddress 10H; FADER
7.6.4	Treble	11.2.18	Subaddress 11H; BALANCE
7.6.5	Bass	11.2.19	Subaddress 12H; MIX
7.6.6	Fader/mute	11.2.20	Subaddress 13H; BEEP
7.6.7	Beep generator and NAV input with output mixer	11.2.21	Subaddress 1FH; AUTOGATE
7.7	RDS demodulator and decoder	12	TEST AND APPLICATION INFORMATION
7.7.1	RDS demodulator	13	PACKAGE OUTLINE
7.7.2	RDS decoder	14	SOLDERING
8	LIMITING VALUES	14.1	Introduction to soldering surface mount packages
9	THERMAL CHARACTERISTICS	14.2	Reflow soldering
10	CHARACTERISTICS	14.3	Wave soldering
11	I ² C-BUS PROTOCOL	14.4	Manual soldering
11.1	Read mode	14.5	Suitability of surface mount IC packages for wave and reflow soldering methods
11.1.1	Data byte 1; STATUS	15	DATA SHEET STATUS
11.1.2	Data byte 2; LEVEL	16	DEFINITIONS
11.1.3	Data byte 3; USN and WAM	17	DISCLAIMERS
		18	PURCHASE OF PHILIPS I ² C COMPONENTS

Car radio integrated signal processor

TEF6892H

1 FEATURES

1.1 General

- High integration
- No external components except coupling capacitors for signal inputs and outputs
- QFP44 package with small Printed-Circuit Board (PCB) footprint.

1.2 I²C-bus

- Fast mode 400 kHz I²C-bus, interfaces to logic levels ranging from 2.5 to 5 V
- Gated I²C-bus loop through to tuner IC
 - Eases PCB layout (crosstalk)
 - Allows mix of 400 kHz and 100 kHz busses
 - Low bus load reduces crosstalk
 - Buffered I/O circuit
 - Supply voltage shift between both buses allowed.
- Shortgate function offers easy control with automatic gating of a single transmission; suited for TEA684x
- Autogate function offers transparent microcontroller control with automatic on/off gating (programmable address).

1.3 Stereo decoder

- FM stereo decoder with high immunity to birdy noise and excellent pilot cancellation
- Integrated IF roll-off correction controlled via I²C-bus
- De-emphasis selectable between 75 and 50 μ s via I²C-bus.

1.4 Noise blanking

- New fully integrated AM noise blanker with excellent performance
- Fully integrated FM noise blanker with superior performance.



1.5 Weak signal processing

- FM weak signal processing with detectors for RF level, Ultrasonic Noise (USN) and Wideband AM (WAM) information
- AM weak signal processing with detectors for level information
- AM processing with soft mute and High Cut Control (HCC)
- FM processing with soft mute, stereo blend and HCC
- Setting of the sensitivity of the detectors and start and slope of the control functions via I²C-bus
- Weather band de-emphasis
- Level, USN and WAM read-out via I²C-bus (signal quality detectors)
- Full support of tuner AF update functions with TEA684x tuner ICs, FM audio processing holds the detectors for the FM weak signal processing in their present state during RDS updating.

1.6 RDS demodulator and decoder

- RDS/RBDS demodulator uses TEA684x reference frequency, no external crystal necessary
- RDS/RBDS decoder with memory for two RDS data blocks provides block synchronization, error correction and flywheel function; block data and status information are available via the I²C-bus.

Car radio integrated signal processor

TEF6892H

1.7 Tone/volume part

- Input selector for four inputs:
 - Two external stereo inputs (CD and TAPE)
 - One mono input (PHONE)
 - One internal stereo input (AM or FM).
- Integrated tone control and audio filters without external components
- Volume control from +20 to –79 dB in 1 dB steps; programmable 20 dB loudness control included
- Programmable loudness control with bass boost or as bass and treble boost
- Treble control from –14 to +14 dB in 2 dB steps
- Bass control from –14 to +14 dB in 2 dB steps with selectable characteristics
- Good undistorted performance for any step size, including mute
- Audio Step Interpolation (ASI) available for the following audio controls:
 - Mute
 - Loudness
 - Volume/balance
 - Bass
 - Fader.
- ASI also realizes Alternative Frequency (AF) mute for inaudible RDS update
- Integrated beep generator
- Navigation (NAV) input
- Output mixer circuit for beep or NAV signal at output stages.

2 GENERAL DESCRIPTION

The TEF6892H is a monolithic BiMOS integrated circuit comprising the stereo decoder function, weak signal processing and ignition noise blanking facility for AM and FM combined with input selector and tone/volume control for AM and FM car radio applications. The RDS/RBDS demodulator function and the RDS/RBDS decoder function are included. The device operates with a supply voltage of 8 to 9 V.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEF6892H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

Car radio integrated signal processor

TEF6892H

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current	normal mode	–	28	–	mA
		standby RDS; audio on	–	24	–	mA
		standby audio; RDS on	–	19	–	mA
		standby	–	15	–	mA
Stereo decoder path						
α_{CS}	channel separation	$f_{FMMPX} = 1 \text{ kHz}$	40	–	–	dB
S/N	signal-to-noise ratio	$f_{FMMPX} = 20 \text{ Hz to } 15 \text{ kHz}$	75	–	–	dB
THD	total harmonic distortion	FM mode; $f_{FMMPX} = 1 \text{ kHz}$	–	–	0.3	%
Tone/volume control						
$V_{i(max)(rms)}$	maximum input voltage level at pins TAPEL, TAPER, CDL, CDR, CDCM, PHONE and PHCM (RMS value)	THD = 0.1%; $G_{vol} = -6 \text{ dB}$	2	–	–	V
$V_{i(NAV)(max)(rms)}$	maximum input voltage level at pin NAV (RMS value)	THD = 1%; $f_{NAV} = 1 \text{ kHz}$	0.3	–	–	V
THD	total harmonic distortion	TAPE and CD inputs; $f_{audio} = 20 \text{ Hz to } 20 \text{ kHz};$ $V_i = 1 \text{ V (RMS)}$	–	0.01	0.1	%
G_{vol}	volume/balance gain control	maximum setting	–	20	–	dB
		minimum setting	–	–59	–	dB
$G_{step(vol)}$	step resolution gain (volume)		–	1	–	dB
$G_{loudness}$	loudness gain control	$f_{loudness(low)} = 50 \text{ Hz};$ high boost on maximum setting; 1 kHz tone	–	0	–	dB
		minimum setting; 1 kHz tone	–	–20	–	dB
G_{treble}	treble gain control	maximum setting	–	14	–	dB
		minimum setting	–	–14	–	dB
$G_{step(treble)}$	step resolution gain (treble)		–	2	–	dB
G_{bass}	bass gain control	maximum setting; symmetrical boost	–	14	–	dB
		minimum setting; asymmetrical cut	–	–14	–	dB
$G_{step(bass)}$	step resolution gain (bass)		–	2	–	dB

Car radio integrated signal processor

TEF6892H

5 BLOCK DIAGRAM

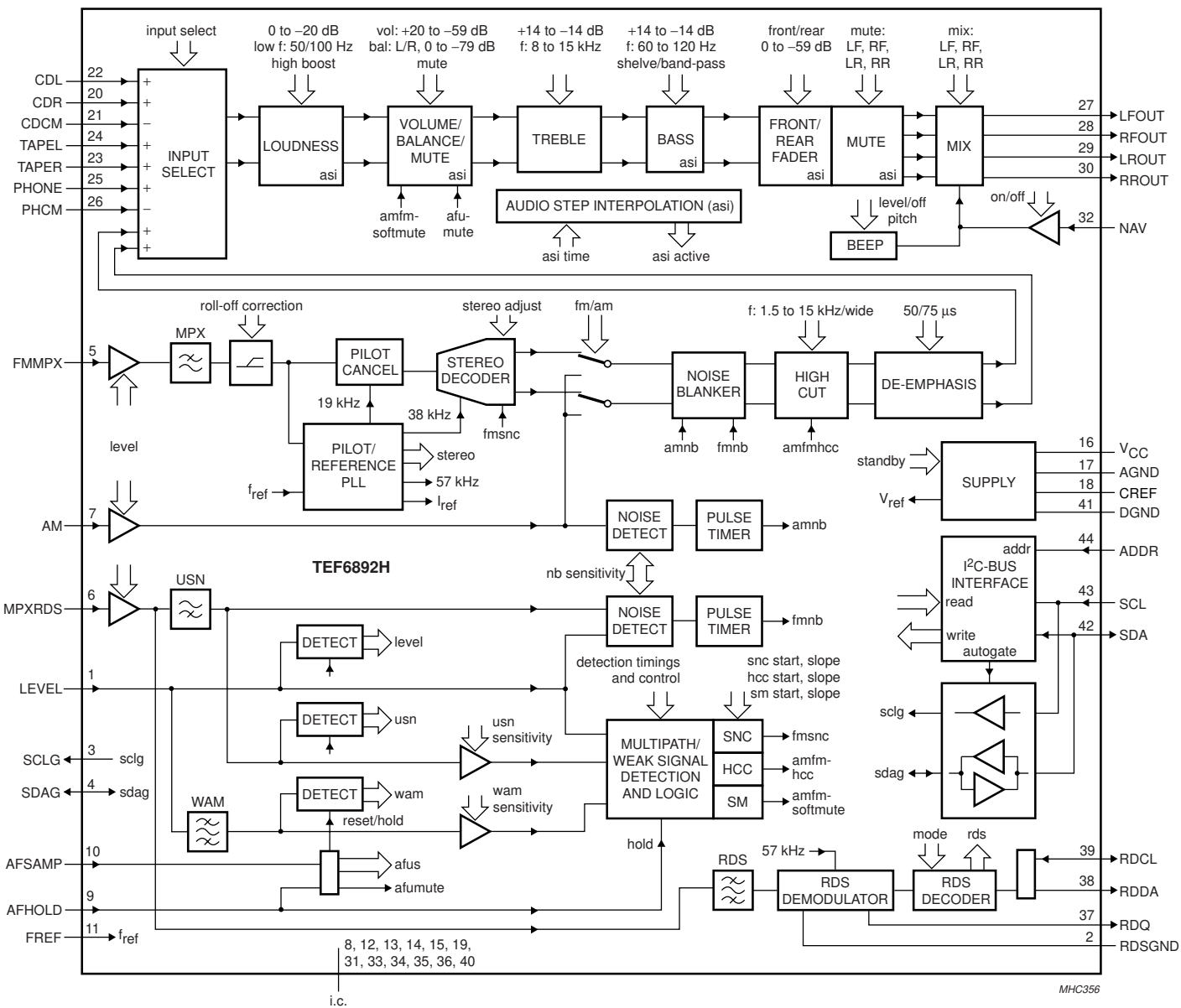


Fig.1 Block diagram.

MHC356

Car radio integrated signal processor

TEF6892H

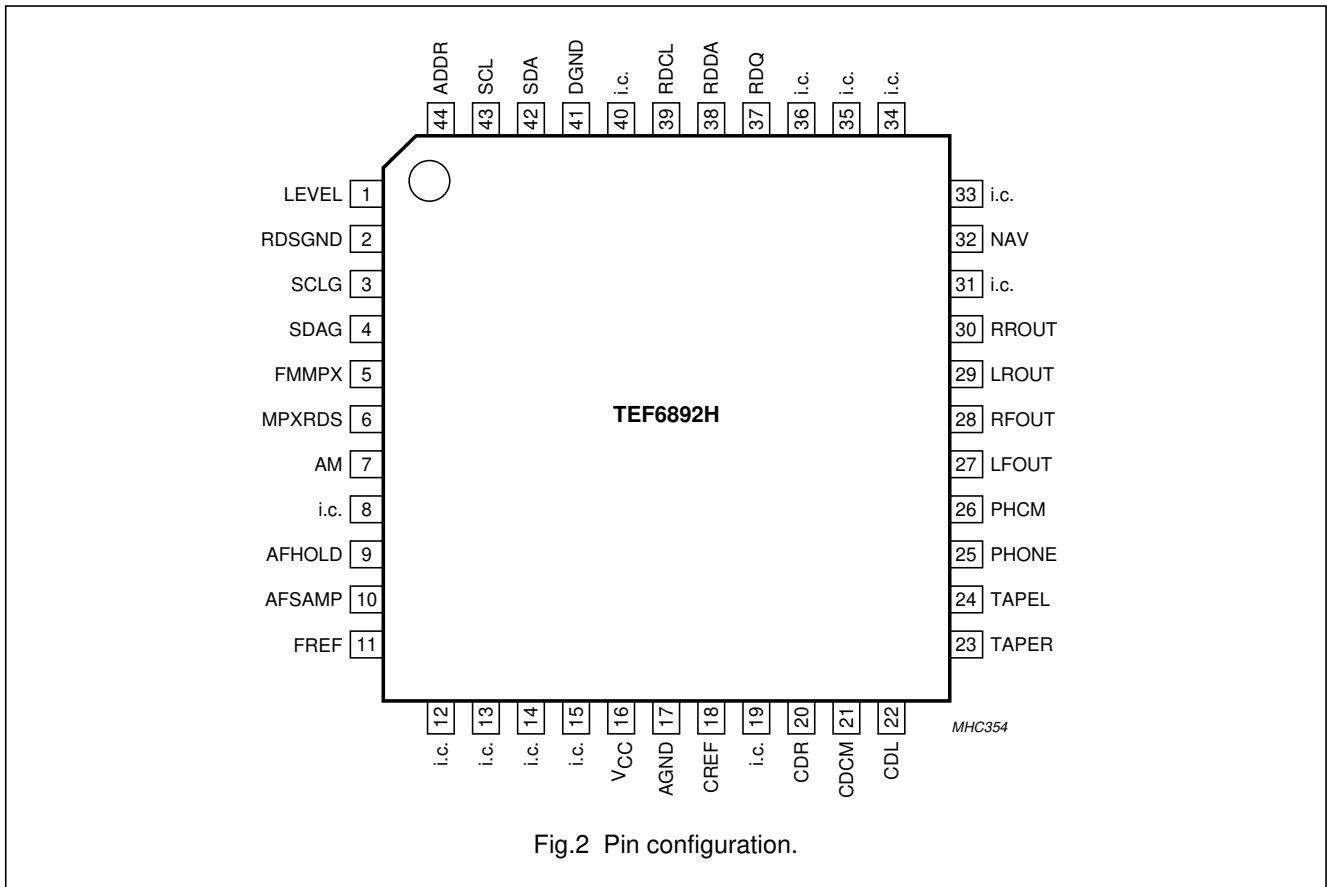
6 PINNING

SYMBOL	PIN	DESCRIPTION
LEVEL	1	level detector input
RDSGND	2	RDS ground
SCLG	3	gated I ² C-bus clock port
SDAG	4	gated I ² C-bus data port
FMMPX	5	FM-MPX input for audio processing
MPXRDS	6	FM-MPX input for weak signal processing, noise blanker and RDS demodulator
AM	7	AM audio input
i.c.	8	internally connected
AFHOLD	9	FM weak signal processing hold input
AFSAMP	10	trigger signal input for quality measurement
FREF	11	reference frequency input 75.4 kHz
i.c.	12	internally connected
i.c.	13	internally connected
i.c.	14	internally connected
i.c.	15	internally connected
V _{CC}	16	supply voltage
AGND	17	analog ground
CREF	18	reference voltage capacitor
i.c.	19	internally connected
CDR	20	CD right input
CDCM	21	CD common input
CDL	22	CD left input
TAPER	23	tape right input
TAPEL	24	tape left input
PHONE	25	phone input
PHCM	26	phone common input
LFOUT	27	left front output
RFOUT	28	right front output
LROUT	29	left rear output
RROUT	30	right rear output
i.c.	31	internally connected
NAV	32	audio input for navigation voice signal
i.c.	33	internally connected
i.c.	34	internally connected
i.c.	35	internally connected
i.c.	36	internally connected
RDQ	37	RDS/RBDS demodulator quality information output
RDDA	38	RDS/RBDS decoder data available or RDS/RBDS demodulator data output
RDCL	39	RDS/RBDS demodulator clock input or output
i.c.	40	internally connected

Car radio integrated signal processor

TEF6892H

SYMBOL	PIN	DESCRIPTION
DGND	41	digital ground
SDA	42	I ² C-bus data input or output
SCL	43	I ² C-bus clock input
ADDR	44	address select input



7 FUNCTIONAL DESCRIPTION

7.1 Stereo decoder

The FMMPX input is the input for the MPX signal from the tuner. The input gain can be selected in three settings to match the input to the RF front-end circuit. A fourth setting is used for weather band mode, which may require a gain of 23.5 dB.

A low-pass filter provides the necessary signal delay for FM noise blanking and suppression of high frequency interferences into the stereo decoder input. The output signal of this filter is fed to the roll-off correction circuit. This circuit compensates the frequency response caused by the low-pass characteristic of the tuner circuit with its IF filters. The roll-off correction circuit is adjustable in four

settings to compensate different frequency responses of the tuner part.

The MPX signal is decoded in the stereo decoder part. A PLL is used for the regeneration of the 38 kHz subcarrier. The fully integrated oscillator is adjusted by a digital auxiliary PLL into the capture range of the main PLL. The auxiliary PLL needs an external reference frequency (75.4 kHz) which is provided by the tuner ICs of the NICE family (TEA684x). The required 19 and 38 kHz signals are generated by division of the oscillator output signal in a logic circuit. The 19 kHz quadrature phase signal is fed to the 19 kHz phase detector, where it is compared with the incoming pilot tone. The DC output signal of the phase detector controls the oscillator (PLL).

Car radio integrated signal processor

TEF6892H

The pilot detector is driven by an internally generated in-phase 19 kHz signal. Its pilot dependent voltage activates the stereo indicator bit and sets the stereo decoder to stereo mode. The same voltage is used to control the amplitude of an anti-phase internally generated 19 kHz signal. In the pilot canceller, the pilot tone is compensated by this anti-phase 19 kHz signal.

The signal is then decoded in the decoder part. The side signal is demodulated and combined with the main signal to the left and right audio channels. A fine adjustment of the roll-off compensation is done by adjusting the gain of the L-R signal in 16 steps. A smooth mono to stereo takeover is achieved by controlling the efficiency of the matrix by the FMSNC signal from the weak signal processing block.

7.2 FM and AM noise blanker

The FM/AM switch selects the output signal of the stereo decoder (FM mode) or the signal from the AM input for the noise blanker block. In FM mode the noise blanker operates as a sample and hold circuit, while in AM mode it mutes the audio signal during the interference pulse. The blanking pulse which triggers the noise blanker is generated in the noise detector block.

7.3 High cut control and de-emphasis

The High Cut Control (HCC) part is a low-pass filter circuit with eight different static roll-off response curves. The cut-off frequencies of these filter curves can be selected by I²C-bus to match different application requirements. The HCC circuit also provides a dynamic control of the filter response. This function is controlled by the AMFMHCC signal from the weak signal processing.

The signal passes the de-emphasis block with two de-emphasis values (50 and 75 μ s), which can be selected via I²C-bus, and is fed to the input selector.

7.4 Noise detector

7.4.1 FM NOISE DETECTOR

The trigger signal for the FM noise detector is derived from the MPXRDS input signal and the LEVEL signal. In the MPXRDS path a four pole high-pass filter (100 kHz) separates the noise spikes from the wanted MPX signal. Another detector circuit triggers on noise spikes on the level voltage. The signals of both detectors are combined to achieve a reliable trigger signal for the noise blanker. AGC circuits in the detector part control the gain depending on the average noise in the signals to prevent false triggering. The sensitivity of the triggering from the

MPXRDS signal can be adjusted in four steps, the triggering from the LEVEL signal in three steps.

7.4.2 AM NOISE DETECTOR

The trigger pulse for the AM noise blanker is derived from the AM audio signal. The noise spikes are detected by a slew rate detector, which detects excessive slew rates which do not occur in normal audio signals. The sensitivity of the AM noise blanker can be adjusted in four steps.

7.5 Multipath/weak signal processing

The multipath (MPH)/weak signal processing block detects quality degradations in the incoming FM signal and controls the processing of the audio signal accordingly. There are three different quality criteria:

- The average value of the level voltage
- The AM components on the level voltage [Wideband AM (WAM)]
- The high frequency components in the MPX signal [Ultrasonic Noise (USN)].

The level voltage is converted to a digital value by an 8-bit analog-to-digital converter. A digital filter circuit (WAM filter) derives the wideband AM components from the level signal. The high frequency components in the MPX signals are measured with an analog-to-digital converter (USN ADC) at the output of the 100 kHz high-pass filter in the MPXRDS path.

The values of these three signals are externally available via the I²C-bus.

In the weak signal processing block the three digital signals are combined in a specific way and used for the generation of control signals for soft mute, stereo blend (stereo noise control, FMSNC) and high cut control (AMFMHCC).

The sensitivities of the detector circuits (WAM and USN) are adjustable via the I²C-bus.

Also the start values and the slopes of the control functions soft mute, stereo blend and high cut control can be set via the I²C-bus.

Soft mute, stereo blend and HCC are set on hold during the AF updating (quality check of alternative frequency) to avoid an influence of the tuning procedure on the weak signal processing conditions.

In AM mode the soft mute and high cut control are available too, the weak signal block is controlled by the average value of the level voltage.

Car radio integrated signal processor

TEF6892H

7.6 Tone/volume control

The tone/volume control part consists of the following stages:

- Input selector
- Loudness control
- Volume/balance control with muting
- Treble control
- Bass control
- Fader and output mute
- Beep generator
- NAV input
- Output mixer.

The settings of all stages are controlled via the I²C-bus.

The stages input selector, loudness, volume/balance, bass, and fader/output mute include the Audio Step Interpolation (ASI) function. This minimizes pops by smoothing the transitions in the audio signal during the switching of the controls. The transition time of the ASI function is programmable by I²C-bus in four steps.

7.6.1 INPUT SELECTOR

The input selector selects one of four input sources:

- Two external stereo inputs (CD and TAPE)
- One external mono input (PHONE)
- One internal stereo input (AM/FM).

7.6.2 LOUDNESS

The output of the input selector is fed into the loudness circuit. Four different loudness curves can be selected via the I²C-bus. The control range is between 0 and –20 dB with a step size of 1 dB; see Figs 16 to 19.

7.6.3 VOLUME/BALANCE

The volume/balance control is used for volume setting and also for balance adjustment. The control range of the volume/balance control is between +20 and –59 dB in steps of 1 dB.

The combination of loudness and volume/balance realizes an overall control range of +20 to –79 dB.

7.6.4 TREBLE

The signal is then fed to the treble control stage. The control range is between +14 and –14 dB in steps of 2 dB. Figure 20 shows the control characteristic. Four different filter frequencies can be selected.

7.6.5 BASS

The characteristic of the bass attenuation curves can be set to shelve or band-pass. Four different frequencies can be selected as centre frequency of the band-pass curve. Figures 21 and 22 show the bass curves with a band-pass filter frequency of 60 Hz. The control range is between +14 and –14 dB in steps of 2 dB.

7.6.6 FADER/MUTE

The four fader/mute blocks are located at the end of the tone/volume chain. The control range of these attenuators is 0 to –59 dB. The step size is:

- 1 dB between 0 and –15 dB
- 2.5 dB between –15 and –45 dB
- 3 dB between –45 and –51 dB
- 4 dB between –51 and –59 dB.

7.6.7 BEEP GENERATOR AND NAV INPUT WITH OUTPUT MIXER

The output mixer circuit can add an additional audio signal to any of the four outputs together with the main signal or instead of the main signal.

The additional signal can be generated internally by the beep generator with four different audio frequencies or applied to the NAV input, for instance a navigation voice signal.

7.7 RDS demodulator and decoder

7.7.1 RDS DEMODULATOR

The RDS demodulator recovers and regenerates the continuously transmitted RDS or RBDS data stream of the multiplex signal (MPXRDS) and provides the signals clock (RDCL), data (RDDA) and quality (RDQ) for external use or further processing by the integrated RDS decoder. The RDS demodulator uses the reference frequency (75.4 kHz) from the tuner IC and does not need a crystal.

7.7.2 RDS DECODER

The RDS decoder provides block synchronization, error correction and flywheel function for reliable extraction of RDS or RBDS block data. Different modes of operation can be selected to fit different application requirements. Availability of new data is signalled by read bit RDAV and output pin RDDA. Up to two blocks of data and status information are available via the I²C-bus in a single transmission.

Car radio integrated signal processor

TEF6892H

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.3	+10	V
V_i	input voltage for any pin		-0.3	$V_{CC} + 0.3$	V
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{esd}	electrostatic discharge voltage	note 1	-200	+200	V
		note 2	-2000	+2000	V

Notes

1. Machine model ($R = 0 \Omega$, $C = 200 \text{ pF}$).
2. Human body model ($R = 1.5 \text{ k}\Omega$, $C = 100 \text{ pF}$).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	61	K/W

10 CHARACTERISTICS

FM part: $f_{FMMPX} = 1 \text{ kHz}$ at $V_{FMMPX} = 767 \text{ mV}$ (RMS); pilot off (100% FM). AM part: $f_{AM} = 1 \text{ kHz}$ at $V_{AM} = 967 \text{ mV}$ (RMS) (100% AM). Treble: 10 kHz filter frequency. Bass: 60 Hz filter frequency. Loudness: 50 Hz filter frequency; treble loudness on. $V_{CC} = 8.5 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; see Fig.23; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		8.0	8.5	9.0	V
I_{CC}	supply current	normal mode	-	28	-	mA
		standby RDS; audio on	-	24	-	mA
		standby audio; RDS on	-	19	-	mA
		standby	-	15	-	mA
Logic pins						
V_{IH}	HIGH-level input voltage	pins SDA, SCL, ADDR, SDAG and RDCL	1.75	-	5.5	V
		pins AFHOLD and AFSAMP	1.75	-	5.5	V
V_{IL}	LOW-level input voltage	pins SDA, SCL, ADDR, SDAG and RDCL	-0.2	-	+1.0	V
		pins AFHOLD and AFSAMP	-0.2	-	+1.0	V
V_{OH}	HIGH-level output voltage	pins RDCL and RDDA; $I_{OH} = 2.5 \mu\text{A}$	2.6	-	-	V
V_{OL}	LOW-level output voltage	pins SCLG, RDCL and RDDA; $I_{OL} = 3 \text{ mA}$; note 1	-	-	0.4	V
		pin SDA; $I_{OL} = 3 \text{ mA}$	-	-	0.4	V

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo decoder and AM path						
$V_{o(FM)(rms)}$	FM mono output voltage (RMS value) on pins LFOUT and RFOUT	$f_{FMMPX} = 1 \text{ kHz}$; 91% FM modulation without pilot ($V_{FMMPX} = 698 \text{ mV}$)	750	950	1200	mV
$V_{o(AM)(rms)}$	AM output voltage (RMS value) on pins LFOUT and RFOUT	$f_{AM} = 1 \text{ kHz}$; $V_{AM} = 870 \text{ mV}$; 90% AM modulation	800	1080	1360	mV
G_i	input gain on pins FMMPX, MPXRDS and AM	see Table 61 ING[1:0] = 00; all inputs ING[1:0] = 01; all inputs ING[1:0] = 10; all inputs ING[1:0] = 11; FMMPX ING[1:0] = 11; MPXRDS and AM	–	0 3 6 23.5 0	–	dB dB dB dB dB
α_{cs}	channel separation	$f_{FMMPX} = 1 \text{ kHz}$	40	–	–	dB
$g_{c(L-R)}$	roll-off correction for coarse adjustment of separation	see Table 45; measure 1 kHz level for L – R modulation; compare to 1 kHz level for L + R modulation CSR[1:0] = 00 CSR[1:0] = 01 CSR[1:0] = 10 CSR[1:0] = 11	–	0 0.4 0.8 1.2	–	dB dB dB dB
$g_{f(L-R)}$	stereo adjust for fine adjustment of separation	see Table 46; measure 1 kHz level for L – R modulation; compare to 1 kHz level for L + R modulation CSA[3:0] = 0000 CSA[3:0] = 0001 : CSA[3:0] = 1110 CSA[3:0] = 1111	–	0 0.2 : 2.8 3.0	–	dB dB dB dB dB
S/N	signal-to-noise ratio	$f_{FMMPX} = 20 \text{ Hz to } 15 \text{ kHz}$; referenced to 1 kHz at 91% FM modulation; DEMP = 1 ($\tau_{de-em} = 50 \mu\text{s}$)	75	–	–	dB
THD	total harmonic distortion	FM mode $f_{FMMPX} = 1 \text{ kHz}$ $V_{FMMPX} = 50\%$; L; pilot on $V_{FMMPX} = 50\%$; R; pilot on	–	–	0.3 0.3 0.3	% % %
$V_{o(bal)}$	mono channel balance $\frac{V_{oL}}{V_{oR}}$	FM mode	–1	–	+1	dB
α_{19}	pilot signal suppression	9% pilot; $f_{pilot} = 19 \text{ kHz}$; referenced to 1 kHz at 91% FM modulation; DEMP = 1 ($\tau_{de-em} = 50 \mu\text{s}$)	40	50	–	dB

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
α	subcarrier suppression	modulation off; referenced to 1 kHz at 91% FM modulation				
		$f_{sc} = 38$ kHz	35	50	–	dB
		$f_{sc} = 57$ kHz	40	–	–	dB
		$f_{sc} = 76$ kHz	50	60	–	dB
PSRR	power supply ripple rejection	FM mode; $f_{ripple} = 100$ Hz; $V_{CC(AC)} = V_{ripple} = 100$ mV (RMS)	24	–	–	dB
ΔV_{out}	frequency response	FM mode				
		$f_{FMMPX} = 20$ Hz	–0.5	–	+0.5	dB
		$f_{FMMPX} = 15$ kHz	–0.5	–	+0.5	dB
$f_{cut-off(de-em)}$	cut-off frequency of de-emphasis filter	–3 dB point; see Fig.15				
		DEMP = 1 ($\tau_{de-em} = 50$ μ s)	–	3.18	–	kHz
		DEMP = 0 ($\tau_{de-em} = 75$ μ s)	–	2.12	–	kHz
$m_{i(pilot)(rms)}$	pilot threshold modulation for automatic switching by pilot input voltage (RMS value)	stereo				
		on	–	4.0	5.5	%
		off	1.3	2.7	–	%
hys_{pilot}	hysteresis of pilot threshold voltage		–	2	–	dB
$V_{ref(min)}$	minimum reference input voltage		–	–	30	mV
f_{ref}	reference frequency for stereo PLL and RDS demodulator		75361	75368	75375	Hz
Noise blanker						
FM PART						
$t_{sup(min)}$	minimum suppression time		–	15	–	μ s
$V_{MPXRDS(M)}$	noise blanker sensitivity at MPXRDS input (peak value of noise pulses)	see Table 62; $t_{pulse} = 10$ μ s; $f_{pulse} = 300$ Hz				
		NBS[1:0] = 00	–	90	–	mV
		NBS[1:0] = 01	–	150	–	mV
		NBS[1:0] = 10	–	210	–	mV
		NBS[1:0] = 11	–	270	–	mV
$V_{LEVEL(M)}$	noise blanker sensitivity at LEVEL input (peak value of noise pulses)	see Table 65; $t_{pulse} = 10$ μ s; $f_{pulse} = 300$ Hz				
		NBL[1:0] = 00	–	9	–	mV
		NBL[1:0] = 01	–	18	–	mV
		NBL[1:0] = 10	–	28	–	mV

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM PART						
$t_{sup(min)}$	minimum suppression time		–	200	–	μ s
M_{AM}	noise blanker sensitivity	see Table 62; $f_{audio} = 2$ kHz NBS[1:0] = 00 NBS[1:0] = 01 NBS[1:0] = 10 NBS[1:0] = 11	– – – –	110 140 175 220	– – – –	% % % %
Weak signal processing						
DETECTORS						
$V_{eq(USN)}$	USN sensitivity equivalent level voltage	see Fig.5; $f_{MPXRDS} = 150$ kHz; $V_{MPXRDS} = 250$ mV (RMS); HCMP = 1; note 2 USS[1:0] = 00 USS[1:0] = 01 USS[1:0] = 10 USS[1:0] = 11	– – – –	2.5 2 1.5 0.5	– – – –	V V V V
$V_{eq(WAM)}$	WAM sensitivity equivalent level voltage	see Fig.6; $V_{LEVEL} = 200$ mV (p-p) at $f = 21$ kHz on the level voltage; HCMP = 1; note 2 WAS[1:0] = 00 WAS[1:0] = 01 WAS[1:0] = 10 WAS[1:0] = 11	– – – –	2.5 2 1.5 0.5	– – – –	V V V V
$t_{LEVEL(attack)}$	level detector attack time (soft mute and HCC)	see Table 49; LETF = 0; SEAR = 0 LET[1:0] = 00 LET[1:0] = 01 LET[1:0] = 10 LET[1:0] = 11 see Table 49; LETF = 1; SEAR = 0 LET[1:0] = 00 LET[1:0] = 01 LET[1:0] = 10 LET[1:0] = 11 search mode; SEAR = 1	– – – – – – – – –	3 3 1.5 0.5 0.5 0.17 0.06 0.06 60	– – – – – – – – –	s s s s s s s s ms

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
$t_{\text{LEVEL(decay)}}$	level detector decay time (soft mute and HCC)	see Table 49; LETF = 0; SEAR = 0					
		LET[1:0] = 00	–	3	–	s	
		LET[1:0] = 01	–	6	–	s	
		LET[1:0] = 10	–	1.5	–	s	
		LET[1:0] = 11	–	1.5	–	s	
		see Table 49; LETF = 1; SEAR = 0					
		LET[1:0] = 00	–	0.5	–	s	
		LET[1:0] = 01	–	0.5	–	s	
LET[1:0] = 10	–	0.17	–	s			
LET[1:0] = 11	–	0.06	–	s			
		search mode; SEAR = 1	–	60	–	ms	
$t_{\text{MPH(attack)}}$	multipath detector attack time (SNC)	see Table 50; SEAR = 0					
		MPT[1:0] = 00	–	0.5	–	s	
		MPT[1:0] = 01	–	0.5	–	s	
		MPT[1:0] = 10	–	0.5	–	s	
		MPT[1:0] = 11	–	0.25	–	s	
		search mode; SEAR = 1	–	60	–	ms	
$t_{\text{MPH(decay)}}$	multipath detector decay time (SNC)	see Table 50; SEAR = 0					
		MPT[1:0] = 00	–	12	–	s	
		MPT[1:0] = 01	–	24	–	s	
		MPT[1:0] = 10	–	6	–	s	
		MPT[1:0] = 11	–	6	–	s	
		search mode; SEAR = 1	–	60	–	ms	
$t_{\text{USN(attack)}}$	USN detector attack time (soft mute and SNC)		–	1	–	ms	
$t_{\text{USN(decay)}}$	USN detector decay time (soft mute and SNC)		–	1	–	ms	
ΔUSS	USN detector desensitization	USN sensitivity setting (USS) versus level voltage (USN sensitivity setting is automatically reduced as level voltage decreases)					
		$V_{\text{LEVEL}} > 1.25 \text{ V}$	–	–	3	–	
		$1.25 \text{ V} > V_{\text{LEVEL}} > 1.125 \text{ V}$	–	–	2	–	
		$1.125 \text{ V} > V_{\text{LEVEL}} > 1.0 \text{ V}$	–	–	1	–	
		$1.0 \text{ V} > V_{\text{LEVEL}}$	–	–	0	–	
$t_{\text{WAM(attack)}}$	WAM detector attack time (SNC)		–	1	–	ms	
$t_{\text{WAM(decay)}}$	WAM detector decay time (SNC)		–	1	–	ms	
$t_{\text{peak(USN)(attack)}}$	peak detector for USN attack time for read-out via I ² C-bus		–	1	–	ms	

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{\text{peak(USN)(decay)}}$	peak detector for USN decay time for read-out via I ² C-bus		–	10	–	ms
$t_{\text{peak(WAM)(attack)}}$	peak detector for WAM attack time for read-out via I ² C-bus		–	1	–	ms
$t_{\text{peak(WAM)(decay)}}$	peak detector for WAM decay time for read-out via I ² C-bus		–	10	–	ms
CONTROL FUNCTIONS						
$V_{\text{start(mute)}}$	soft mute start voltage	see Fig.12; voltage at pin LEVEL that causes $\alpha_{\text{mute}} = 3 \text{ dB}$; MSL[1:0] = 11 MST[2:0] = 000 MST[2:0] = 001 MST[2:0] = 010 MST[2:0] = 011 MST[2:0] = 100 MST[2:0] = 101 MST[2:0] = 110 MST[2:0] = 111	– – – – – – – –	0.75 0.88 1 1.12 1.25 1.5 1.75 2	– – – – – – – –	V V V V V V V V
C_{mute}	soft mute slope $C_{\text{mute}} = \frac{\Delta\alpha_{\text{mute}}}{\Delta V_{\text{eq}}}$	see Fig.13; slope of soft mute attenuation with respect to level voltage; MST[2:0] = 000 MSL[1:0] = 00 MSL[1:0] = 01 MSL[1:0] = 10 MSL[1:0] = 11	– – – –	8 16 24 32	– – – –	dB/V dB/V dB/V dB/V
$\alpha_{\text{mute(max)}}$	maximum soft mute attenuation by USN	see Fig.14; $f_{\text{MPXRDS}} = 150 \text{ kHz}$; $V_{\text{MPXRDS}} = 0.6 \text{ V (RMS)}$; USS[1:0] = 11 UMD[1:0] = 00 UMD[1:0] = 01 UMD[1:0] = 10 UMD[1:0] = 11	– – – –	3 6 9 12	– – – –	dB dB dB dB
$V_{\text{start(SNC)}}$	SNC stereo blend start voltage	see Fig.7; voltage at pin LEVEL that causes channel separation = 10 dB; SSL[1:0] = 10 SST[3:0] = 0000 : SST[3:0] = 1000 : SST[3:0] = 1111	– – – – –	1.5 : 2.0 : 2.45	– – – – –	V V V V V

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{SNC}	SNC slope $C_{SNC} = \frac{\Delta\alpha_{cs}}{\Delta V_{eq}}$	see Fig.8; slope of channel separation between 30 dB and 10 dB with respect to level voltage; SST[3:0] = 1010				
		SSL[1:0] = 00	–	38	–	dB/V
		SSL[1:0] = 01	–	51	–	dB/V
		SSL[1:0] = 10	–	63	–	dB/V
		SSL[1:0] = 11	–	72	–	dB/V
$V_{start(HCC)}$	HCC start voltage	see Fig.9; $f_{audio} = 10$ kHz; voltage at pin LEVEL that causes $\alpha_{HCC} = 3$ dB; HSL[1:0] = 10				
		HST[2:0] = 000	–	1.17	–	V
		HST[2:0] = 001	–	1.42	–	V
		HST[2:0] = 010	–	1.67	–	V
		HST[2:0] = 011	–	1.92	–	V
		HST[2:0] = 100	–	2.17	–	V
		HST[2:0] = 101	–	2.67	–	V
		HST[2:0] = 110	–	3.17	–	V
		HST[2:0] = 111	–	3.67	–	V
C_{HCC}	HCC slope $C_{HCC} = \frac{\Delta\alpha_{HCC}}{\Delta V_{eq}}$	see Fig.10; $f_{audio} = 10$ kHz; HST[2:0] = 010				
		HSL[1:0] = 00	–	9	–	dB/V
		HSL[1:0] = 01	–	11	–	dB/V
		HSL[1:0] = 10	–	14	–	dB/V
		HSL[1:0] = 11	–	18	–	dB/V
$\alpha_{HCC(max)}$	maximum HCC attenuation	see Fig.10; $f_{audio} = 10$ kHz				
		HCSF = 1	–	10	–	dB
		HCSF = 0	–	14	–	dB
$f_{cut-off}$	cut-off frequency of fixed HCC	see Table 56; –3 dB point (first order filter)				
		HCF[2:0] = 000	–	1.5	–	kHz
		HCF[2:0] = 001	–	2.2	–	kHz
		HCF[2:0] = 010	–	3.3	–	kHz
		HCF[2:0] = 011	–	4.7	–	kHz
		HCF[2:0] = 100	–	6.8	–	kHz
		HCF[2:0] = 101	–	10	–	kHz
		HCF[2:0] = 110	–	wide	–	–
		HCF[2:0] = 111	–	unlimited	–	–
Analog-to-digital converters for I²C-bus						
LEVEL ANALOG-TO-DIGITAL CONVERTER (8-BIT); see Fig.4						
$V_{LEVEL(min)}$	lower voltage limit of conversion range		–	0.25	–	V

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{LEVEL(max)}$	upper voltage limit of conversion range		–	4.25	–	V
ΔV_{LEVEL}	bit resolution voltage		–	15.7	–	mV
ULTRASONIC NOISE ANALOG-TO-DIGITAL CONVERTER (4-BIT); see Fig.5						
$V_{USN(min)(rms)}$	conversion range lower voltage limit (RMS value)	$f_{FMMPX} = 150 \text{ kHz}$	–	0	–	V
$V_{USN(max)(rms)}$	conversion range upper voltage limit (RMS value)	$f_{FMMPX} = 150 \text{ kHz}$	–	0.75	–	V
$\Delta V_{USN(rms)}$	bit resolution voltage (RMS value)		–	50	–	mV
WIDEBAND AM ANALOG-TO-DIGITAL CONVERTER (4-BIT); see Fig.6						
$V_{WAM(min)(p-p)}$	lower voltage limit of conversion range (peak-to-peak value)	$f_{LEVEL} = 21 \text{ kHz}$	–	0	–	mV
$V_{WAM(max)(p-p)}$	upper voltage limit of conversion range (peak-to-peak value)	$f_{LEVEL} = 21 \text{ kHz}$	–	800	–	mV
$\Delta V_{WAM(p-p)}$	bit resolution voltage (peak-to-peak value)		–	53.3	–	mV
Tone/volume control						
Z_i	input impedance at pins TAPEL, TAPER, CDL and CDR		80	–	–	$k\Omega$
	input impedance at pin PHONE		50	–	–	$k\Omega$
Z_o	output impedance at pins LFOUT, RFOUT, LROUT and RROUT		–	–	100	Ω
$G_{s(main)}$	signal gain from main source input to LFOUT, RFOUT, LROUT and RROUT outputs		–1	–	+1	dB
$G_{s(NAV)}$	signal gain from NAV input to LFOUT, RFOUT, LROUT and RROUT outputs		–1.5	0	+1.5	dB
$V_{i(max)(rms)}$	maximum input voltage level at pins TAPEL, TAPER, CDL, CDR and PHONE (RMS value)	THD = 0.1%; $G_{vol} = -6 \text{ dB}$	2	–	–	V
$V_{i(NAV)(max)(rms)}$	maximum input voltage level at pin NAV (RMS value)	THD = 1%	0.3	–	–	V

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(max)(rms)}$	maximum output voltage (RMS value)	THD = 0.1%; $G_{vol} = +6$ dB	2	–	–	V
		worst case load: $R_L = 2$ k Ω , $C_L = 10$ nF, THD = 1%	2	–	–	V
f_{max}	frequency response (pins TAPER, TAPEL, CDR and CDL)	upper –0.5 dB point; referenced to 1 kHz	20	–	–	kHz
CMRR	common mode rejection ratio	$f_{audio} = 20$ Hz to 20 kHz on CD and PHONE inputs				
		$G_{vol} = 0$ dB	40	–	–	dB
		$G_{vol} = -15$ dB	55	–	–	dB
α_{cs}	channel separation	$f_{audio} = 20$ Hz to 20 kHz	60	80	–	dB
α_S	input isolation of one selected source to any other input	$f_{audio} = 1$ kHz	90	105	–	dB
		$f_{audio} = 20$ Hz to 10 kHz	75	90	–	dB
		$f_{audio} = 20$ kHz	70	–	–	dB
THD	total harmonic distortion	TAPE and CD inputs				
		$f_{audio} = 20$ Hz to 10 kHz; $V_i = 1$ V (RMS)	–	0.01	0.1	%
		$f_{audio} = 1$ kHz; $V_i = 2$ V (RMS); $G_{vol} = 0$ dB	–	0.02	0.1	%
		$f_{audio} = 20$ Hz to 10 kHz; $V_i = 2$ V (RMS); $G_{vol} = -10$ dB	–	0.02	0.2	%
		$f_{audio} = 25$ Hz; $V_i = 500$ mV (RMS); $G_{bass} = +8$ dB; $G_{vol} = 0$ dB	–	0.05	0.2	%
		$f_{audio} = 4$ kHz; $V_i = 500$ mV (RMS); $G_{treble} = +8$ dB; $G_{vol} = 0$ dB	–	0.01	0.2	%
		NAV input; $f_{audio} = 1$ kHz; $V_o = 300$ mV (RMS)	–	–	1	%
$V_{noise(rms)}$	noise voltage (RMS value)	CCIR-ARM weighted and 20 kHz 'brick wall' without input signal and shorted AF inputs				
		$G_{vol} = 0$ dB	–	12	20	μ V
		$G_{bass} = +6$ dB; $G_{treble} = +6$ dB; $G_{vol} = 0$ dB	–	24	35	μ V
		$G_{vol} = 20$ dB; TAPE input (stereo)	–	71	100	μ V
		$G_{vol} = 20$ dB; CD input (quasi-differential)	–	100	140	μ V
		$G_{vol} = -10$ dB	–	10	18	μ V
		$G_{vol} = -40$ dB; $G_{loudness} = -20$ dB	–	9.5	13.5	μ V
		outputs muted	–	5	12	μ V
		using 'A-weighting' filter and 20 kHz 'brick wall'; $G_{vol} = -10$ dB; $G_{loudness} = -10$ dB	–	6.8	10	μ V
		NAV input	–	16	40	μ V

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT		
ΔG_{step}	step error (all controls) between all adjoining steps, all outputs	$G = +20$ to -36 dB	–	–	0.5	dB		
		$G = -36$ to -59 dB	–	–	1.0	dB		
T_{CASI}	ASI time constant (switching time from any setting to any other setting)	see Table 67	–	1	–	ms		
		AST[1:0] = 00	–	3	–	ms		
		AST[1:0] = 01	–	10	–	ms		
		AST[1:0] = 10	–	30	–	ms		
$V_{\text{offset(max)}}$	maximum DC offset	between any two settings (non-consecutive) on any one audio control or any one dynamic weak signal processing control	–	7	–	mV		
		PSRR	power supply ripple rejection	$V_{\text{CC(AC)}} = V_{\text{ripple}} = 200$ mV (RMS)	–	–	–	–
				$f_{\text{ripple}} = 20$ to 100 Hz	35	46	–	dB
				$f_{\text{ripple}} = 1$ kHz	50	75	–	dB
α_{ct}	crosstalk between bus inputs and signal outputs	$f_{\text{clk}} = 100$ kHz; note 3	–	110	–	dB		
		$f_{\text{ripple}} = 1$ to 20 kHz	50	65	–	dB		
$t_{\text{turn-on}}$	turn-on time from V_{CC} applied to 66% final DC voltage at outputs		–	100	–	ms		
LOUDNESS								
$f_{\text{loudness(low)}}$	loudness low boost frequency; without influence of coupling capacitors	amplitude decrease = -3 dB	–	–	–	–		
		LLF = 0	–	50	–	Hz		
$f_{\text{loudness(high)}}$	loudness filter response; without influence of coupling capacitors	LLF = 1	–	100	–	Hz		
		amplitude decrease = -1 dB; frequency referred to 100 kHz; high boost on	–	10	–	kHz		
G_{loudness}	loudness gain control	$f_{\text{loudness(low)}} = 50$ Hz; high boost on; see Fig.16	–	–	–	–		
		maximum setting; 1 kHz tone	–	0	–	dB		
		minimum setting; 1 kHz tone	–	-20	–	dB		
		minimum setting; 50 Hz tone	–	-3	–	dB		
		minimum setting; 10 kHz tone	–	-16	–	dB		
		minimum setting; 100 kHz tone	–	-15	–	dB		
VOLUME								
G_{vol}	volume/balance gain control	see Table 73	–	–	–	–		
		maximum setting	–	20	–	dB		
		minimum setting	–	-59	–	dB		
		mute attenuation; 20 Hz to 20 kHz input	–	-80	-70	dB		

Car radio integrated signal processor

TEF6892H

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{\text{step(vol)}}$	step resolution gain (volume)	see Table 73	–	1	–	dB
ΔG_{set}	gain set error	$G_{\text{vol}} = +20$ to -36 dB	–1	0	+1	dB
		$G_{\text{vol}} = -36$ to -59 dB	–3	0	+3	dB
ΔG_{track}	gain tracking error between left and right	$G_{\text{vol}} = +20$ to -36 dB	–	0	1	dB
		$G_{\text{vol}} = -36$ to -59 dB	–	0	3	dB
TREBLE						
$f_{\text{cut-off(treble)}}$	treble control filter cut-off frequency	see Table 77; -3 dB frequency referred to 100 kHz				
		TRF[1:0] = 00	–	8	–	kHz
		TRF[1:0] = 01	–	10	–	kHz
		TRF[1:0] = 10	–	12	–	kHz
G_{treble}	treble gain control	see Table 76				
		maximum setting	–	14	–	dB
$G_{\text{step(treble)}}$	step resolution gain (treble)	see Table 76	–	2	–	dB
		minimum setting	–	–14	–	dB
BASS						
$f_{\text{c(bass)}}$	bass control filter centre frequency	see Table 81				
		BAF[1:0] = 00	–	60	–	Hz
		BAF[1:0] = 01	–	80	–	Hz
		BAF[1:0] = 10	–	100	–	Hz
Q_{bass}	bass filter quality factor	$G_{\text{bass}} = +12$ dB	–	1.0	–	–
		BAF[1:0] = 11	–	120	–	Hz
EQ_{bow}	equalizer bowing	$f_{\text{audio}} = 1$ kHz; $V_i = 500$ mV (RMS); $G_{\text{bass}} = +12$ dB; $f_{\text{c(bass)}} = 60$ Hz; $G_{\text{treble}} = +12$ dB; $f_{\text{cut-off(treble)}} = 10$ kHz; see Fig.3	–	1.8	–	dB
G_{bass}	bass gain control	see Table 80				
		maximum setting; symmetrical boost	–	14	–	dB
		minimum setting; asymmetrical cut	–	–14	–	dB
$G_{\text{step(bass)}}$	step resolution gain (bass)	see Table 80	–	2	–	dB
		minimum setting; symmetrical cut	–	–14	–	dB
FADER						
G_{fader}	fader gain control	see Table 84				
		maximum setting	–	0	–	dB
		minimum setting	–	–59	–	dB
		mute attenuation; 20 Hz to 20 kHz input	–	–80	–66	dB

Car radio integrated signal processor

TEF6892H

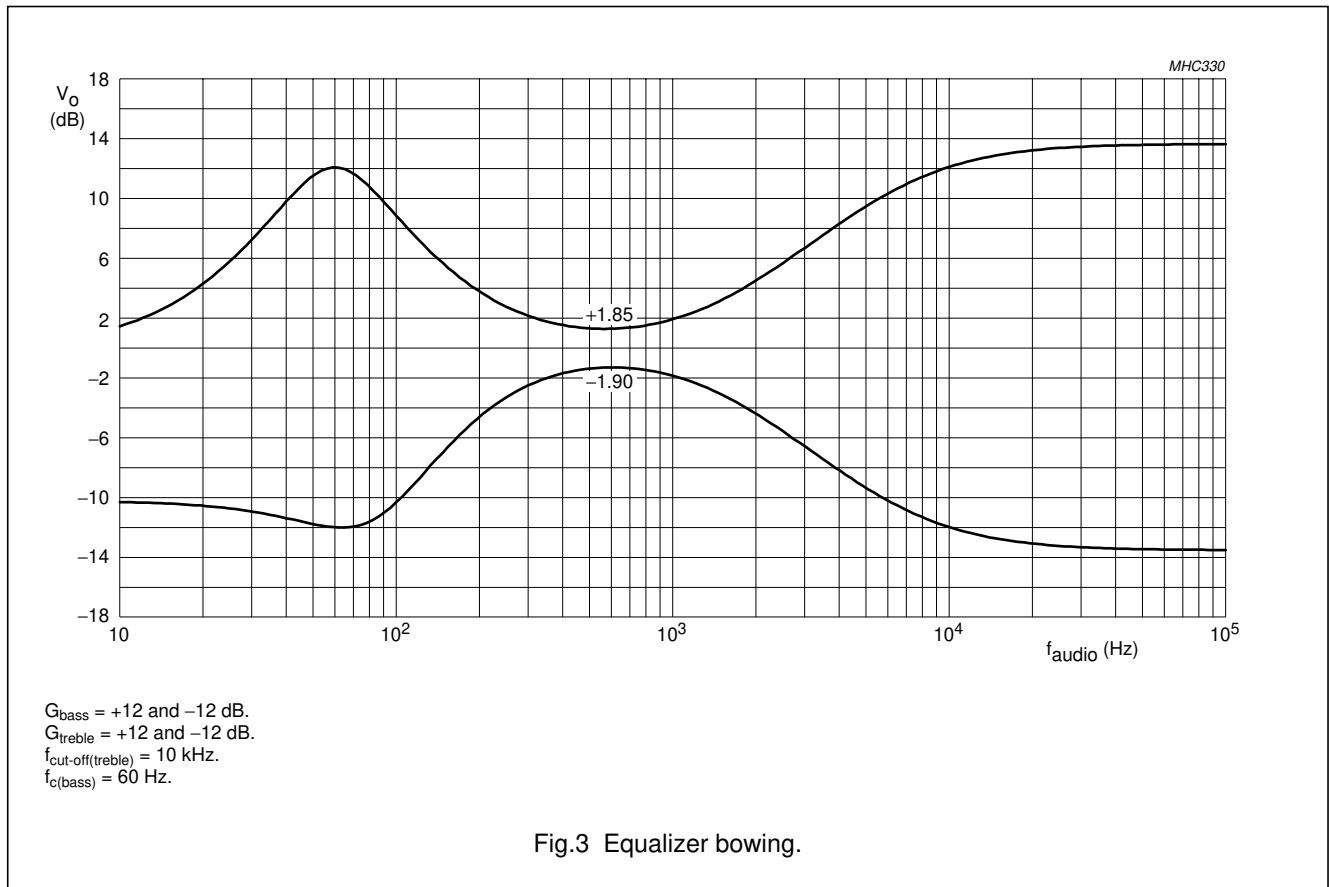
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{\text{step(fader)}}$	step resolution gain (fader)	see Table 84				
		$G_{\text{fader}} = 0$ to -15 dB	–	1	–	dB
		$G_{\text{fader}} = -15$ to -45 dB	–	2.5	–	dB
		$G_{\text{fader}} = -45$ to -51 dB	–	3	–	dB
		$G_{\text{fader}} = -51$ to -59 dB	–	4	–	dB
α_{mute}	audio mute	volume control: mute and output muted (bits MULF, MURF, MULR and MURR)	90	–	–	dB
BEEP						
f_{beep}	beep generator frequency	see Table 93				
		BEF[1:0] = 00	–	500	–	Hz
		BEF[1:0] = 01	–	1	–	kHz
		BEF[1:0] = 10	–	2	–	kHz
		BEF[1:0] = 11	–	3	–	kHz
$V_{\text{beep(rms)}}$	beep generator audio level (RMS value)	see Table 92				
		BEL[2:0] = 000	–	0	–	mV
		BEL[2:0] = 001	–	13.3	–	mV
		BEL[2:0] = 010	–	18	–	mV
		BEL[2:0] = 011	–	28	–	mV
		BEL[2:0] = 100	–	44	–	mV
		BEL[2:0] = 101	–	60	–	mV
BEL[2:0] = 110	–	90	–	mV		
		BEL[2:0] = 111	–	150	–	mV
THD_{beep}	total harmonic distortion of beep generator	$f_{\text{beep}} = 1$ kHz or 2 kHz	–	–	7	%
Power-on reset (all registers in default setting, outputs muted, standby mode)						
$V_{\text{th(POR)}}$	threshold voltage of Power-on reset		–	6.3	–	V

Notes

- The LOW voltage of pin SCLG is influenced by V_{SCL} : $V_{\text{SCLG(LOW)}} \geq V_{\text{SCL(LOW)}} + 0.22$ V.
- The equivalent level voltage is that value of the level voltage (at pin LEVEL) which results in the same weak signal control effect (for instance HCC roll-off) as the output value of the specified detector (USN, WAM and MPH).
- Crosstalk between bus inputs and signal outputs: $\alpha_{\text{ct}} = 20 \log \frac{V_{\text{bus(p-p)}}}{V_{\text{o(rms)}}$

Car radio integrated signal processor

TEF6892H



Car radio integrated signal processor

TEF6892H

11 I²C-BUS PROTOCOL

Table 1 Write mode

S ⁽¹⁾	address (write)	A ⁽²⁾	subaddress	A ⁽²⁾	data byte(s)	A ⁽²⁾	P ⁽³⁾
------------------	-----------------	------------------	------------	------------------	--------------	------------------	------------------

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

S ⁽¹⁾	address (read)	A ⁽²⁾	data byte(s)	A ⁽²⁾	data byte	NA ⁽³⁾	P ⁽⁴⁾
------------------	----------------	------------------	--------------	------------------	-----------	-------------------	------------------

Notes

1. S = START condition.
2. A = acknowledge.
3. NA = not acknowledge.
4. P = STOP condition.

Table 3 IC address byte

IC ADDRESS						MODE
0	0	1	1	0	0	ADDR
						R/ \bar{W}

Table 4 Description of IC address byte

BIT	SYMBOL	DESCRIPTION
7 to 2	–	001100+(ADDR) = IC address.
1	ADDR	Address bit. 0 = pin ADDR is grounded; 1 = pin ADDR is floating.
0	R/ \bar{W}	Read/Write. 0 = write mode; 1 = read mode.

11.1 Read mode

11.1.1 DATA BYTE 1; STATUS

Table 5 Format of data byte 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STIN	ASIA	AFUS	POR	RDAV	ID2	ID1	ID0

Car radio integrated signal processor

TEF6892H

Table 6 Description of data byte 1

BIT	SYMBOL	DESCRIPTION
7	STIN	Stereo indicator. 0 = no pilot signal detected; 1 = pilot signal detected.
6	ASIA	ASI active. 0 = not active; 1 = ASI step is in progress.
5	AFUS	AF update sample. 0 = LEV, USN and WAM information is taken from main frequency (continuous mode); 1 = LEV, USN and WAM information is taken from alternative frequency. Continuous mode during AF update and sampled mode after AF update. Sampled mode reverts to continuous main frequency information after read.
4	POR	Power-on reset. 0 = standard operation (valid I ² C-bus register settings); 1 = Power-on reset detected since last read cycle (I ² C-bus register reset). After read the bit will reset to POR = 0.
3	RDAV	RDS data available. This bit indicates, that RDS block data is available.
2 to 0	ID[2:0]	Identification. TEF6892H device type identification; ID[2:0] = 010.

11.1.2 DATA BYTE 2; LEVEL

Table 7 Format of data byte 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 8 Description of data byte 2

BIT	SYMBOL	DESCRIPTION
7 to 0	LEV[7:0]	Level. 8-bit value of level voltage from tuner; see Fig.4.

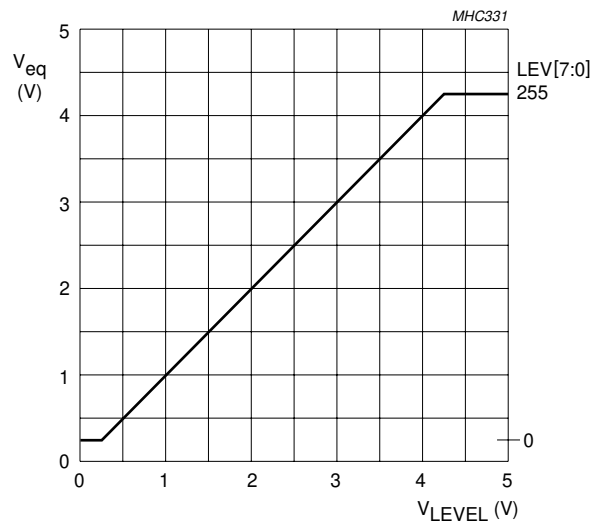


Fig.4 Equivalent level voltage V_{eq} (MPH and LEV detector) as a function of level voltage V_{LEVEL} .