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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TEF6901A

Integrated car radio

Rev. 03 — 20 March 2008 Product data sheet

1. General description

The TEF6901A is a single-chip car radio integrated circuit with FM/AM tuner, stereo decoder, weak signal processing and audio processing. Radio Data System (RDS)/Radio Broadcast Data System (RBDS) demodulator for radio data reception is included.

FM tuner with double conversion to IF1 = 10.7 MHz and IF2 = 450 kHz with integrated image rejection for both IF1 and IF2; integrated channel filter with variable bandwidth control; capable of US FM, Europe FM, Japan FM and Eastern Europe FM. AM tuner with double conversion to IF1 = 10.7 MHz and IF2 = 450 kHz; capable of Long Wave (LW), Medium Wave (MW) and full range Short Wave (SW) (11 m to 120 m bands).

Multiplex (MPX) stereo decoder, ignition noise blanker and extensive weak signal processing.

Audio processing with flexible source selection, volume, balance, fader, input gain control and inaudible tuning mute. Integrated audio filters for bass and treble and loudness control function.

The device can be controlled via the fast-mode I^2C-bus (400 kHz) and includes autonomous tuning functions for easy control without microcontroller timing. No manual alignments are required.

2. Features

- FM Radio Frequency (RF) front-end with large dynamic range
- Integrated FM channel filter with controlled bandwidth
- Fully integrated FM demodulator
- Fully integrated stereo decoder with high immunity for birdy noise
- FM noise blanker with adaptive detection at MPX and level
- Signal quality detection: level, AM wideband, frequency deviation, ultrasonic noise/adjacent channel
- FM weak signal processing: stereo blend, high cut control and soft mute
- AM RF Automatic Gain Control (AGC) circuit for external cascode AGC and Positive Intrinsic Negative (PIN) diode AGC
- Dual AM noise blanking system
- AM weak signal processing: high cut control and soft mute
- Low phase noise local oscillator
- In-lock detection for optimized adaptive Phase-Locked Loop (PLL) tuning speed
- Crystal oscillator reference with low harmonics
- Inaudible soft slope tuning mute for AM and FM
- Sequential state machine supporting each tuning action

- Integrated RDS/RBDS radio data demodulator
- Flexible audio input source selection
- Integrated audio processing and tone filtering
- Treble, bass and loudness tone control
- Volume, balance, fader and input gain control
- Audio controls with Audio Step Interpolation (ASI) for pop-free function
- Compact Disc (CD) dynamics compression
- Volume Unit (VU)-meter audio level read-out

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{CC}	analog supply voltage on pins VCC, VCCPLL, VCCVCO, VCCRF, AMMIX2OUT1, AMMIX2OUT2, MIX1OUT1 and MIX1OUT2		8	8.5	9	V
Supply current in FM mode						
I_{CC}	total supply current inclusive I_{V60}		-	102	-	mA
Supply current in AM mode						
I_{CC}	total supply current inclusive I_{V60}		-	89	-	mA
AM overall system parameters						
f_{tune}	AM tuning frequency	LW	144	-	288	kHz
		MW	522	-	1710	kHz
		SW	2.3	-	26.1	MHz
V_{sens}	sensitivity voltage	f_{RF} = 990 kHz; m = 0.3; f_{mod} = 1 kHz; B_{AF} = 2.15 kHz; (S+N)/N = 26 dB; dummy aerial 15 pF/60 pF	-	50	-	µV
S/N	ultimate signal-to-noise ratio		54	58	-	dB
THD	total harmonic distortion	200 µV < V_{RF} < 1 V; m = 0.8; f_{AF} = 400 Hz	-	0.4	1	%
IP3	3rd-order intercept point	Δf = 40 kHz	-	130	-	dBµV
FM overall system parameters						
f_{tune}	FM tuning frequency		65	-	108	MHz
V_{sens}	sensitivity voltage (RF input voltage at (S+N)/N = 26 dB)	Δf = 22.5 kHz; f_{mod} = 1 kHz; DEMP = 1; B = 300 Hz to 22 kHz; measured with 75 Ω dummy antenna and test circuit	-	2	-	µV
(S+N)/N	maximum signal plus noise-to-noise ratio of MPXAM output voltage	V_i = 3 mV; Δf = 22.5 kHz; f_{mod} = 1 kHz; DEMP = 1; B = 300 Hz to 22 kHz; measured with 75 Ω dummy antenna and test circuit	-	60	-	dB
THD	total harmonic distortion	Δf = 75 kHz	-	0.5	1	%
IP3	3rd-order intercept point	Δf = 400 kHz	-	120	-	dBµV

Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Stereo decoder path							
α_{cs}	channel separation	f_{FMMPX} = 1 kHz		40	-	-	dB
S/N	signal-to-noise ratio	$f_{MPXAMIN}$ = 20 Hz to 15 kHz; referenced to 1 kHz at 91 % FM modulation; DEMP = 1		70	-	-	dB
THD	total harmonic distortion	FM mode; DEMP = 1; measured with 15 kHz brick-wall low-pass filter; $f_{MPXAMIN}$ = 200 Hz to 15 kHz		-	-	0.3	%
Tone/volume control							
$V_{i(max)}$	maximum input voltage	THD = 0.2 %; G_{vol} = −6 dB; pins INAL, INAR, INAC, INBL, INBR, INC and IND		2	-	-	V
THD	total harmonic distortion	configured as non-inverting, single-ended inputs; f_{audio} = 20 Hz to 10 kHz; V_i = 1 V (RMS)		-	0.02	0.1	%
G_{vol}	volume/balance gain control	see Table 83					
		maximum setting	[1]	-	20	-	dB
		minimum setting	[1]	-	−75	-	dB
$G_{step(vol)}$	step resolution			-	1	-	dB
G_{treble}	treble gain control	TRE[2:0] = 111; TREM = 1		-	14	-	dB
		TRE[2:0] = 111; TREM = 0		-	−14	-	dB
$G_{step(treble)}$	step resolution gain			-	2	-	dB
G_{bass}	bass gain control	BAS[3:0] = 0111; BASM = 1		-	14	-	dB
		BAS[3:0] = 0111; BASM = 0		-	−14	-	dB
$G_{step(bass)}$	step resolution gain			-	2	-	dB

[1] The input gain setting ING and the volume setting VOL define the overall volume. The overall range is limited to −83 dB to +28 dB. For values > +28 dB the actual value is +28 dB. For overall values < −83 dB the actual value is mute.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TEF6901AH	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

5. Block diagram

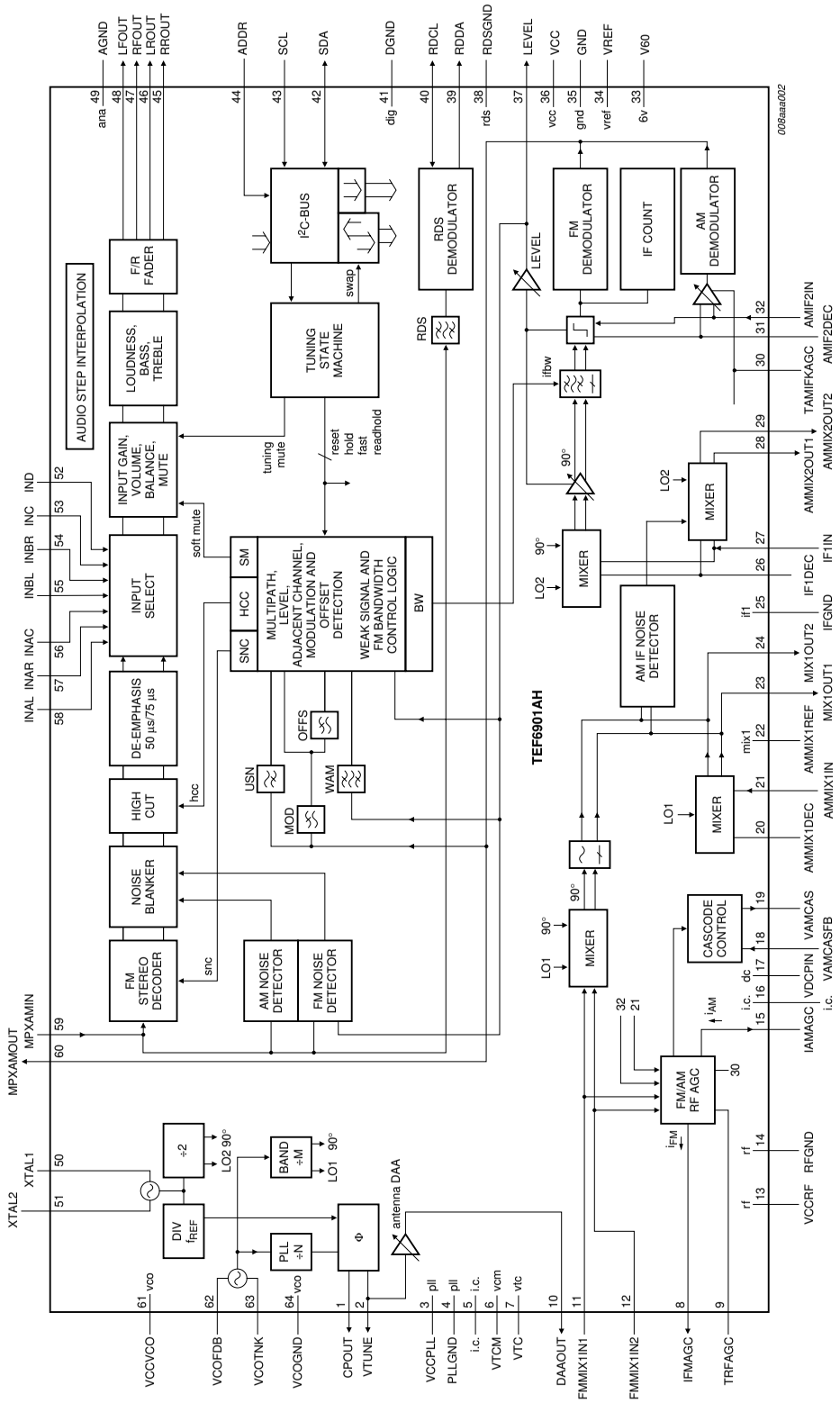

Fig 1. Block diagram of TEF6901AH

6. Pinning information

6.1 Pinning

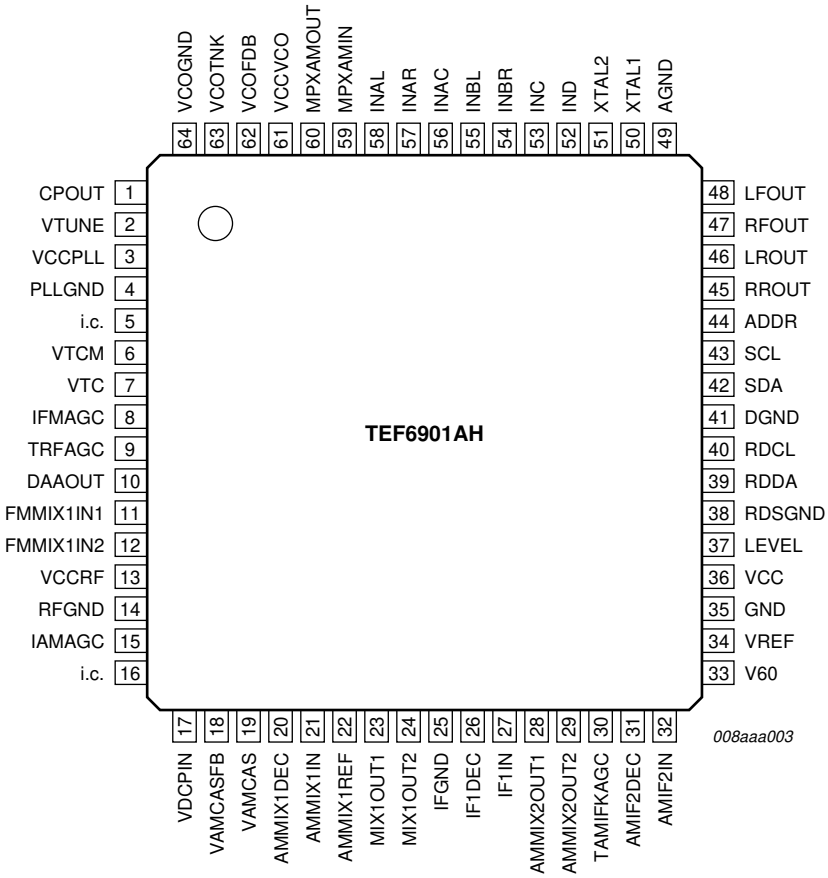

Fig 2. Pin configuration for QFP64

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CPOUT	1	charge pump output
VTUNE	2	tuning voltage; 3 mA charge pump output
VCCPLL	3	tuning PLL supply voltage
PLLGND	4	PLL ground
i.c.	5	internally connected; leave open
VTCM	6	Intermediate Frequency (IF) filter reference voltage
VTC	7	IF filter center voltage
IFMAGC	8	PIN diode current FM AGC
TRFAGC	9	FM and AM RF AGC time constant
DAAOUT	10	antenna Digital Auto Alignment (DAA) output

Table 3. Pin description *...continued*

Symbol	Pin	Description
FMMIX1IN1	11	FM mixer 1 input 1
FMMIX1IN2	12	FM mixer 1 input 2
VCCRF	13	AM/FM RF supply voltage
RFGND	14	RF ground
IAMAGC	15	PIN diode current AM AGC
i.c.	16	internally connected; leave open
VDCPIN	17	AM PIN diode DC bias voltage
VAMCASFB	18	feedback for cascode AM AGC
VAMCAS	19	cascode AM AGC
AMMIX1DEC	20	AM mixer 1 decoupling
AMMIX1IN	21	AM mixer 1 input
AMMIX1REF	22	AM mixer 1 reference
MIX1OUT1	23	AM and FM mixer 1 output 1 at IF1
MIX1OUT2	24	AM and FM mixer 1 output 2 at IF1
IFGND	25	IF ground
IF1DEC	26	AM and FM mixer 2 decoupling
IF1IN	27	AM and FM mixer 2 input
AMMIX2OUT1	28	AM mixer 2 output 1 at IF2
AMMIX2OUT2	29	AM mixer 2 output 2 at IF2
TAMIFKAGC	30	AM IF AGC and FM keyed AGC time constant
AMIF2DEC	31	AM IF2 input decoupling
AMIF2IN	32	AM IF2 input
V60	33	input for FM filter and demodulator supply current
VREF	34	reference voltage for noise decoupling
GND	35	ground
VCC	36	8.5 V supply voltage
LEVEL	37	AM and FM level voltage output
RDSGND	38	RDS ground
RDDA	39	RDS/RBDS demodulator data and quality output
RDCL	40	RDS/RBDS demodulator clock input or output
DGND	41	digital ground
SDA	42	I^2C-bus Serial Data (SDA) input and output
SCL	43	I^2C-bus Serial Clock (SCL) input
ADDR	44	I^2C-bus slave address select input
RROUT	45	right rear audio output
LROUT	46	left rear audio output
RFOUT	47	right front audio output
LFOUT	48	left front audio output
AGND	49	analog ground
XTAL1	50	crystal oscillator 1
XTAL2	51	crystal oscillator 2

Table 3. Pin description *...continued*

Symbol	Pin	Description
IND	52	audio input D, signal input
INC	53	audio input C, common mode or signal input
INBR	54	audio input B, right channel
INBL	55	audio input B, left channel
INAC	56	audio input A, left channel inverted (or other options)
INAR	57	audio input A, right channel
INAL	58	audio input A, left channel
MPXAMIN	59	MPX and AM audio input to radio processing
MPXAMOUT	60	MPX and AM audio output from tuner part
VCCVCO	61	Voltage-Controlled Oscillator (VCO) supply voltage
VCOFDB	62	VCO feedback
VCOTNK	63	VCO tank circuit
VCOGND	64	VCO ground

7. Functional description

7.1 FM mixer 1

The FM quadrature mixer 1 converts FM RF (65 MHz to 108 MHz) to an IF frequency of 10.7 MHz. The FM mixer provides image rejection and a large dynamic range. Low and high injection Local Oscillator (LO) can be selected via the I^2C-bus.

7.2 FM RF AGC

AGC detection at the FM front-end mixer input with programmable threshold. When the threshold is exceeded, the PIN diode drive circuit sources a current to an external PIN diode circuit, keeping the RF signal level constant. Keyed AGC function is selectable via the I^2C-bus and uses the in-band level information derived from the limiter. The AGC PIN diode drive circuit can optionally deliver a fixed current; this local mode can be used for search tuning on absolute RF levels. In AM mode, the FM AGC PIN diode drive circuit can be set to source a fixed current into the external FM PIN diode circuitry.

7.3 FM mixer 2

The FM quadrature mixer 2 converts 10.7 MHz IF1 to 450 kHz IF2 and includes image rejection with the integrated channel filter. Two gain settings can be selected to compensate for high ceramic filter insertion loss.

7.4 FM IF2 channel filter

The order and dynamic range of the FM IF2 channel filter is designed for operation with only one external ceramic filter. The filter characteristic is optimized to combine high selectivity with low distortion. The bandwidth of the filter can be set to a range of fixed settings or automatically via the bandwidth control algorithm. When the automatic mode is selected the bandwidth depends on the signal conditions.

7.5 FM limiter and level detection

The limiter amplifies the IF filter output signal, removes AM modulations from the IF signal and supplies a well defined signal for the FM demodulator. From the limiter also the Radio Signal Strength Information (RSSI) is derived which is converted to a suitable level voltage with minimum temperature drift.

7.6 FM demodulator

The fully integrated FM demodulator converts the IF signal from the limiter to the FM multiplex output signal with low distortion.

7.7 Center frequency and bandwidth tuning and center frequency DAA

The center frequency as well as the bandwidth of both the IF filter and demodulator are coupled to the crystal reference frequency. A coarse alignment (IFCAP) sets the circuit operating range and the center frequency fine adjustment is achieved with a 6-bit alignment (IFCF).

7.8 Bandwidth control algorithm

The bandwidth of the IF filter can be selected with 5 bits, directly via I^2C-bus or automatically via the bandwidth control algorithm. The bandwidth control algorithm detects the amount of adjacent channel interference, the deviation of the desired signal, detuning, multipath and signal strength to define the optimum bandwidth setting of the IF filter. Flexibility on the algorithm settings is provided via the I^2C-bus control.

7.9 VCO and dividers

The varactor tuned LC oscillator together with the dividers provides the local oscillator signal for both AM and FM front-end mixers. The VCO has an operating frequency of approximately 160 MHz to 250 MHz. In FM mode the VCO frequency is divided by 2 or 3. These dividers generate in-phase and quadrature-phase output signals used in the FM front-end mixer for image rejection. In AM mode the VCO frequency is divided by 6, 8, 10, 16 or 20 depending on the selected AM band. The amplitude of the VCO is controlled by a digital AGC to ensure a safe oscillation start-up at a wide range of the loaded Q.

7.10 Crystal oscillator

The crystal oscillator provides a 20.5 MHz signal. A divider-by-two generates in-phase and quadrature-phase mixer frequencies for the conversion from IF1 to IF2 including image rejection. The reference divider generates from the crystal frequency various reference frequencies for the tuning PLL. Also timing signals for the sequential machine as well as references for the integrated FM channel filter, the stereo decoder and the integrated audio filters and the RDS demodulator are derived from the crystal reference.

7.11 Tuning PLL

The tuning PLL locks the VCO frequency divided by the programmable divider ratio to the reference frequency. Due to the combination of different charge pump signals in the PLL loop filter, the loop parameters are adapted dynamically. Tuning to different RF frequencies is done by changing the programmable divider ratio. The tuning step size is selected with the reference frequency divider setting.

7.12 Antenna DAA

For FM operation the antenna Digital Auto Alignment (DAA) measures the VCO tuning voltage and multiplies it with a factor defined by the 7-bit DAA setting to generate a tuning voltage for the FM antenna tank circuit (RF selectivity). In AM mode the DAA setting controls a fixed voltage.

7.13 AM RF AGC control

The AM front-end is designed for the application of an external Junction Field Effect Transistor (JFET) low noise amplifier with cascode AGC and PIN diode AGC both controlled by an integrated AGC control circuit. Four AGC thresholds of the detector at the first mixer input are selectable via I^2C-bus. Detectors at the RF mixer input and at the AMIF2 input prevent undesired overload (see Figure 40). AGC information can be read out via I^2C-bus. The PIN diode current drive circuit includes a pull-up current source for reverse biasing of the PIN diode, when the AGC is not active to achieve a low parasitic capacitance.

7.14 AM mixer 1

The large dynamic range AM mixer converts AM RF (144 kHz to 26.1 MHz) to an IF frequency of 10.7 MHz.

7.15 AM IF noise blanker

The spike detection for the AM IF noise blanker is at the output of the AM front-end mixer. Blanking is realized at the second AM mixer.

7.16 AM IF AGC amplifier and demodulator

The 450 kHz IF2 signal after the ceramic channel selection filter is amplified by the IF AGC amplifier and demodulated.

7.17 AM level detection

The IF2 signal used for AM IF AGC and demodulation is also used in the limiter circuit for in-band level detection.

7.18 AM and FM level DAA

The start and slope of the level detector output are programmable to achieve level information independent of gain spread in the signal channel.

7.19 AM and FM IF counter

The output signal from the limiter is used for IF counting in both AM and FM.

7.20 Tuning mute

A soft slope tuning mute is controlled by the sequential machine for different tuning actions to eliminate audible effects of tuning and band switching.

7.21 FM stereo decoder

A low-pass filter provides additional suppression of high frequency interferences at the stereo decoder input and the necessary signal delay for FM noise blanking.

The MPX signal is decoded in the stereo decoder part. An integrated oscillator and pilot PLL is used for the regeneration of the 38 kHz subcarrier. The required 19 kHz and 38 kHz signals are generated by division of the oscillator output signal in logic circuitry.

By means of a 19 kHz quadrature detector the pilot PLL oscillator frequency is locked to the incoming 19 kHz stereo pilot. A pilot level voltage derived from a 19 kHz in-phase detector is used for stereo detection and for generation of an anti-phase 19 kHz signal to remove the pilot tone from the audio signal.

The signal is then decoded in the decoder part. The L-R side signal is demodulated using the 38 kHz subcarrier and combined with the main signal to the left and right audio channel. A fine adjustment is done by adjusting the gain of the L-R signal. A smooth mono to stereo takeover is achieved by controlling the efficiency of the matrix by the Stereo Noise Control (SNC) signal from the weak signal processing block.

7.22 FM and AM AF noise blanker

The FM or AM tuner operation selects between two noise blanker operations optimized for FM or AM ignition noise suppression.

In FM mode the noise blanker operates as a modified sample and hold circuit with ultrasonic noise detection on MPX and detection of noise spikes on level.

In AM mode the audio signal is muted during the interference pulse triggered by slew-rate detection of the audio signal.

7.23 Fixed high cut and high cut control

The high cut part is a low-pass filter circuit with seven bandwidth settings. The cut-off frequencies of the filter curves can be selected to match different application requirements (fixed high cut).

The high cut circuit also provides a dynamic control of the filter response, the High Cut Control (HCC). This function is controlled by the HCC signal from the weak signal processing.

7.24 De-emphasis

The signal passes the low-pass filter de-emphasis block and is then fed to the source selector. The de-emphasis time constant can be selected between the standards of 50 µs and 75 µs.

7.25 Weak signal processing

The weak signal processing block detects quality degradations in the incoming signal and controls the processing of the audio signal accordingly. The weak signal processing block has three different quality criteria: The average value of the level voltage, AM components on the level voltage (WAM = wideband AM) and high frequency components in the MPX signal (USN = ultrasonic noise).

In the weak signal processing block these signals are combined in specific ways and used for the generation of control signals for soft mute, stereo blend (SNC = stereo noise control) and HCC. Detector time constants of soft mute, HCC and SNC can be selected independently.

In AM mode, soft mute and HCC are controlled by the average value of the level voltage.

7.26 Audio step interpolation

The tone/volume blocks of source selector, volume/balance, bass/loudness, fader and output mute include the Audio Step Interpolation (ASI) function. This minimizes audible pops by smoothing the transitions in the audio signal during the switching of the controls.

7.27 Source selector

The source selector selects one out of several input sources:

- One internal stereo signal (AM/FM tuner)
- Seven input pins allow many combinations of external sources by means of flexible input selection

  Three of the seven input pins can connect to:

  – 1 stereo signal with ground input for common mode rejection (CD)

  – 1 stereo signal and 1 mono signal

  Four more input pins can connect to:

  – 1 stereo signal (AUX) and 1 mono signal with common mode rejection or differential input (PHONE)

  – 1 stereo signal (AUX) and 2 mono signals (e.g. NAV and BEEP)

  – 2 stereo signals (AUX and AUX-2)

  – 1 stereo signal with common mode rejection (CD-2) and 1 mono signal (e.g. BEEP)

  – 1 stereo signal with differential input (CD-symmetrical)

7.28 VU-meter read

The input audio level of external sources can read out via the I^2C-bus. Audio level information is available on a logarithmic scale. In radio mode the AM or FM modulation index is available in the same way.

7.29 Volume and balance

The volume/balance control is used for volume setting and also for balance adjustment. The control range of the volume/balance control is between +20 dB and −75 dB in steps of 1 dB.

7.30 CD compression

Dynamic volume compression is available for external input sources. This option is generally used for audio from CD or other digital formats to reduce the very high dynamic range of these signals into a range suitable for the car environment.

7.31 Bass

The bass tone control stage controls the low audio frequencies with a modified shelve curve response. The control range is between +14 dB and −14 dB in steps of 2 dB. Four different filter cut-off frequencies can be selected.

7.32 Treble

The treble tone control stage controls the high audio frequencies with a shelve curve response. The control range is between +14 dB and −14 dB in steps of 2 dB. Four different filter cut-off frequencies can be selected.

7.33 Loudness

An integrated loudness function can be activated which controls bass and treble in relation to the user volume setting. The control range of the bass frequencies is limited to 20 dB and the optional treble range to 4 dB. Different volume ranges can be selected for the loudness control.

7.34 Fader

The fader is located at the end of the tone/volume chain. The balance between the front and rear channel can be controlled by attenuation of either the front or the rear channel. Control range is 0 dB to −64 dB with a step size of 1 dB. Optionally the fader attenuation can be activated for front and rear channels together.

7.35 RDS/RBDS demodulator

The RDS demodulator recovers and regenerates the continuously transmitted RDS or RBDS data stream that may be part of the FM MPX signal and provides the signals clock (RDCL) and data (RDDA) for further processing by a hardware or software RDS decoder. Unbuffered demodulator output and buffered 16-bit output mode are available. The output modes are compatible with stand-alone demodulator devices as well as digital and analog signal processor standards. In case of buffered output mode additional RDS Quality (RDQ) demodulation quality information is available optional.

8. I²C-bus protocol

SDA and SCL HIGH and LOW internal thresholds are specified according to both 2.5 V and 3.3 V I²C-bus, however also SDA and SCL signals from a 5 V bus are supported. The maximum I²C-bus communication speed is 400 kbit/s in accordance with the I²C-bus fast mode specification.

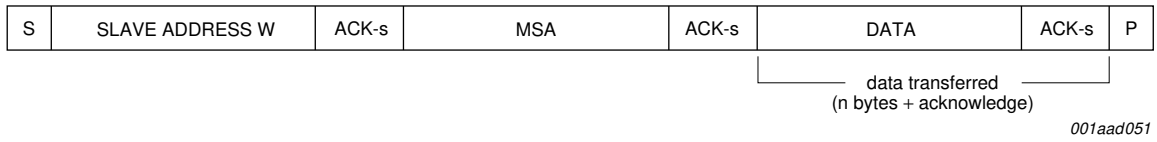

Fig 3. Write mode

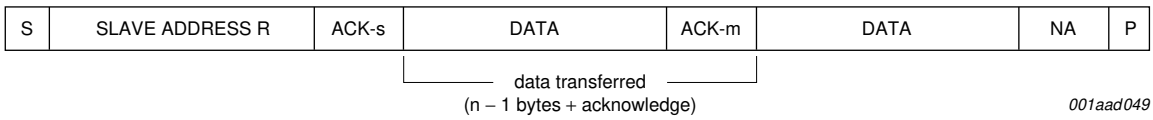

Fig 4. Read mode

Table 4. Description of I²C-bus format

Code	Description
S	START condition
Slave address W	1100 0000b for pin ADDR grounded
	1100 0010b for pin ADDR floating
Slave address R	1100 0001b for pin ADDR grounded
	1100 0011b for pin ADDR floating
ACK-s	acknowledge generated by the slave
ACK-m	acknowledge generated by the master
NA	not acknowledge generated by the master
MSA	mode and subaddress byte
Data	data byte
P	STOP condition

8.1 Read mode

Application restriction to use the read mode: Read transmissions should not be stopped after read byte 4 (IFBW) since this will disturb level read-out, weak signal processing and bandwidth control. Read transmission can be stopped after any of the other read bytes 0 to 3, 5 or 6.

The read data is loaded into the I²C-bus output register at the ACK clock pulse preceding the data byte.

Table 5. Read register overview

Data byte	Name	Reference
0	IFCOUNTER	Section 8.1.1
1	LEVEL	Section 8.1.2
2	USN/WAM	Section 8.1.3
3	MOD	Section 8.1.4
4	IFBW	Section 8.1.5
5	ID	Section 8.1.6
6	TEMP	Section 8.1.7

8.1.1 Read mode: data byte IFCOUNTER

Table 6. IFCOUNTER - format of data byte 0

7	6	5	4	3	2	1	0
IFCM1	IFCM0	IFCS	IFCA	IFC3	IFC2	IFC1	IFC0

Table 7. IFCOUNTER - data byte 0 bit description

Bit	Symbol	Description
7 and 6	IFCM[1:0]	IF counter mode; IFCM reads 00 immediately after I²C-bus start of PRESET, SEARCH, AFU, JUMP or CHECK until the first IFC result of the new tuning is available.
		00 = no new counter result available (IFC value is previous result or reset state)
		01 = new counter result available (IFC value is new result)
		10 = counter result from AF update (IFC value is AF result, value is held until I²C-bus read). Also the detector information of LEV, USN, WAM and MOD shows AF update results.
		11 = Power-On Reset (POR) or undefined state of the state machine is detected. The I²C-bus data is reset to POR state.
5	IFCS	IF counter sign
		0 = the IF counter result indicates a positive **RF** frequency error
		1 = the IF counter result indicates a negative **RF** frequency error
4	IFCA	IF counter accuracy
		0 = IF counter result with 1 kHz resolution in FM mode and 0.5 kHz resolution in AM mode
		1 = IF counter result with 8 kHz resolution in FM mode and 4 kHz resolution in AM mode
3 to 0	IFC[3:0]	IF counter result; see Table 8

Table 8. IF counter result

IFC3	IFC2	IFC1	IFC0	Deviation from nominal value in FM		Deviation from nominal value in AM	
				IFCA = 0	IFCA = 1	IFCA = 0	IFCA = 1
0	0	0	0	0 kHz to 1 kHz	reset state	0 kHz to 0.5 kHz	reset state
0	0	0	1	1 kHz to 2 kHz	-	0.5 kHz to 1 kHz	-
0	0	1	0	2 kHz to 3 kHz	16 kHz to 24 kHz	1 kHz to 1.5 kHz	8 kHz to 12 kHz
0	0	1	1	3 kHz to 4 kHz	24 kHz to 32 kHz	1.5 kHz to 2 kHz	12 kHz to 16 kHz
0	1	0	0	4 kHz to 5 kHz	32 kHz to 40 kHz	2 kHz to 2.5 kHz	16 kHz to 20 kHz
0	1	0	1	5 kHz to 6 kHz	40 kHz to 48 kHz	2.5 kHz to 3 kHz	20 kHz to 24 kHz
0	1	1	0	6 kHz to 7 kHz	48 kHz to 56 kHz	3 kHz to 3.5 kHz	24 kHz to 28 kHz
0	1	1	1	7 kHz to 8 kHz	56 kHz to 64 kHz	3.5 kHz to 4 kHz	28 kHz to 32 kHz
1	0	0	0	8 kHz to 9 kHz	64 kHz to 72 kHz	4 kHz to 4.5 kHz	32 kHz to 36 kHz
1	0	0	1	9 kHz to 10 kHz	72 kHz to 80 kHz	4.5 kHz to 5 kHz	36 kHz to 40 kHz
1	0	1	0	10 kHz to 11 kHz	80 kHz to 88 kHz	5 kHz to 5.5 kHz	40 kHz to 44 kHz
1	0	1	1	11 kHz to 12 kHz	88 kHz to 96 kHz	5.5 kHz to 6 kHz	44 kHz to 48 kHz
1	1	0	0	12 kHz to 13 kHz	96 kHz to 104 kHz	6 kHz to 6.5 kHz	48 kHz to 52 kHz

Table 8. IF counter result *...continued*

IFC3	IFC2	IFC1	IFC0	Deviation from nominal value in FM		Deviation from nominal value in AM	
				IFCA = 0	IFCA = 1	IFCA = 0	IFCA = 1
1	1	0	1	13 kHz to 14 kHz	104 kHz to 112 kHz	6.5 kHz to 7 kHz	52 kHz to 56 kHz
1	1	1	0	14 kHz to 15 kHz	112 kHz to 120 kHz	7 kHz to 7.5 kHz	56 kHz to 60 kHz
1	1	1	1	15 kHz to 16 kHz	≥ 120 kHz	7.5 kHz to 8 kHz	≥ 60 kHz

After a tuning action, which is activated by the state machine, the IF counter is reset at that moment when tuning is established (PLL in-lock). The first counter result is available from 2 ms after reset. For FM further results can be obtained from 4 ms, 8 ms, 16 ms and 32 ms after reset, the increasing count time attenuates influence of FM modulation on the counter result. After this, the counter continues at the maximum count time of 32 ms (see Figure 5). For AM the count time is fixed to 2 ms and results are available every 2 ms.

After AF Update (AFU) sampling the IF counter read value is held (IFCM = 10) (see Figure 6, Figure 17 and Figure 18) for easy I²C-bus read-out. The counter itself remains active in the background in 2 ms count time mode. The IF counter data hold is released after I²C-bus read.

IFCM reads 00 immediately after I²C-bus start of PRESET, SEARCH, AFU, JUMP or CHECK until the first new tuning IFC result is available.

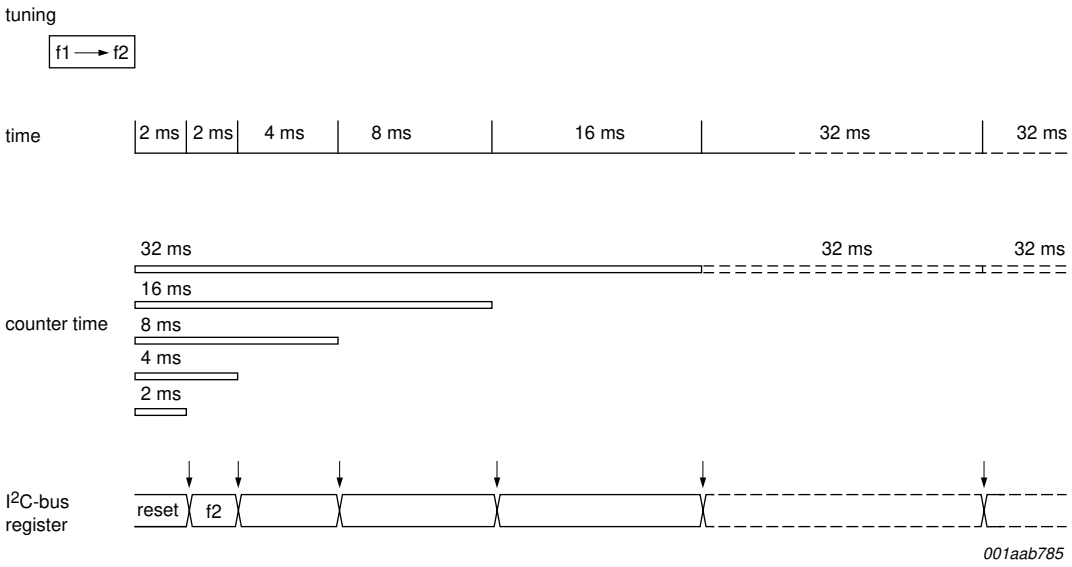

Fig 5. IF counter in FM mode after tuning

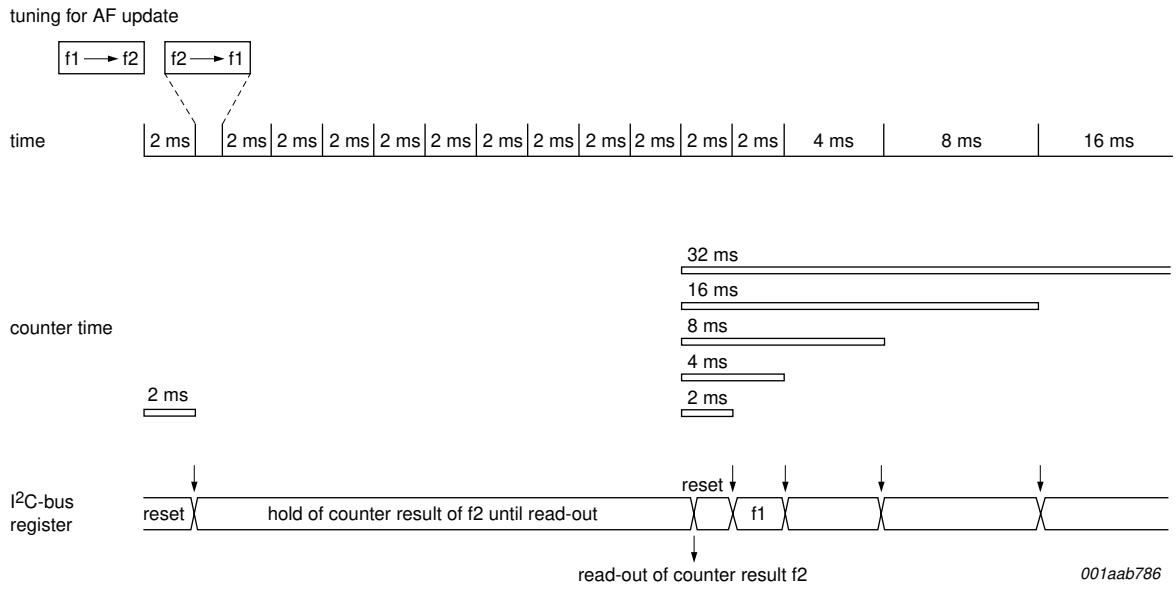

Fig 6. IF counter in FM mode during and after AF update

8.1.2 Read mode: data byte LEVEL

Table 9. LEVEL - format of data byte 1

7	6	5	4	3	2	1	0
LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 10. LEVEL - data byte 1 bit description

Bit	Symbol	Description
7 to 0	LEV[7:0]	level detector; this byte indicates the LEVEL voltage between 0.25 V (LEV = 0) and 4.25 V (LEV = 255) from the tuner part; $V_{LEVEL} = {}^{1}/_{64}LEV[7:0] + 0.25$ V; see Figure 7

After AF update sampling the level read value is held (indicated by IFCM = 10) for easy I²C-bus read-out. The level detector remains active in the background. The LEV data hold is released after I²C-bus read.

To reduce the influence of modulation in AM mode the LEV information is additionally filtered by a slow 60 ms detector. Fast level information is made available during AF update and check tuning.

For standard operation the following level alignment (byte LEVELALGN; see Table 43) is used:

- FM and AM level slope; ΔLEV = 51 (ΔV_{LEVEL} = 0.80 V) at ΔV_{RF} = 20 dB (measured at V_{RF} = 200 μV and V_{RF} = 20 μV)
- FM mode level start; LEV = 78 (V_{LEVEL} = 1.47 V) at V_{RF} = 20 μV
- AM mode level start; LEV = 63 (V_{LEVEL} = 1.24 V) at V_{RF} = 20 μV

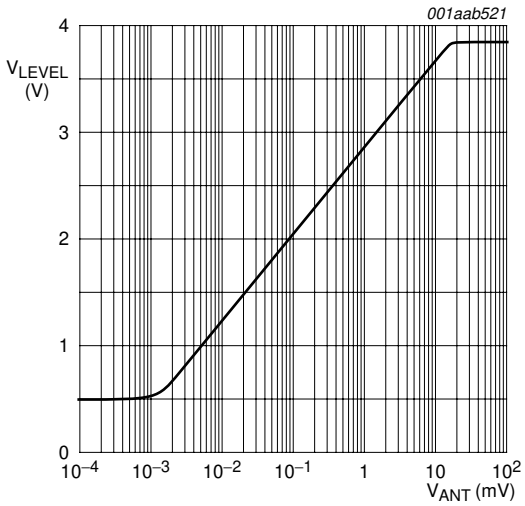

Fig 7. FM RF antenna input signal and level output voltage

8.1.3 Read mode: data byte USN/WAM

Table 11. USN/WAM - format of data byte 2

7	6	5	4	3	2	1	0
USN3	USN2	USN1	USN0	WAM3	WAM2	WAM1	WAM0

Table 12. USN/WAM - data byte 2 bit description

Bit	Symbol	Description
7 to 4	USN[3:0]	ultrasonic noise detector; this value indicates the USN content of the MPX audio signal; see Figure 24
3 to 0	WAM[3:0]	wideband AM detector; this value indicates the WAM content of the LEVEL voltage; see Figure 24

After AF update sampling the USN and WAM read value is held (indicated by IFCM = 10) for easy I²C-bus read-out. The USN and WAM detectors remain active in the background. The USN and WAM data hold is released after I²C-bus read.

8.1.4 Read mode: data byte MOD

Table 13. MOD - format of data byte 3

7	6	5	4	3	2	1	0
MOD4	MOD3	MOD2	MOD1	MOD0	STIN	TAS1	TAS0

Table 14. MOD - data byte 3 bit description

Bit	Symbol	Description
7 to 3	MOD[4:0]	modulation detector; this value indicates the audio modulation; see Table 15
		FM between 0 kHz and 150 kHz FM deviation
		AM between 0 % and 200 % modulation
		FM offset detector; a read value of 31 indicates offset detection. The offset detector is part of the FM bandwidth control algorithm and detects adjacent channel breakthrough.
		VU-meter; when an external audio source is selected and VU-meter read is active (see subaddress 17h; see Table 97) MOD indicates the audio input level (RMS) between 0 V and 2 V; see Table 15.
2	STIN	stereo indicator; this bit indicates if a stereo pilot signal has been detected
		0 = no pilot signal detected
		1 = pilot signal is detected and the FM stereo decoder is activated
1 and 0	TAS[1:0]	Tuning action state; state machine information. The signal TAS informs about internal control functions of the tuner action state machine. This way the progress of tuner actions can be monitored by the microcontroller.
		00 = inactive
		01 = starting mute
		10 = PLL tuning
		11 = tuning ready with mute active

Table 15. MOD detector

MOD4	MOD3	MOD2	MOD1	MOD0	FM radio Δf	AM radio m	VU	External source
0	0	0	0	0	< 1.5 kHz	< 2 %	-	< 0.02 V
0	0	0	0	1	1.5 kHz	2 %	−34 dB	0.02 V
0	0	0	1	0	3 kHz	4 %	−28 dB	0.04 V
0	0	0	1	1	4.5 kHz	6 %	−24 dB	0.06 V
0	0	1	0	0	6 kHz	8 %	−22 dB	0.08 V
0	0	1	0	1	7.5 kHz	10 %	−20 dB	0.1 V
0	0	1	1	0	9.5 kHz	13 %	−18 dB	0.13 V
0	0	1	1	1	12 kHz	16 %	−16 dB	0.16 V
0	1	0	0	0	15 kHz	20 %	−14 dB	0.2 V
0	1	0	0	1	19 kHz	25 %	−12 dB	0.25 V
0	1	0	1	0	24 kHz	32 %	−10 dB	0.32 V
0	1	0	1	1	30 kHz	40 %	−8 dB	0.4 V
0	1	1	0	0	38 kHz	50 %	−6 dB	0.5 V

Table 15. MOD detector *...continued*

MOD4	MOD3	MOD2	MOD1	MOD0	FM radio Δf	AM radio m	VU	External source
0	1	1	0	1	47 kHz	63 %	−4 dB	0.63 V
0	1	1	1	0	60 kHz	80 %	−2 dB	0.8 V
0	1	1	1	1	75 kHz	100 %	0 dB	1 V
1	0	0	0	0	95 kHz	125 %	2 dB	1.25 V
1	0	0	0	1	120 kHz	160 %	4 dB	1.6 V
1	0	0	1	0	150 kHz	200 %	6 dB	2 V
1	0	0	1	1	-	-	-	-
:	:	:	:	:	:	:	:	:
1	1	1	1	0	-	-	-	-
1	1	1	1	1	offset detection	-	-	-

The indicated amplitude levels are approximate values.

In the case of FM radio, carrier modulation is measured (MPX FM deviation). Timing is fixed with fast 30 ms release time. Depending upon reception conditions and internal offsets small modulation levels may be indicated as MOD[4:0] = 0 0000b. After AF update sampling the MOD read value is held (indicated by IFCM = 10) for easy I^{2}C-bus read-out. The MOD detector remains active in the background. The MOD data hold is released after I^{2}C-bus read.

In the case of AM radio, carrier modulation is measured (AM). Timing is fixed with fast 30 ms release time. Modulation may exceed 100 % in cases of special modulation schemes as used by some stations. After AF update sampling, the MOD read value is held (indicated by IFCM = 10) for easy I^{2}C-bus read-out. The MOD detector remains active in the background. The MOD data hold is released after I^{2}C-bus read.

With external source selection and VU-meter mode disabled (AVUM = 0 and COMP = 0) FM or AM modulation is indicated equal to radio mode.

With external source selection and VU-meter mode enabled (AVUM = 1 or COMP = 1) the audio input level of the external source is indicated (i.e. the audio level as found on the line input pins). For stereo signals left and right channels are combined for MOD read ($0.5 \times L + 0.5 \times R$). VU-meter timing is defined by setting HTC. For AVUM control see subaddress 17h; see Table 97. In case of AF update sampling the AM or FM modulation value is indicated with data hold (indicated by IFCM = 10) for easy I^{2}C-bus read-out. The MOD data hold is released after I^{2}C-bus read and VU-meter indication continues.

8.1.5 Read mode: data byte IFBW

Table 16. IFBW - format of data byte 4

7	6	5	4	3	2	1	0
RAGC1	RAGC0	ASIA	IFBW4	IFBW3	IFBW2	IFBW1	IFBW0

Table 17. IFBW - data byte 4 bit description

Bit	Symbol	Description
7 and 6	RAGC[1:0]	RF AGC indicator; PIN diode current on pins IAMAGC or IFMAGC
		00 = FM: < 0.05 mA AM: < 0.1 mA
		01 = FM: 0.05 mA to 0.5 mA AM: 0.1 mA to 0.5 mA
		10 = 0.5 mA to 2.5 mA
		11 = > 2.5 mA
5	ASIA	ASI active; this bit indicates activity of the audio step interpolation function
		0 = ASI is not active
		1 = ASI step is in progress
4 to 0	IFBW[4:0]	FM IF filter bandwidth control; 57 kHz (0 0000) to 165 kHz (1 1111). The bandwidth read data equals the write data definition (at DYN = 0; see Table 28).

8.1.6 Read mode: data byte ID

Table 18. ID - format of data byte 5

7	6	5	4	3	2	1	0
IFCAPG	-	-	-	-	ID2	ID1	ID0

Table 19. ID - data byte 5 bit description

Bit	Symbol	Description
7	IFCAPG	IF filter gear; read value is used for IFCAP adjustment (byte IFCAP); see Table 47
6 to 3	-	reserved
2 to 0	ID[2:0]	device type identification 000 = TEF6901A

8.1.7 Read mode: data byte TEMP

Table 20. TEMP - format of data byte 6

7	6	5	4	3	2	1	0
TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 21. TEMP - data byte 6 bit description

Bit	Symbol	Description
7 to 0	TEMP[7:0]	on-chip temperature; 1 step ≈ 1 K; relative indication

8.2 Write mode

The device is controlled by the I²C-bus. After the Integrated Circuit (IC) address the MSA byte contains the control of the tuning action via the bits MODE[2:0] and subaddressing via bits SA[4:0] (see Figure 8).

All circuits are controlled by the CONTROL register. Any data change in the CONTROL register has immediate effect and will change the operation of the circuit accordingly. The subaddress range 00h to 05h includes data that may lead to audible disturbance when changed. Therefore the subaddress range 00h to 05h is not loaded in the CONTROL register directly but loaded in a BUFFER register instead. This allows the IC to take care of tuning actions and mute control, freeing the microcontroller from cumbersome controls and timings. The subaddress range of 06h onwards does not contain such critical data. I²C-bus information in this range will be loaded in the CONTROL register directly (at acknowledge of each byte).

Controlled by a state machine the BUFFER data will be loaded in the CONTROL register for new settings. However at the same time the CONTROL data is loaded in the BUFFER register. This register swap action allows a fast return to the previous setting because the previous data remains available in the BUFFER register (see Figure 10, Figure 11 and Figure 12).

Via MODE several operational modes can be selected for the state machine. MODE offers all standard tuning actions as well as generic control for flexibility. The state machine controls the tuner directly by controlling the I²C-bus data. Internal circuits like the IF counter, mute and weak signal processing are controlled complementary to the tuner action. The state machine operation starts at the end of transmission (P = STOP). In case a previous action is still active this is overruled and the new action defined by MODE is started immediately.

When only the address byte is transmitted no action is started and no setting is changed, this can be used to test the presence of the device on the bus. To minimize the I²C-bus transmission time only bytes that include data changes need to be written. Following the MSA byte the transmission can start at any given data byte defined by the subaddress (SA) bits. In case of MODE = preset, search or load the value of buffered data that is not overwritten by the new transmission will equal the control register content, i.e. the current tuner state. Instead in case of MODE = buffer, AF update, jump, check or end any not overwritten BUFFER data remains to be the existing BUFFER register content, i.e. the previous tuner state.

After power-on reset, all registers, including the reserved registers, should be initialized with their default settings (see Table 22) using a preset mode tuning action (see Table 25). The tuning mute circuit is muted. An action of the state machine is required to de-mute the circuit, for this purpose preset mode (bits MODE[2:0] = 001) is best fitted since it assures fast settling of all parameters before mute is released.

Table 22. Write mode subaddress overview

Subaddress	Name	Default	Reference
00h	BANDWIDTH	1111 1110	Section 8.2.2
01h	PLLM	0000 1000	Section 8.2.3
02h	PLLL	0111 1110	Section 8.2.3
03h	DAA	0100 0000	Section 8.2.4
04h	AGC	0000 0000	Section 8.2.5
05h	BAND	0010 0000	Section 8.2.6
06h	LEVELALGN	1000 0100	Section 8.2.8
07h	IFCF	0010 0000	Section 8.2.9
08h	IFCAP	0000 1000	Section 8.2.10
09h	ACD	0100 1010	Section 8.2.11
0Ah	SENSE	1000 0101	Section 8.2.12
0Bh	TIMING	0110 0110	Section 8.2.13
0Ch	SNC	0111 0100	Section 8.2.14
0Dh	HIGHCUT	0110 1111	Section 8.2.15
0Eh	SOFTMUTE	0110 1010	Section 8.2.16
0Fh	RADIO	0001 1010	Section 8.2.17
10h	INPUT	0000 1010	Section 8.2.18
11h	VOLUME	0011 0000	Section 8.2.19
12h	TREBLE	0000 1100	Section 8.2.20
13h	BASS	0000 1100	Section 8.2.21
14h	FADER	0000 0000	Section 8.2.22
15h	OUTPUT	0000 1111	Section 8.2.23
16h	BALANCE	1000 0000	Section 8.2.24
17h	LOUDNESS	0000 1100	Section 8.2.25
18h	POWER	0000 0110	Section 8.2.26
19h to 1Eh	reserved	0000 0000	Section 8.2.27
1Fh	TEST	0000 0000	Section 8.2.28

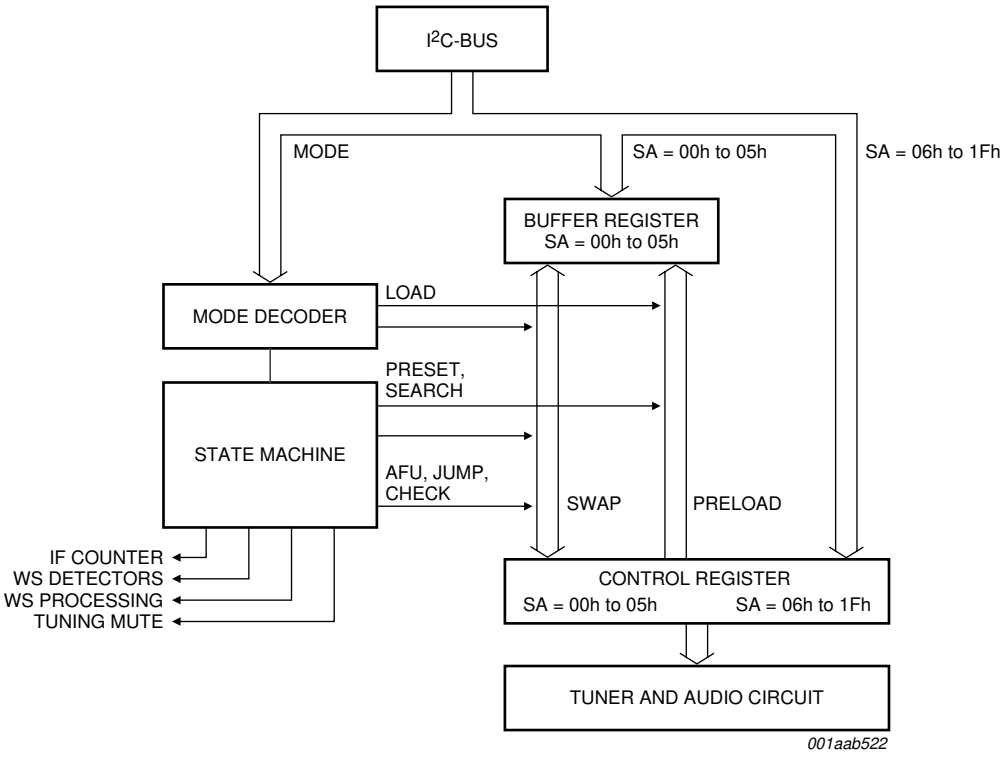

Fig 8. I²C-bus and state machine control

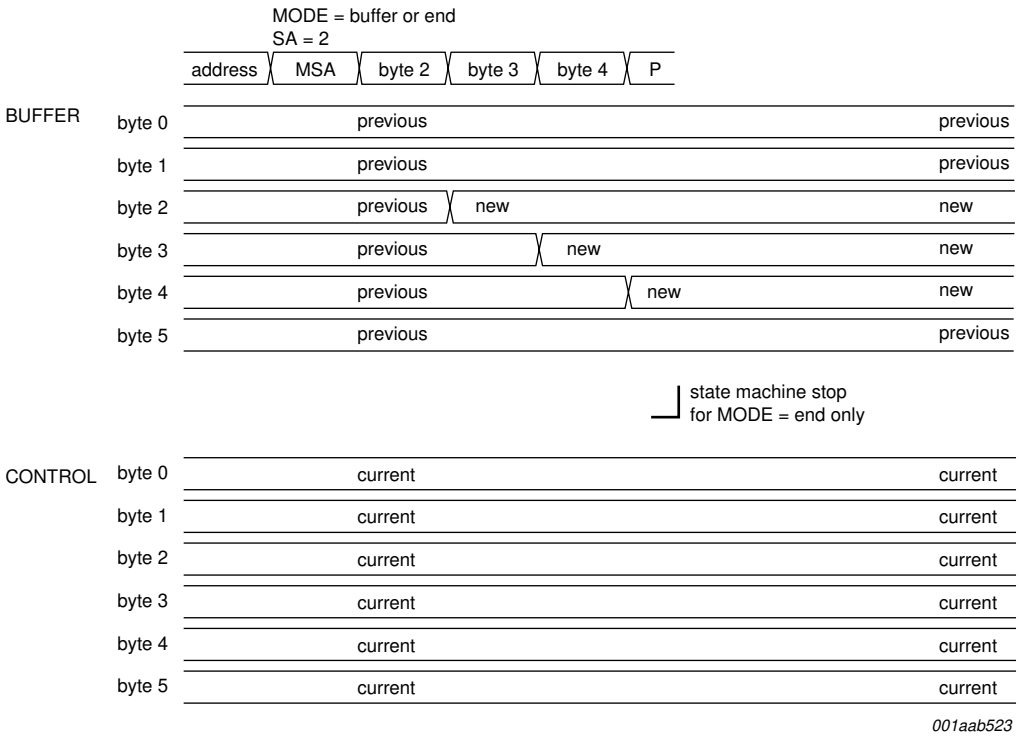

Fig 9. Write without state machine action, no preload, no register swap

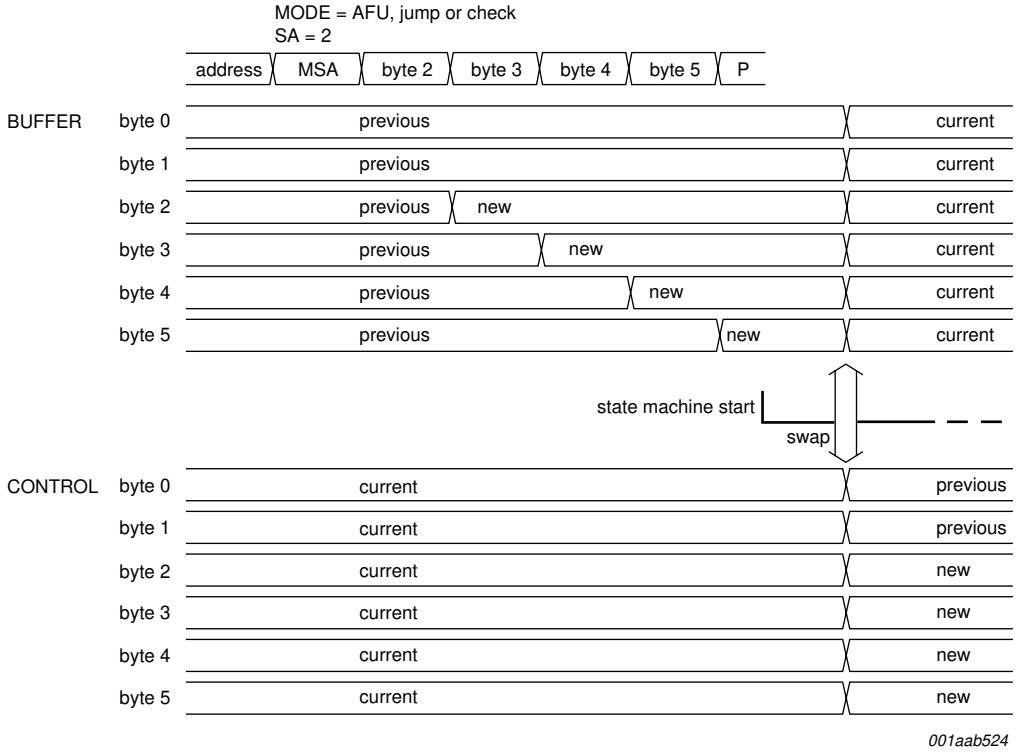

Fig 10. Write with state machine action and swap, no preload