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Intel® Curie™ Module

Datasheet

March 2017

Document rev. 1.3

The Intel® Curie™ module is a hardware product offering design flexibility in a small form factor. This complete, low-power solution comes with compute, motion sensor, Bluetooth® low energy, battery-charging, and pattern matching capabilities for optimized analysis of sensor data—enabling quick and easy identification of actions and motions.

Intel® Quark™ SE Microcontroller C1000 Processor Core

- x86 ISA-compatible CPU
- 32 MHz clock, 32-bit address bus
- 8 kB 2-way L1 instruction cache
- 1.33 DMIPs/MHz, total of 42.56 DMIPs max.

Sensor Subsystem

- ARC* EM4 DSP core with floating point unit
- 8 kB L1 instruction cache, 8 kB data CCM
- Tightly coupled IO to interface sensors/actuators
- 1.4 DMIPS/MHz

Pattern Recognition Accelerator

- Built-in Neuron nodes
- K-Nearest Neighbors (k-NN) and Radial Basis Functions (RBF)

Sensor Subsystem Interfaces

- Two I²C master with standard and fast modes
- Two SPI master up to 16 MHz clock with 4 chip selects
- 19 channel 12-bit ADC
- 16 GPIOs
- Two timers

Power Management

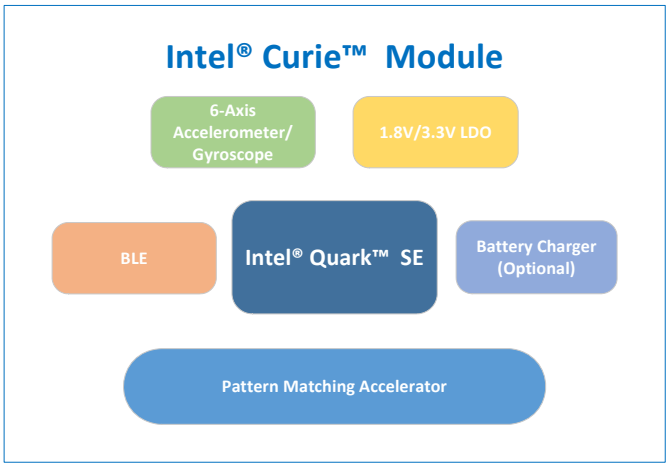
- SoC states: Active, Sleep and Off
- Sensor subsystem: Sensing active, sensing wait and sensing standby
- Platform power DC-DC 1.8 V, 3.3 V

Memory

- 384 kB Flash +8 kB OTP Flash
- 80 kB SRAM

Thermals

- -25 to 70°C operating range



Security

- Secure boot and update
- Isolated SRAM regions
- Flash (NVM) read/write access

Host Interfaces

- USB 1.1 FS device
- Two I²C master/slave with standard, fast & fast mode plus
- Two SPI master up to 16MHz clock with 4 chip selects
- One SPI slave
- Two UARTs, 300 kBaud to 2 MBaud
- Four timers
- Four PWM
- I²S with sample size from 12 to 32-bit
- 32 GPIOs
- 19 comparators

Clock

- 32 kHz and 32 MHz crystal oscillators
- 32 MHz oscillator
- 32 kHz RTC and AON counters/timers
- control

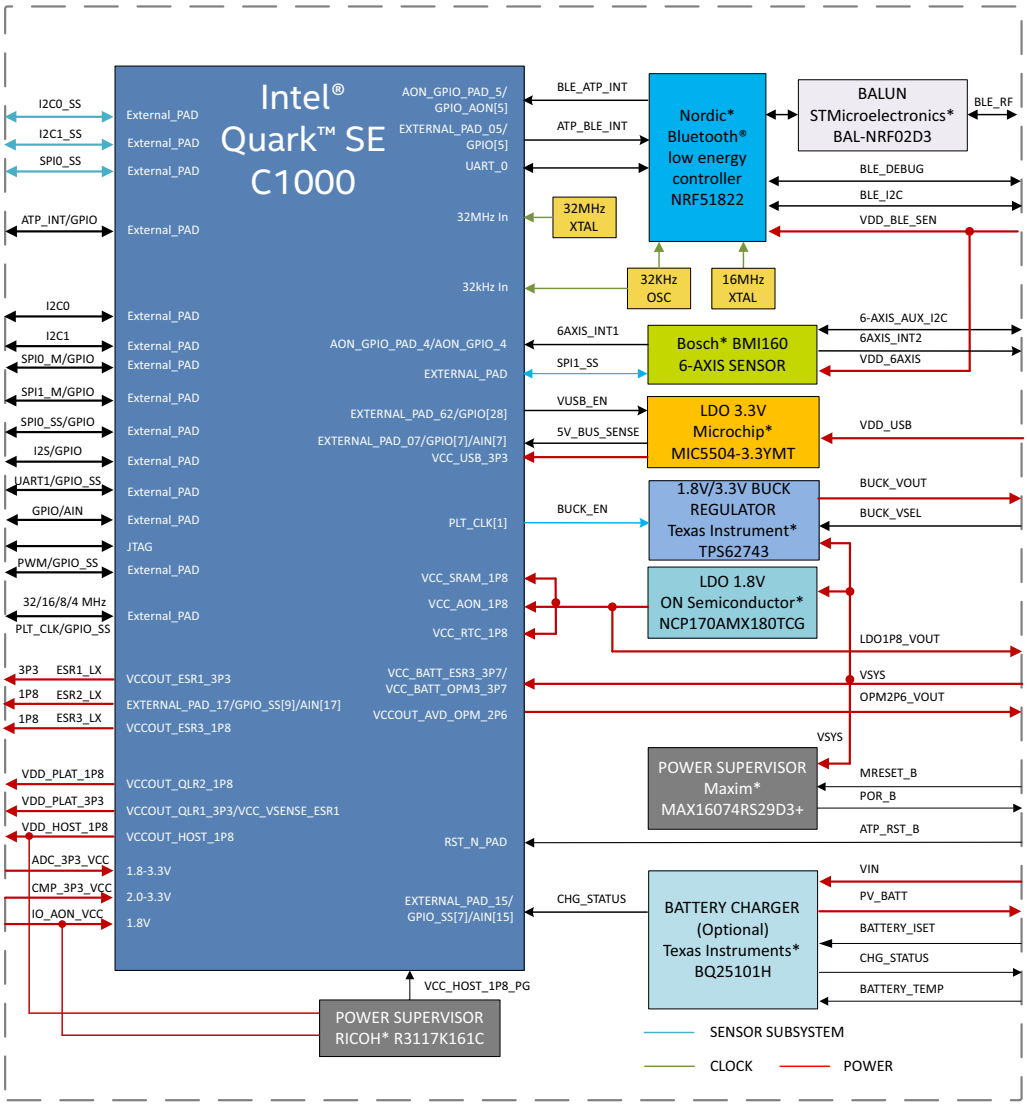
Hardware Reference Designs

Intel has multiple reference designs available through select partners and ODMs. One reference design for the maker community, for example, is the Arduino 101* (branded Genuino 101* in some countries) board which can be used for quick prototyping of concepts. It has the same pin configuration as the Arduino UNO, making it compatible with the majority of components in the Arduino community.

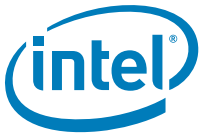
Intel Software Platform

Intel offers several software solutions for the Intel® Curie™ module. These include an open source solution designed to assist developers by increasing the speed and ease of development for a wide variety of products. The Intel® Curie™ Open Developer Kit (ODK) provides access to software, firmware, and services needed for a variety of use cases. The software platform affords more flexibility to the developers to build with multiple environments and the capability to integrate into different IDEs.

Intel® Curie™ Module Block Diagram



For more information, please visit: http://www.intel.com/curie



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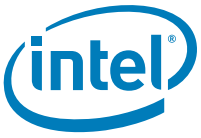
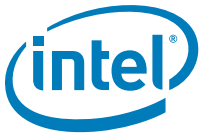
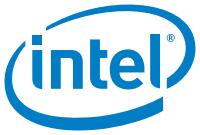
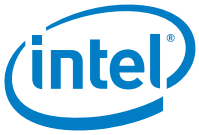


Tables



Figures





Revision History

Revision	Description	Date
1.0	Initial release.	August 2016
1.1	Reorganized the content into the existing chapters and renamed some chapters. Updated the list of reference documents. Added sections about Manufacturing Information, Ordering information, Package marking, and ESD considerations. Updated Table 1-9 to remove external pull-up/pull-down recommendation for JTAG signals.	October 2016
1.2	Added reference to *Intel® Curie™ Power Sequence Considerations* application note in the Power and timing considerations section of the Specifications chapter.	November 2016
1.21	Minor fixes.	December 2016
1.3	Restructured and expanded the content of chapters "Ball Map and Pin Definitions", "Specifications", and "Detailed Description". Also updated the content of the front cover.	March 2017

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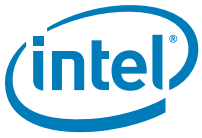


About This Datasheet

This section introduces the Intel® Curie™ module. It covers:

- Intel® Curie™ module
- Intended audience
- Resources, references and terminology

Intel® Curie™ module

This datasheet documents the Intel® Curie™ module, an advanced device built around the Intel® Quark™ SE microcontroller C1000, integrating compute, sense, awareness, connectivity and a programmable input/output controller within a common package.[1] See Chapter 3, "Detailed Description", for more descriptive details.

Intended audience

This datasheet is intended to provide detailed technical information about the Intel® Curie™ module to the vendors, system integrators, and other engineers and technicians who need this level of information.

Resources, references and terminology

See Chapter 4, "Reference and Resources" for information on Software support, Related documents, and Intel® Curie™ module-related community resources as well as Component reference and a list of Terminology.

1. Note that this module is not a FCC-certified module. Emission testing has been performed and designs based on the Intel® Curie™ module that have FCC certification are available, but all new designs based on the module require regulatory approval prior to public availability.

1 Ball Map and Pin Definitions

1.1 Module physical bump map

Table 1-1 shows a map of the module pin out map as a top view into the part.

Table 1-1. Module ball / pin map

	1	2	3	4						21	22	23	24
A	NO BALL	ATP_GND1	I2S_RXD	SPI0_M_CS1						6AXIS_SDA	6AXIS_SCL	6AXIS_INT2	ATP_GND1
B	I2S_RWS	I2S_RSCK	SPI0_M_CS0	ATP_RST_B						SPI1_M_CS2	SPI1_M_MISO	BLE_SDA	BT_GPIO
C	I2S_TWS	I2S_TSCK	SPI0_M_CS2	SPI0_M_SCK						SPI1_M_SCK	SPI1_M_CS3	ATP_GND1	GPIO/AIN_14
D	I2S_TXD	I2C1_SDA	SPI0_M_MOSI	SPI0_M_MISO						SPI1_M_CS1	SPI1_M_CS0	MRESET_B	BLE_SW_CLK
E	I2C1_SCL	I2C1_SS_SDA	PLT_CLK_0	ATP_SPI_S_SCK						AON_IO_VCC	SPI1_M_MOSI	POR_B	BLE_SWDIO
F	I2C1_SS_SCL	PWM3_OUT	ATP_SPI_S_CS	ATP_SPI_S_MOSI						ATP_INT3	ATP_INT0	BLE_SCL	BLE_RF
G	PWM2_OUT	PWM1_OUT	ATP_SPI_S_MISO	SPI0_SS_CS3						ATP_GND1	COMP_AREF	BLE_DEC2	ATP_GND1
H	PWM0_OUT	GPIO/AIN_12	SPI0_SS_CS1	SPI0_SS_CS0						GPIO/AIN_11	CMP_3P3_VCC	ADC_3P3_VCC	VDD_BLE_SEN
J	AVD_OPM_2P6	GPIO/AIN_10	SPI0_SS_MISO	SPI0_SS_SCK						UART1_TX	UART1_CTS	USB_DM	USB_DP
K	BUCK_VOUT	BUCK_VSEL	SPI0_SS_CS2	VDD_USB						UART1_RTS	UART1_RX	ATP_TRST_B	VIN[1]
L	LDO1P8_VOUT	GPIO/AIN_13	ATP_INT2	VSYS						ATP_ADC_AGND	BATT_ISET	ATP_TCK	ATP_TMS
M	PV_BATT	VDD_PLAT_1P8	SPI0_SS_MOSI	ESR2_LX						ATP_TDI	CHG_STATUS	ATP_TDO	I2C0_SCL
N	ESR1_LX	VDD_PLAT_3P3	ATP_INT1	ESR2_VBATT						VIN[2]	BATT_TEMP	I2C0_SS_SDA	I2C0_SS_SCL
P	ATP_GND1	ESR1_VBATT	VDD_HOST_1P8	ESR3_LX						SW_FG_VBATT	ATP_GND1	I2C0_SDA	ATP_GND1

1.2 Module-to-SoC mapping table

The Intel® Curie™ module is based on the Intel® Quark™ SE microcontroller C1000. Some of the microcontroller signals are used internally within the module to operate the integrated Bosch* BMI160 six-axis sensor, the battery charger and the Nordic* nRF51822 Bluetooth® low energy controller, while other SoC signals are routed directly to the module interface.

Table 1-2 provides the list of high-level reference mapping signals between the Intel Quark microcontroller core and the Intel Curie module. It also includes, where available, alternate functions that interface pins can be configured for.

Consult the Intel® Quark™ SE microcontroller C1000 datasheet for additional information on specific microcontroller functions and registers.

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
A1	No Ball	-	-	-	-	-
A2	ATP_GND1[3]	ATP_GND1[3]	VSS3	ATP_GND1	VSS	F3
A3	I2S_RXD	I2S_RXD	GPIO[15]	I2S_RXD	EXTERNAL_PAD_49	B8
A4	SPI0_M_CS1	SPI0_M_CS_B[1]	GPIO[25]	SPI0_M_CS_B[1]	EXTERNAL_PAD_59	A10
A21	6AXIS_SDA	6AXIS_SDA	ASDX (6AXIS / 2)	-	6AXIS I^2C to external magnetometer to get 9AXIS	-
A22	6AXIS_SCL	6AXIS_SCL	ASCX (6AXIS / 3)	-		-
A23	6AXIS_INT2	6AXIS_INT2	INT2 (6AXIS / 9)	-	6AXIS Interrupt to external magnetometer to get 9AXIS	-
A24	ATP_GND1[9]	ATP_GND1[9]	VSS9	ATP_GND1	VSS	M1
B1	I2S_RWS	I2S_RWS	GPIO[17]	I2S_RWS	EXTERNAL_PAD_51	B9
B2	I2S_RSCK	I2S_RSCK	GPIO[16]	I2S_RSCK	EXTERNAL_PAD_50	A8
B3	SPI0_M_CS0	SPI0_M_CS_B[0]	GPIO[24]	SPI0_M_CS_B[0]	EXTERNAL_PAD_58	E8
B4	ATP_RST_B	RST_B	RST_B		RST_N_PAD	F11
B21	SPI1_M_CS2	SPI1_M_CS_B[2]	GPIO[13]	SPI1_M_CS_B[2]	EXTERNAL_PAD_47	B07
B22	SPI1_M_MISO	SPI1_M_MISO	GPIO[9]	SPI1_M_MISO	EXTERNAL_PAD_43	D6
B23	BLE_SDA	BLE P0_31 / E8	-	-	BLE I^2C to external device optional	-
B24	BT_GPIO	BLE P0_18 / H1	-	-	BLE GPIO to external device optional	-
C1	I2S_TWS	I2S_TWS	GPIO[19]	I2S_TWS	EXTERNAL_PAD_53	C9
C2	I2S_TSCK	I2S_TSCK	GPIO[18]	I2S_TSCK	EXTERNAL_PAD_52	A9
C3	SPI0_M_CS2	SPI0_M_CS_B[2]	GPIO[26]	SPI0_M_CS_B[2]	EXTERNAL_PAD_60	B10
C4	SPI0_M_SCK	SPI0_M_SCK	GPIO[21]	SPI0_M_SCK	EXTERNAL_PAD_55	D8

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
C21	SPI1_M_SCK	SPI1_M_SCK	GPIO[8]	SPI1_M_SCK	EXTERNAL_PAD_42	C6
C22	SPI1_M_CS3	SPI1_M_CS_B[3]	GPIO[14]	-	EXTERNAL_PAD_48	A7
C23	ATP_GND1[5]	ATP_GND1[5]	VSS5	ATP_GND1	VSS	L12
C24	GPIO/AIN_14	GPIO_SS[6]	GPIO_SS[6]	AIN[14]	EXTERNAL_PAD_14	F01
D1	I2S_TXD	I2S_TXD	GPIO[20]	I2S_TXD	EXTERNAL_PAD_54	D9
D2	I2C1_SDA	I2C1_SDA	I2C1_SDA	-	EXTERNAL_PAD_23	D2
D3	SPI0_M_ MOSI	SPI0_M_MOSI	GPIO[23]	SPI0_M_MOSI	EXTERNAL_PAD_57	E9
D4	SPI0_M_ MISO	SPI0_M_MISO	GPIO[22]	SPI0_M_MISO	EXTERNAL_PAD_56	E7
D21	SPI1_M_CS1	SPI1_M_CS_B[1]	GPIO[12]	SPI1_M_CS_ B[1]	EXTERNAL_PAD_46	C7
D22	SPI1_M_CS0	SPI1_M_CS_B[0]	GPIO[11]	SPI1_M_CS_ B[0]	EXTERNAL_PAD_45	D7
D23	MRESET_B	MR (MAX16074 / B2)	-	-	-	-
D24	BLE_SW_CLK	SWDCLK (BLE / H2)	GPIO[27]	SPI0_M_CS_ B[3]	EXTERNAL_PAD_61	C10
E1	I2C1_SCL	I2C1_SCL	-	-	EXTERNAL_PAD_22	D1
E2	I2C1_SS_ SDA	I2C1_SS_SDA	-	-	EXTERNAL_PAD_26	B3
E3	PLT_CLK_0	PLT_CLK[0]	GPIO_SS[14]	PLT_CLK[0]	EXTERNAL_PAD_67	D12
E4	ATP_SPI_S_ SCK	SPI_S_SCK	GPIO[2]	AIN[2]/ SPI_S_SCK	EXTERNAL_PAD_02	H5
E21	AON_IO_VCC	AON_IO_VCC	VCC_IO_AON1	VCC_IO_AON1	VCC_IO_AON1	A11
			VCC_IO_AON2	VCC_IO_AON2	VCC_IO_AON2	G6
E22	SPI1_M_ MOSI	SPI1_M_MOSI	GPIO[10]	SPI1_M_MOSI	EXTERNAL_PAD_44	E6
E23	POR_B	RESETN (MAX16074 / B1)	-	-	Power supervisory Power On Reset output	-
E24	BLE_SWDIO	SWDIO (BLE/J2)	GPIO[6]	AIN[6]	EXTERNAL_PAD_06	H4
F1	I2C1_SS_SCL	I2C1_SS_SCL	I2C1_SS_SCL	-	EXTERNAL_PAD_27	A3
F2	PWM3_OUT	PWM[3]	GPIO_SS[13]	PWM[3]	EXTERNAL_PAD_66	B11
F3	ATP_SPI_S_ CS	SPI_S_CS_B	GPIO[0]	AIN[0] / SPI_S_CS_B	EXTERNAL_PAD_00	F2
F4	ATP_SPI_S_ MOSI	SPI_S_MOSI	GPIO[3]	AIN[3] / SPI_S_MOSI	EXTERNAL_PAD_03	J6
F21	ATP_INT3	ATP_INT3	GPIO_AON[3]	-	AON_GPIO_PAD_3	F9
F22	ATP_INT0	ATP_INT0	GPIO_AON[0]	-	AON_GPIO_PAD_0	G9
F23	BLE_SCL	BLE P0_30 / D8		-	BLE I^2C to external device optional	-
F24	BLE_RF	BALUN SE / A1	-	-	Antenna Micro Strip (50 ohms)	-

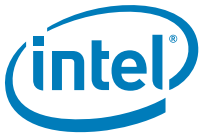


Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
G1	PWM2_OUT	PWM[2]	GPIO_SS[12]	PWM[2]	EXTERNAL_PAD_65	C11
G2	PWM1_OUT	PWM[1]	GPIO_SS[11]	PWM[1]	EXTERNAL_PAD_64	D11
G3	ATP_SPI_S_MISO	SPI_S_MISO	GPIO[1]	AIN[1]	EXTERNAL_PAD_01	G4
G4	SPI0_SS_CS3	SPI0_SS_CS_B[3]	GPIO[30]	SPI0_SS_CS_B[3]	EXTERNAL_PAD_34	A4
G21	ATP_GND1[7]	ATP_GND1[7]	VSS7	ATP_GND1	VSS	M11
G22	COMP_AREF	COMP_AREF	COMP_AREF	-	COMP_AREF (or AREF_PAD)	F5
G23	BLE_DEC2	DEC2 (BLE / F1)	-	-	-	-
G24	ATP_GND1[6]	ATP_GND1[6]	VSS6	ATP_GND1	VSS	M12
H1	PWM0_OUT	PWM[0]	GPIO_SS[10]	PWM[0]	EXTERNAL_PAD_63	E10
H2	GPIO/AIN_12	GPIO_SS[4]	GPIO_SS[4]	AIN[12]	EXTERNAL_PAD_12	J04
H3	SPI0_SS_CS1	SPI0_SS_CS_B[1]	SPI0_SS_CS_B[1]	-	EXTERNAL_PAD_32	C4
H4	SPI0_SS_CS0	SPI0_SS_CS_B[0]	SPI0_SS_CS_B[0]	-	EXTERNAL_PAD_31	D4
H21	GPIO/AIN_11	GPIO_SS[3]	GPIO_SS[3]	AIN[11]	EXTERNAL_PAD_11	G1
H22	CMP_3P3_VCC	CMP_3P3_VCC	VCC_CMP_3P3[2]	-	VCC_CMP_3P3[2]	J3
			VCC_CMP_3P3[1]	-	VCC_CMP_3P3[1]	M2
H23	ADC_3P3_VCC	-	-	-	-	-
H24	VDD_BLE_SEN	-	-	-	-	-
J1	OPM2P6_VOUT	OPM2P6_VOUT	VCC_AVD_OPM_2P6	-	VCCOUT_AVD_OPM_2P6	K11
		AVD_OPM_2P6	VCCOUT_AVD_OPM_2P6	-		
		VCC_AVD_OPM_2P6	VCC_AVD_OPM_2P6	-	VCC_AVD_OPM_2P6	K12
		AVD_OPM_2P6		-		
J2	GPIO/AIN_10	GPIO_SS[2]	-	AIN[10]	EXTERNAL_PAD_10	K5
J3	SPI0_SS_MISO	SPI0_SS_MISO	SPI0_SS_MISO	-	EXTERNAL_PAD_28	C3
J4	SPI0_SS_SCK	SPI0_SS_SCK	SPI0_SS_SCK	-	EXTERNAL_PAD_30	D3
J21	UART1_TX	UART1_TX	GPIO_SS[8]	AIN[16]/ UART1_TXD	EXTERNAL_PAD_16	L4
J22	UART1_CTS	UART1_CTS	GPIO_SS[0]	AIN[8]/ UART1_CTS_B	EXTERNAL_PAD_08	L5
J23	USB_DM	USB_DM	USB_DN	-	USB_PADN	H2
J24	USB_DP	USB_DP	USB_DP	-	USB_PADP	H1

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
K1	BUCK_VOUT	BUCK_VOUT	-	-	-	-
K2	BUCK_VSEL	VSEL1,3 (TPS62743)	-	-	-	-
K3	SPI0_SS_CS2	SPI0_SS_CS2]	SPI0_SS_CS_B[2]	GPIO[29]	EXTERNAL_PAD_03	B4
K4	VDD_USB	VDD_USB	-	-	EXTERNAL_PAD_07	G3
K21	UART1_RTS	UART1_RTS	GPIO_SS[1]	AIN[9]/ UART1_RTS_B	EXTERNAL_PAD_09	M5
K22	UART1_RX	UART1_RX	GPIO_SS[9]	AIN[17]/ UART1_RXD	EXTERNAL_PAD_17	M4
K23	ATP_TRST_B	ATP_TRST_B	TRST_B	-	TRST_PAD	G5
K24	VIN[1]	VIN (BQ25101 / A2)	-	-	-	-
L1	LDO1P8_VOUT	LDO1P8_VOUT	VCC_AON_1P8[2]	-	VCC_AON_1P8	A2
			VCC_SRAM_1P8	-	VCC_SRAM_1P8	C8
			VCC_RTC_1P8	-	VCC_RTC_1P8	G10
			VCC_AON_1P8[1]	-	VCC_AON_1P8	J7
L2	GPIO/AIN_13	GPIO/AIN_13]	GPIO_SS[5]	AIN[13]	EXTERNAL_PAD_13	G2
L3	ATP_INT2	ATP_INT2	GPIO_AON[2]	-	AON_GPIO_PAD_2	E12
L4	VSYS	VSYS	VCC_BATT_OPM_3P7	-	VCC_BATT_OPM_3P7	L10
			VCC_BATT_ESR3_3P7	-	VCC_BATT_ESR3_3P7	M9
L21	ATP_ADC_AGND	ATP_ADC_AGND	VSS_ADC_AGND	-	VSS_ADC_AGND	L3
L22	BATT_ISET	BATT_ISET	-	-	-	-
L23	ATP_TCK	ATP_TCK	TCK	-	TCK_PAD	G7
L24	ATP_TMS	ATP_TMS	TMS	-	TMS_PAD	F6
M1	PV_BATT	OUT (BQ25101 / A1)	-	-	-	-
M2	VDD_PLAT_1P8	VDD_PLAT_1P8	VCCOUT_QLR2_1P8	-	VCCOUT_QLR2_1P8	J11
M3	SPI0_SS_MOSI	SPI0_SS_MOSI	SPI0_SS_MOSI	-	EXTERNAL_PAD_29	E3
M4	ESR2_LX	ESR2_LX	VCCOUT_ESR2_1P8	-	EXTERNAL_PAD_17	J12
M21	ATP_TDI	ATP_TDI	TDI	-	TDI_PAD	F4
M22	CHG_STATUS	CHGN (BQ25101 / C1)	GPIO_SS[7]	AIN[15]	EXTERNAL_PAD_15	J5
M23	ATP_TDO	ATP_TDO	TDO	-	TDO_PAD	F8
M24	I2C0_SCL	I2C0_SCL	I2C0_SCL	-	EXTERNAL_PAD_20	C1

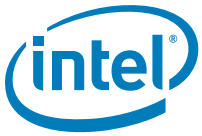
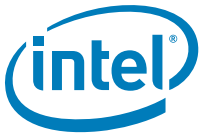


Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
N1	ESR1_LX	ESR1_LX	VCCOUT_ESR1_3P3	-	VCCOUT_ESR1_3P3	J8
N2	VDD_PLAT_3P3	VDD_PLAT_3P3	VCC_VSENSE_ESR1	-	VCC_VSENSE_ESR1	H9
			VCCOUT_QLR1_3P3	-	VCCOUT_QLR1_3P3	J9
N3	ATP_INT1	ATP_INT1	GPIO_AON[1]	-	AON_GPIO_PAD_1	E11
N4	ESR2_VBATT	ESR2_VBATT	VCC_BATT_ESR2_3P7	-	VCC_BATT_ESR2_3P7	L11
N21	VIN[2]	VIN (BQ25101 / A2)	-	-	-	-
N22	BATT_TEMP	TSN (BQ25101 / B1)	-	-	-	-
N23	I2C0_SS_SDA	I2C0_SS_SDA	I2C0_SS_SDA	-	EXTERNAL_PAD_24	E1
N24	I2C0_SS_SCL	I2C0_SS_SCL	I2C0_SS_SCL	-	EXTERNAL_PAD_25	E2
P1	ATP_GND1[1]	ATP_GND1[1]	VSS1	ATP_GND1	VSS	A1
P2	ESR1_VBATT	ESR1_VBATT	VCC_BATT_ESR1_3P7	-	VCC_BATT_ESR1_3P7	M10
P3	VDD_HOST_1P8	VDD_HOST_1P8	VCC_HOST_1P8[2]	-	VCC_HOST_1P8[2]	A5
			VCC_HOST_1P8[1]	-	VCC_HOST_1P8[1]	H6
			VCC_PLL_1P8	-	VCC_PLL_1P8	K3
			VCCOUT_HOST_1P8	-	VCCOUT_HOST_1P8	K10
P4	ESR3_LX	ESR3_LX	VCCOUT_ESR3_1P8	-	VCCOUT_ESR3_1P8	K9
P21	SW_FG_VBATT	SW_FG_VBATT / AIN[4])	-	-	EXTERNAL_PAD_04	K6
P22	ATP_GND1[4]	-	-	-	-	-
P23	I2C0_SDA	I2C0_SDA	I2C0_SDA	-	EXTERNAL_PAD_21	C2
P24	ATP_GND1[10]	ATP_GND1[10]	VSS9	ATP_GND1	VSS	M01
-	Internal to 6AXIS	6AXIS_MISO	SDO (6AXIS / 1)	SPI1_SS_MISO	-	B5
-		6AXIS_MOSI	SDX (6AXIS / 14)	SPI1_SS_MOSI	EXTERNAL_PAD_36	C5
-		6AXIS_SCLK	SCX (6AXIS / 13)	SPI1_SS_SCK	EXTERNAL_PAD_37	D5
-		6AXIS_CS	CSB (6AXIS / 12)	SPI1_SS_CS_B[0]	EXTERNAL_PAD_38	E5
-		6AXIS_INT1	INT1 (6AXIS / 4)	GPIO_AON[4]	AON_GPIO_PAD_4	F10

Table 1-2. Intel® Curie™ module to Intel® Quark™ SE microcontroller C1000 signal mapping (continued)

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Primary Function	Alt Function1	Alt Function2	Intel® Quark™ SE Microcontroller C1000/ Component Ball Name	Intel Quark microcontroller Ball Number
-	Internal to BLE	UART0_CTS	P0_12 (BLE / J5)	SPI1_SS_CS_B[2]	UART0_CTS_B	A6
-		UART0_TXD	P0_09 (BLE / J7)	UART0_TXD	GPIO[31]	B2
-		UART0_RTS	P0_10 (BLE / H6)	SPI1_SS_CS_B[3]	UART0_RTS_B	B6
-		UART0_RXD	P0_11 (BLE / J6)	UART0_RXD	AIN[18]	K4
-		ATP_BLE_INT	GPIO[5]	AIN[5]	EXTERNAL_PAD_05	L6
-	ATP_GND1	ATP_GND1[2]	VSS2	ATP_GND1	VSS	B1
-		ATP_GND1	VSS8			M6
-	GND	-	-	-	VSS_IO_AON1	B12
-		-	-	-	VSS_IO_AON2	F7
-		-	-	-	VSS_GNDSENSE_OPM	K7
-		-	-	-	VSS_PLL	L2
-		-	-	-	VSS_RTC	H11
-		-	-	-	VSS_USB	J1
-		-	-	-	VSS_AVS_ESR1	L7
-		-	-	-	VSS_GNDSENSE_ESR1	L8
-		-	-	-	VSS_AVS_ESR2	H7
-		-	-	-	VSS_GNDSENSE_ESR2	H8
-		-	-	-	VSS_GNDSENSE_ESR3	M7
-		-	-	-	VSS_AVS_ESR3	M8
-		-	-	-	VSS_AVSS_CMP1	H3
-		-	-	-	VSS_AVSS_CMP2	L1
-		-	PLT_REG_EN	-	PLT_REG_EN	H10
-	VSYS	VCC (MAX16074 / A2)	-	-	Power supervisory Power On Reset output	-



1.3 Pin definitions

This section presents the Intel® Curie™ module pins and their definitions grouped by function.

Note: The ball names differ from the Intel® Curie™ module to the Intel® Quark™ SE microcontroller C1000 processor core integrated in the module. Table 1-2 above shows the mapping between the two.

1.3.1 Battery and power management pins

Table 1-3 lists the pins on the module that provide battery and power management functionality.

The Intel® Curie™ module has a built-in battery charger, which is optional to use. The user can bypass this internal charger. Refer to the *Battery Charging and Management* section of the *Intel® Curie™ Module Design Guide* for more information.

Table 1-3. Battery and power management pins

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Function
J1	OPM2P6_VOUT	2.6 V reference voltage output. Can be used to power CMP_3P3_VCC. Otherwise leave disconnected.
K4	VDD_USB	DC power for USB interface (optional). This is supplied to the module by the USB cable or external 5V supply. It is also connected to SoC AIN7 internally via voltage divider to be able to detect the voltage presence by software (22k pull-down / 36k pull-up to VDD_USB). Then USB voltage converter can be enabled d by VUSB_EN (GPIO28) to provide 3.3V to the SoC for USB controller.
K24, N21	VIN[1], VIN[2]	Battery charger input voltage, These two pins are connected together internally in module to provide more current. Both pins externally need to be connected to the same voltage source.
L1	LDO1P8_VOUT	AON LDO power output. If used outside Intel® Curie™ module, maximum of 50mA can be drawn externally. It is also connected internally to the SoC VCC_AON_1P8[1], VCC_AON_1P8[2], VCC_SRAM_1P8.
L4	VSYS	Main DC input power. Provides input voltage to BUCK_VOUT (TPS62743) converter, VCC_BATT_OPM_3P7 (SoC), VCC_BATT_ESR3_3P7 (SoC), VCC_AON_PWR (NCP170AMX180TCG).
L22	BATT_ISET	Use a Pull-Down resistor value 0.54-13.5kohm to set charging current. Do not leave floating. Refer to (BQ2510H) datasheet for ISET.
M1	PV_BATT	Battery charger output (4.35 V maximum ±50 mV) to battery (positive) to charge it. External application circuit can be added for protection or / and fuel gauge circuit.
M22	CHG_STATUS	Open drain (15 mA maximum) pulls low when battery is being charged.
N21	See K24 above	
N22	BATT_TEMP	Connect to battery thermistor. See TI BQ25101H* Datasheet for details. If battery does not have internal thermistor to measure temperature, then external thermistor can be used touching the battery to measure temperature for safety and meeting charging requirement of the battery manufacture for reliability.
P21	SW_FG_VBATT	Analog input for software fuel gauge (bat voltage measurement). Connected to SoC AIN4 and can be configured via software to use ADC to measure voltage or current.

1.3.2 Platform buck converter pins

Table 1-4 lists the pins that provide platform control for the buck converter integrated in the module.

Table 1-4. Platform buck converter pins

Ball No.	Ball Name	Function
K1	BUCK_VOUT	Buck converter output of 1.8 V / 3.3 V. It can be connected and used for Awake ON (AON) IO supply voltage. Connect a 0.1 uF decoupling capacitor. The input voltage requirement is minimum of 3.7 V and maximum of 4.4 V. Internal signal BUCK_EN (GPIO_SS15) signal is used for software to disable or enable this converter. If software does not configure the BUCK_EN signal and leave it floating then AON_IO_VCC will enable it via a 10M pull-up resistor. It is highly recommended to enable and disable this via software. In some noisy application this pull-up may not be enough to keep this converter enabled all the time.
K2	BUCK_VSEL	0 (Ground) sets BUCK_VOUT to 1.8 V 1 (VSYS) sets BUCK_VOUT to 3.3 V

1.3.3 Additional buck converter pins

Table 1-5 lists the other pins that provide access to the buck converter integrated in the module.

Table 1-5. Additional buck converter pins

Ball No.	Ball Name	Function
M2	VDD_PLAT_1P8	Platform 1.8 V output[1]
M4	ESR2_LX	External inductor and capacitor connection (for Platform 1V8)[1]
N1	ESR1_LX	External inductor and capacitor connection (for Platform 3V3)[1]
N2	VDD_PLAT_3P3	Platform 3.3 V output[1]
N4	ESR2_VBATT	DC input for switching regulator 2[1]
P2	ESR1_VBATT	DC input for switching regulator 1[1]
P3	VDD_HOST_1P8	1.8 V input to host SoC
P4	ESR3_LX	External inductor and capacitor connection (for Host 1V8)

Notes:

1. Refer to the *Intel® Curie™ Module Design Guide* for guidance on the use of these pins. for further information regarding these pins, refer to the Power Architecture section of the *Intel® Quark™ SE Microcontroller C1000 Datasheet* (in the *Power Management* chapter).

1.3.4 Reference voltage pins

Table 1-6 lists the reference voltage pins for the module.

Table 1-6. Reference voltages on module

Ball No.	Ball Name	Function
E21	AON_IO_VCC	Alway-on GPIO supply voltage
G22	COMP_AREF	Comparator reference voltage external input. Software selectable external 0-3.63 V or internal 1.09 V reference voltage
H22	CMP_3P3_VCC	Comparator supply voltage. See Table 2-6 for voltage specifications.
H23	ADC_3P3_VCC	ADC supply and reference voltage

1.3.5 Module ground pins

Table 1-7 lists the ground pins for the module.

Table 1-7. Ground pins

Ball No.	Ball Name	Function
A2	ATP_GND1[3]	Module ground
A24	ATP_GND1[9]	Module ground
C23	ATP_GND1[5]	Module ground
G21	ATP_GND1[7]	Module ground
G24	ATP_GND1[6]	Module ground
L21	ATP_ADC_AGND	Analog ground. Can be connected directly to analog ground at a single point.
P1	ATP_GND1[1]	Module ground
P22	ATP_GND1[4]	Module ground
P24	ATP_GND1[10]	Module ground

1.3.6 Reset pins

Table 1-8 lists the reset pins for the module.

Table 1-8. Reset pins

Ball No.	Ball Name	Function
B4	ATP_RST_B	SoC hardware reset. Active low. See Section 2.2.6 for information on reset wiring.
D23	MRESET_B	Manual reset. Connect POR_B to reset signal ATP_RST_B and pull low trigger a hardware reset. Refer Power supervisor chip (MAX16074) datasheet for more information.
E23	POR_B	Power on reset from power supervisor chip. Active low / open drain requires a pull-up on this signal. Refer Power supervisor chip (MAX16074) datasheet for more information.

1.3.7 Debugging pins

Table 1-9 lists debugging pins for the module.

When the JTAG emulator is used to connect to the debugging pins on the module, the emulator options need to be configured appropriately to ensure there are no conflicts with these debugging pins.

Table 1-9. Debugging pins

Ball No.	Ball Name	Function
D24	BLE_SW_CLK	Two wire debug interface. For JTAG programming using J-Link. This is also connected to a GPIO[27] signal.
E24	BLE_SWDIO	Two wire debug interface. For JTAG programming using J-Link. This is also connected to a GPIO[6] signal.
K23	ATP_TRST_B	JTAG emulator debugger / programmer TRST signal.
L23	ATP_TCK	JTAG emulator debugger / programmer TCK signal.
L24	ATP_TMS	JTAG emulator debugger / programmer TMS signal.
M21	ATP_TDI	JTAG emulator debugger / programmer TDI signal.
M23	ATP_TDO	JTAG emulator debugger / programmer TDO signal.

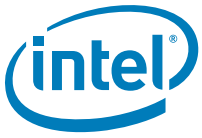
1.3.8 Wake-capable interrupt pins

Table 1-10 lists the pins that are capable of waking the Intel® Quark™ SE microcontroller from a sleep state.

These signals can be programmed to be GPIO input or output. These are always powered.

Table 1-10. Intel® Quark™ SE microcontroller C1000 always-on wake capable interrupt pins

Ball No.	Ball Name	Function	Drive (Low / High)
F21	ATP_INT3	AON GPIO_AON3 / Always On Wake capable digital IO / Interrupt 3, can be configured for one of the two cores.	4mA / 8mA
F22	ATP_INT0	AON GPIO_AON0 / Always On Wake capable digital IO / Interrupt 0, can be configured for one of the two cores.	4mA / 8mA
L3	ATP_INT2	AON GPIO_AON2 / Always On Wake capable digital IO / Interrupt 2, can be configured for one of the two cores.	4mA / 8mA
N3	ATP_INT1	AON GPIO_AON1 / Always On Wake capable digital IO / Interrupt 1, can be configured for one of the two cores.	4mA / 8mA



1.3.9 Clock out pin

Table 1-11 documents the clock out pin on the module.

The software can configure the PLT_CK_0 pin to bring out the SoC core clock (32/16/8/4). It can be used for debugging or for synchronizing the application circuitry. To reduce the power consumption, and if the application does not need it, you should not enable this pin.

Table 1-11. Clock out pin

Ball No.	Ball Name	Primary Function	Alt Function1	Drive (Low / High)
E3	PLT_CLK_0	32/16/8/4MHz Clock output from module	GPIO_SS[14]	4/8mA

1.3.10 GPIO pin mapping

The following subsections document the general purpose input/output (GPIO) pins for the module. These generic pins can be programmed either as input or as output pins at run time. The GPIO pins can be configured for primary or alternate function. Table 1-14 provides the mapping for the multiple functions each pin can be used for.

Table 1-15 documents the internal GPIO signals within the module.

1.3.10.1 GPIO/ analog input pins

Table 1-12 documents the GPIO pins capable of receiving analog inputs. Please note that the internal pull-up resistors are disabled at reset.

Table 1-12. GPIO/ analog input pins

Ball No.	Ball Name	Primary Function	Alt Function1	Drive (Low / High)	Internal Pull-up / Pull-down
C24	GPIO/AIN_14	GPIO_SS[6] (Should be used only for sensor devices)	AIN[14]	Selectable as 4/8	47 kohm
J2	GPIO/AIN_10	GPIO_SS[2] (Should be used only for sensor devices)	AIN[10]		
H21	GPIO/AIN_11	GPIO_SS[3] (Should be used only for sensor devices)	AIN[11]		
H2	GPIO/AIN_12	GPIO_SS[4] (Should be used only for sensor devices)	AIN[12]		
L2	GPIO/AIN_13	GPIO_SS[5] (Should be used only for sensor devices)	AIN[13]		
M22	CHG_STATUS	GPIO_SS[7] (Should be used only for sensor devices)[1]	AIN[15]		

Notes:

1. For CHG_STATUS, please note:
   - CHG_STATUS can be read via software at GPIO_SS[7] / AIN[15]
   - Charge status: Open drain (LOW) means charging and open means complete first charging cycle is complete
   - GPIO_SS[7] / AIN[15] is connected to the external pin (M22) for the device hardware to read the state
   - Internal or external pull-up resistor should be used for this pin
   - If the battery charger is not used then AIN[15] can be used as an external analog input or GPIO_SS[7]. Disable the battery charger by connecting BATT_TEMP to ground.
   - CHG_STATUS or GPIO_SS[7] / AIN[15] is also connected to Nordic* nRF51822 port P0_00. Make sure you keep this pin floating and do not define it as output.

1.3.10.2 GPIO/ AON/ INT mapping module to SoC

Table 1-13 shows the GPIO pins that are directly connected from the Intel® Curie™ module to the Intel® Quark™ SE microcontroller.

Please note that only AON pins and timers can wake the module from sleep. See Section 1.3.8, "Wake-capable interrupt pins".

Table 1-13. GPIO/ AON/ INT

Intel® Curie™ Module Ball No.	Intel® Curie™ Module Ball Name	Intel® Quark™ SE Microcontroller C1000 Signal	Intel® Quark™ SE Microcontroller C1000 Pin
C24	AIN[14]	GPIO_SS[6]	F1
F21	ATP_INT3	GPIO_AON3	F9
F22	ATP_INT0	GPIO_AON0	G9
J2	AIN[10]	GPIO_SS[2]	K5
H21	AIN[11]	GPIO_SS[3]	G1
H2	AIN[12]	GPIO_SS[4]	J4
L2	AIN[13]	GPIO_SS[5]	G2
L3	ATP_INT2	GPIO_AON2	E12
N3	ATP_INT1	GPIO_AON1	E11

1.3.10.3 GPIO multifunction mapping

GPIO pins can be configured for primary or alternate functions. Table 1-14 provides the mapping for the multiple functions each pin can be used for.

Table 1-14. GPIO/ multifunction lines

Intel® Curie™ Module Ball No.	Primary Function	Alternate Function 1	Alternate Function 2
A3	12S_RXD	GPIO[15]	-
A4	SPI0_M_CS1	GPIO[25]	-
B1	I2S_RWS	GPIO[17]	-
B2	I2S_RSCK	GPIO[16]	-
B3	SPI0_M_CS0	GPIO[24]	-
B21	SPI1_M_CS2	GPIO[13]	-
B22	SPI1_M_MISO	GPIO[9]	-
C1	I2S_TWS	GPIO[19]	-
C2	I2S_TSCK	GPIO[18]	-
C3	SPI0_M_CS2	GPIO[26]	-
C4	SPI0_M_SCK	GPIO[21]	-
C21	SPI1_M_SCK	GPIO[8]	-
C22	SPI1_M_CS3	GPIO[14]	-
D1	I2S_TXD	GPIO[20]	-
D3	SPI0_M_MOSI	GPIO[23]	-
D4	SPI0_M_MISO	GPIO[22]	-

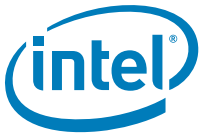


Table 1-14. GPIO/ multifunction lines (continued)

Intel® Curie™ Module Ball No.	Primary Function	Alternate Function 1	Alternate Function 2
D21	SPI1_M_CS1	GPIO[12]	-
D22	SPI1_M_CS0	GPIO[11]	-
E3	PLT_CLK[0]	GPIO_SS[14]	-
E4	SPI_S_CLK	GPIO[2]	AIN[2]
E22	SPI1_M_MOSI	GPIO[10]	-
F2	PWM3_out	GPIO_SS[13]	-
F3	SPI_S_CS_B	GPIO[0]	AIN[0]
F4	SPI_S_MOSI_B	GPIO[3]	AIN[3]
G1	PWM2_out	GPIO_SS[12]	-
G2	PWM1_out	GPIO_SS[11]	-
G3	SPI_S_MISO	GPIO[1]	AIN[1]
G4	SPI0_SS_CS3	GPIO[30]	-
H1	PWM0_out	GPIO_SS[10]	-
J21	UART1_TX	GPIO_SS[8]	AIN[16]
J22	UART1_CTS_B	GPIO_SS[0]	AIN[8]
K3	SPI0_SS_CS2	GPIO[29]	-
K21	UART1_RTS_B	GPIO_SS[1]	AIN[9]
K22	UART1_RX	GPIO_SS[9]	AIN[17]

1.3.10.4 Internal GPIO mapping

Table 1-15 documents the internal GPIO signals within the Intel® Curie™ module.

Some application software can be designed using SW_FG_VBAT to interrupt the Intel® Quark™ SE microcontroller to control the application external battery charging / protection circuit in addition to the battery charger internal resources. The Intel® Quark™ SE microcontroller can monitor the voltages and send signals to the application circuit to turn on and off the supply voltage (VIN) to the charger circuit.

BLE_SW_CLK signal has a 22 kohm internal pull-down resistor to keep it from floating.

BLE_SWDIO signal has a 22 kohm internal pull-up resistor to keep it from floating.

BLE_SW_CLK and BLE_SWDIO are used with the J-Link emulator to program or debug the Bluetooth® low energy controller. It is also connected to the Intel® Quark™ SE microcontroller for the software to implement the debugging function and programming capability if required by the application.