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TFA9879

Mono BTL class-D audio amplifier for portable applications with digital input

Rev. 02 — 15 October 2010 Product data sheet

1. Introduction

The TFA9879 is a high-efficiency filter-free mono class-D audio amplifier with two separate digital inputs for mobile applications.

2. General description

The TFA9879 contains a processor that supports a range of sound processing features including a 5-band parametric equalizer, separate bass and treble control, a dynamic range compressor, soft clip control and volume control. Excellent audio performance combined with high Power Supply Rejection Ratio (PSRR) is achieved through the use of a closed loop configuration.

Two independent digital audio inputs (I^2S-bus / PCM / IOM2) are available for connecting both a baseband and a multimedia processor.

The TFA9879 is available in a HVQFN24 package.

3. Features and benefits

3.1 General features

- Closed loop amplifier for:
  - High power supply rejection ratio
  - Excellent audio performance
- Digital input for high RF immunity
- High efficiency for maximizing battery life
- Wide supply voltage range (fully operational from 2.5 V to 5.5 V)
- Delivers high output power into 4 Ω and 8 Ω load impedances
- Phase-Locked Loop (PLL); no system clock required
- Protection including diagnostics via I^2C-bus:
  - OverCurrent Protection (OCP) to protect against short circuits across the speaker, to the supply line or to ground
  - OverTemperature Protection (OTP)
  - Digital inputs protected with UnderFrequency Protection (UFP), OverFrequency Protection (OFP) and Invalid Bit-clock Protection (IBP)
- ‘Pop noise’ free at power-up/power down, during sample rate switching and when switching between digital inputs
- Four separate I^2C-bus addresses for multi-channel applications

- 1.8 V / 3.3 V tolerant digital inputs
- Only three external components required

3.2 Programmable Digital Sound Processor (DSP)

- Digital volume control (−70 dB to +24 dB)
- Digital parametric 5-band equalizer
- Bass and treble control (−18 dB to +18 dB)
- Dynamic range compressor:
  - Programmable attack and release levels
  - Programmable attack and release rates
- Soft and hard mute control
- Programmable DC blocking via high-pass filter
- Power limiter (0 dB to −124 dB in 0.5 dB steps)
- Zero crossing volume control
- Stereo-to-mono down-mix function

3.3 Interface format support for digital audio inputs

- I^2S formats (f_s = 8 kHz to 96 kHz):
  - Philips standard I^2S-bus
  - Japanese I^2S-bus MSB-justified
  - Sony I^2S-bus LSB-justified
- PCM / IOM2 formats (f_s = 8 kHz or f_s = 16 kHz):
  - Long frame sync
  - Short frame sync

4. Applications

- Mobile phones
- Portable Navigation Devices (PND)
- PDAs
- Notebooks
- Portable gaming devices
- MP3 and MP4 players

5. Quick reference data

Table 1. Quick reference data

All parameters are guaranteed for V_{DDD} = 1.8 V; V_{DDP} = 3.7 V; R_L = 8 Ω; L_L = 44 μH; f_i = 1 kHz; f_s = 48 kHz; clip control off; T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDP}	power supply voltage	on pin V_{DDP}		2.5	-	5.5	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		1.65	1.8	1.95	V
I_P	supply current	on pin V_{DDP}; Amplifier mode with load; soft mute on		-	5.7	-	mA
		on pin V_{DDP}; Power-down mode		-	-	20	μA
I_{DDD}	digital supply current	on pin V_{DDD}; Amplifier mode		-	1.2	-	mA
		on pin V_{DDD}; Power-down mode	[1]	-	5	15	μA
$P_{o(RMS)}$	RMS output power	R_L = 8 Ω					
		THD + N = 1 %		0.65	0.7	-	W
		THD + N = 10 %		-	0.85	-	W
		R_L = 4 Ω					
		THD + N = 1 %		-	1.2	-	W
		THD + N = 10 %		-	1.5	-	W
		R_L = 8 Ω; V_{DDP} = 4.2 V					
		THD + N = 1 %		-	0.9	-	W
		THD + N = 10 %		-	1.1	-	W
		R_L = 4 Ω; V_{DDP} = 4.2 V					
		THD + N = 1 %		-	1.6	-	W
		THD + N = 10 %		-	1.95	-	W
		R_L = 8 Ω; V_{DDP} = 5.0 V					
		THD + N = 1 %		-	1.35	-	W
		THD + N = 10 %		-	1.6	-	W
		R_L = 4 Ω; V_{DDP} = 5.0 V					
		THD + N = 1 %		-	2.35	-	W
		THD + N = 10 %		-	2.75	-	W
η_{po}	output power efficiency	$P_{o(RMS)}$ = 850 mW		-	92	-	%

[1] After switching from Off/Amplifier mode to Power-down mode.

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9879HN	HVQFN24	plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm	SOT616_3

7. Block diagram

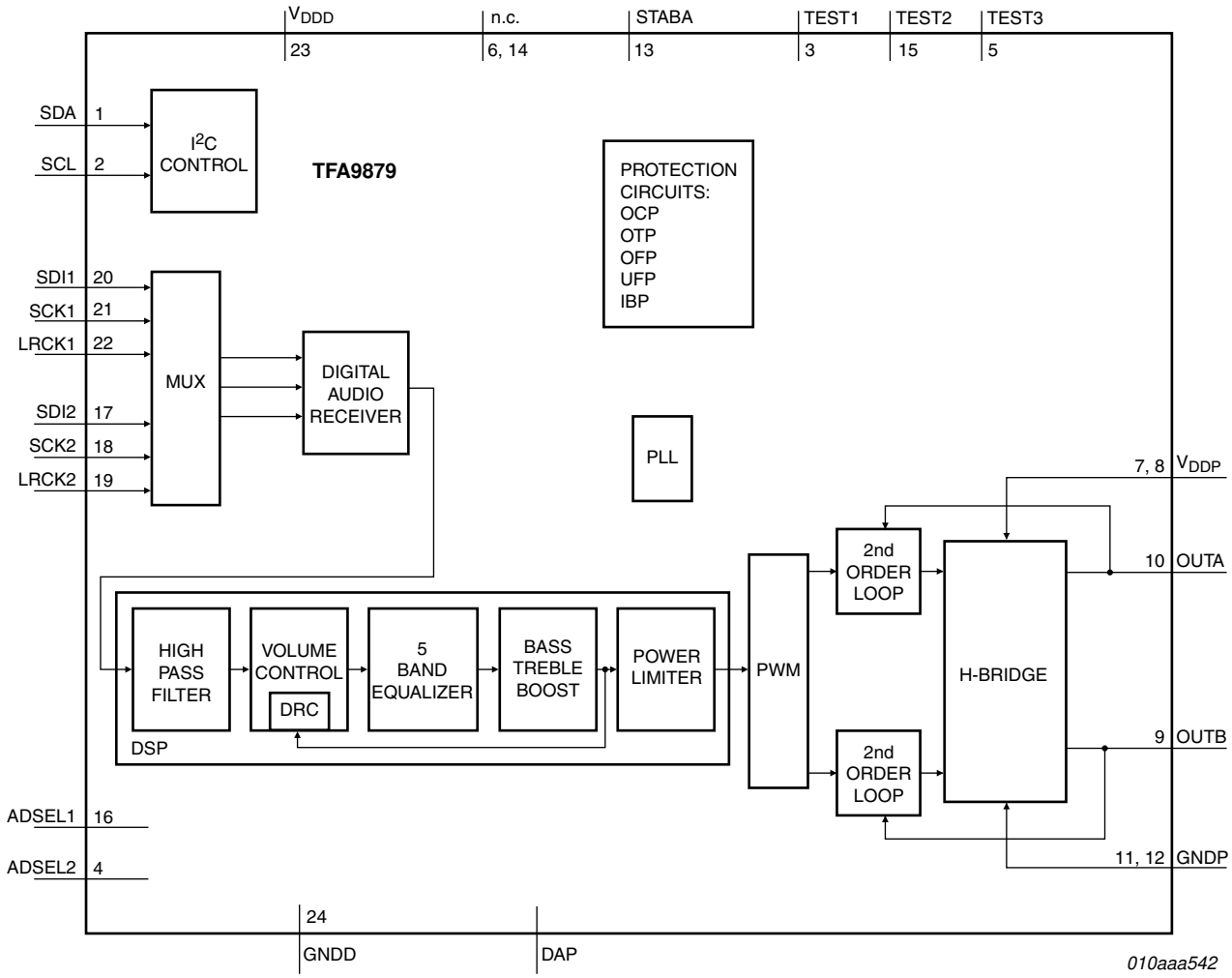
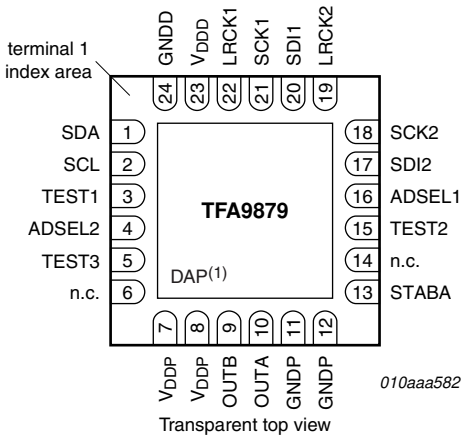


Fig 1. Block diagram

8. Pinning information

8.1 Pinning



(1) Exposed Die Attach Paddle (DAP)

Fig 2. Pin configuration

8.2 Pin description

Table 3. Pin description

Symbol	Pin	Pin Type	Description
SDA	1	IO	I²C-bus data input/output
SCL	2	I	I²C-bus bit clock input
TEST1	3	I	test signal input 1; for test purposes only; connect to PCB ground
ADSEL2	4	I	address selection input 2
TEST3	5	I	test signal input 3; for test purposes only; connect to PCB ground
n.c.	6	-	not connected; connect to PCB ground
V_{DDP}	7, 8	P	analog supply voltage (2.5 V to 5.5 V)
OUTB	9	O	output B (negative)
OUTA	10	O	output A (positive)
GNDP	11, 12	P	analog ground, PCB ground reference
STABA	13	O	1.8 V analog stabilizer output
n.c	14	-	not connected; connect to PCB ground
TEST2	15	I	test signal input 2; for test purposes only; connect to PCB ground
ADSEL1	16	I	address selection input 1
SDI2	17	I	digital audio data input 2
SCK2	18	I	digital audio bit clock input 2
LRCK2	19	I	digital audio word select input 2
SDI1	20	I	digital audio data input 1
SCK1	21	I	digital audio bit clock input 1
LRCK1	22	I	digital audio word select input 1

Table 3. Pin description *...continued*

Symbol	Pin	Pin Type	Description
V_{DDD}	23	P	digital supply voltage (1.8 V)
GNDD	24	P	digital ground, PCB ground reference
DAP	-	P	exposed Die Attached Paddle (DAP); connect to PCB ground

9. Functional description

The TFA9879 is a high-efficiency mono Bridge Tied Load (BTL) class-D amplifier with digital audio inputs. It supports all commonly used formats.

The key functional blocks of the TFA9879 are shown in Figure 1. In the digital domain, the audio signal is processed and converted into a Pulse Width Modulated (PWM) signal using a 3-level modulation. In the analog domain, the PWM signal is amplified using a second order feedback loop.

The audio signal-processing path is described below:

1. The MUX selects the serial interface input to be used.
2. The digital audio receiver translates the serial input signal into a standard internal mono audio stream.
3. The programmable high-pass filter blocks DC signals and low frequency signals.
4. The volume control provides both gain and attenuation functionality and can be adjusted by the user or dynamically via the Dynamic Range Compressor (DRC). The volume control can be used to adjust the signal level between −70 dB and +24 dB.
5. The 5-band parametric equalizer can be used to equalize the mono audio stream. It can be used for speaker transfer curve compensation to optimize the audio performance of the speakers.
6. The bass and treble boost function provides another way to adjust the sound.
7. The power limiter limits the maximum output signal of the TFA9879. The power limiter settings are 0 dB to −124 dB in steps of 0.5 dB. This function can be used to limit the maximum output power delivered to the speakers at a fixed supply voltage and speaker impedance.
8. The PWM controller block converts the audio signal into a 3-level modulated PWM signal. The 3-level modulation provides a high signal-to-noise performance and eliminates clock jitter noise.
9. The second order feedback loop ensures excellent audio performance and high power supply rejection ratio.
10. The H-BRIDGE allows the TFA9879 to deliver the required output power between terminals OUTA and OUTB.

The internal clocks of the TFA9879 are derived from the digital audio interface (SCK1 and SCK2) using a PLL. The reference input for the PLL is selected via the digital input MUX.

The audio signal path can be selected via the I^2C-bus interface.

The PLL block generates the system clock.

The following protection circuits are built into the TFA9879:

- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- UnderFrequency Protection (UFP)
- OverFrequency Protection (OFP)
- Invalid Bit-clock Protection (IBP)
- DC-blocking

9.1 Operating modes

The TFA9879 supports the following operating modes, which are controlled via the I^2C-bus interface:

- **Power-down mode**, used to switch off the device; current consumption is reduced to a minimum; the I^2C-bus remains operational; the PWM outputs are disabled.
- **Off mode**, in which the class-D amplifier is switched off; the TFA9879 is completely biased and the PWM outputs are disabled.
- **Amplifier mode,** in which the digital inputs are used to generate a signal between OUTA and OUTB.

The TFA9879 device control settings are detailed in Table 21.

9.1.1 Power-up/power-down

The power-up and power-down timing of the TFA9879 is illustrated in Figure 3. The external power supply levels, V_{DDP} and V_{DDD}, should be within the specified operating ranges before the operating mode is selected. Bit POWERUP in the Device control register (Table 21) must be set to 1 before the operating mode can be selected via bits OPMODE. After the turn-on delay ($t_{d(on)}$), the device automatically generates a soft un-mute function. A soft mute function is generated when OPMODE is set to 0. The TFA9879 should be set to Power-down mode before the power supplies are disconnected or turned off.

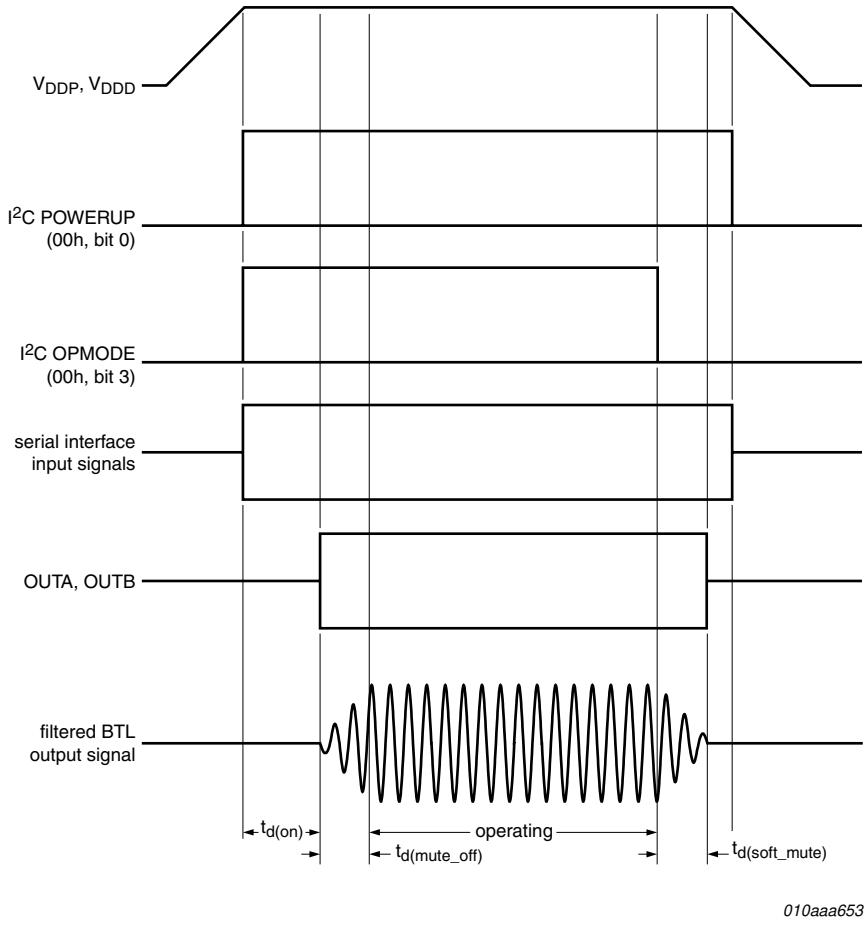


Fig 3. Power-up/power-down timing

9.1.2 Supported Digital audio data formats

The TFA9879 supports a commonly used range of I²S, PCM and IOM2 digital audio data formats. The I²S formats, selected via bits I2S_SET in the Serial interface control register (Table 22), are listed in Table 4. The PCM/IOM2 formats are listed in Table 5. The TFA9879 automatically detects the number of slots by measuring the ratio between the sync frequency (8 kHz) and the data clock. Table 24 details the I²C settings for the PCM/IOM2 formats.

Table 4. I²S-supported digital audio data formats

SCK frequency	Interface format (MSB first)	Supported data format
32 f_s	I²S (Philips) standard	up to 16-bit data
32 f_s	MSB-justified	up to 16-bit data
32 f_s	LSB-justified - 16 bits	16-bit data
64 f_s	I²S (Philips) standard	up to 24-bit data
64 f_s	MSB-justified	up to 24-bit data
64 f_s	LSB-justified - 16 bits	16-bit data
64 f_s	LSB-justified - 18 bits	18-bit data
64 f_s	LSB-justified - 20 bits	20-bit data
64 f_s	LSB-justified - 24 bits	24-bit data

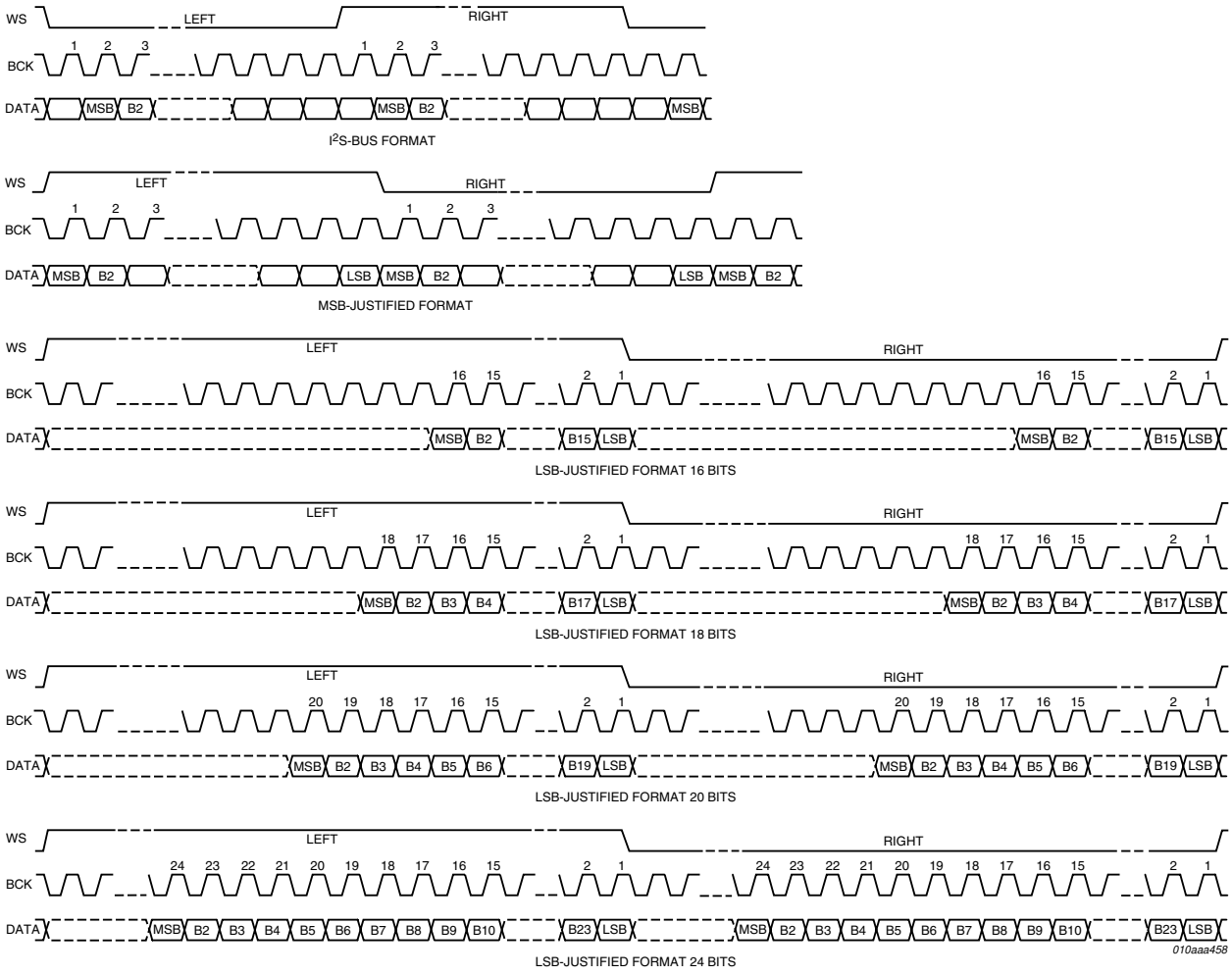


Fig 4. I²S-supported digital audio data formats

Table 5. PCM/IOM2-supported audio data formats

Number of slots	f_s (kHz)	Sync frequency (kHz) on LRCK pin	Supported data formats	Data clock (kHz) on SCK pin
2	8 or 16	8	8-bit data	128
2	8 or 16	8	8-bit data	128
4	8 or 16	8	8-bit data	256
4	8 or 16	8	8-bit data	256
6	8 or 16	8	8-bit data	384
8	8 or 16	8	8-bit data	512
12	8 or 16	8	8-bit data	768
16	8 or 16	8	8-bit data	1024
reserved				
2	8 or 16	8	16-bit data	256
3	8 or 16	8	16-bit data	384
4	8 or 16	8	16-bit data	512
6	8 or 16	8	16-bit data	768
8	8 or 16	8	16-bit data	1024
12	8 or 16	8	16-bit data	1536
12	8 or 16	8	16-bit data	1536

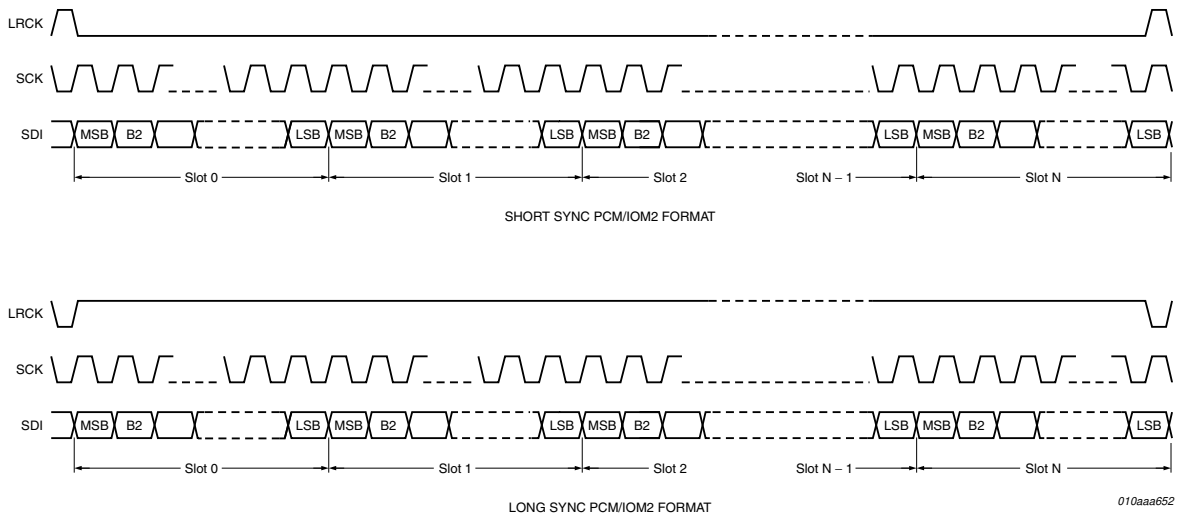


Fig 5. PCM/IOM2-supported digital audio data formats

9.2 Digital Signal Processor (DSP) features

9.2.1 Serial interface selection

The TFA9879 contains two serial interfaces. The active interface is selected via bit INPUT_SEL in the Device control register (see Table 21). When this bit is toggled, the following sequence is initiated:

- Soft mute is activated for $128/f_s$ seconds
- The TFA9879 switches to Off mode and the serial interface input is toggled
- The TFA9879 switches back to Operating mode and soft mute is released

9.2.2 Mono selection

Mono selection is used to select the digital audio input channel to be amplified. The options are:

- Left channel
- Right channel
- Left + right channels (sum divided by two)

Separate Mono selection is provided for the two serial interfaces via bits MONO_SEL in the Serial interface control registers (addresses 01h and 03h; see Table 22).

9.2.3 Programmable high-pass filter

The TFA9879 features a first-order high-pass filter on the digital audio input to block DC and low frequency signals. DC values at the output can damage the speaker.

The high-pass filter cut-off frequency is determined by:

- The high-pass filter control setting (bits HP_CTRL, see Table 30)
- The sample frequency, f_s

The relationship between these parameters and the cut-off frequency is defined in Equation 1:

$$f_{high(-3dB)} = \frac{-f_s \times ln\left(\frac{4096 - HP\_CTRL}{4096}\right)}{2\pi} \quad (1)$$

HP_CTRL can be programmed to any integer value between 0 and 511 (see Table 30). The high-pass filter is bypassed if HP_CTRL = 0 or bit HPF_BP in the Bypass control register is set to 1 (see Table 27).

9.2.4 De-emphasis

Digital de-emphasis is sometimes needed, especially with older recordings. Emphasis and de-emphasis originate in the FM transmission, in which the Signal-to-Noise Ratio (SNR) is not flat over the signal band (in fact the SNR gets worse as the signal frequency increases). To achieve good SNR over the complete audio band, the high frequency components of the audio signal were amplified prior to transmission (this is called Emphasis).

The de-emphasis filter is a simple first order filter. The cut-off frequency of the de-emphasis low-pass filter is approximately 3.5 kHz. The TFA9879 de-emphasis filter is supported for four sample frequencies, as detailed in Table 6.

Table 6. De-emphasis control

[1:0] Control value[1]	f_s (kHz)
00[2]	de-emphasis inactive
01	32
10	44.1
11	48

[1] Value selected via bits DE_PHAS in the De-emphasis, soft/hard mute and power limiter control register (see Table 32).

[2] Default value.

9.2.5 Equalizer

The equalizer can be used for speaker curve compensation or for customer equalizer settings, such as jazz, pop, rock or classical music. The equalizer function can be bypassed or configured as 5-band.

9.2.5.1 Equalizer band function

The shape of each parametric equalizer band is determined by the following three filter parameters:

- (Relative) center frequency $\omega = 2\pi(f_c/f_s)$
- Quality factor Q
- Gain factor G

In the above equation, f_c is the center frequency and f_s is the sample frequency.

The definition of the quality factor is the center frequency divided by the 3 dB bandwidth (see Equation 2). In parametric equalizers this is only valid when the gain is set very low (−30 dB).

$$Q = \frac{f_c}{f_2 - f_1}; \quad \begin{aligned} f_1: \quad & 20log_{10}\left(\frac{A_{f_1}}{A_{f_c}}\right) = 3\text{dB} \quad f_c > f_1 \\ f_2: \quad & 20log_{10}\left(\frac{A_{f_2}}{A_{f_c}}\right) = 3\text{dB} \quad f_2 > f_c \end{aligned} \tag{2}$$

Each band filter can be programmed to perform a band-suppression (G < 1) or a band-amplification (G > 1) function around the center frequency.

Each band of the TFA9879 equalizer has a second order Regalia-Mitra all-pass filter structure. The structure is shown in Figure 6.

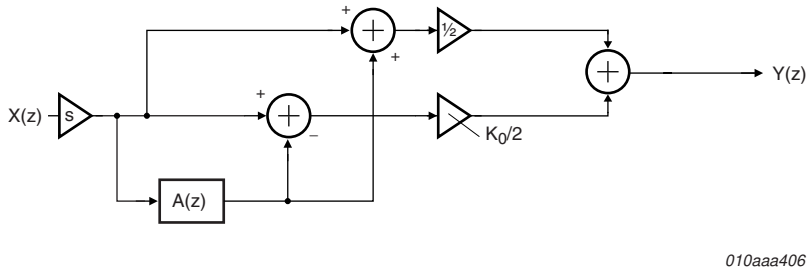


Fig 6. Regalia-Mitra filter flow diagram

The transfer function of this all-pass filter is given in Equation 3:

$$H(z) = 1/2 \cdot (1 + A(z)) + K_0/2 \cdot (1 - A(z)) \quad (3)$$

A(z) is the second order filter structure. The transfer function of A(z) is given in Equation 4:

$$A(z) = \frac{K_1 + K_2 \cdot (1 + K_1) \cdot Z^{-1} + Z^{-2}}{1 + K_2 \cdot (1 + K_1) \cdot Z^{-1} + K_1 \cdot Z^{-2}} \quad (4)$$

Z^{-1} equals one f_s delay period. The relationship between the programmable parameters K_0, K_1 and K_2 and the filter parameters G, ω and Q is shown in Equation 5 and Equation 6.

Equation 5 can be used to calculate band suppression (G < 1) functions.

$$\left.\begin{aligned} K_0 &= G \\ K_1 &= -\cos\omega \\ K_2 &= (2Q \cdot G - \sin\omega)/(2Q \cdot G + \sin\omega) \end{aligned}\right|_{G<1} \quad (5)$$

Equation 6 can be used to calculate band amplification (G ≥ 1) functions.

$$\left.\begin{aligned} K_0 &= G \\ K_1 &= -\cos\omega \\ K_2 &= (2Q - \sin\omega)/(2Q + \sin\omega) \end{aligned}\right|_{G \geq 1} \quad (6)$$

The ranges of the parametric equalizer settings for each band are:

- The gain, G, is from –30 dB to +12 dB.
- The center frequency, f_c, is from 0.0004 ´ f_s to 0.49 ´ f_s.
- The quality factor, Q, is from 0.001 to 8.

Filter coefficients need to be entered for each filter stage via the I²C-bus interface to configure the filters (see Section 10.4.3).

Figure 7, Figure 8 and Figure 9 illustrate some possible equalizer band transfer functions. The relationships are symmetrical for the suppression and amplification functions. A skewing effect can be observed at higher frequencies.

For optimum numerical noise performance, different configurations are available for a given filter transfer function. The binary filter configuration parameters t_1 and t_2 control the actual configuration and should be chosen according to Equation 7.

$$t_1 = \begin{cases} 0 & K_1 \leq 0 \\ 1 & K_1 > 0 \end{cases}$$
$$t_2 = \begin{cases} 0 & K_2 \geq 0 \\ 1 & K_2 < 0 \end{cases} \quad (7)$$

A maximum of 12 dB amplification, with respect to the input signal, can be achieved per equalizer stage. The equalizer band signals are processed in sequence, from the highest (Band A) to the lowest (Band E). Each band can attenuate the signal by 6 dB so, in order to prevent numerical clipping at filter settings of over 6 dB amplification, band filters can be scaled by 0 dB or −6 dB. For optimum numerical noise performance, steps of −6 dB amplification should be applied to the bands in sequence, starting with B and A, as long as they are able to amplify the signal without clipping.

A filter scale factor, s, is associated with each of the equalizer bands and is set via the relevant EQx_s control bit (see Table 25).

Table 7. Equalizer filter scale factor settings

s	scale factor (dB)
0	0
1	−6

9.2.5.2 Equalizer band control

For compact representation with positive signed parameters, parameters k_1' and k_2' are introduced in Equation 8.

$$k_0' = K_0$$
$$k_1' = \begin{cases} 1 - K_1 & t_1 = 0 \\ 1 + K_1 & t_1 = 1 \end{cases}$$
$$k_2' = \begin{cases} 1 - K_2 & t_2 = 0 \\ 1 + K_2 & t_2 = 1 \end{cases} \quad (8)$$

Parameters K_0, k_1', k_2', t_1, t_2 and s must be combined in two 16-bit control words, word1 and word2 (see Table 24 and Table 25), using the format shown in Table 8. Parameters k_1' and k_2' are unsigned floating-point representations in Equation 8.

$$k_x' = M \cdot 2^{-E}\Big|_{M<1} \quad (9)$$

In Equation 9, M is the unsigned mantissa and E the negative signed exponent. For example, in word2 bits [14:8] = [0111 010] represent $k_2' = (7/2^4) \times 2^{-2} = 1.09375 \times 10^{-1}$.

Table 8. Equalizer control word construction

Word	Section	Data
word1	15	t_1
word1	[14:4]	11 mantissa bits of k_1'
word1	[3:0]	four exponent bits of k_1'
word2	15	t_2
word2	[14:11]	four mantissa bits of k_2'
word2	[10:8]	three exponent bits of k_2'
word2	[7:1]	k_0'
word2	0	s

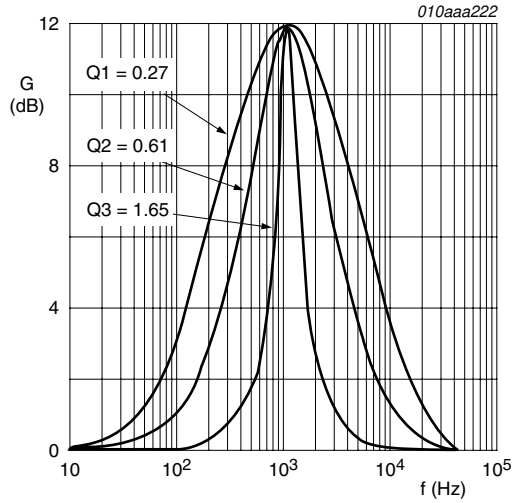


Fig 7. Transfer functions for selected values of Q, the quality factor

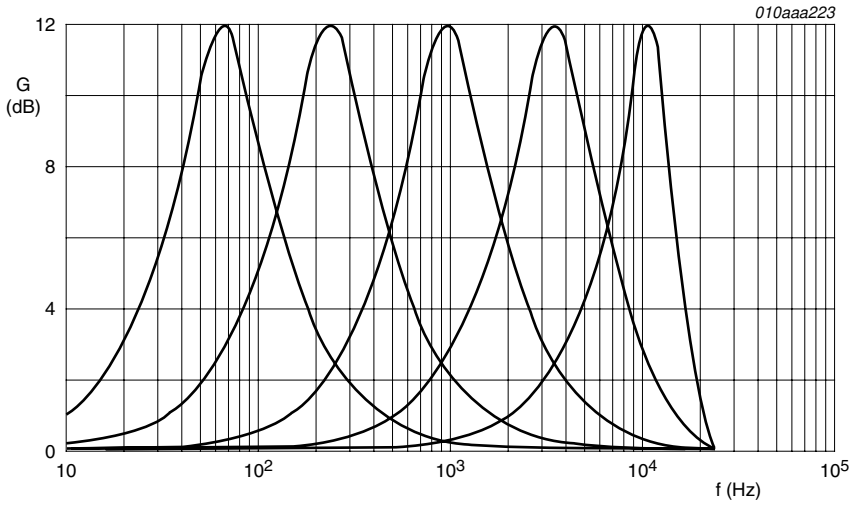


Fig 8. Transfer functions for selected values of f_c, the center frequency

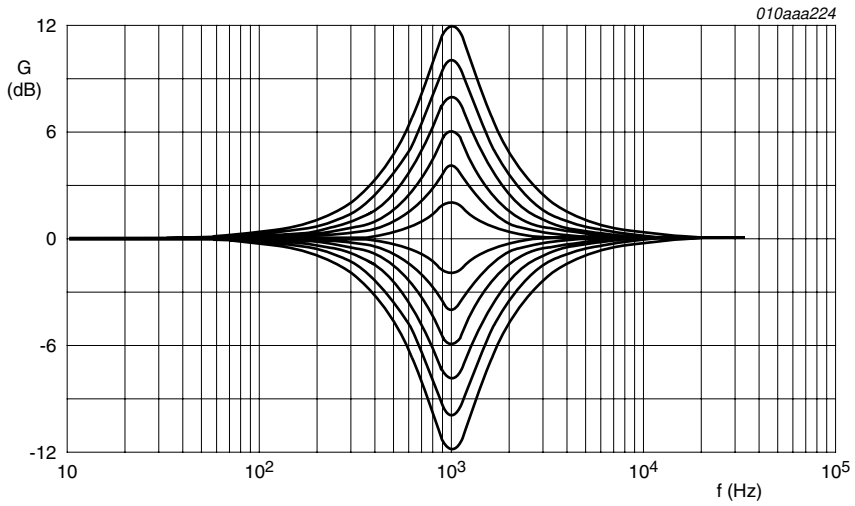


Fig 9. Transfer functions for selected values of G, the gain factor

9.2.6 Bass and treble control

The TFA9879 contains first order shelving filters for bass and treble control. The device can attenuate or boost the bass and high frequency signals independently in 2 dB steps within a −18 dB to +18 dB range. Attenuation and boosting are dependent on the audio signal zero crossing settings (see Section 9.2.9 for further details). The bass and treble corner frequencies are adjustable.

The bass and treble corner frequencies, as a function of the I^2C control settings and the sample rate, are given in Table 9.

Table 9. Corner frequency settings for bass and treble control

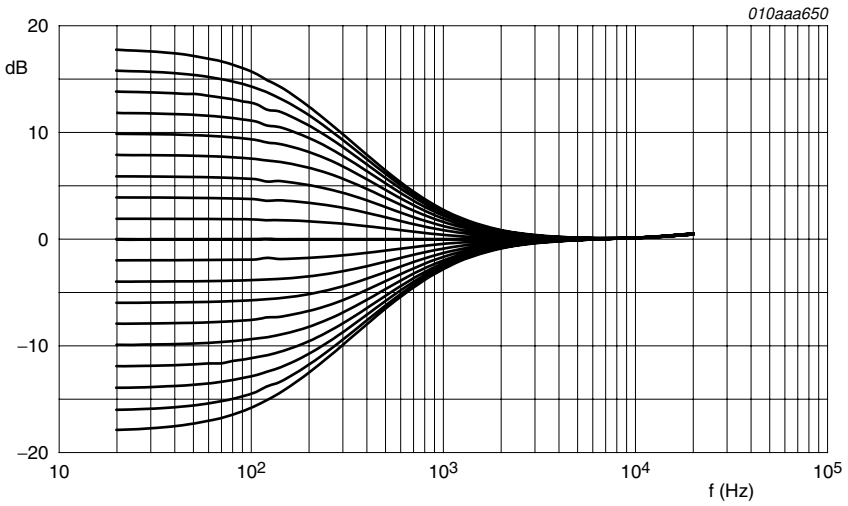
Control value	f_s (kHz)	Corner frequency (Hz)	
		Bass[1]	Treble[2]
00	8, 16, 32, 64	181	1090
	11.025, 22.05, 44.1, 88.2	250	1500
	12, 24, 48, 96	272	1630
01[3]	8, 16, 32, 64	218	2180
	11.025, 22.05, 44.1, 88.2	300	3000
	12, 24, 48, 96	326	3260
10	8, 16, 32, 64	300	3000
	11.025, 22.05, 44.1, 88.2	413	4130
	12, 24, 48, 96	450	4500
11	reserved		

[1] Value selected via bits F_BASS in the Bass and treble control register (see Table 29).

[2] Value selected via bits F_TREBLE in the Bass and treble control register (see Table 29).

[3] Default value.

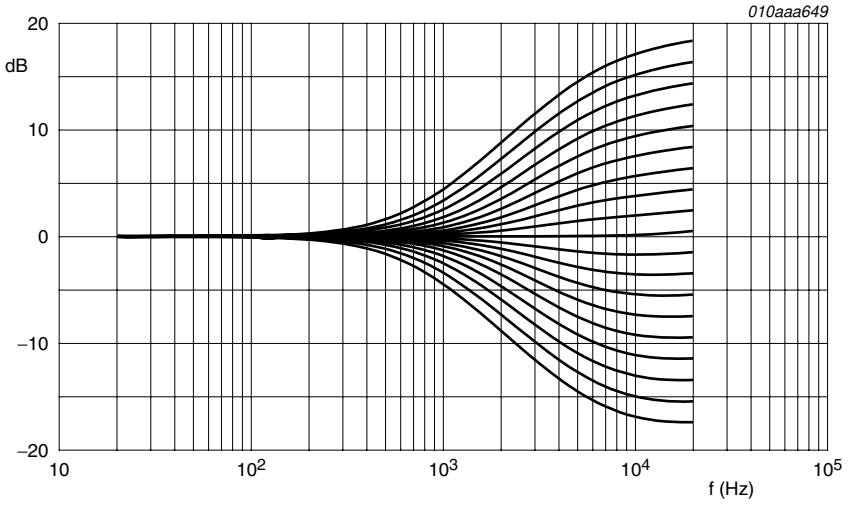
Figure 10 shows the bass function for a range of attenuation and boost settings with a sample rate of 48 kHz and a corner frequency of 272 Hz.



V_{DDP} = 3.7 V, 2 × 8 Ω BTL configuration, treble control = 0 dB, clip control on

Fig 10. Bass function in 2 dB steps; the treble control is set to flat

Figure 11 shows the treble function for a range of attenuation and boost settings with a sample rate of 48 kHz and a corner frequency of 1630 Hz.



V_{DDP} = 3.7 V, 2 × 8 Ω BTL configuration, bass control = 0 dB, clip control on

Fig 11. Treble function in 2 dB steps; the bass control is set to flat

9.2.7 Muting

The TFA9879 support two muting options, which are controlled via the I²C-bus interface:

- Soft muting
- Hard muting

Soft muting prevents audible pops. The function smoothly reduces the gain setting of the audio channel to the mute level according to a raised cosine shape. Soft muting is performed in 128 / f_s steps. Soft de-mute results in a similar gain increase. Bit S_MUTE in Table 32 enables and disables the soft mute function.

The hard mute function immediately switches the outputs to 50 % duty-cycle pulses. As a result, the input signals are abruptly blocked. Hard mute takes priority over soft mute. Hard mute is enabled and disabled via bit H_MUTE in Table 32.

9.2.8 Digital volume control

The digital volume control has a range of −70 dB to + 24 dB, programmable in 0.5 dB steps. The default setting is mute (0 × BD). Attenuation and boosting behavior is affected by the zero crossing volume setting (see Section 9.2.9 for further details).

The volume control settings, and the resulting amplification or suppression factors, are detailed in Table 10.

Table 10. Volume control amplification and suppression

Control value[1]	Gain (dB)
00h	+24
01h	+23.5
.. ....	steps of 0.5 dB
BBh	−69.5
BCh	−70
BDh[2]	mute
.. ....	mute
FFh	mute

[1] Control value is selected via bits VOL in the Volume control register (see Table 31).

[2] Default value.

9.2.9 Zero-crossing volume control

The TFA9879 employs zero-crossing volume control to minimize pop noise when the volume or bass/treble control is changing.

When zero-crossing volume control is enabled (ZR_CRSS = 1; see Table 31), the TFA9879 increases or decreases the gain only when the audio signal passes a zero crossing.

9.2.10 Dynamic Range Compressor (DRC)

The TFA9879 provides a DRC to automatically adjust power levels according to programmable attack and release levels. The attack level is related to the peak value of the signal; the release level is related to the RMS value of the signal. The attack level is programmable using 16 available levels in the range −12 dB to +10 dB. The release level is programmable using 16 available levels in the range −29 dB to 0 dB relative to the attack level. The signal level is measured after Equalizer, Bass and Treble processing, but before it reaches the power limiter.

The DRC can be bypassed via bit DRC_BP in Table 27.

9.2.10.1 Functional description

The DRC compresses the dynamic range of the audio stream. The volume control, equalizer or bass/treble controls can be set so that the audio stream exceeds the 0 dBFs clip level. The DRC can be programmed to compress the louder audio content when this occurs, while quieter sounds remain unaffected, i.e. the DRC soft clips the audio stream. This is useful when background noise overpowers quiet audio passages. Increasing the volume using the volume control can make quiet audio passages audible but can cause louder audio passages to be distorted by clipping. The DRC prevents this distortion happening by reducing the volume during loud audio passages and increasing it again for quiet passages.

The design of the DRC feedback loop, incorporating the equalizer and bass and treble controls, is illustrated in Figure 12.

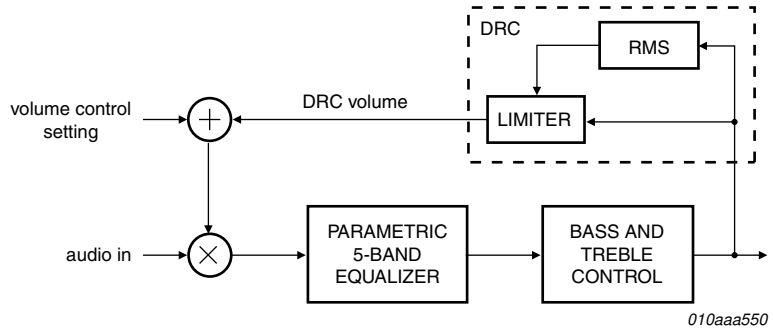


Fig 12. DRC feedback design

9.2.10.2 DRC control

The DRC has four programmable control settings:

- Attack level
- Attack rate
- Release level
- Release rate

The DRC reduces the volume when the audio signal level exceeds the attack level. The attack level is based on the audio peak value. When the audio signal level drops below the attack level, the DRC stops reducing the volume. The rate of decrease is programmable via the attack rate. The DRC increases the audio signal level again when it drops below the release level. This level is based on the audio RMS-value and is related to the attack level. The rate of increase is programmable via the release level. The DRC stops increasing the volume when the audio signal level reaches the release level or the DRC volume falls to 0 dB.

Figure 13 shows the attack and release behavior of the DRC.

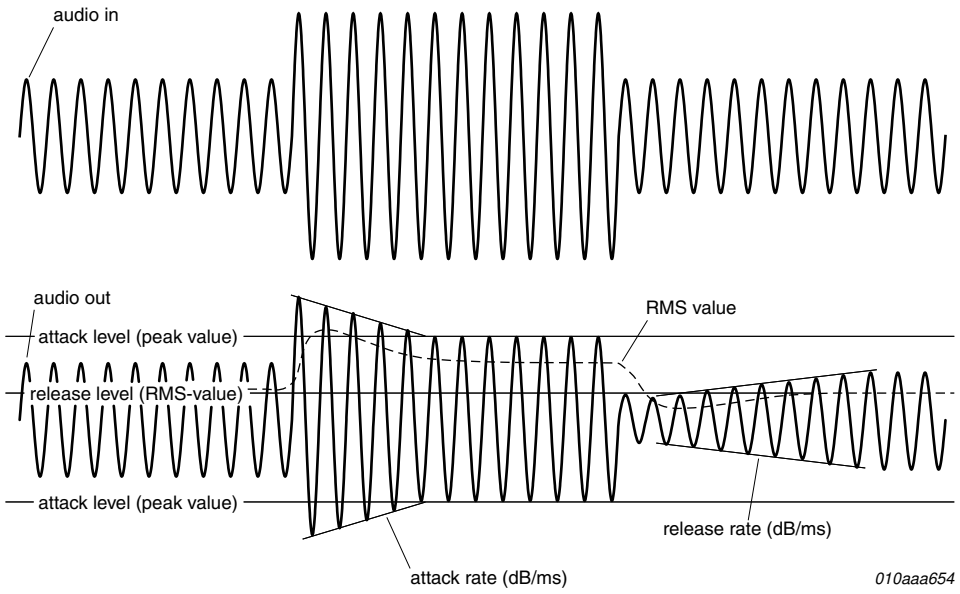


Fig 13. DRC attack and release behavior

Table 11. DRC attack and release levels

Control value: attack level[1]	Attack level based on peak value; absolute value (dBFS)	Control value: release level[2]	Release level based on RMS value (relative to the attack level[3]) (dB)
0000	−12	0000	−29
0001	−10	0001	−26
0010	−8	0010	−23
0011	−6	0011	−20
0100	−5	0100	−18
0101	−4	0101	−16
0110	−3	0110	−14
0111	−2	0111	−12
1000	−1	1000	−10
1001[4]	0	1001	−8
1010	1	1010	−6
1011	2	1011[4]	−4
1100	4	1100	−3
1101	6	1101	−2
1110	8	1110	−1
1111	10	1111	0

[1] The control value is selected via bits AT_LVL in the DRC control register (see Table 28).

[2] The control value is selected via bits RL_LVL in the DRC control register (see Table 28).

[3] 0 dB (RMS) release level equals 0 dB (peak) attack level.

[4] Default value.

Table 12. DRC attack and release rates

Control value: attack rate[1]	Attack rate (dB/ms)	Control value: release rate[2]	Release rate (dB/ms)
0000	3	0000	0.5
0001	2.7	0001	0.137
0010[3]	2.25	0010	0.075
0011	1.8	0011	0.05
0100	1.35	0100	0.036
0101	0.9	0101	0.03
0110	0.45	0110	0.026
0111	0.225	0111	0.021
1000	0.15	1000	0.020
1001	0.11	1001	0.017
1010	0.09	1010[3]	0.015
1011	0.075	1011	0.014
1100	0.065	1100	0.013
1101	0.06	1101	0.012
1110	0.055	1110	0.011
1111	0.05	1111	0.01

[1] The control value is selected via bits AT_RATE in the DRC control register (see Table 28).

[2] The control value is selected via bits RL_RATE in the DRC control register (see Table 28).

[3] Default value.

9.2.11 Power limiter

The power limiter controls the maximum output voltage in Amplifier mode. This feature makes it possible to limit the output voltage across a peripheral (speaker) when necessary.

The TFA9879 output voltage is dependent on:

- The analog supply voltage on pin V_{DDP}
- The gain of the power limiter (G)
- The power limiter input signal (X_i)

The bass/treble output signal is connected to the power limiter input and is relative to the Fraction of Full Scale (FFS), from −1 to +1.

Equation 10 shows the relationship between these settings and the output voltage between pins OUTA and OUTB in the audio bandwidth:

$$V_o = \begin{cases} X_i \times G \times 5.91 & X_i \times G \times 5.91 < V_{DDP} \\ V_{DDP} & X_I \times G \times 5.91 \geq V_{DDP} \end{cases} \text{(V)} \quad (10)$$

Equation 10 only applies with no load and with clip control off (see Section 9.3). Clip control and the R_{DSon} of the power switches reduce the maximum clipped output signal. The power limiter gain can be reduced in 249 steps of 0.5 dB in the range 0 dB to −124 dB.

The maximum peak output voltage for the first ten power limiter gain settings is given in Table 13.

Table 13. Power limiter control settings

All parameters are guaranteed for V_{DDP} = 5 V; no load; f_i = 1 kHz; f_s = 48 kHz; clip control off; T_{amb} = 25 °C unless otherwise specified.

Control value[1]	Power limiter gain (dB)	Maximum peak output voltage (V)
00h[2]	0.0	V_{DDP}
01h	−0.5	V_{DDP}
02h	−1.0	V_{DDP}
03h	−1.5	V_{DDP}
04h	−2.0	4.7
05h	−2.5	4.4
06h	−3.0	4.2
07h	−3.5	4.0
08h	−4.0	3.7
09h	−4.5	3.5

[1] The control value is selected via bits P_LIM in the De-emphasis, soft/hard mute and power limiter control register (see Table 32).

[2] Default value.

9.3 Class-D amplification and clip control

A fourth order sigma delta PWM converter converts the digital audio streams into 3-level modulated PWM signals. The analog back end amplifies the two PWM signals in a BTL configuration with complementary output stages.

One of two clip control configurations can be selected:

- Smooth clipping, clip control on
- Maximum power, clip control off

If smooth clipping is selected (CLIPCTRL = 0; see Table 27), the clipping behavior will have no artefacts. To obtain the maximum possible output power, the device can be set to maximum power.

The PWM frequency is related to the I^2S input sample rate as detailed in Table 4.

Table 14. Power limiter control settings

PWM frequency (kHz)	Sample rate (kHz)	SCK relative to sample rate
256	8, 16, 32, 64	32 ×, 64 ×
352.8	11.025, 22.05, 44.1, 88.2	32 ×, 64 ×
384	12, 24, 48, 96	32 ×, 64 ×

9.4 Protection

The TFA9879 incorporates a wide range of protection circuits to facilitate optimal and safe application.

The following protection circuits are included in the TFA9879:

- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- UnderFrequency Protection (UFP)
- OverFrequency Protection (OFP)
- Invalid Bit-clock Protection (IBP)
- DC-blocking via high-pass filter (see Section 9.2.3)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

9.4.1 OverTemperature Protection (OTP)

This is a 'hard' protection to prevent heat damage to the TFA9879. Overtemperature protection is triggered when the junction temperature exceeds 130 °C. When this happens, the output stages are set floating. OTP can be cleared automatically via a programmable timer or via the I²C-bus interface, after which the output stages will start to operate normally again. The programmable timer settings, selected via bits L_OTP in the Bypass control register (Table 27), are:

- 4.5 μs
- 100 ms
- 1 s

OTP can also be set to no recovery. Setting the TFA9879 to Off mode and subsequently to Amplifier mode clears the OTP when no recovery is selected.

9.4.2 OverCurrent Protection (OCP)

The output current of the class-D amplifiers is current limited. When an output stage exceeds a current in the range 1.3 A to 2.3 A, the output stages are set floating. OCP can be cleared automatically via a programmable timer or via the I²C-bus interface, after which the output stages will start to operate normally again. The programmable timer settings, selected via bits L_OCP in the Bypass control register (Table 27), are:

- 4.5 μs
- 27.5 μs
- 10 ms

The OCP can also be set to no recovery. Setting the TFA9879 to Off mode and subsequently to Amplifier mode clears the OCP when no recovery is selected.

9.4.3 UnderFrequency Protection (UFP)

UFP sets the output stages floating when the clock input source is too low ($< f_{UFP}$). This can happen if, for example, the selected sample frequency (bits I2S_FS in Table 22) is not in line with the applied sample rate. The PWM switching frequency can become critically low when the frequency of the input clock is lower than the selected sample frequency. Without UFP, peripheral devices in an application might be damaged.

The UFP status can be monitored by polling the I²C status register (Table 33). The alarm will be raised when the input sample rate is too low.

9.4.4 OverFrequency Protection (OFP)

OFP sets the output stages floating when the clock input source is too high (>f_{OFP}). This can happen if, for example, the selected sample frequency (bits I2S_FS in Table 22) is not in line with the applied sample rate. The PWM controller can become unstable when the frequency of the input clock is higher than the selected sample frequency. Without OFP, peripheral devices in an application might be damaged.

The OFP status can be monitored by polling the I²C status register (Table 33). The alarm will be raised when the input sample rate is too high.

9.4.5 Invalid Bit-clock Protection (IBP)

If the SCK-to-LRCK ratio is not supported, the audio signal will be distorted. This occurs because the sound processing blocks will be operating at frequencies out of synchronization with the sample rate.

IBP prevents this happening by shutting down the TFA9879 if the IBP alarm is raised for the selected channel. This will disconnect the digital audio path.

Valid SCK-to-LRCK ratios for PCM interface formats are 16, 32, 48, 64, 96, 128 and 192. For I²S interface formats, valid SCK-to-LRCK ratios are 32 and 64.

9.4.6 Overview of protection circuits

Table 15 provides an overview of the protection circuits implemented.

Table 15. Overview of protection circuits

Protection circuits				
Symbol	**Conditions**	**I²C flag**	**Output**	**Recovery**
OTP	T_j > 130 °C	OTP	floating	automatic when timer set to 4.5 µs, 100 ms or 1 s (via bits L_OTP in Table 27) and T_j < 130 °C; via I²C-bus when no recovery is selected
OCP	$I_O > I_{O(ocp)}$	OCP	floating	automatic when timer set to 4.5 µs, 27.5 µs or 10 µs (via bits L_OCP in Table 27) and $I_O < I_{O(ocp)}$; via I²C-bus when no recovery is selected
UFP	PWM frequency < 96 kHz	UFP	floating	restart (fault to operating when PWM frequency > 96 kHz)
OFP	PWM frequency > 1031 kHz	OFP	floating	restart (fault to operating when PWM frequency < 1031 kHz)
IBP	SCK/WS is not 16 ± 1, 32 ± 1, 48 ± 1, 64 ± 1 or 128 ± 1	IBP	floating	restart (fault to operating when SCK/WS is 16 ± 1, 32 ± 1, 48 ± 1, 64 ± 1 or 128 ± 1)

10. I²C-bus interface and register settings

10.1 I²C-bus interface

The TFA9879 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control the TFA9879 and to transmit and receive data.

The TFA9879 can operate only in I²C slave mode, as a slave receiver or as a slave transmitter.

The TFA9879 is accessed via an 8-bit code (see Table 16). Bits 1 to 7 contain the device address. Bit 0 (R/$\overline{W}$) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for multichannel applications. Applying the appropriate voltage to pins ADSEL1 (A1) and ADSEL2 (A2) select the required I^{2}C address as detailed in Table 16.

Table 16. I^{2}C-bus device address

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
1	1	0	1	1	A2	A1	R/$\overline{W}$

Table 17. I^{2}C pin voltages in I^{2}C control mode

Logic value	Voltage on pins ADSEL1 and ADSEL2
0	< V_{IL}
1	> V_{IH}

10.2 I^{2}C-bus write cycle

The sequence of events that needs to be followed when writing data to the TFA9879's I^{2}C-bus registers is detailed in Table 18. One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9879, followed by the R/$\overline{W}$ bit set to 0.
3. The TFA9879 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9879 register address to which the first data byte will be written.
5. The TFA9879 asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The TFA9879 asserts an acknowledge.
8. The microcontroller transmits the second byte (the least significant byte).
9. The TFA9879 asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address will have been auto-incremented by the TFA9879.

Table 18. I^{2}C-bus write cycle

Start	TFA9879 Address	R/$\overline{W}$		TFA9879 first register address		MSB		LSB		More data...	Stop
S	11011A_2A_1	0	A	ADDR	A	MS1	A	LS1	A	<....>	P