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TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

16 GBIT (2G × 8 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TH58NVG4S0HTAK0 is a single 3.3V 16 Gbit (18,253,611,008 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (4096 + 256) bytes × 64 pages × 8192blocks. The device has two 4352-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 4352-byte increments. The Erase operation is implemented in a single block unit (256 Kbytes + 16 Kbytes: 4352 bytes × 64 pages).

The TH58NVG4S0HTAK0 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	x8
Memory cell array	4352 × 128K × 8 × 4
Register	4352 × 8
Page size	4352 bytes
Block size	(256K + 16K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 8032 blocks
  Max 8192 blocks

- Power supply
  V_{CC} = 2.7V to 3.6V

- Access time

Cell array to register	25 μs max
Serial Read Cycle	25 ns min (CL=50pF)

- Program/Erase time

Auto Page Program	300 μs/page typ.
Auto Block Erase	2.5 ms/block typ.

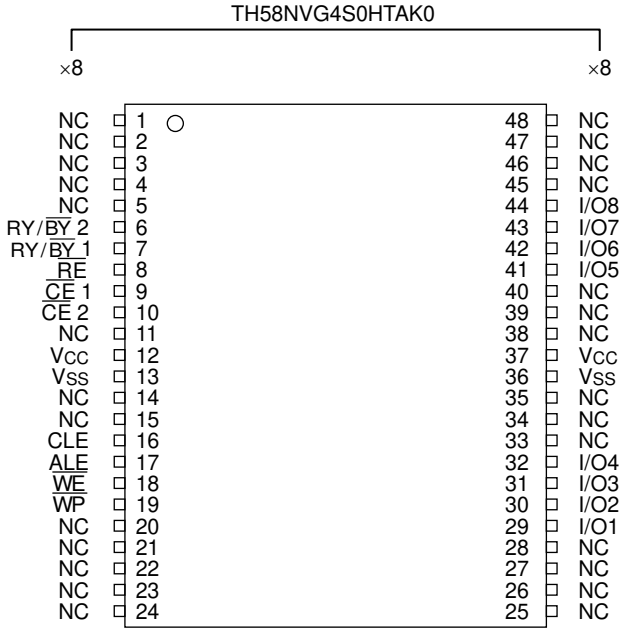
- Operating current

Read (25 ns cycle)	30 mA max.
Program (avg.)	30 mA max
Erase (avg.)	30 mA max
Standby	200 μA max

- Package
  TSOP I 48-P-1220-0.50 (Weight: 0.56 g typ.)

- 8 bit ECC for each 512Byte is required.

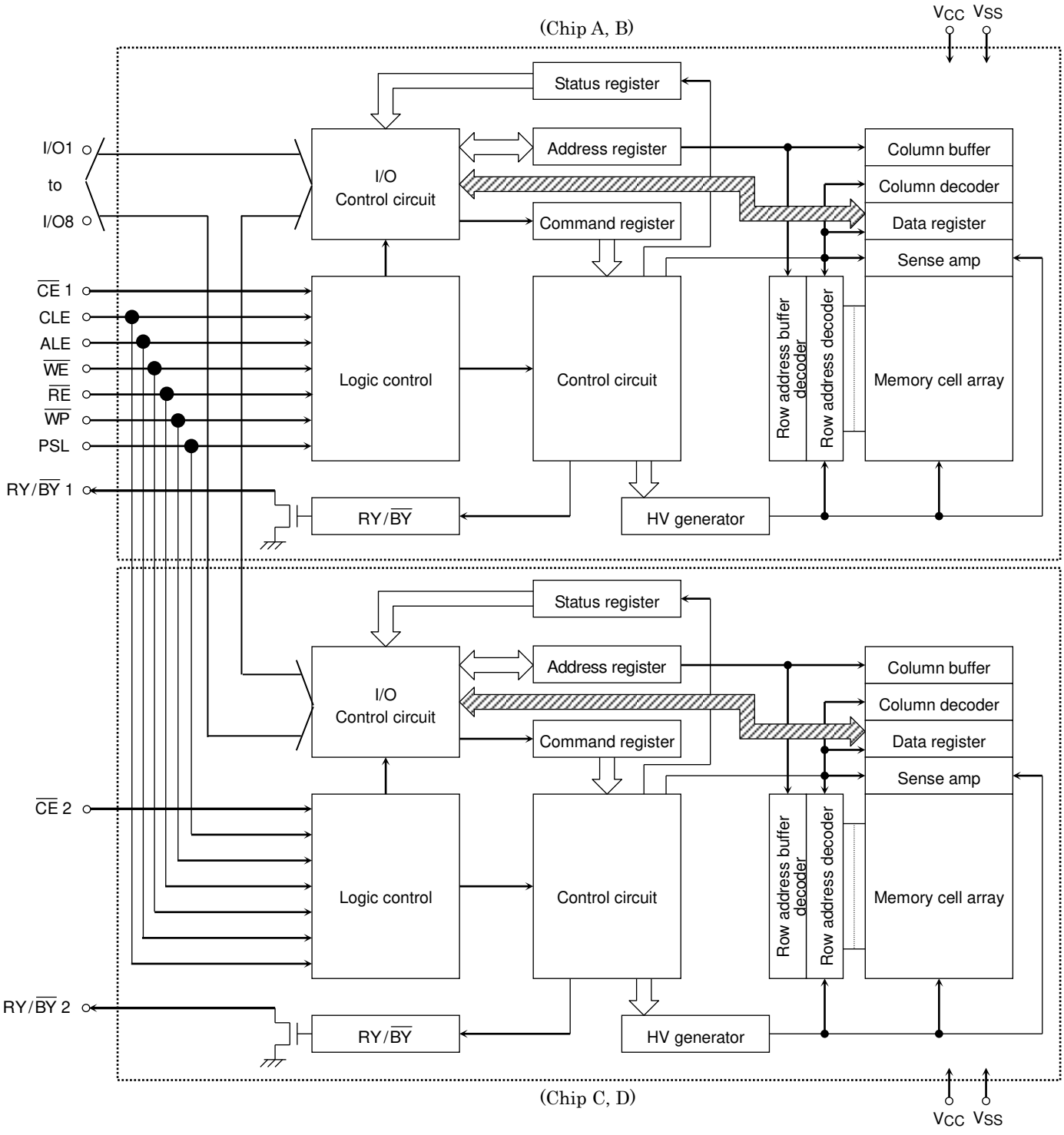
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$ 1	Chip enable (Chip A,B)
$\overline{CE}$ 2	Chip enable (Chip C,D)
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$ 1	Ready/Busy (Chip A,B)
RY/$\overline{BY}$ 2	Ready/Busy (Chip C,D)
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 150	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	40	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	40	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	8032	—	8192	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime
The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	2.7	—	3.6	V
V_{IH}	High Level input Voltage	Vcc x 0.8	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	−0.3*	—	Vcc x 0.2	V

* −2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = -40 to 85°C, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±40	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±40	μA
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, tcycle = 25 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	200	μA
V_{OH}	High Level Output Voltage	I_{OH} = −0.1 mA	Vcc − 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output current of RY/$\overline{BY}$ pin	V_{OL} = 0.2 V	—	4	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85°C, Vcc = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	12	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	12	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CEA}	$\overline{CE}$ Access Time	—	25	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	$\overline{RE}$ High to Output Hold Time	25	—	ns
t_{RLOH}	$\overline{RE}$ Low to Output Hold Time	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns
t_{CSD}	$\overline{CE}$ High to ALE or CLE Don't Care	0	—	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	60	—	ns
t_{R}	Memory Cell Array to Starting Address	—	25	μs
$t_{DCBSYR1}$	Data Cache Busy in Read Cache (following 31h and 3Fh)	—	25	μs
$t_{DCBSYR2}$	Data Cache Busy in Page Copy (following 3Ah)	—	30	μs
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

*1: tCLS and tALS can not be shorter than tWP

*2: tCS should be longer than tWP + 8ns.

AC TEST CONDITIONS

PARAMETER	CONDITION
	V_{CC}: 2.7 to 3.6V
Input level	V_{CC} – 0.2 V, 0.2 V
Input pulse rise and fall time	3 ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output load	C_L (50 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document.)

PROGRAMMING AND ERASING CHARACTERISTICS

(Ta = -40 to 85°C, V_{CC} = 2.7 to 3.6V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	300	700	μs	
$t_{DCBSYW1}$	Data Cache Busy Time in Write Cache (following 11h)	—	—	10	μs	
$t_{DCBSYW2}$	Data Cache Busy Time in Write Cache (following 15h)	—	—	700	μs	(2)
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	2.5	5	ms	

(1) Refer to Application Note (12) toward the end of this document.

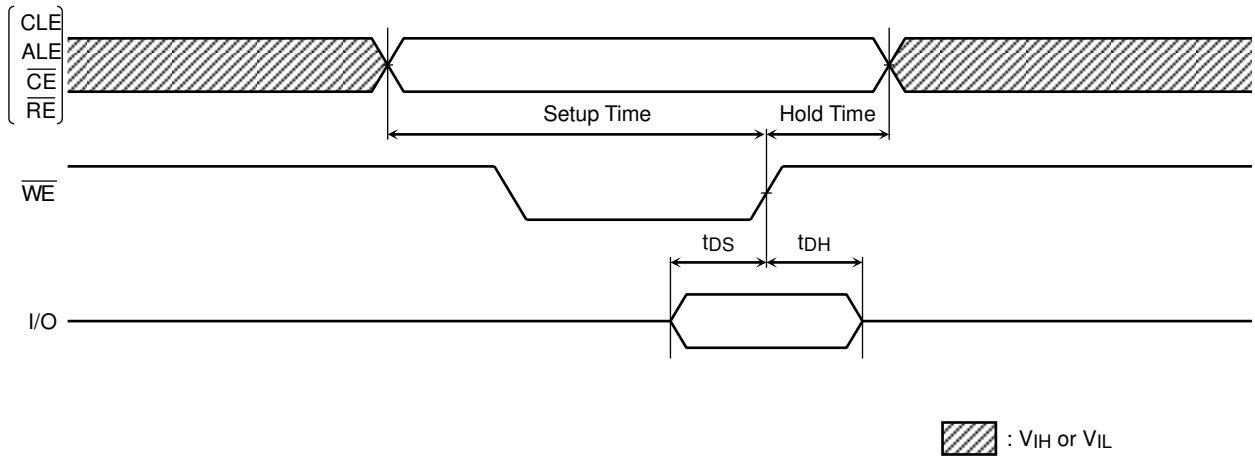
(2) $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Data Output

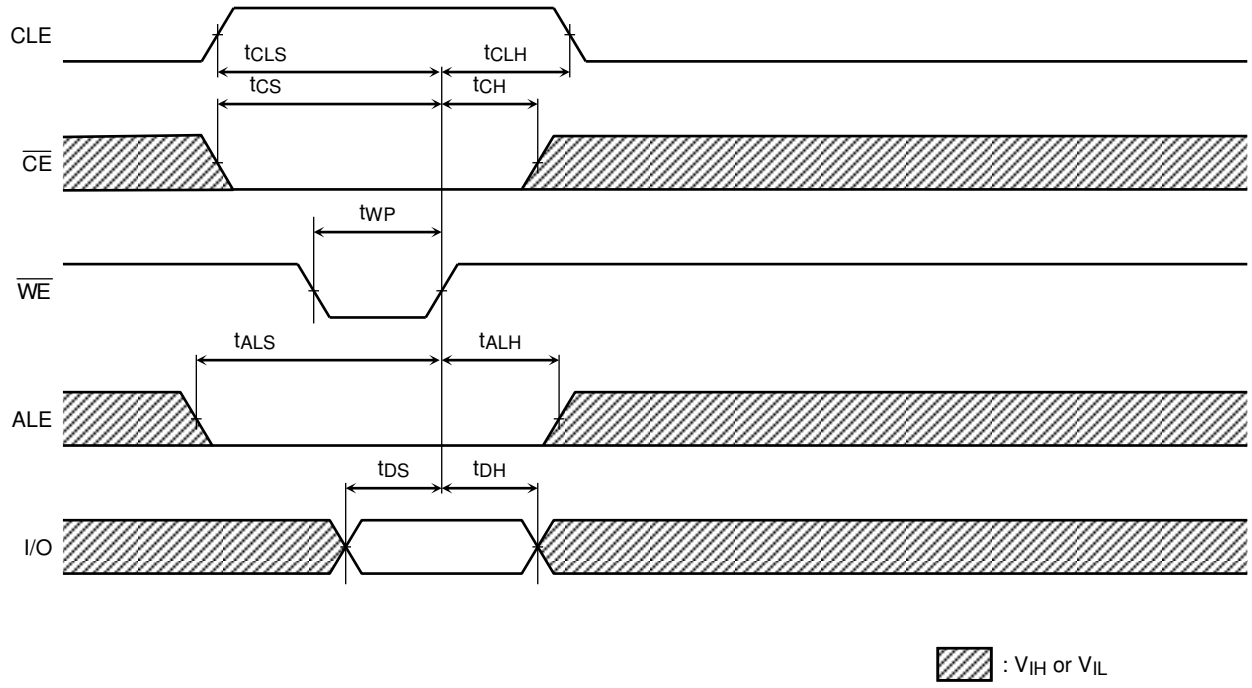
When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE,ALE,/CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

TIMING DIAGRAMS

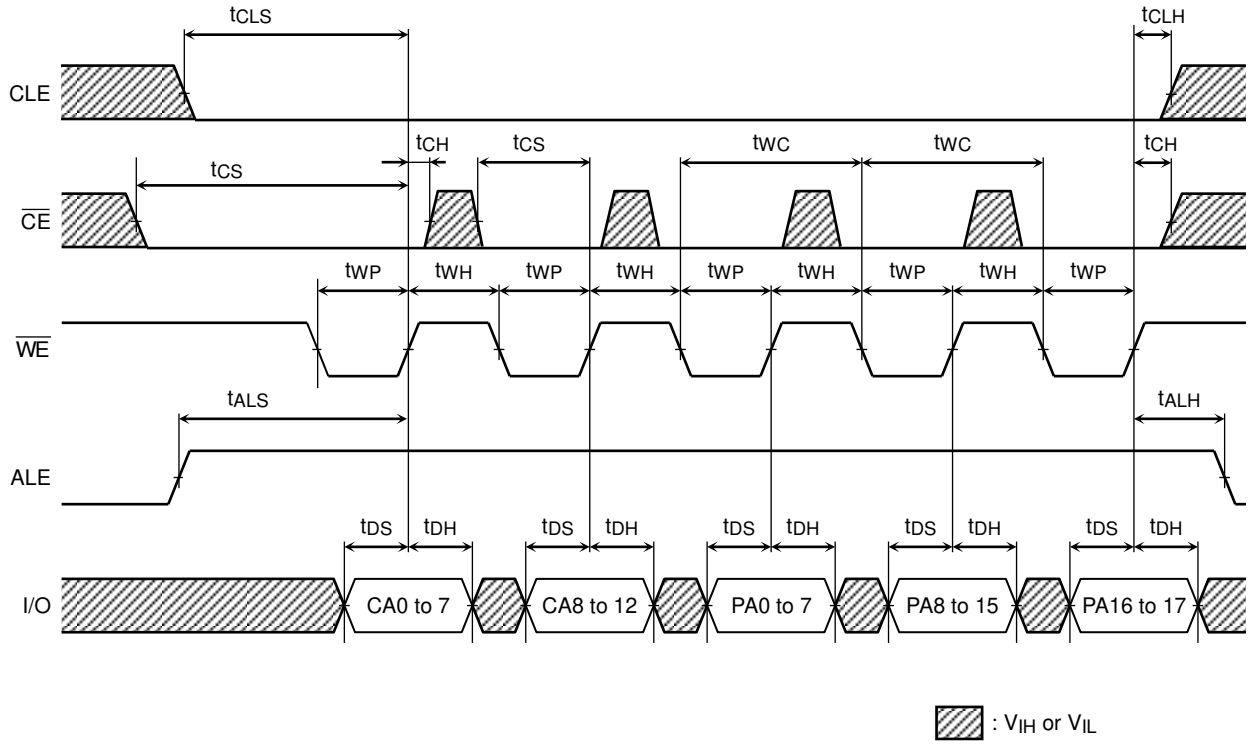
Latch Timing Diagram for Command/Address/Data



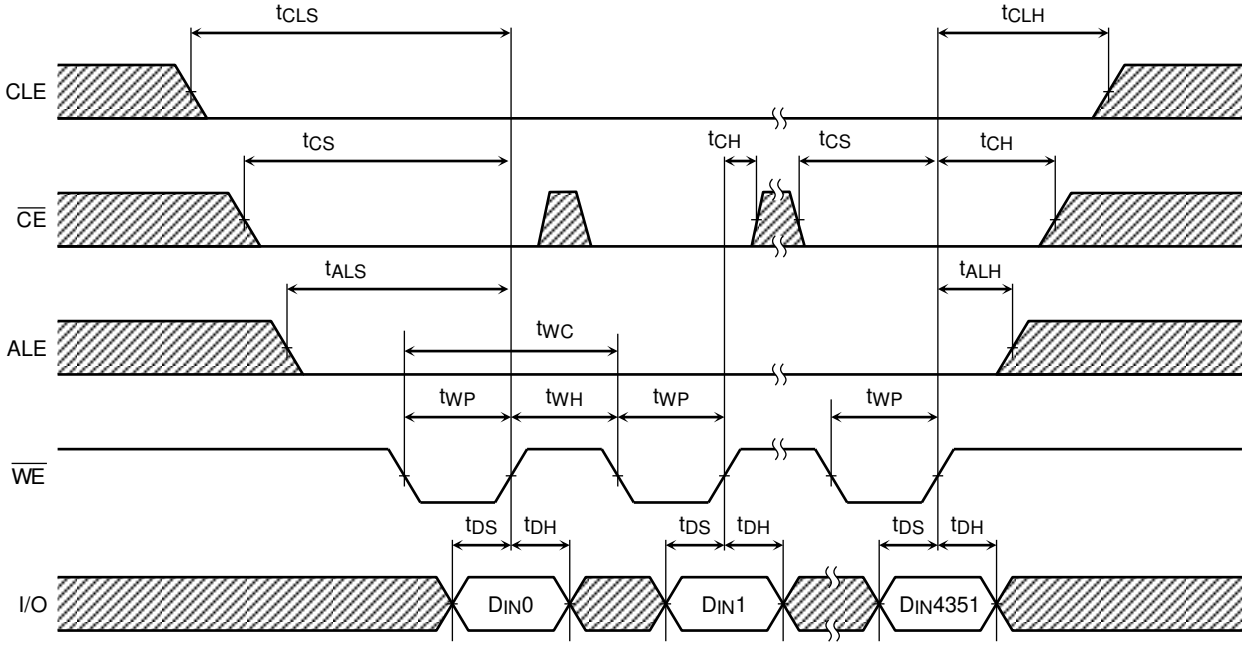
Command Input Cycle Timing Diagram



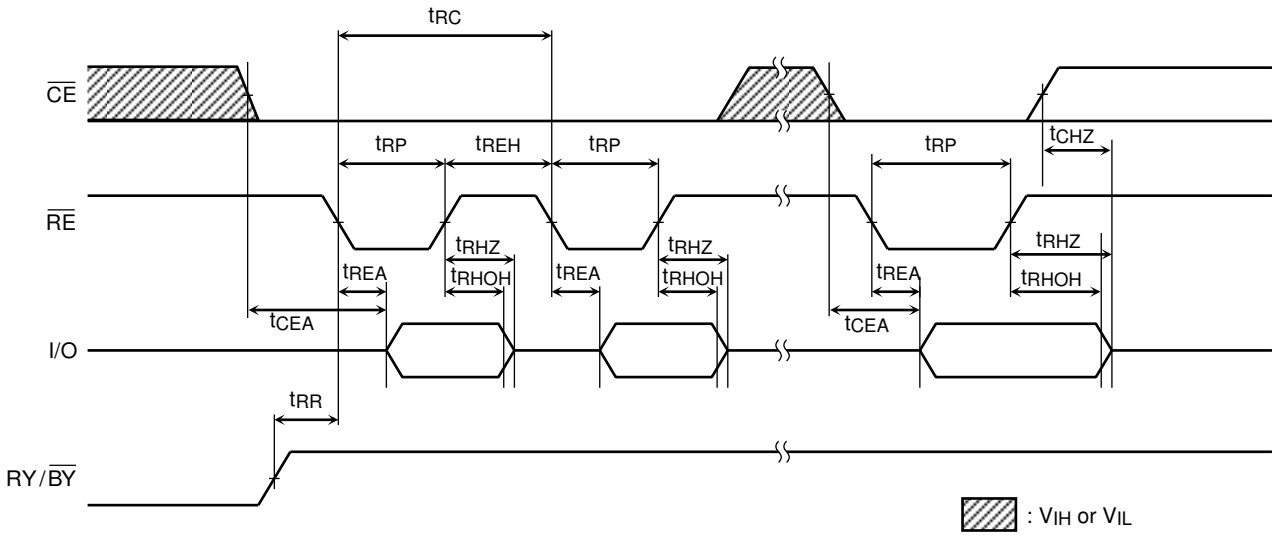
Address Input Cycle Timing Diagram



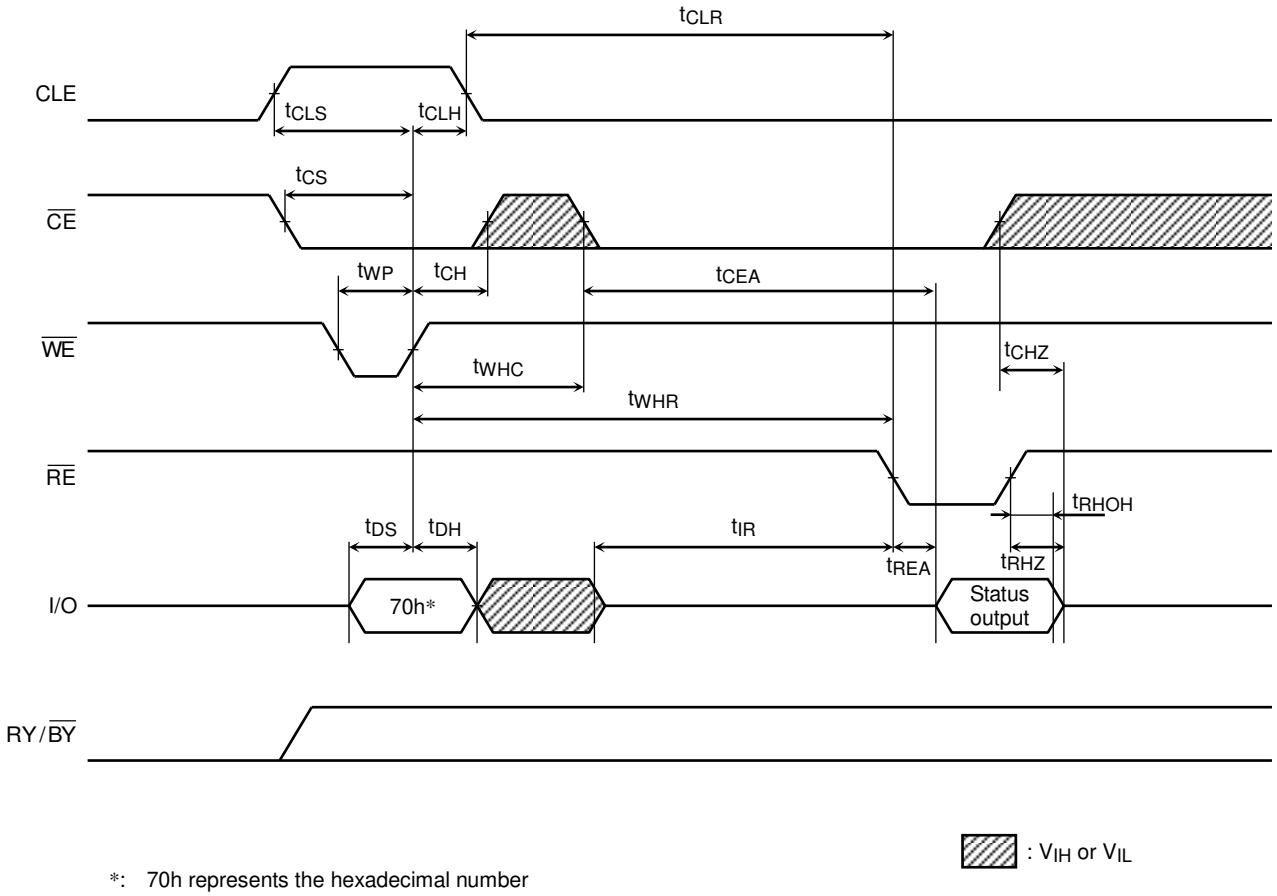
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

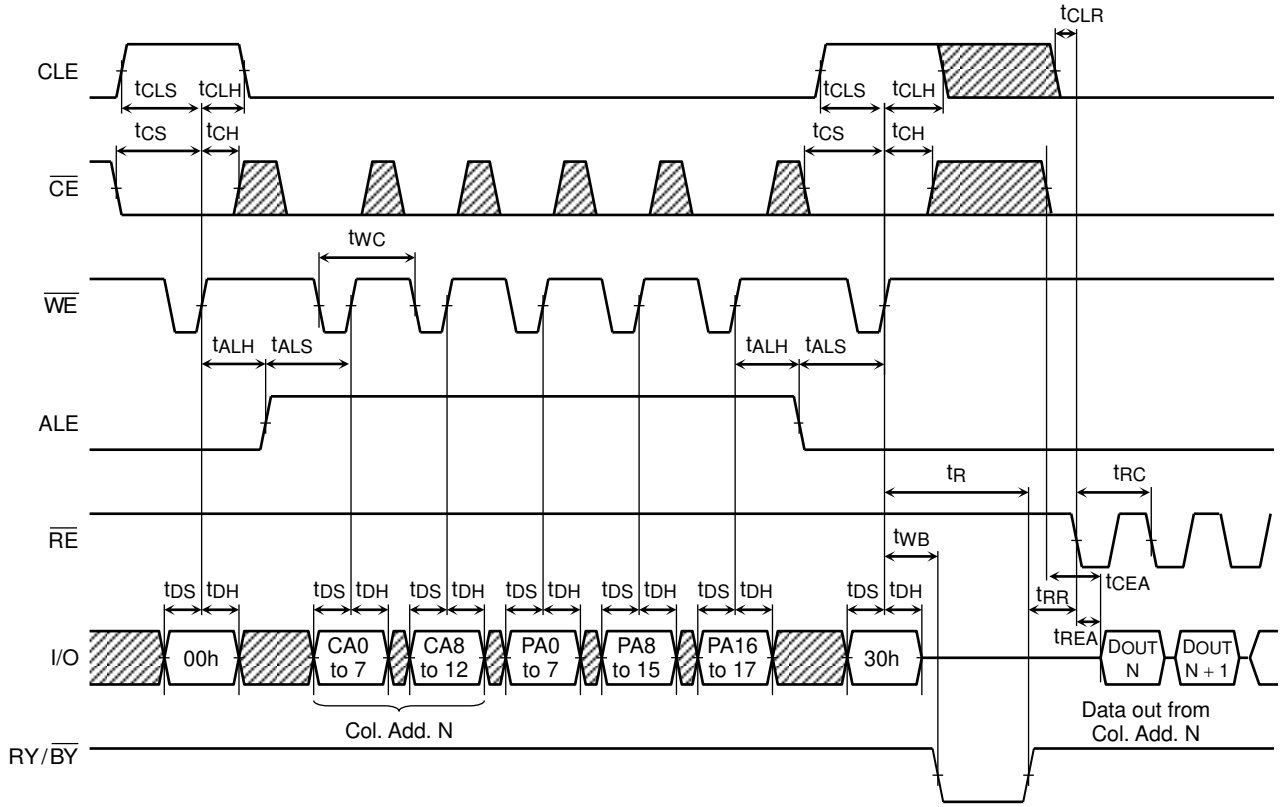


Status Read Cycle Timing Diagram

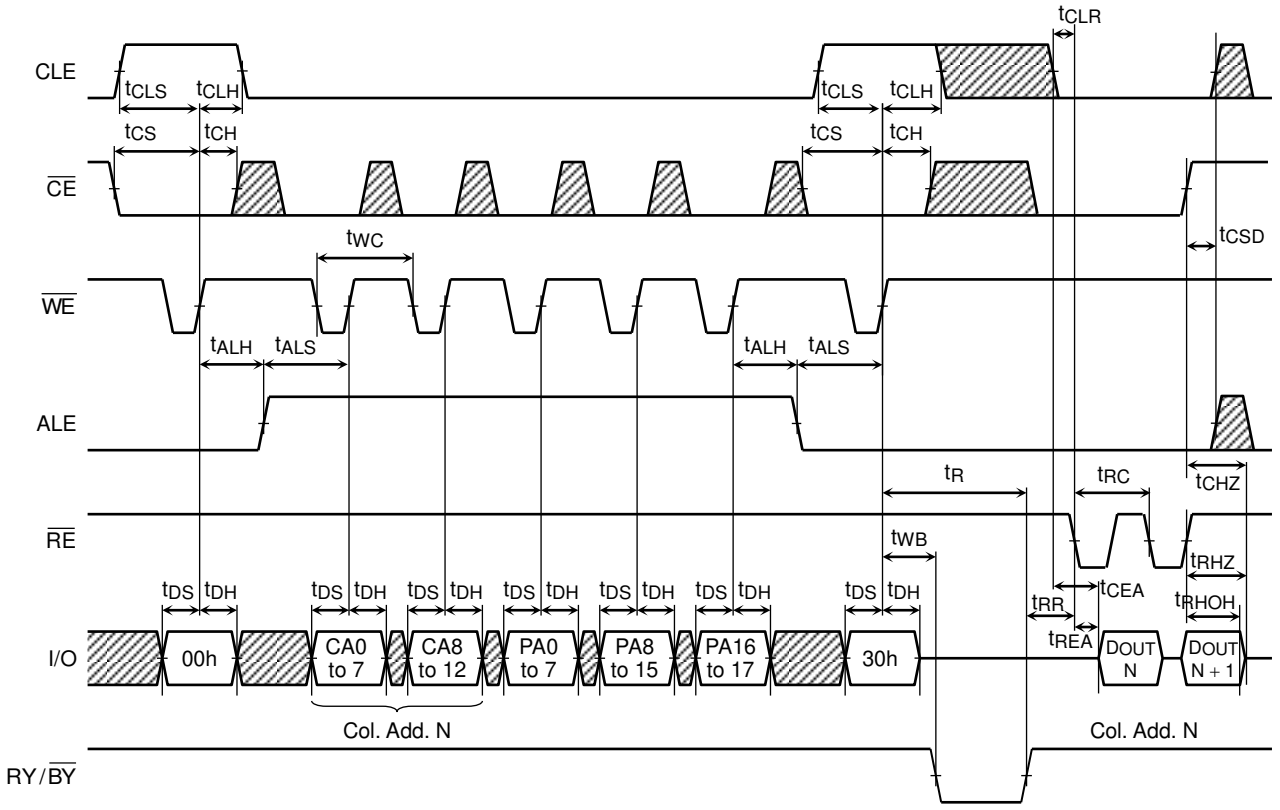


*: 70h represents the hexadecimal number

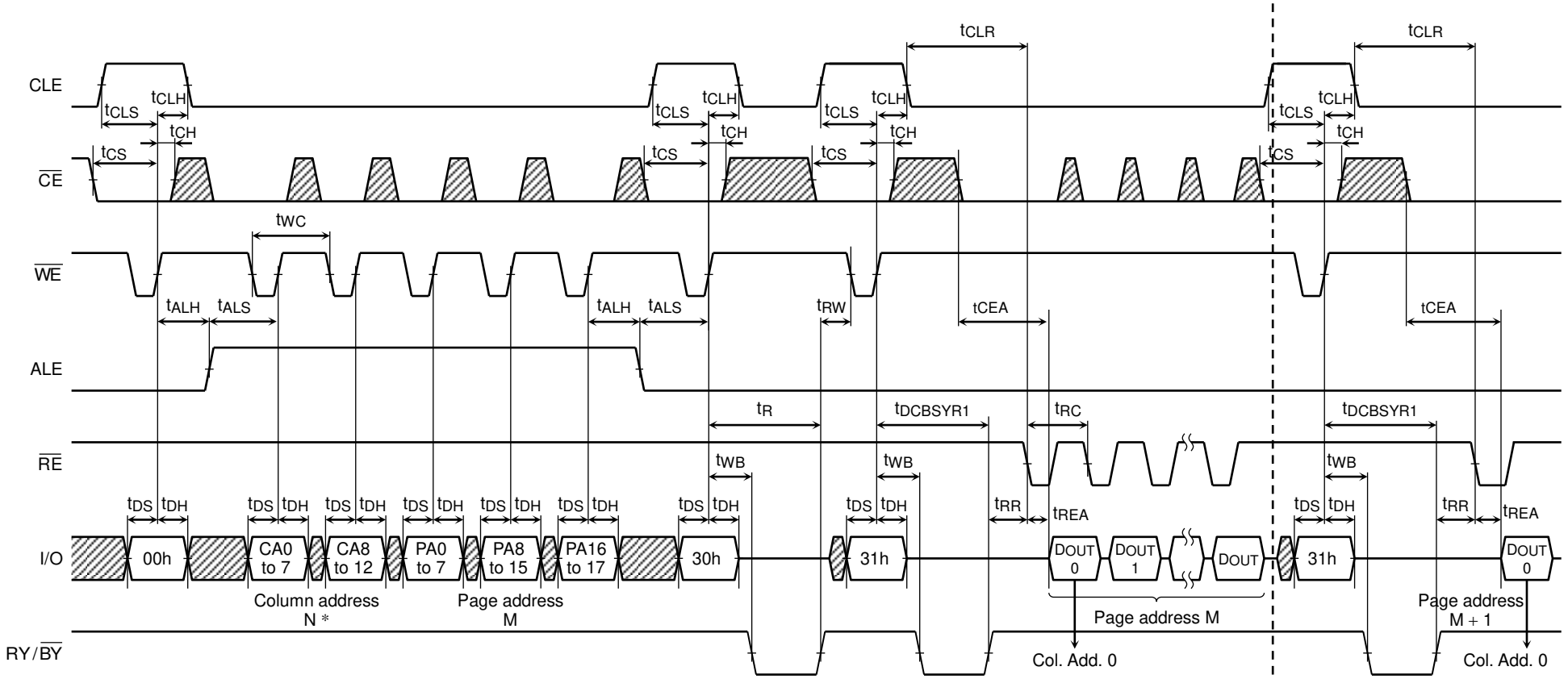
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

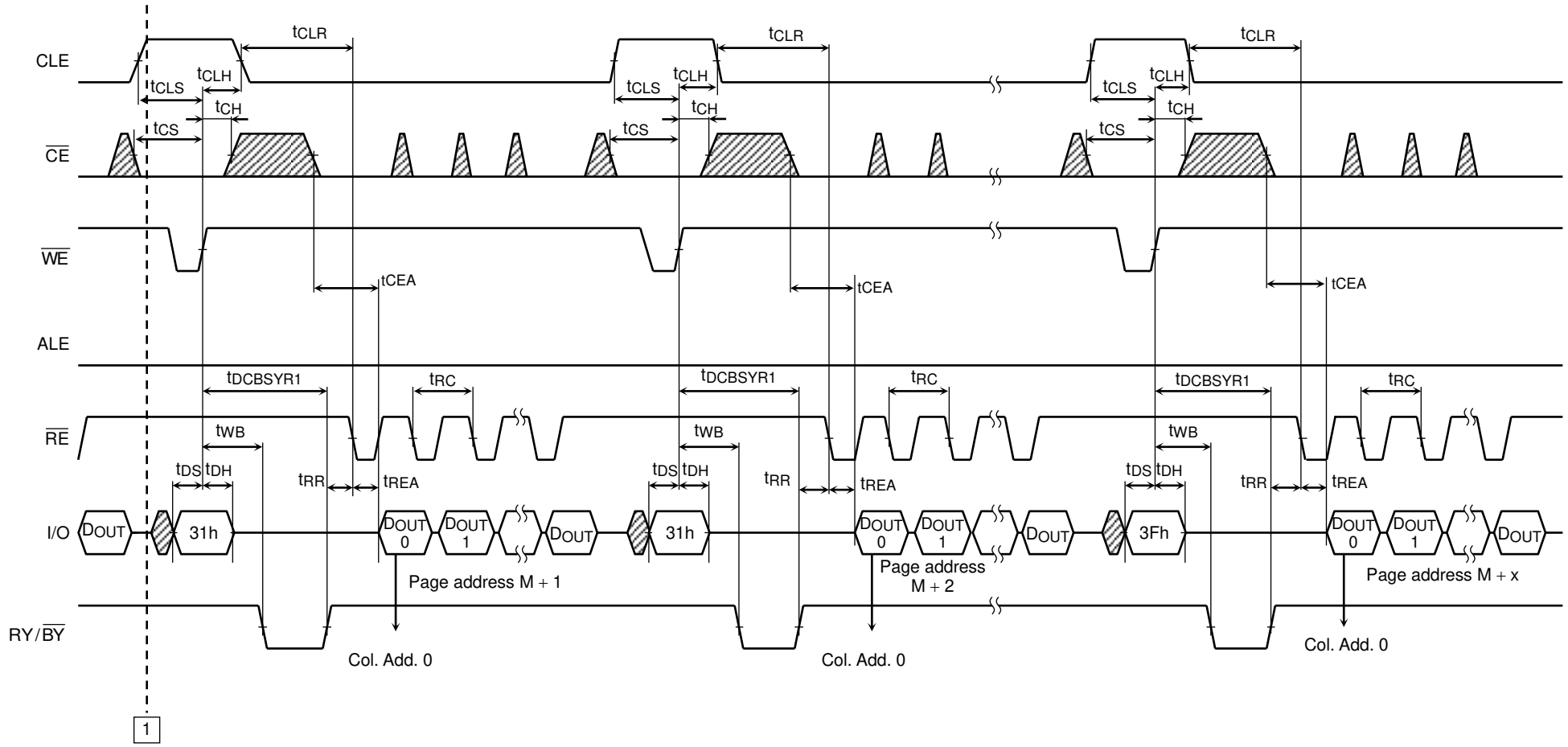


Read Cycle with Data Cache Timing Diagram (1/2)



* The column address will be reset to 0 by the 31h command input.

Read Cycle with Data Cache Timing Diagram (2/2)



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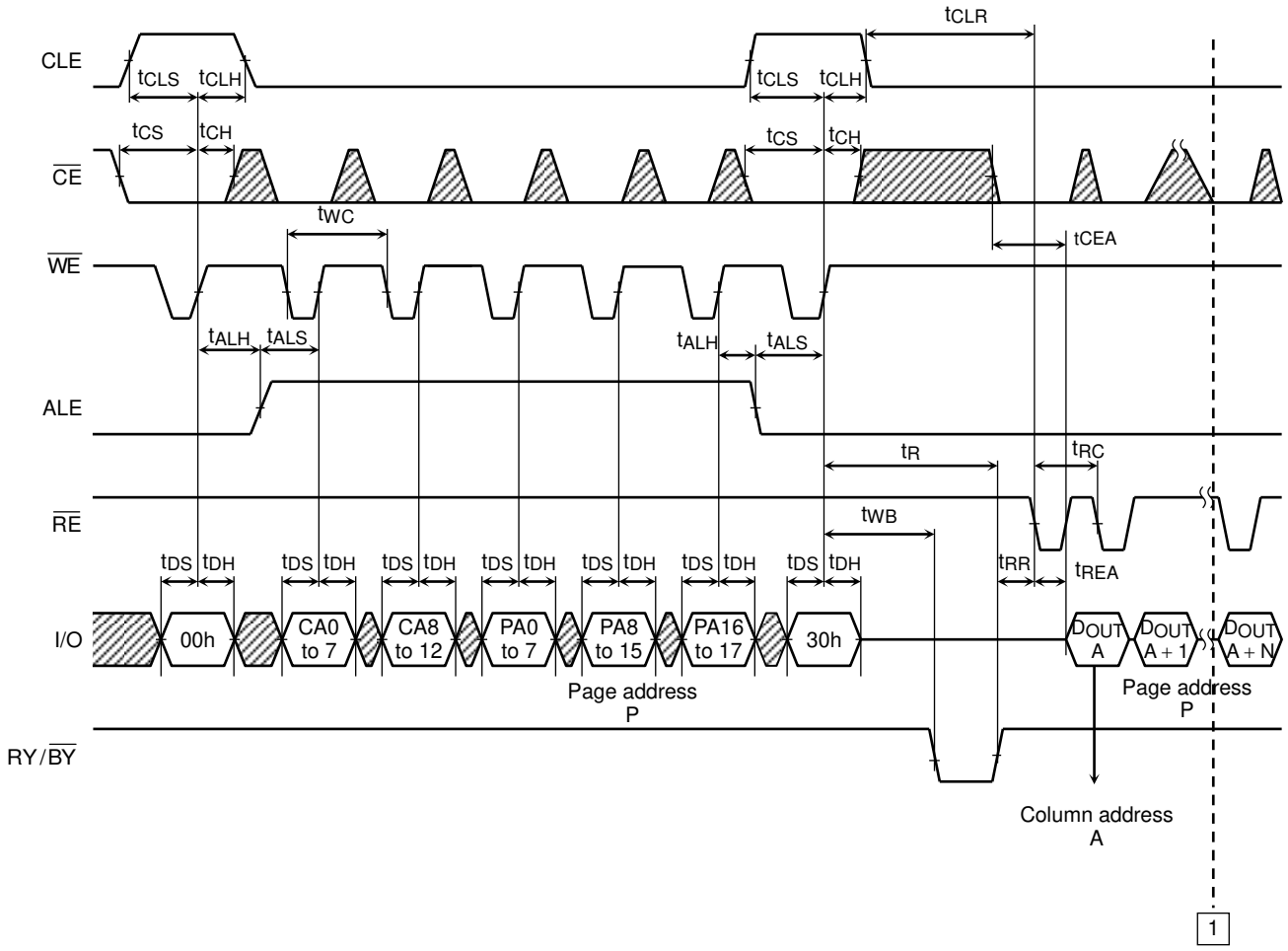
Make sure to terminate the operation with 3Fh command.

Column Address Change in Read Cycle Timing Diagram (1/2)



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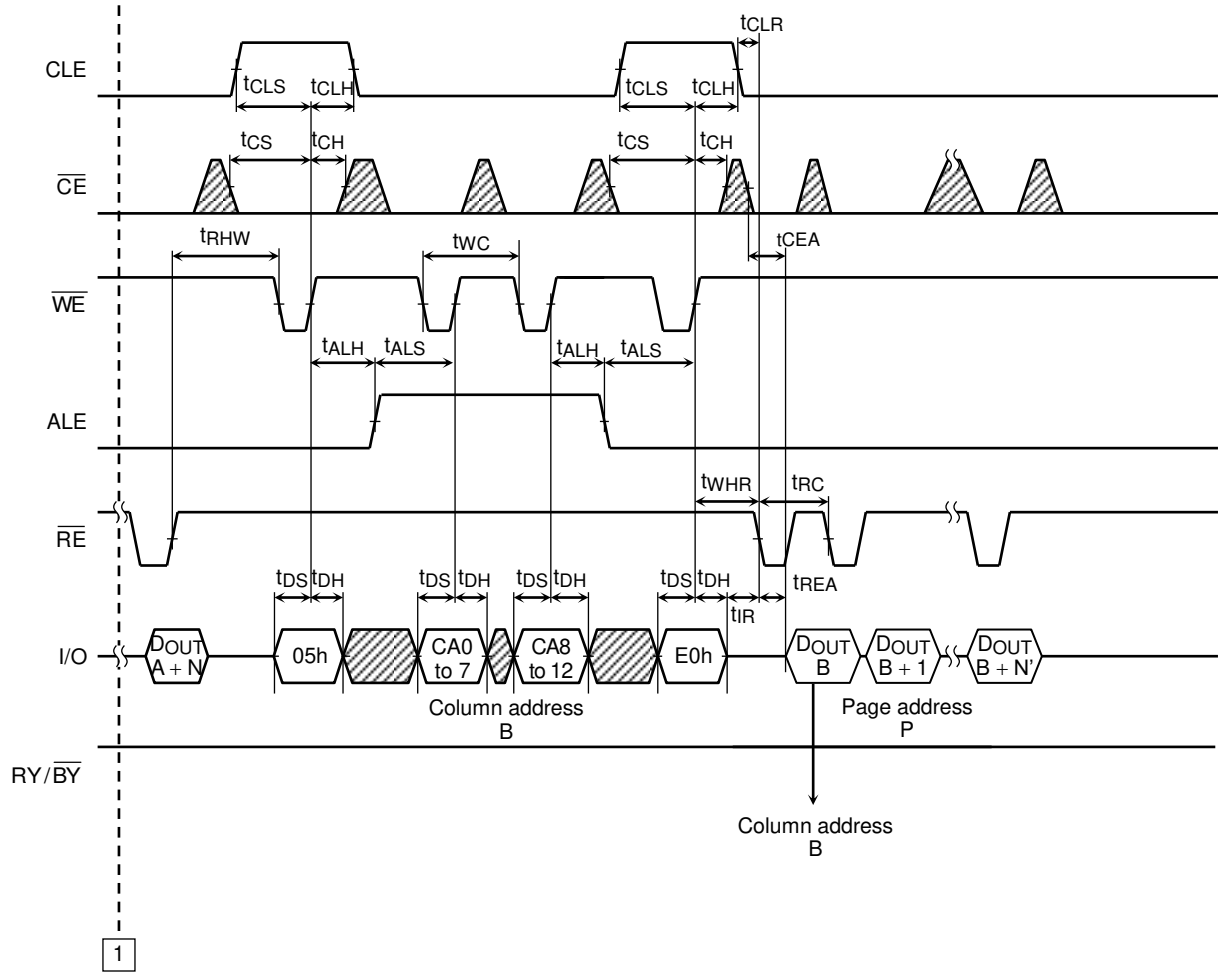
Column Address Change in Read Cycle Timing Diagram (2/2)



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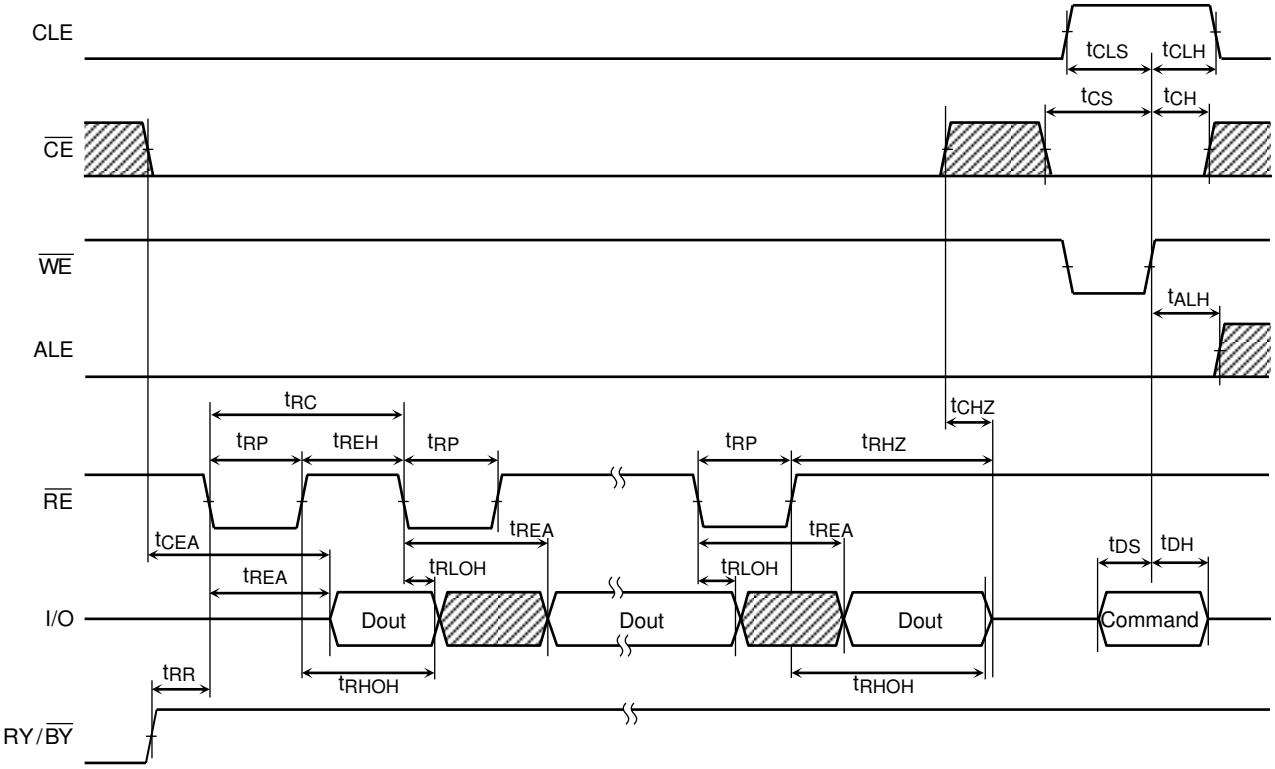
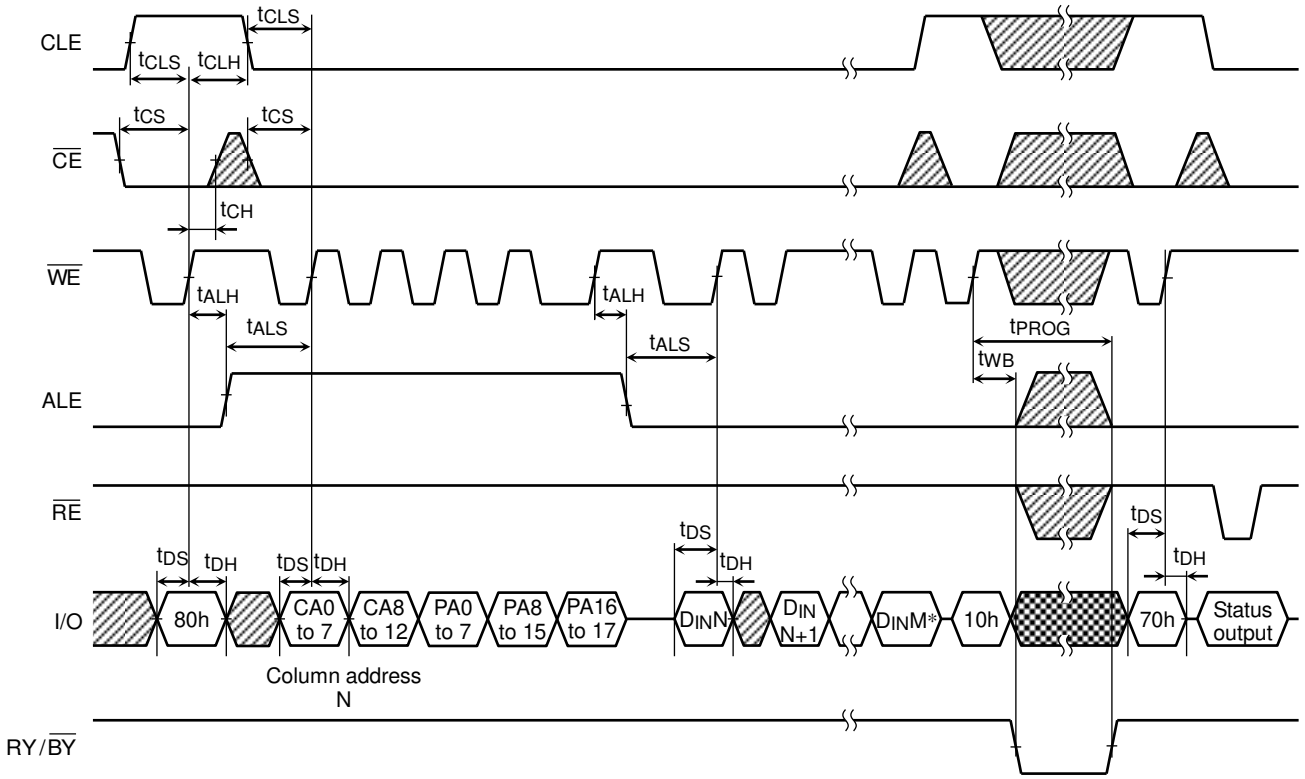
Data Output Timing Diagram



Auto-Program Operation Timing Diagram

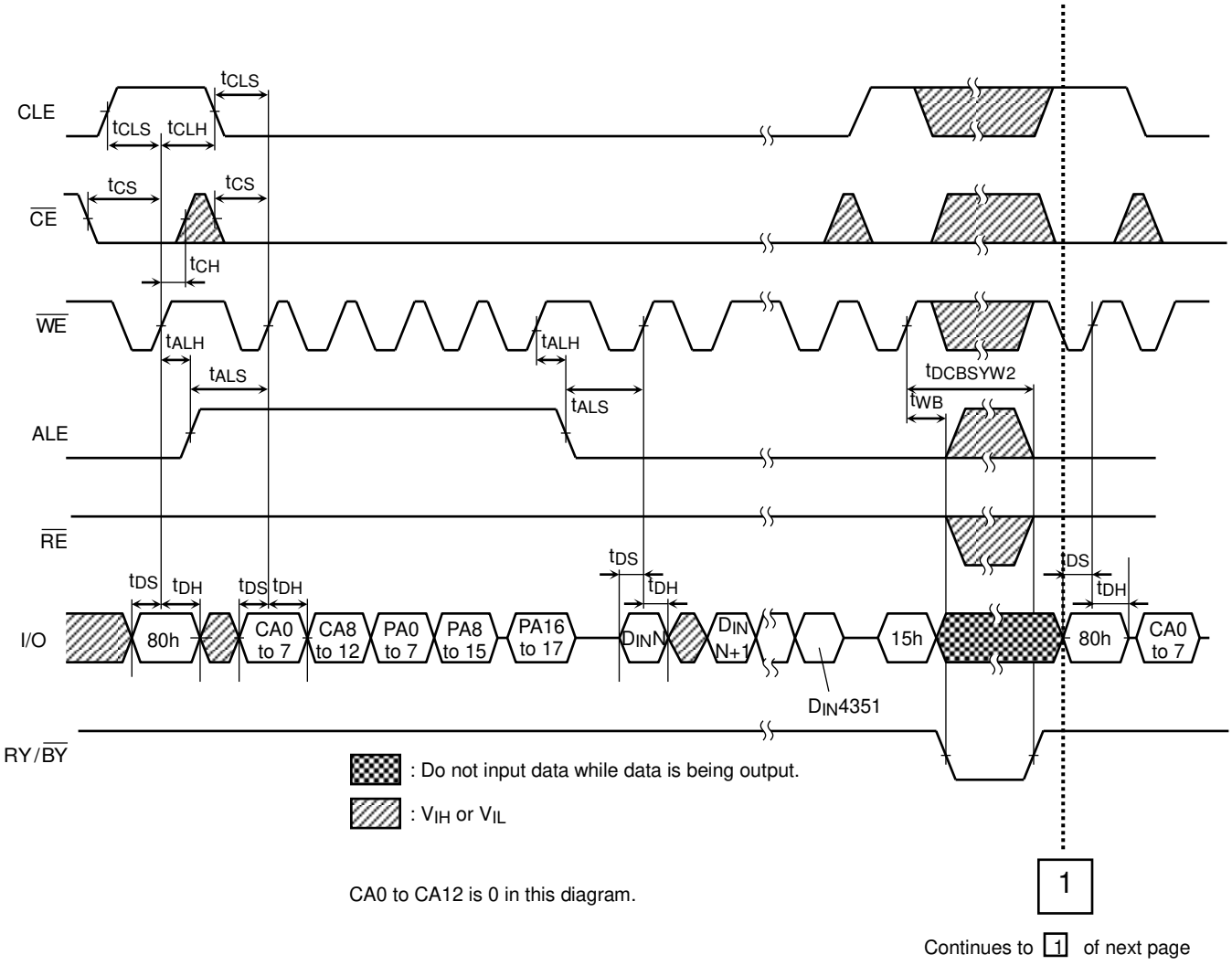


: Do not input data while data is being output.

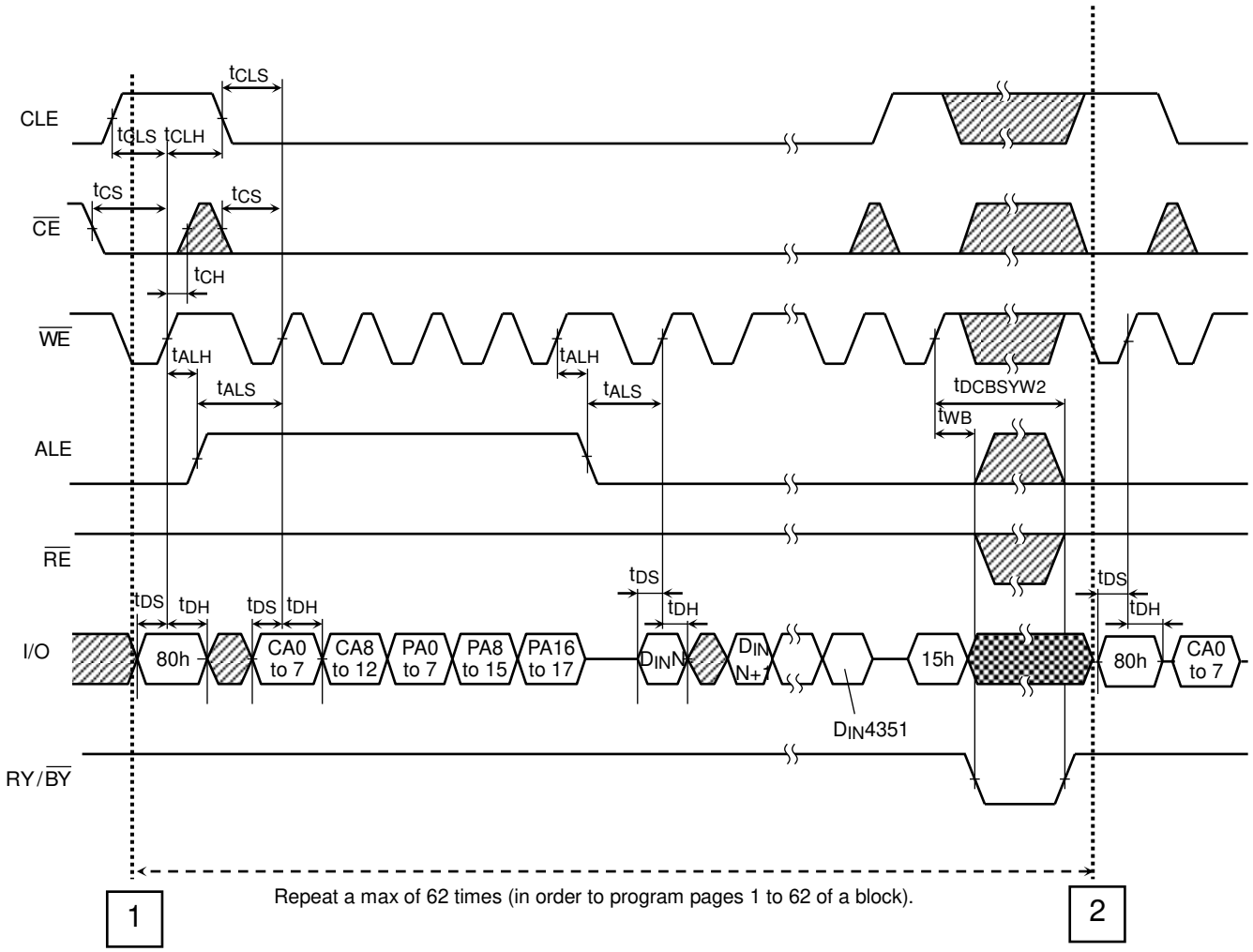
: V_{IH} or V_{IL}

*) M: up to 4351 (byte input data for ×8 device).

Auto-Program Operation with Data Cache Timing Diagram (1/3)



Auto-Program Operation with Data Cache Timing Diagram (2/3)



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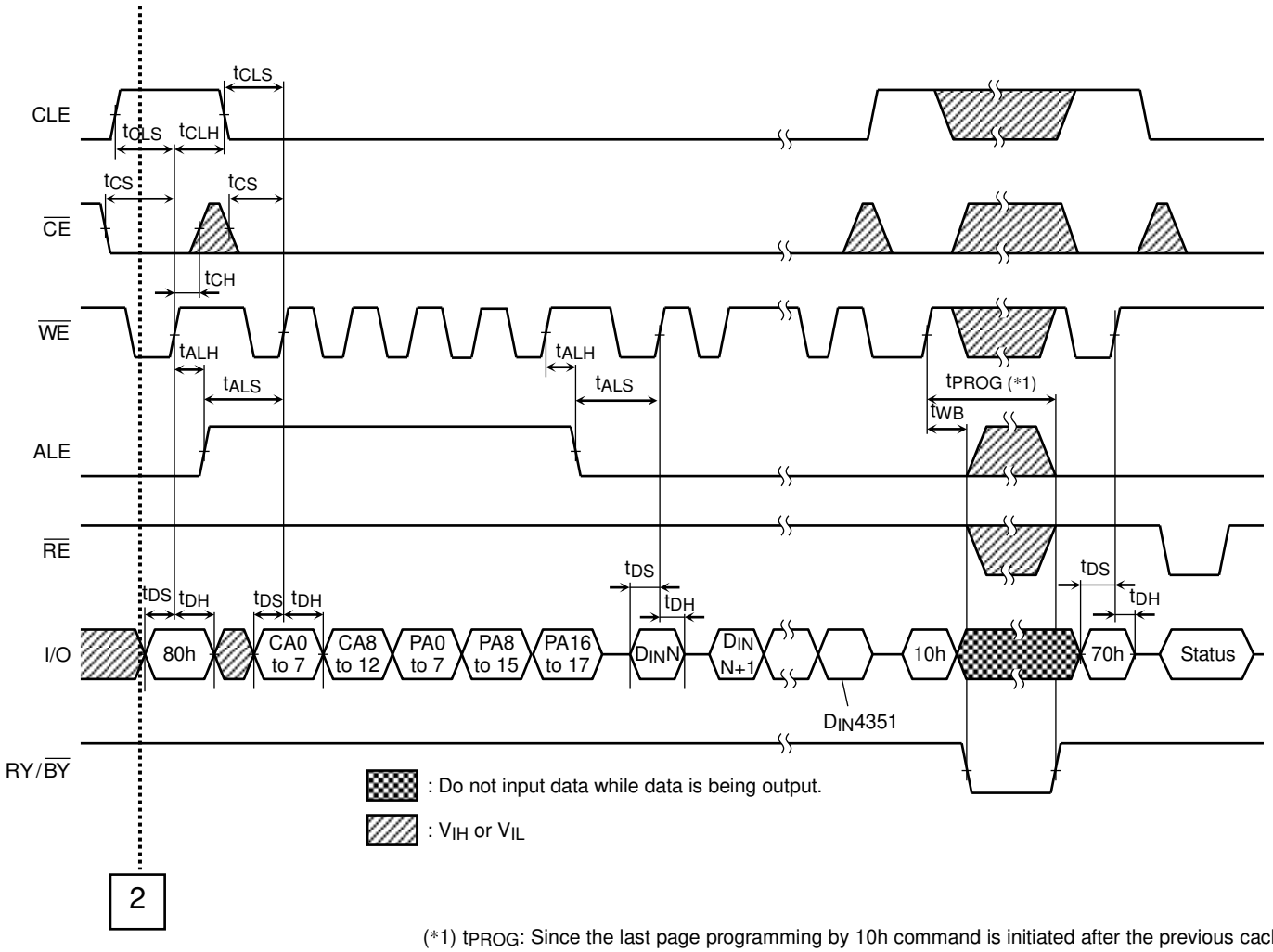
: Do not input data while data is being output.

: V_{IH} or V_{IL}

Auto-Program Operation with Data Cache Timing Diagram (3/3)



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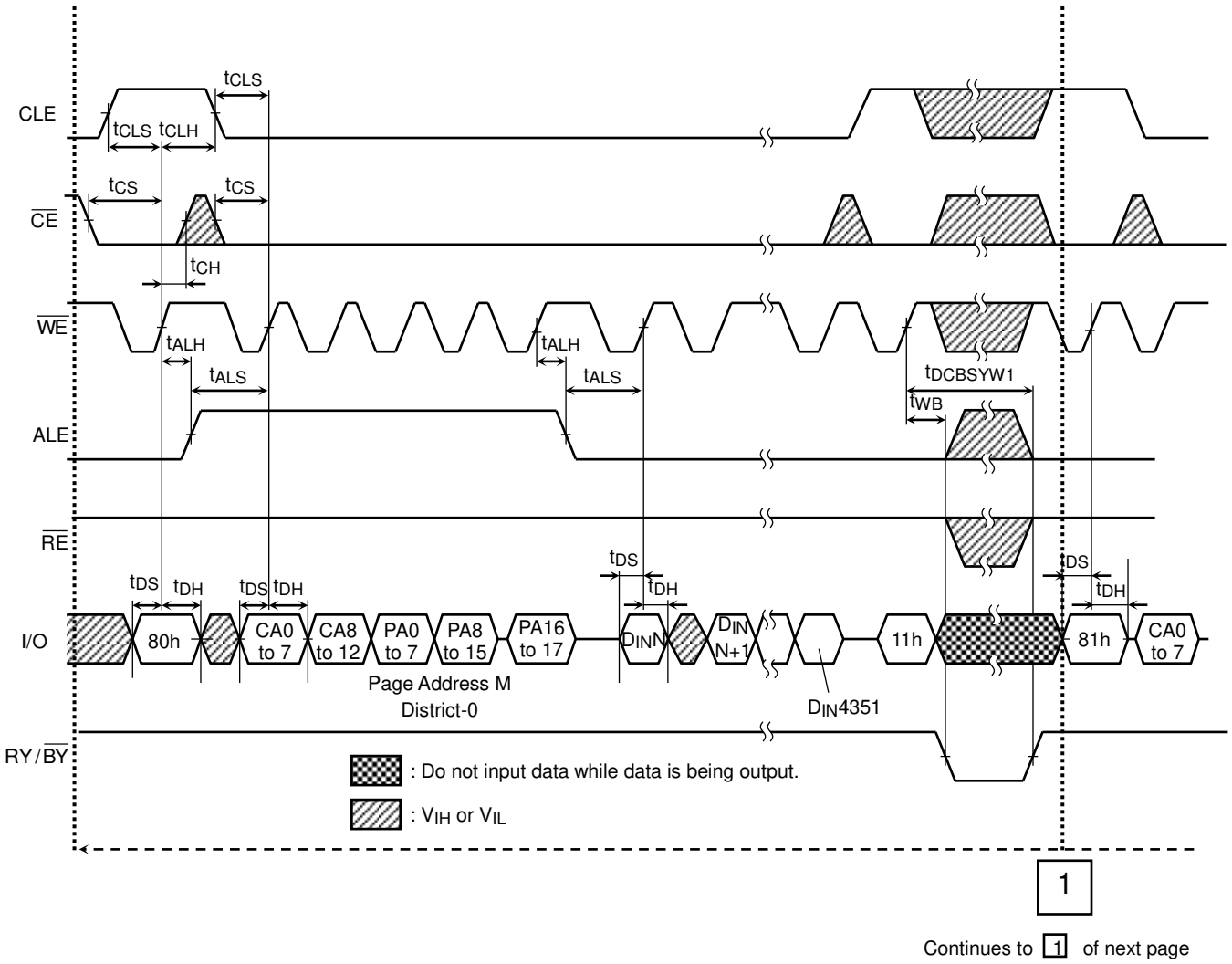
(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page − A
A = (command input cycle + address input cycle + data input cycle time of the last page)

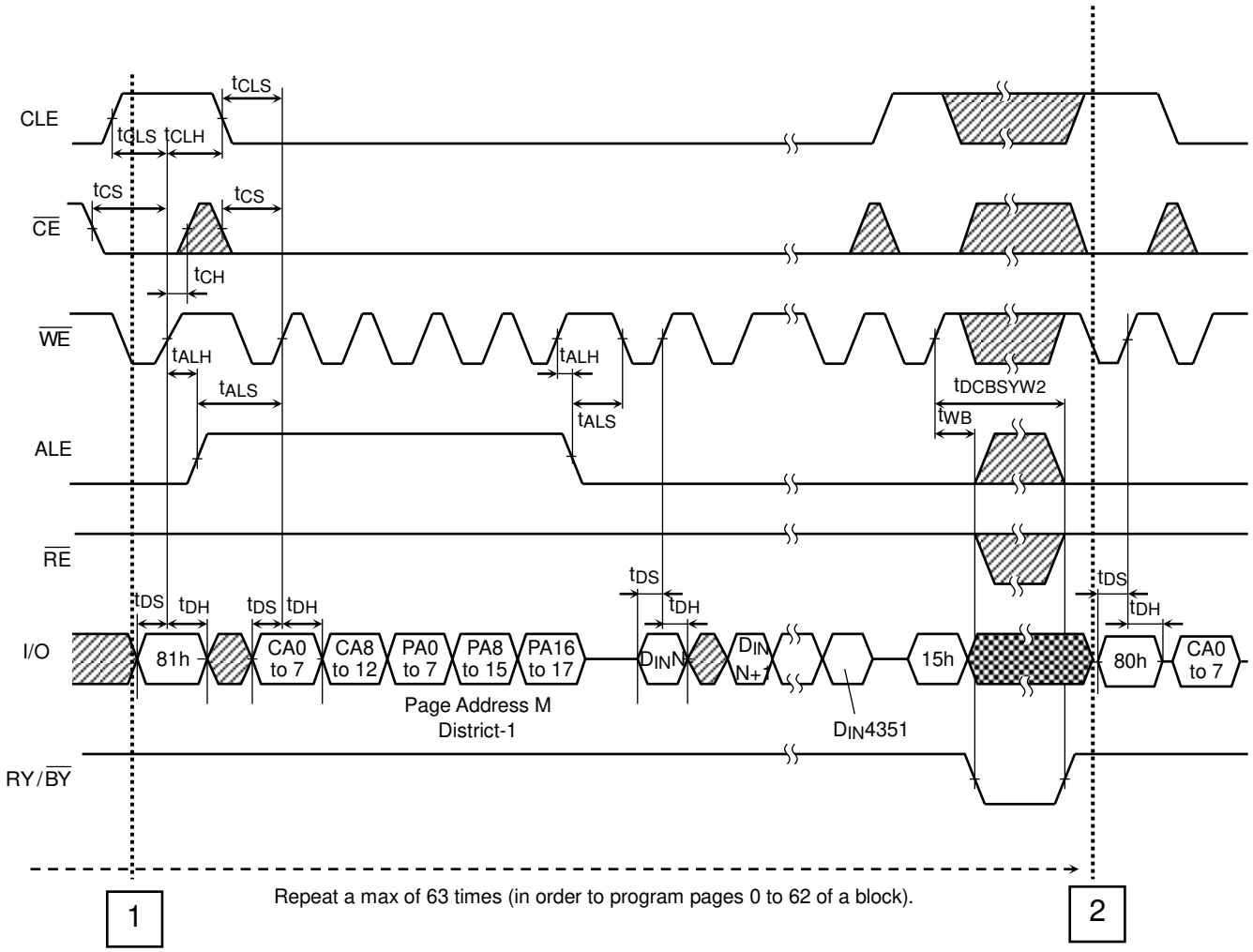
If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 80h-10h- command sequence.
If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

Multi-Page Program Operation with Data Cache Timing Diagram (1/4)



Multi-Page Program Operation with Data Cache Timing Diagram (2/4)



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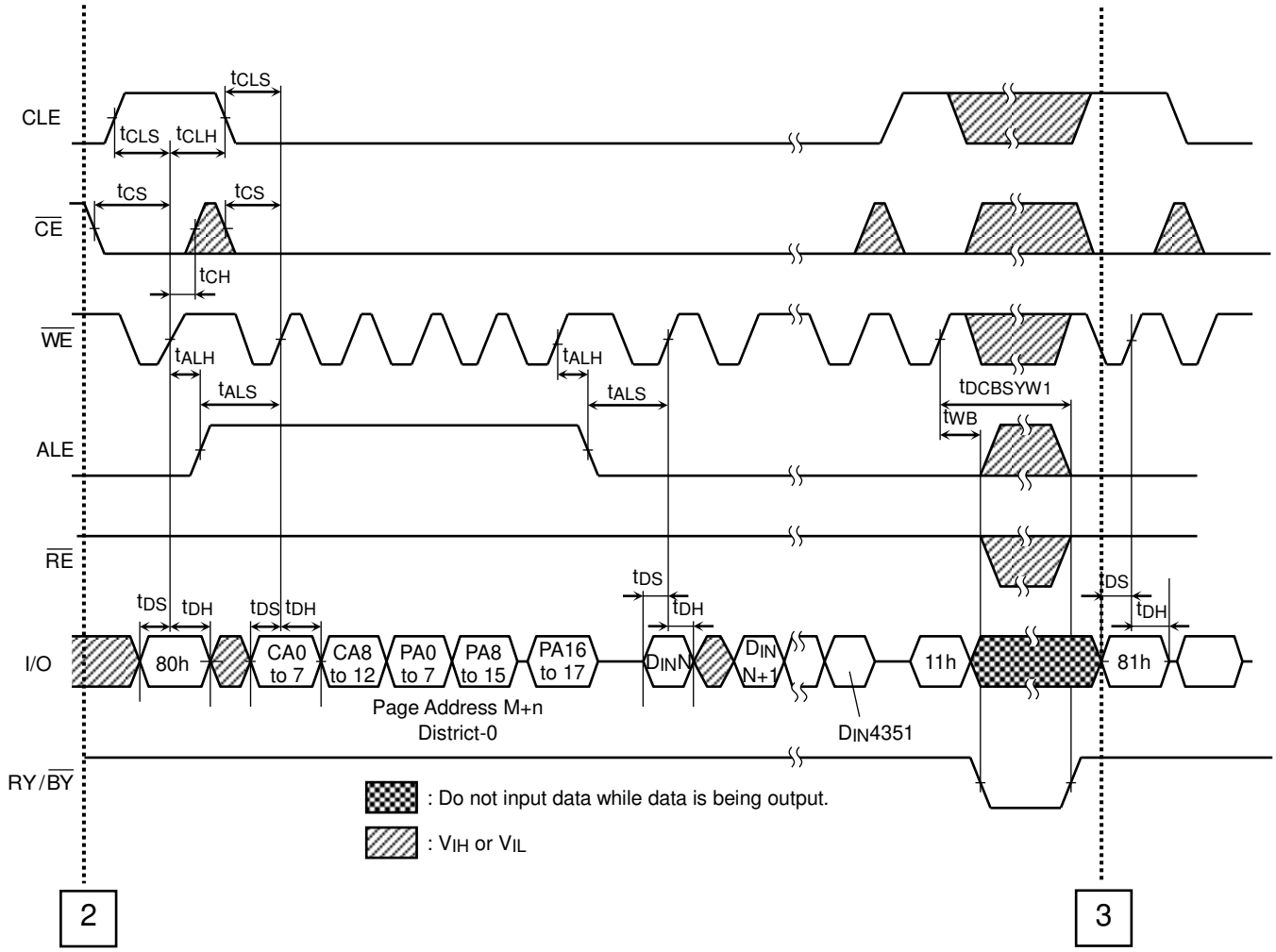
: Do not input data while data is being output.

: V_{IH} or V_{IL}

Multi-Page Program Operation with Data Cache Timing Diagram (3/4)



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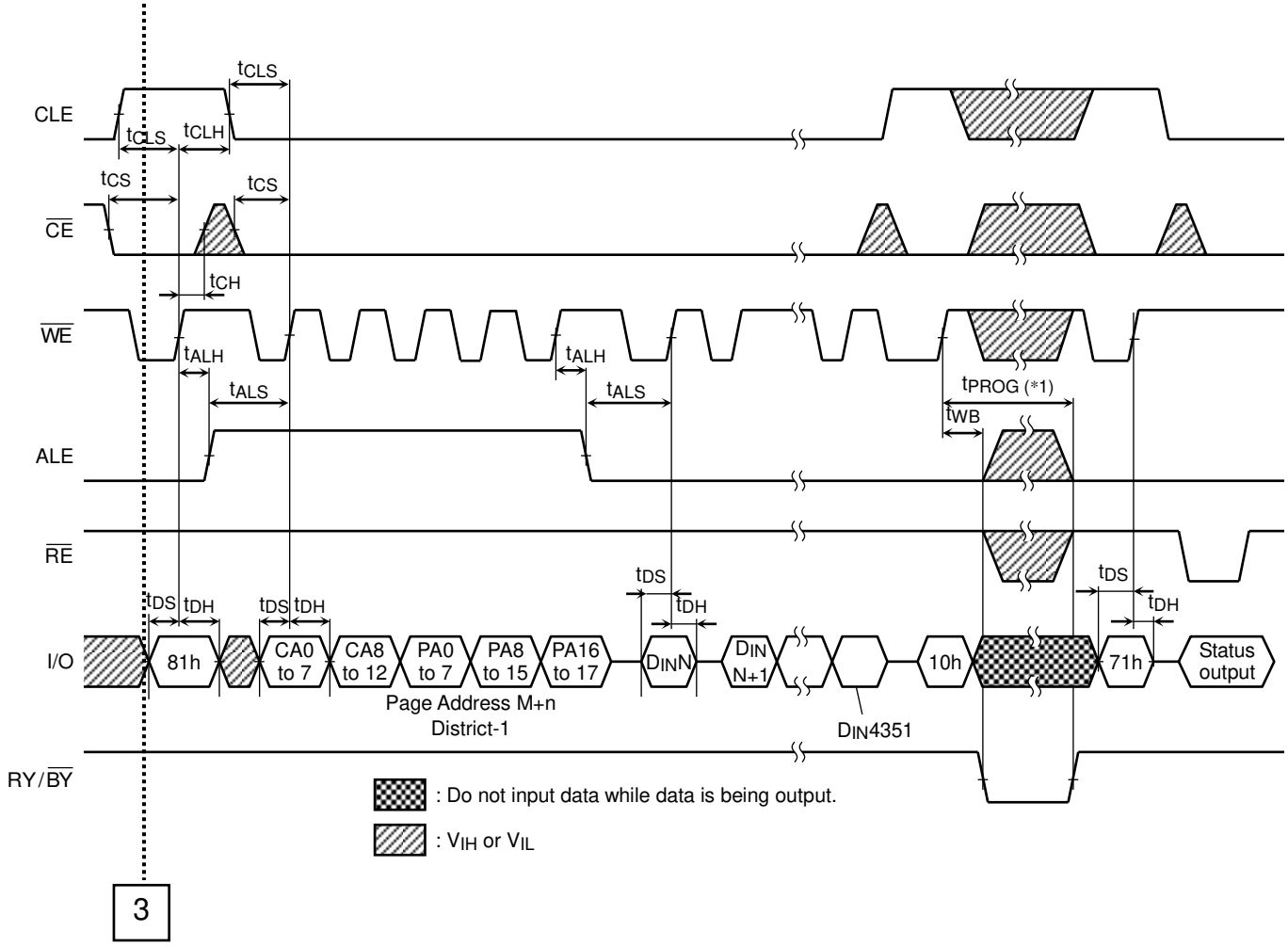
Multi-Page Program Operation with Data Cache Timing Diagram (4/4)



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(*1) t_{PROG}: Since the last page programming by 10h command is initiated after the previous cache program, the t_{PROG} during cache programming is given by the following equation.

t_{PROG} = t_{PROG} of the last page + t_{PROG} of the previous page − A
A = (command input cycle + address input cycle + data input cycle time of the last page)

If "A" exceeds the t_{PROG} of previous page, t_{PROG} of the last page is t_{PROG} max.

(Note) Make sure to terminate the operation with 81h-10h- command sequence.
If the operation is terminated by 81h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

Auto Block Erase Timing Diagram