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# TH8062

***Voltage Regulator with LIN Transceiver***

## *Features*

- Compatible to LIN Specification 2.0 and SAE J2602
- Operating voltage $V_S$ = 6 ... 18 V
- Low standby current consumption of typ. 15 µA in sleep mode
  - "noload" current < 200µA
- Linear low drop voltage regulator 5V/70mA ±2%
  - Output current limitation
- LIN-Bus Transceiver
  - Compatible to ISO9141 functions
  - Baud rate up to 20 kBaud
  - Slew rate control for best EME behavior
  - Low slew mode for optimized SAE J2602 transmission
  - High EMI immunity
  - High signal symmetry for using in RC – based slave nodes up to 2% clock tolerance
  - Current limitation
  - Bus input voltages -24V to 30V independent from VBat
- Wake-up via LIN bus traffic
- Reset output (default 8ms/4.65V)
  - Reset time adjustable to 4ms, 15ms and 30ms during IC final test
- Over temperature shutdown
- Automotive temperature range of –40°C to 125°C
- CMOS compatible interface to microcontroller
- Load dump protected (40V)
- Small SOIC8 package
- Pin compatible to the Melexis TH8061

### *Ordering Information*

| *Part No.* | *Temperature Range* | *Package* | *Version* | *POR-Time* |
|---|---|---|---|---|
| TH8062 KDC AA | K (-40 to 125 °C) | DC (SOIC8) | A | A (8ms) |
| **On Request** | | | | |
| TH8062 KDC AB | K (-40 to 125 °C) | DC (SOIC8) | A | B (4ms) |
| TH8062 KDC AC | K (-40 to 125 °C) | DC (SOIC8) | A | C (30ms) |
| TH8062 KDC AD | K (-40 to 125 °C) | DC (SOIC8) | A | D (15ms) |

## *General Description*

The TH8062 consists of a low-drop voltage regulator 5V/70mA and a LIN bus transceiver. The LIN transceiver is suitable for LIN bus systems conform to LIN specification revision 2.0 and SAE J2602.
The combination of voltage regulator and bus transceiver makes it possible to develop simple, but powerful and cheap slave nodes in LIN Bus systems.

## *Contents*

## *List of Figures*

# 1. Functional Diagram

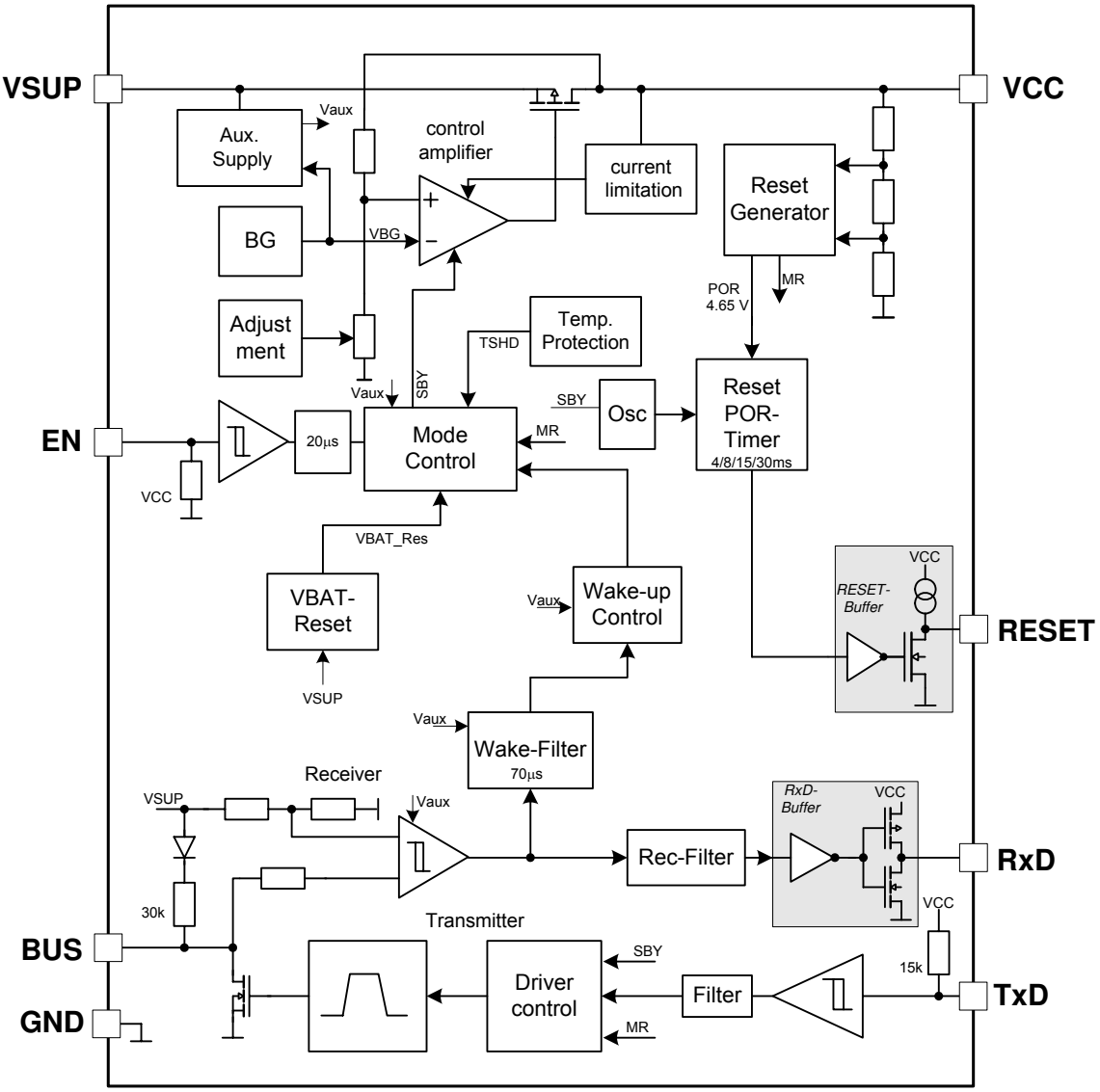


**Figure 1 - Block diagram**

# 2. Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.
The absolute maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device. Correct operating of the device cannot be guaranteed if any of these limits are exceeded.

## 2.1 Operating Conditions

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{SUP}$ | 6 | 18 | V |
| Output voltage | $V_{CC}$ | 4.85 | 5.15 | V |
| Operating ambient temperature | $T_A$ | -40 | +125 | °C |
| Junction temperature | $T_J$ | | +150 | °C |

## 2.2 Absolute Maximum Ratings

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage at VSUP | $V_{SUP}$ | | -1.0 | 18 | V |
| Jump start capability | | T ≤ 300 s | - | 30 | |
| Load dump | | T ≤ 500ms | - | 40 | |
| Input voltage at pin BUS | $V_{BUS}$ | | -24 | 30 | V |
| | | T ≤ 500ms | - | 40 | |
| Difference VSUP-VCC | $V_{SUP}$-$V_{CC}$ | | -0.3 | 40 | V |
| Input voltage at pin EN | $V_{INEN}$ | | -0.3 | $V_{SUP}$+0.3 | V |
| Input voltage at pin TxD, RxD, RESET | $V_{IN}$ | | -0.3 | $V_{CC}$+0.3 | V |
| Input current at pin EN, TxD, RxD, RESET | $I_{IN}$ | | -25 | 25 | mA |
| Input current for short circuit of pin VSUP and VCC | $I_{INSH}$ | | -500 | 500 | mA |
| ESD Capability on pin BUS, VBAT, GND | $ESD_{BUSHB}$ | Human body Model, 100pF via 1.5kΩ | -4 | 4 | kV |
| ESD Capability on pin TxD, RxD, EN, RESET, VCC | $ESD_{BUSHB}$ | Human body Model, 100pF via 1.5kΩ | -2 | 2 | kV |
| Power dissipation | $P_0$ | | Internal limited [1] | | |
| Thermal resistance from junction to ambient | $R_{THJA}$ | | | 130 | K/W |
| Junction temperature [2] | $T_J$ | | | 150 | °C |
| Storage temperature | $T_{STG}$ | | -55 | 150 | °C |

[1] See chapter 4.1 Safe Operating Area
[2] See chapter 3.5 Overtemperature Shutdown

## 2.3 Static Characteristics

Unless otherwise specified all values in the following tables are valid for $V_{SUP}$ = 6 to 18V and $T_{AMB}$ = -40 to 125°C. All voltages are referenced to ground (GND), positive currents flow into the IC.

### 2.3.1. Voltage Regulator and Reset Unit

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | T[1] |
|---|---|---|---|---|---|---|---|
| **VSUP** | | | | | | | |
| Operating voltage | $V_{SUP}$ | | 6 | 12 | 18 | V | B |
| Supply current, VCC „noload“ | $I_{Snl}$ | $V_{SUP}$ = 13V,<br>$V_{EN}$ = $V_{CC}$ ,<br>$C_{LOAD}$=22µF,<br>BUS: 1k to VSUP, | | 150 | 250 | µA | A |
| Supply current, „sleep mode“ | $I_{Ssleep}$ | $V_{SUP}$ = 13V, $V_{EN}$ = 0V,<br>BUS: 1k to VSUP | | 15 | 30 | µA | A |
| $V_{SUP}$ under voltage reset “off” threshold | $V_{SUVR\_OFF}$ | $V_{SUP}$ ramp up | 3.2 | 3.7 | 4.2 | V | A |
| $V_{SUP}$ under voltage reset “on” threshold | $V_{SUVR\_ON}$ | $V_{SUP}$ ramp down | 2.7 | 3.1 | 3.5 | V | A |
| $V_{SUP}$ under voltage reset hysteresis | $V_{SUVR\_HYS}$ | $V_{SUVR\_OFF}$ - $V_{SUVR\_ON}$ | 0.2 | | | V | A |
| **VCC** | | | | | | | |
| Output voltage VCC | $V_{CCn}$ | 6V ≤ $V_{SUP}$ ≤ 18V<br>1mA ≤ $I_{LOAD}$ ≤ 70mA<br>$T_A$ = 25°C<br>$T_A$ = -40°C to 125°C | <br><br>4.90<br>4.85 | 5.0 | <br><br>5.10<br>5.15 | V | A |
| | $V_{CCh}$ | 18V ≤ $V_{SUP}$ ≤ 40V<br>$I_{LOAD}$ = 10mA | 4.80 | | 5.25 | V | A |
| Drop-out voltage [2] | $V_{D10}$ | $I_{VCC}$ = 10mA | | 75 | 120 | mV | A |
| | $V_{D30}$ | $I_{VCC}$ = 30mA | | 220 | 350 | mV | A |
| | $V_{D70}$ | $I_{VCC}$ = 70mA | | 500 | 800 | mV | A |
| Line regulation | $V_{LNR}$ | 6V ≤ $V_{SUP}$ ≤ 18V | | | 20 | mV | A |
| Load regulation | $V_{LDR10}$ | $I_{LOAD}$ = 1mA → 10mA | | | 50 | mV | A |
| | $V_{LDR30}$ | $I_{LOAD}$ = 1mA → 30mA | | | 90 | mV | A |
| | $V_{LDR70}$ | $I_{LOAD}$ = 1mA → 70mA | | | 150 | mV | A |
| Output current limitation | $I_{VCC\_max}$ | $V_{SUP}$ > 0V | 80 | 110 | 140 | mA | A |
| Ripple Rejection on VSUP | PSRR | $V_{SUP}$ = 12V, $f_i$ = 120Hz, $V_{iP-P}$ = 1V, $I_{LOAD}$ = 10mA | | t.b.d | | dB | |
| Reset threshold - POR | $V_{RES(ON)}$ | VCC ramp up, t > $t_{rr}$ | 4.4 | 4.65 | 4.8 | V | A |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | T[1] |
|---|---|---|---|---|---|---|---|
| Reset threshold – low voltage reset | $V_{RES(OFF)}$ | VCC ramp down, t > $t_{rr}$ | 4.4 | 4.65 | 4.8 | V | A |
| Vres Hysteresis<br>$V_{RESHYS} = \lvert V_{RES(ON)} - V_{RES(OFF)} \rvert$ | $V_{RESHYS}$ | | | | 150 | mV | C |
| Master reset threshold | $V_{MRES}$ | | 3.0 | 3.15 | 3.3 | V | D |
| **Enable Input EN** | | | | | | | |
| Input voltage low | $V_{ENL}$ | | -0.3 | | 0.8 | V | B |
| Input voltage high | $V_{ENH}$ | | 2.0 | | $V_{SUP}$ +0.3 | V | B |
| Hysteresis | $V_{ENHYS}$ | | 50 | | 300 | mV | C |
| Pull-down resistor EN low | $R_{pdENL}$ | $0V \leq V_{EN} \leq 0.8V$ | 14 | 25 | 36 | kΩ | A |
| Pull-down current EN high | $I_{pdENH}$ | $V_{EN} \geq V_{ENH}$ | 0.5 | 2 | 10 | µA | A |
| **Output RESET** | | | | | | | |
| Output voltage low | $V_{OL1\_RESET}$ | $I_{OUT}$ = 1 mA, $V_{SUP} \geq 6$ V | | | 0.8 | V | A |
| Pull-up current | $I_{pu}$ | | -500 | -375 | -250 | µA | A |
| **Thermal Protection** | | | | | | | |
| Thermal shutdown | $T_{JSHD}$ | | 155 | | 180 | °C | D |
| Thermal recovery | $T_{JREC}$ | | 126 | | | °C | D |

[1] A = 100% serial test, B = Operating parameter, C = Only used for data characterization (cpk), D = Value guaranteed by design

[2] The nominal $V_{CC}$ voltage is measured at $V_{SUP}$ =12V. If the $V_{CC}$ voltage is 100mV below its nominal value then the voltage drop is $V_D = V_{SUP} - V_{CC}$.

### 2.3.2. LIN Bus Interface

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | T[1] |
|---|---|---|---|---|---|---|---|
| **General** | | | | | | | |
| Pull up current BUS (recessive) | $I_{INBUSpu}$ | $V_{BUS}$ = 18 V, $V_{SUP}$ = 6V | | | 20 | µA | A |
| Pull up resistor BUS | $R_{BUSpu}$ | $V_{SUP}$ = 12V, $V_{BUS}$ = 0V | 20 | 30 | 60 | kΩ | A |
| Reverse current BUS (recessive) | $-I_{INBUSrev}$ | $V_{SUP}$ = 12V, $V_{BUS}$ = 0V | -1 | | | mA | A |
| Reverse current BUS (loss of battery) | $I_{INBUS\_lob}$ | $V_{SUP}$ = 0V, 0V ≤ $V_{BUS}$ ≤ 18V | | | 20 | µA | A |
| Reverse current BUS (loss of ground) | $I_{INBUS\_log}$ | $V_{SUP}$= 12V, 0V ≤ $V_{BUS}$ ≤ 18V | -1 | | 1 | mA | A |
| **Receiver** | | | | | | | |
| Receive threshold | $V_{thr\_rec}$, $V_{thr\_dom}$ | 7.0 V ≤ $V_{SUP}$ ≤ 18 V | 0.4 | | 0.6 | $V_{SUP}$ | A |
| Centre point of receive threshold $V_{thr\_cnt} = (V_{thr\_rec}+V_{thr\_dom})/2$ | $V_{thr\_cnt}$ | | 0.475 | 0.5 | 0.525 | | A |
| Hysteresis of receive threshold $V_{thr\_hys} = V_{thr\_rec}-V_{thr\_dom}$ | $V_{thr\_hys}$ | | | 0.15 | 0.175 | | A |
| **Transmitter** | | | | | | | |
| Output voltage BUS (dominant) | $V_{BUSdom\_1}$ | $I_{BUS}$ = 40mA | | | 1.2 | V | A |
| Current limitation BUS | $I_{LIM}$ | $V_{BUS}$ = $V_{SUP}$, TxD = 0V | 41 | 120 | 200 | mA | A |
| **Input TxD** | | | | | | | |
| Pull-up resistor | $R_{pu\_TxD}$ | $V_{IN}$ = 0V | 9.5 | 15 | 23 | kΩ | A |
| Input voltage low TxD | $V_{IL}$ | | | | 0.3 | $V_{CC}$ | A |
| Input voltage high TxD | $V_{IH}$ | | 0.7 | | | $V_{CC}$ | A |
| **Output RxD** | | | | | | | |
| Output voltage Low RxD | $V_{OL}$ | $I_{OUT}$ = 1 mA | | | 0.8 | V | A |
| Output voltage High RxD | $V_{OH}$ | $I_{OUT}$ = -1 mA | $V_{CC}$ - 0.8 | | | V | A |

[1] A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk), D = Value guaranteed by design

## 2.4 Dynamic Characteristics

6V ≤ $V_{SUP}$ ≤ 18V, -40°C ≤ $T_A$ ≤ 125°C, unless otherwise specified

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | T[1] |
|---|---|---|---|---|---|---|---|
| **RESET** | | | | | | | |
| Reset time | $t_{Res}$ | $V_{SUP}$ = 12V,Vers. "A" | 5.6 | 8 | 10.4 | ms | A |
| | | $V_{SUP}$ = 12V,Vers. "B" | 2.8 | 4 | 5.2 | ms | A |
| | | $V_{SUP}$ = 12V,Vers. "C" | 10.5 | 15 | 19.5 | ms | A |
| | | $V_{SUP}$ = 12V,Vers. "D" | 21 | 30 | 39 | ms | A |
| Reset rising time | $t_{rr}$ | $V_{SUP}$ = 12V | 3.0 | 6.5 | 12 | µs | A |
| **Wake-up and Mode Select** | | | | | | | |
| Wake up time | $t_{wake\_BUS}$ | | 30 | 70 | 150 | µs | A |
| Debouncing time EN | $t_{deb\_EN}$ | | 2 | 6 | 15 | µs | D |
| Propagation delay EN to sleep mode | $t_{pd\_EN\_sleep}$ | $C_{Load}$ = 22µF<br>$R_{Load}$ = 169 Ohm | | | 400 | µs | A |
| Propagation delay EN to normal mode | $t_{pd\_EN\_norm}$ | $C_{Load}$ = 22µF<br>$R_{Load}$ = 169 Ohm | | | 400 | µs | A |
| Setup time TxD to EN for low slew mode | $t_{set\_TxD\_LS}$ | | 5 | | | µs | B |
| Hold time TxD after EN for low slew mode | $t_{hold\_TxD\_LS}$ | | 20 | | | µs | B |
| **General LIN Parameter** | | | | | | | |
| Slew rate rising edge BUS | $dV/dT_{rise}$ | Normal Mode<br>BUS-Load: 1kOhm/1nF | 0.8 | 1.5 | 2.5 | V/µs | C |
| Slew rate falling edge BUS | $dV/dT_{fall}$ | | -2.5 | -1.5 | -0.8 | V/µs | C |
| Slew rate rising edge BUS | $dV/dT_{rise}$ | Low Slew Mode<br>BUS-Load: 1kOhm/1nF | 0.3 | 0.8 | 1.3 | V/µs | C |
| Slew rate falling edge BUS | $dV/dT_{fall}$ | | -1.3 | -0.8 | -0.3 | V/µs | C |
| Receiver debouncing time | $t_{deb\_BUS}$ | | 1.5 | 2.8 | 4.0 | µs | C |
| Receiver propagation delay BUS->RxD | $t_{dr\_RxD}$<br>$t_{df\_RxD}$ | $C_{L(RXD)}$ = 50 pF | | | 6 | µs | A |
| Symmetry propagation delay BUS->RxD | $t_{dsym\_RxD}$ | $t_{dr\_RXD}$ - $t_{df\_RXD}$ | -2 | | 2 | µs | A |
| Internal capacity | $C_{BUS}$ | Pulse at BUS via 10kOhm with 0/10 V; VSUP = open | | 25 | 35 | pF | D |

| Parameter | Symbol | Condition | Min | Typ | Max | Unit | T[1] |
|---|---|---|---|---|---|---|---|
| **LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (20kbit/s)** | | | | | | | |
| Conditions: Normal slew mode; $V_{SUP}$ =7.0V to 18V; BUS loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF<br>TxD signal: $t_{Bit}$ = 50µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns | | | | | | | |
| Minimal recessive bit time [2] | $t_{rec(min)}$ | | 40 | 50 | 58 | µs | |
| Maximum recessive bit time [2] | $t_{rec(max)}$ | | 40 | 50 | 58 | µs | |
| Duty cycle 1 | $D_1$ | $D_1 = t_{rec(min)} / (2*t_{Bit})$ | 0.396 | | | | A |
| Duty cycle 2 | $D_2$ | $D_2 = t_{rec(max)} / (2*t_{Bit})$ | | | 0.581 | | A |
| **LIN transceiver parameter according to LIN Physical Layer Spec. rev. 2.0, table 3.4 (10.4kbit/s)** | | | | | | | |
| Conditions: Low slew mode; $V_{SUP}$ =7.0V to 18V; BUS loads: 1kΩ/1nF; 660Ω/6.8nF; 500Ω/10nF<br>TxD signal: $t_{Bit}$ = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns | | | | | | | |
| Minimal recessive bit time [2] | $t_{rec(min)}$ | | 80 | 96 | 113 | µs | |
| Maximum recessive bit time [2] | $t_{rec(max)}$ | | 80 | 96 | 113 | µs | |
| Duty cycle 1 | $D_1$ | $D_1 = t_{rec(min)} / (2*t_{Bit})$ | 0.417 | | | | A |
| Duty cycle 2 | $D_2$ | $D_2 = t_{rec(max)} / (2*t_{Bit})$ | | | 0.590 | | A |
| **LIN transceiver parameter according to SAE J2602 (10.4kbit/s)** | | | | | | | |
| Conditions: Low slew mode; $V_{SUP}$ =7.0V to 18V; BUS loads: 1kΩ/1nF;660Ω/6.8nF;500Ω/10nF<br>TxD signal: $t_{Bit}$ = 96µs, $t_{wH} = T_{wL} = t_{Bit}$; $t_{rise} = t_{fall}$ < 100ns | | | | | | | |
| Minimal recessive delay TxD -> BUS [2] | $t_{x\_rec\_min}$ | | | | 48 | µs | |
| Maximum recessive delay TxD -> BUS [2] | $t_{x\_rec\_max}$ | | | | 48 | µs | |
| Minimal dominant delay TxD -> BUS [2] | $t_{x\_dom\_min}$ | | | | 48 | µs | |
| Maximum dominant delay TxD -> BUS [2] | $t_{x\_dom\_max}$ | | | | 48 | µs | |
| Maximum rec. to dom. delay | $T_{r\_d\_max}$ | $t_{x\_rec\_max} - t_{x\_dom\_min}$ | | | 15.9 | µs | A |
| Maximum dom. to rec. delay | $T_{d\_r\_max}$ | $t_{x\_dom\_max} - t_{x\_rec\_min}$ | | | 17.2 | µs | A |

[1] A = 100% serial test, B = Operating parameter, C = only used for data characterization (cpk), D = Value guaranteed by design
[2] See chapter 2.5 Timing Diagrams

## 2.5 Timing Diagrams

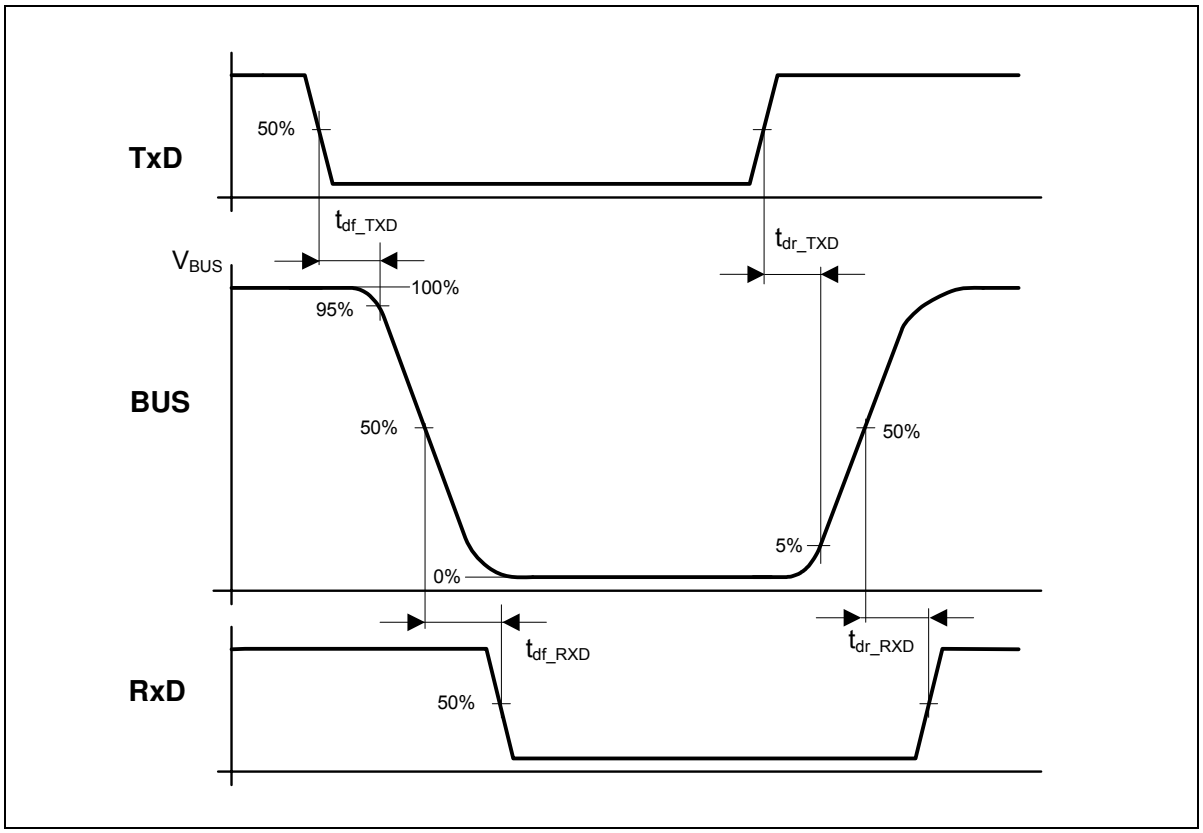


**Figure 2 - Timing diagram for propagation delays**

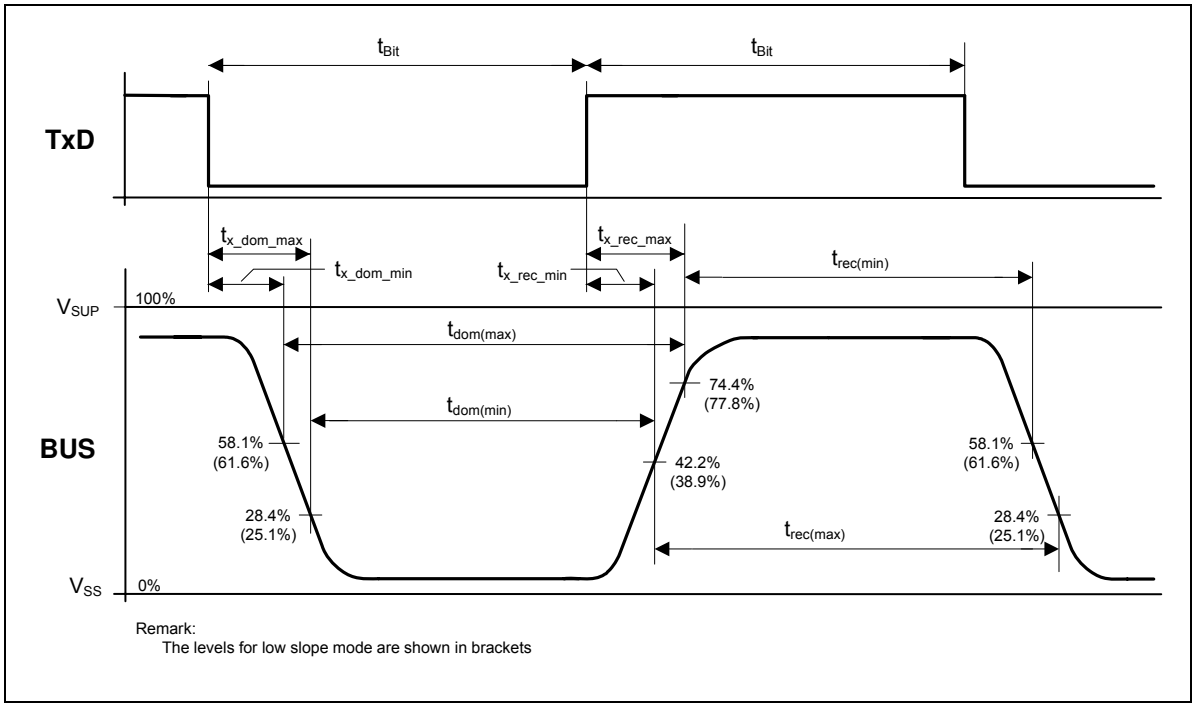


**Figure 3 - Timing diagram for duty cycle acc. to LIN 2.0 and J2602**

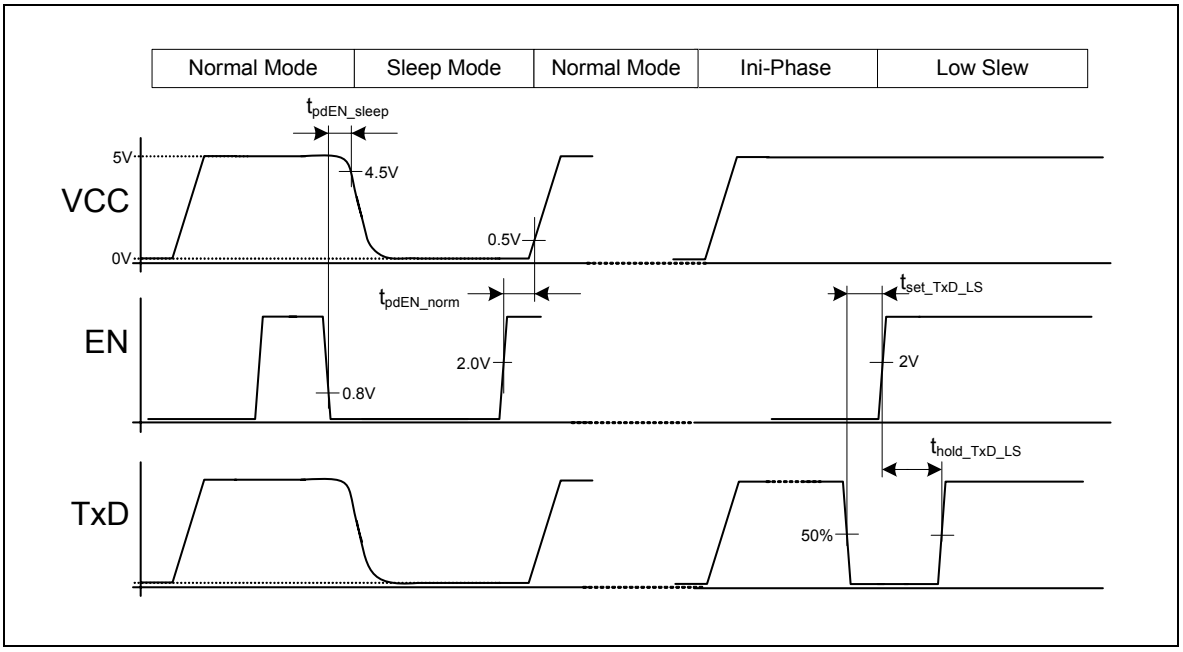


**Figure 4 - Timing Diagram for EN mode selection**

# 3. Functional Description

The TH8062 consists of a low drop voltage regulator 5V/70mA and a LIN bus transceiver, which is a bi-directional bus interface for data transfer between LIN bus and the LIN protocol controller.
Additionally integrated is a RESET unit with a fixed power-on-reset delay of 8ms (optional 4,15 or 30ms).

## 3.1 Operating Modes

The TH8062 provides three main operating modes “normal”, “sleep” and “low slew” and the intermediate states “Ini-state” and “thermal shutdown”. The main modes are fixed states defined by basic actions (VSUP start, EN or wake-up). The intermediate states are soft states. They aren’t defined by logical actions but by changes of voltage (VSUP, VCC) or junction temperature.

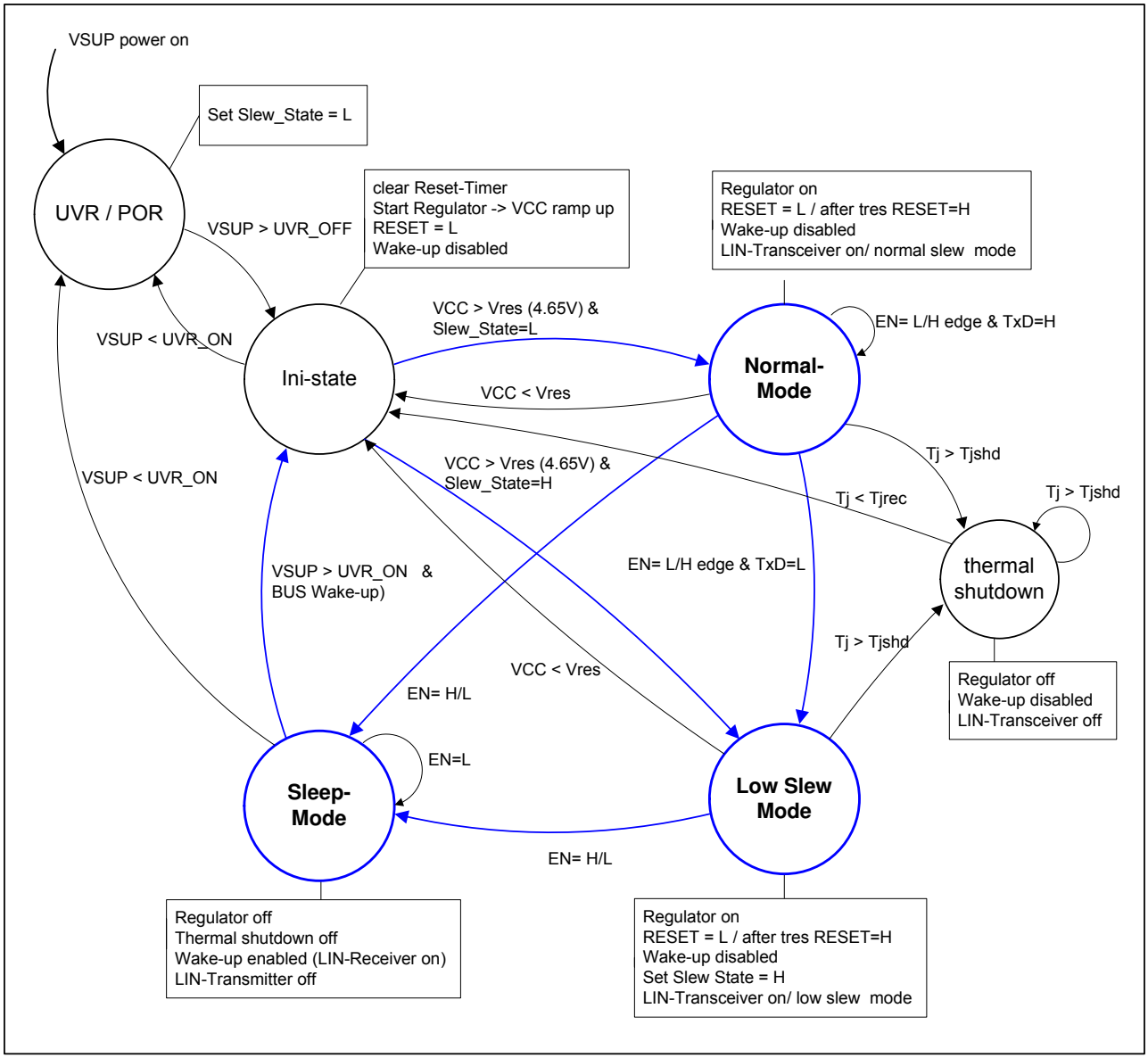


**Figure 5 - State diagram of operating modes**

### *Normal Mode*

This mode is the base mode. The bus transceiver is able to send with a max baud rate of 20kbit/s.
The whole TH8062 is active. Switching to normal mode can be done via the following actions:

- Start of $V_{SUP}$ or after under voltage reset
- Rising edge at EN (EN=high) and TxD=high (local wake-up)
- Activity on the LIN bus (remote wake-up)

### *Sleep Mode*

Sleep mode is most current saving. With a falling edge on EN (EN=low) the TH8062 is switched from normal mode into sleep mode. The voltage regulator and the reset unit will be switched off and the LIN transceiver is in recessive state.
Switching into sleep mode can be done independently from the current transceiver state. That means if the transmitter is in dominant state this state will be cancelled and it will be switched to recessive state.

### *Low Slew Mode*

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.
Switching to this mode is possible with a combination of rising edge on EN together with a low level on TxD. The IC operates in this mode until the next under voltage reset occurs.

### *POR-state*

This is the power-on-reset state of the TH8062, while Vsup < $V_{SUVR\_OFF}$. If the prior state was sleep mode, the TH8062 switches via the ini-state to normal mode.

### *Ini-state*

This is an intermediate state, which will pass through after switch on of VSUP or VCC. The TH8062 remains in this state if $V_{CC}$ is below $V_{RES}$ (Reset output = L) and Vsup > $V_{SUVR\_ON}$.

### *Thermal Shutdown*

If the junction temperature $T_J$ is higher than $T_{JSHD}$ (>155°C), the TH8062 will be switched into the thermal shutdown mode. The behaviour within this mode is comparable with the sleep mode except for LIN transceiver operating. The transceiver is completely disabled; no wake-up functionality is available.
If $T_J$ falls below the thermal recovery temperature $T_{JREC}$ (typ. 140°C) the TH8062 will be recover to the previous state (normal, sleep or low slew).

## 3.2 Initialization

Initialization starts when the power supply is switched on as well as every rising edge on of the TH8062 via the EN pin.

### *VSUP- Power-ON*

If $V_{SUP}$ is switched on the TH8062 starts to normal mode via the POR- and Ini-state. A combination of dynamic POR and under voltage reset circuitry generates a POR signal, which switches the TH8062 into normal mode. This power on behaviour is independent from the status of the EN-pin.

Power-on reset and under-voltage reset operate independent from each other, which secures the independence from the rise time of VSUP. During fast VSUP edges the power-on reset will be active. If the increasing of VSUP is very slow (> 1ms/V) and $V_{SUP}$ > $V_{SUVR\_OFF}$ (typ. 4.2V) the under voltage reset unit initializes the voltage regulator.

The effects of both POR circuits at different VSUP slopes will show in Figure 6.

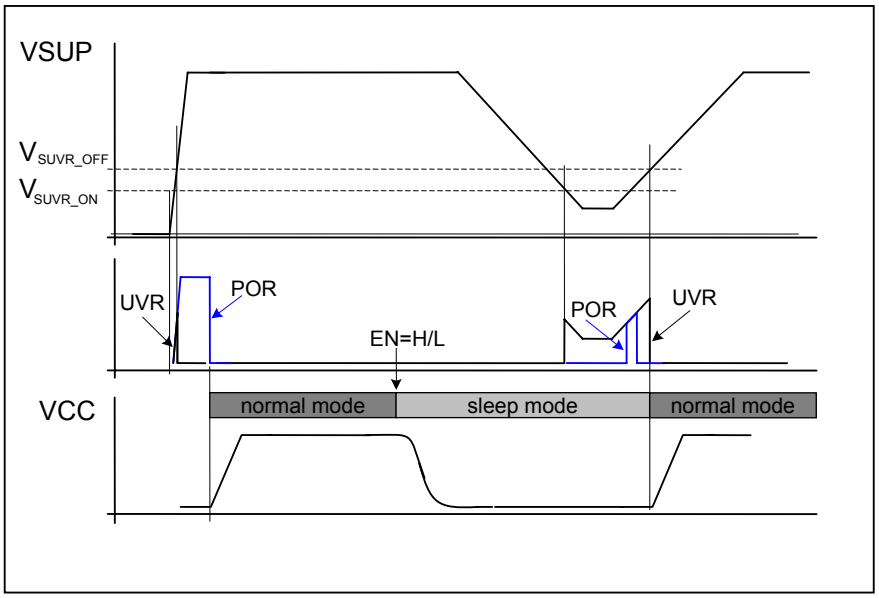


**Figure 6 - Operating of power-on and under-voltage reset**

After POR the voltage regulator starts and the VCC voltage will be output. If $V_{CC}$>$V_{MRes}$ the bus interface will be activated. If the $V_{CC}$ voltage level is higher than $V_{RES}$, the reset time $t_{Res}$ is started. After $t_{Res}$ the RESET output switches from low to high (see Figure 11).
The Initialization procedure operates after POR independent from the EN voltage.

### *Start of Linear Regulator via Wake-up*

The initialization is only being done for the VCC circuitry parts. This procedure begins with leaving the master reset state ($V_{CC}$ > $V_{MRes}$) and runs in the same manner as the VSUP-Power-On.

## 3.3 Wake-Up

If the regulator is put into sleep mode it can be woken up with the BUS interface. Every pulse on the BUS (high pulse or low pulse) with a pulse width of min. 70µs switches on the regulator.
The low slew mode has to be selected again if necessary.
After the BUS has woken up the regulator, it can only be switched off with a high level followed by a low level on the EN pin.

## 3.4 VSUP under voltage reset

The under voltage detection unit inhibits an undefined behaviour of the TH8062 under low voltage condition (VSUP < 4V). If VSUP drops below $V_{SUVR\_ON}$ (typ. 3.1V) the under voltage detection becomes active and the IC will be switched to POR state. The following increasing of VSUP above $V_{SUVR\_OFF}$ (typ. 3.7V) cancels this POR state and the voltage regulator starts with the initialization sequence.

***VSUP under voltage in Normal Mode***

Supply Voltages below $V_{SUVR\_OFF}$ do not influence the voltage regulator. The output voltage Vcc follows VSUP.

***VSUP under voltage in Sleep Mode***

No exit from the sleep mode will take place if the VSUP voltage drops down to $V_{SUVR\_ON}$ (typ. 3.5V). The under voltage reset becomes active (POR-state) if the voltage drops below 2.7V. As a result of this functioning, the sleep mode is left to the normal mode. If VSUP rises again above $V_{SUVR\_OFF}$ (typ. 4.2V) the IC initializes the voltage regulator and continues to work with the normal mode.

The under voltage reset unit secures stable functioning in the under voltage range of VSUP down to GND level. The dynamic Power-On-Reset secures a defined internal state independent from the duration of the VSUP drop, which guarantees a stable restart.

***VSUP under voltage in Low Slew Mode***

The behaviour of TH8062 at low VSUP voltages is equal to the sleep mode. The low slew mode will be cancelled, if VSUP drops below $V_{SUVR\_ON}$ in this mode. The TH8062 enters the normal mode, if VSUP rises again above $V_{SUVR\_OFF}$.

## 3.5 Overtemperature Shutdown

If the junction temperature is 155°C < $T_J$ < 175°C the over-temperature recognition will be activated and the regulator voltage will be switched off. The $V_{CC}$ voltage drops down, the reset state is entered and the bus-transceiver is switched off (recessive state).
After $T_J$ falls below 140°C the TH8062 will be initialized again (see Figure 11). This initialisation starts independently from the voltage levels on EN and BUS. Within the thermal shutdown mode the transceiver can not switch to the normal mode neither with local nor with remote wake-up.
The operation of the TH8062 is possible between $T_{Amax}$ (125°C) and the switch off temperature, but small parameter differences can appear.
After over-temperature switch-off the IC behaves as described in chapter 3.8 RESET.

## 3.6 LIN BUS Transceiver

The TH8062 has an integrated bi-directional bus interface device for data transfer between LIN bus and the LIN protocol controller.
The transceiver consists of a driver with slew rate control, wave shaping and current limitation and a receiver with high voltage comparator followed by a debouncing unit.

### *Transmit Mode*

During transmission the data at the pin TxD will be transferred to the BUS driver to generate a bus signal. To minimize the electromagnetic emission of the bus line, the BUS driver has an integrated slew rate control and wave shaping unit.
Transmitting will be interrupted in the following cases:

- Sleep mode
- Thermal Shutdown active
- Master Reset ($V_{CC}$ < 3.15V)

The recessive BUS level is generated from the integrated 30k pull up resistor in serial with an active diode This diode prevents the reverse current of $V_{BUS}$ during differential voltage between VSUP and BUS ($V_{BUS}$>$V_{SUP}$).
No additional termination resistor is necessary to use the TH8062 in LIN slave nodes. If this IC is used for LIN master nodes it is necessary that the BUS pin is terminated via an external 1kΩ resistor in series with a diode to VBAT.

### *Receive Mode*

The data signals from the BUS pin will be transferred continuously to the pin RxD. Short spikes on the bus signal are suppressed by the implemented debouncing circuit (τ = 2.8µs).

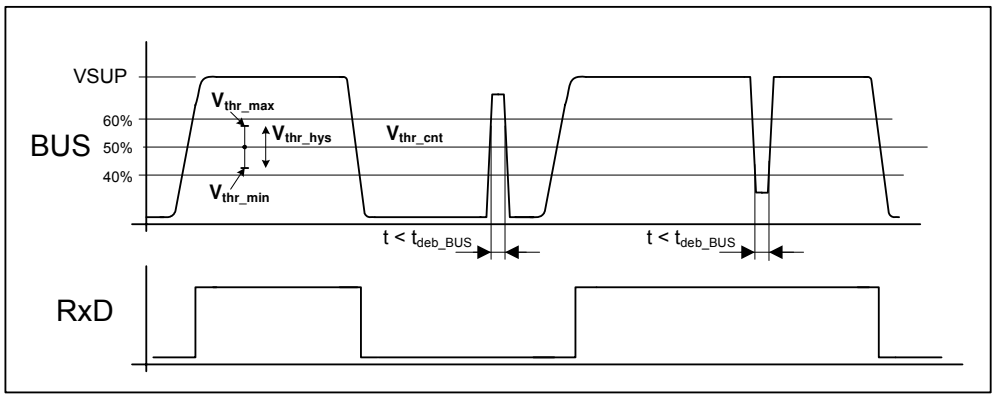


**Figure 7 - Receive mode impulse diagram**

The receive threshold values $V_{thr\_max}$ and $V_{thr\_min}$ are symmetrical to the centre voltage of 0.5*$V_{SUP}$ with a hysteresis of 0.175*$V_{SUP}$. Including all tolerances the LIN specific receive threshold values of 0.4*$V_{SUP}$ and 0.6*$V_{SUP}$ will be securely observed.

### *Slew Modes and Data rates*

The TH8062 is a ***constant slew rate*** transceiver which means that the bus driver works with a mode depended slew rate. In normal mode the slew rate is typical 1.6 V/µs (max. baudrate 20kbit/s) and in low slew mode typical 0.8 V/µs. The lower slew rate in low slew mode associated with a baud rate of 10.4kbit/s improves the EME behaviour.
The LIN transceiver of TH8062 is compatible to the physical layer specification according to LIN 2.0 specification for data rates up to 20kbit/s and the SAE specification J2602 for data rates up to 10.4kbit/s.
The constant slew rate principle is very robust against voltage drops and can operate with RC- oscillator systems with a clock tolerance up to ±2% between 2 nodes.

### *Low Slew Mode*

In this mode the slew rate is switched from the normal value of typ. 1.6V/µs to a low value of typ. 0.8V/µs. This mode is optimized to send with a maximum baud rate of 10.4kbit/s (acc. to SAE J2602). Because of this reduction of the slew rate the EME behaviour is improved especially in the frequency range of 100 kHz to 10MHz.

### *Input TxD*

The 5V input TxD controls directly the BUS level:

| | | |
|---|---|---|
| TxD = low | -> | BUS = low (dominant level) |
| TxD = high | -> | BUS = high (recessive level) |

The TxD pin has an internal pull up resistor connected to VCC. This guarantees that an open TxD pin generates a recessive BUS level.

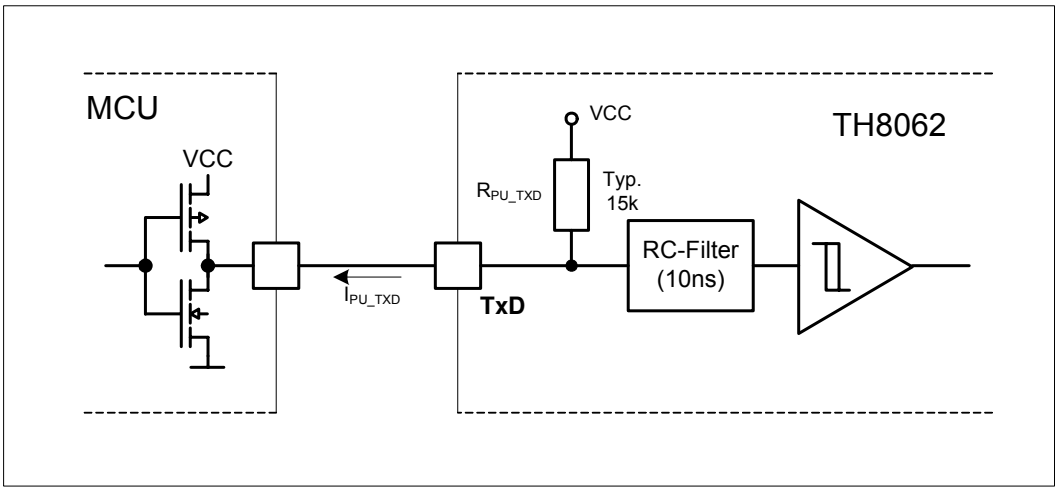


**Figure 8 - TxD input circuitry**

### *Output RxD*

The received BUS signal will be output to the RxD pin:

BUS < $V_{thr\_cnt}$ – 0.5 * $V_{thr\_hys}$ -> RxD = low
BUS > $V_{thr\_cnt}$ + 0.5 * $V_{thr\_hys}$ -> RxD = high

This output is a push-pull driver between VCC and GND with an output current of 1mA.

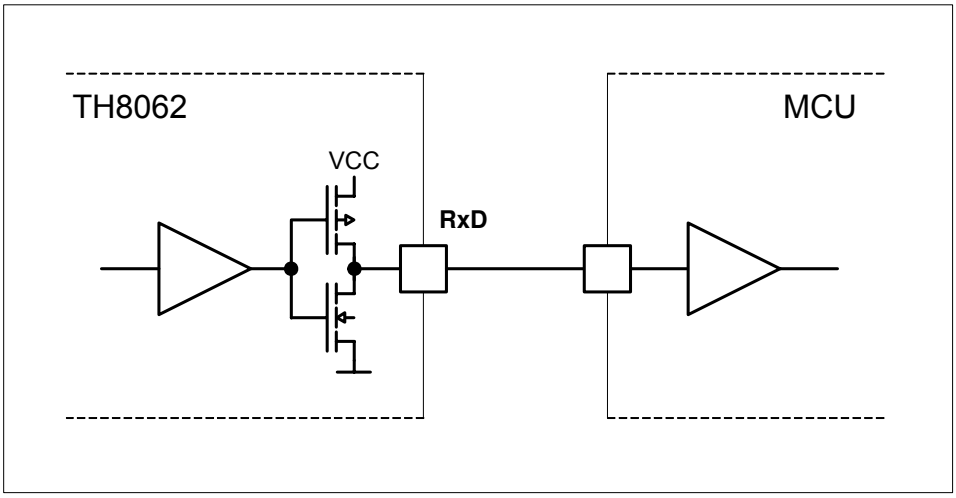


**Figure 9 - RxD output circuitry**

## 3.7 Linear Regulator

The TH8062 has an integrated low drop linear regulator with a p-channel-MOSFET as driving transistor. This regulator outputs a voltage of 5V ±3% and a current of ≤70mA within an input voltage range of 6V ≤ $V_{SUP}$ ≤ 18V. The current limitation unit limits the output current for short circuits or overload to 130mA respectively drop-down of the $V_{CC}$ voltage.

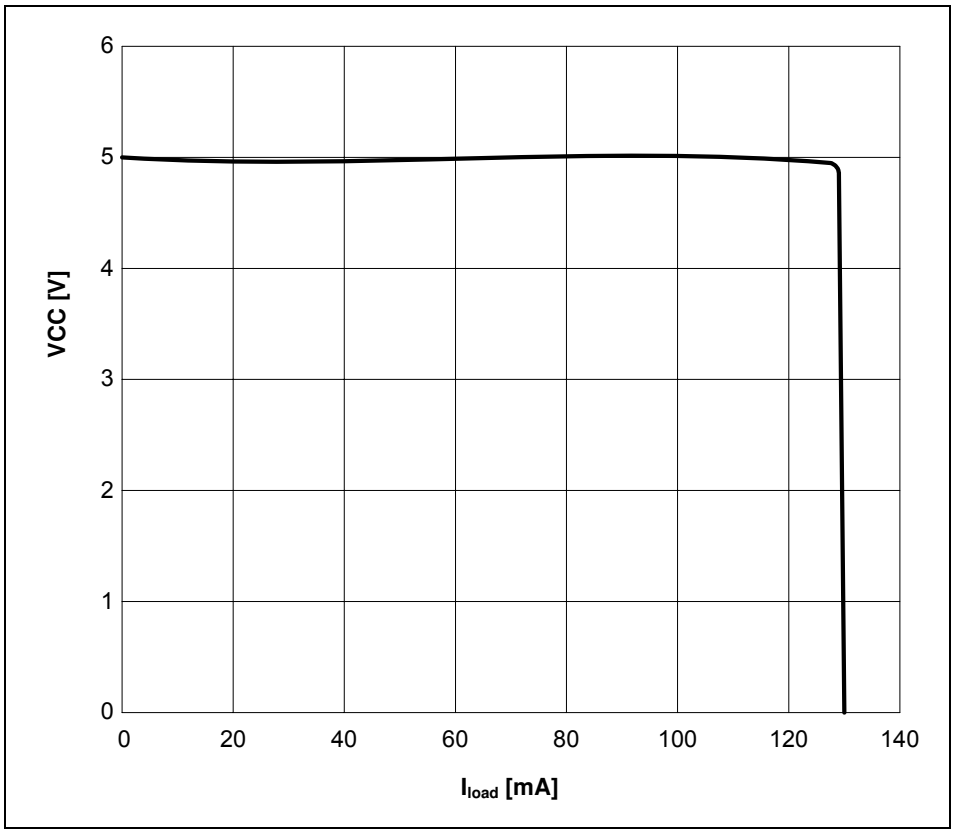


**Figure 10 - Characteristic of current limitation VCC = f ($I_{VCC}$)**

## 3.8 RESET

The TH8062 contains a reset unit which secures the correct initialization and generation of the reset signal. The RESET pin outputs the reset state of the TH8062. The POR timer will be started if $V_{SUP}$ is switched on and $V_{CC}$> POR threshold. After the time $t_{Res}$ the RESET output is switched from low to high.

The RESET unit combines a VCC low voltage detection unit with fixed POR timer  This output is switched from low to high if $V_{SUP}$ is switched on and $V_{CC}$>$V_{RES}$ after the time $t_{Res}$ .
All conditions which cause a drop of the $V_{CC}$ voltage will be detected from the low voltage reset unit which generates a reset signal. The TH8062 will be reinitialized if the $V_{CC}$ voltage rises above the low voltage limit. If the voltage $V_{CC}$ drops below $V_{RES}$ then the RESET output is switched from high to low after the time $t_{rr}$ has been reached. For this reason short breaks of the $V_{CC}$ voltage and uncontrolled reset generations will be inhibited. The circuitry of the RESET output driver guarantees, that the reset low level during decreasing of the $V_{CC}$ voltage will be kept secure (see Figure 12).

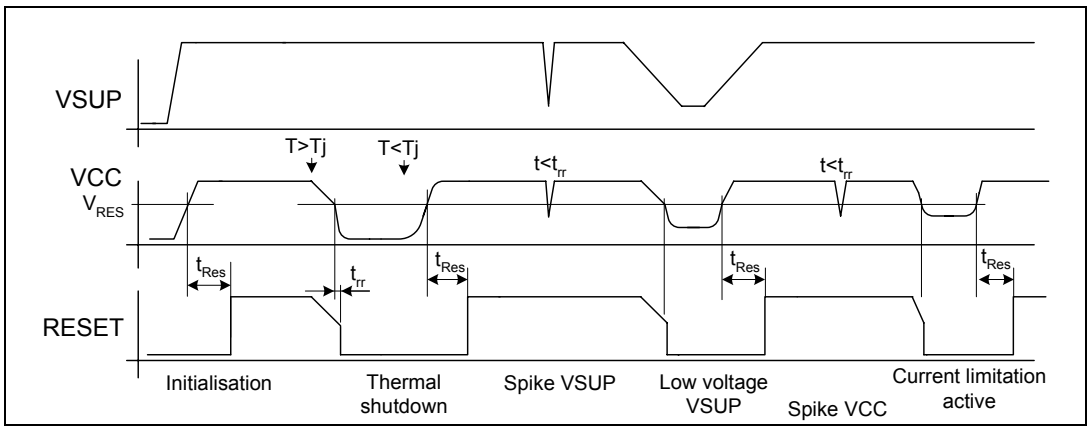


**Figure 11 - Reset behaviour**

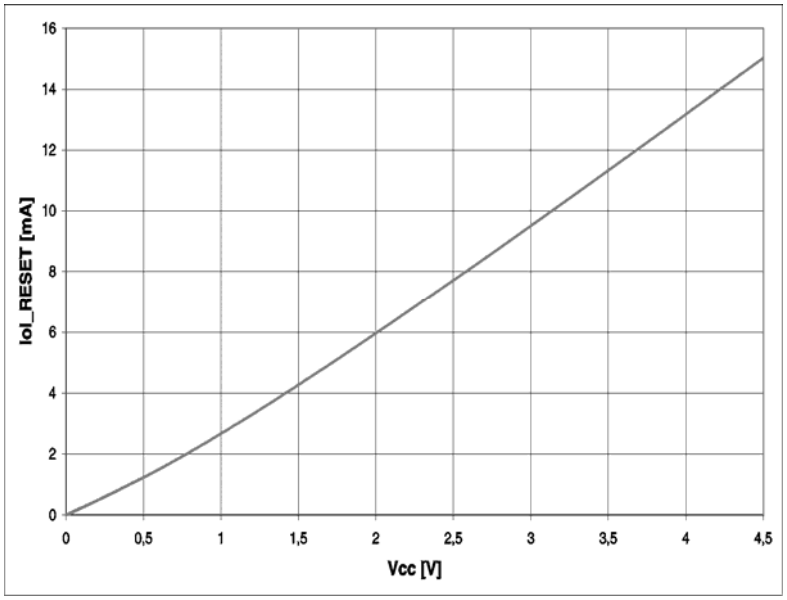


**Figure 12 - Output current of reset output vs. VCC voltage**

### 3.8.1. Programmability of Power-ON-Reset Delay

The standard POR time of the TH8062 is typ. 8ms. During final test it is possible to re-program this time to other values. Possible values are 4ms, 15ms and 30ms. See ordering code for details.

## 3.9 Mode Input EN

The TH8062 is switched into the sleep mode with a falling edge and into normal mode with a rising edge at the EN pin. The normal mode will be kept as long as EN = high.
The deactivation of TH8062 with a falling edge at EN can be done independently from the state of the bus-transceiver.

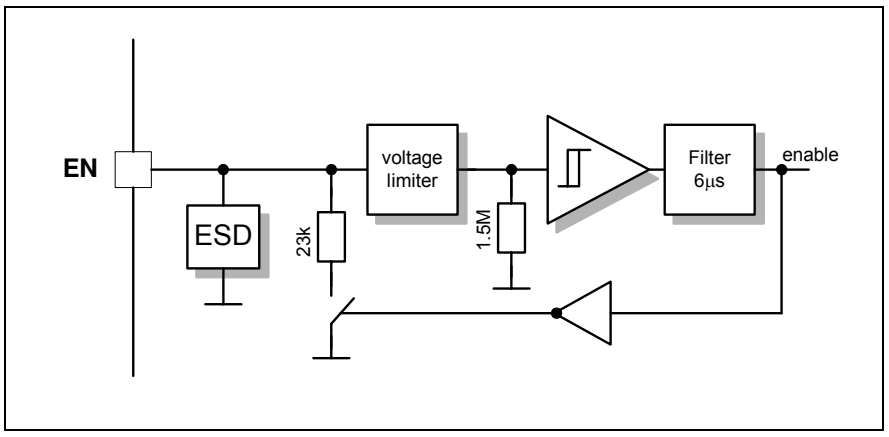


**Figure 13 - EN input circuitry**

The maximum input voltage is VSUP. The threshold is typ. 1.4V and therefore also 5V and 3.3V CMOS levels can be used as input signal. Figure 13 shows the internal circuitry of the EN pin.
The EN input has an internal pull down resistor of typ. 25k to secure that if this pin is not connected a low level will be generated. An input debouncing filter of 6µs suppresses effectively disturbance couplings via the EN pin
It will use different pull down resistors for normal and sleep mode to minimize the sleep mode current.
The wide input voltage range allows different EN control possibilities. If the EN input is connected to a CMOS output of the MCU, a falling edge switches the TH8062 into sleep mode (the regulator is also switched off). The wake up is only possible via the bus line.

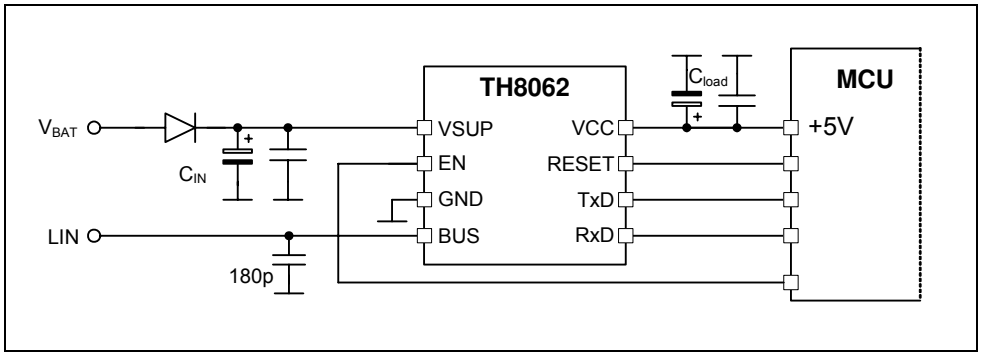


**Figure 14 - EN controlled via MCU**

If the application doesn't need the wake up capability of the TH8062 a direct connection EN to VSUP is possible. In this case the TH8062 operates in permanent normal mode. Also possible is the external (outside of the module) control of the EN line via a VBAT signal. If this is a direct VBAT signal an external reverse battery protection has to be added to the circuitry.

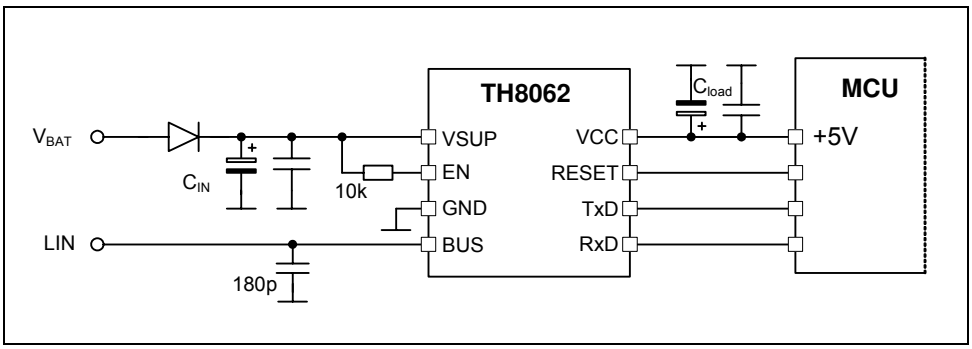


**Figure 15 - Permanent normal mode**

# 4. Application Hints

## 4.1 Safe Operating Area

The maximum power dissipation depends on the thermal resistance of the package and the PCB, the temperature difference between Junction and Ambient as well as the airflow.
The power dissipation can be calculated with:

$$P_D = (V_{SUP} - V_{CC}) * I_{VCC} + P_{D\_TX}$$

The power dissipation of the transmitter $P_{D\_TX}$ depends on the transceiver configuration and its parameters as well as on the bus voltage $V_{BUS}=V_{BAT}-V_D$, the resulting termination resistance $R_L$, the capacitive bus load $C_L$ and the bit rate. Figure 16 shows the dependence of power dissipation of the transmitter as function of $V_{SUP}$. The conditions for calculation of the power dissipation is $R_L$=500Ω, $C_L$=10nF, bit rate=20kbit and duty cycle on TxD of 50%

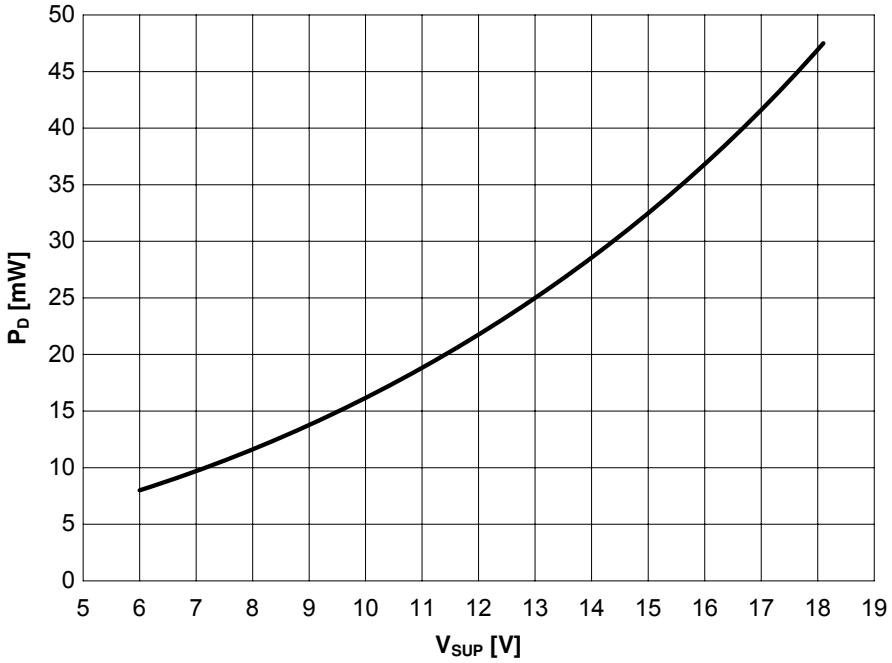


**Figure 16 - Power dissipation LIN transceiver @ 20kbit**

The permitted package power dissipation can be calculated:

$$P_{Dmax} = \frac{T_j - T_A}{R_{THJ-A}}$$

If we consider that $P_{D\_TX\_max}$= f ($V_{SUP}$) the max output current $I_{VCC}$ on $V_{CC\ can}$ be calculated:

$$I_{VCCmax} = \frac{\frac{T_j - T_A}{R_{THJ-A}} - P_{D\_TX\_max\ @\ VSUP}}{VSUP - VCC}$$

$T_J$ -$T_A$ is the temperature difference between junction and ambient and $R_{th}$ is the thermal resistance of the package. The thermal energy is transferred via the package and the pins to the ambient. This transfer can be improved with additional ground areas on the PCB as well as ground areas under the IC.

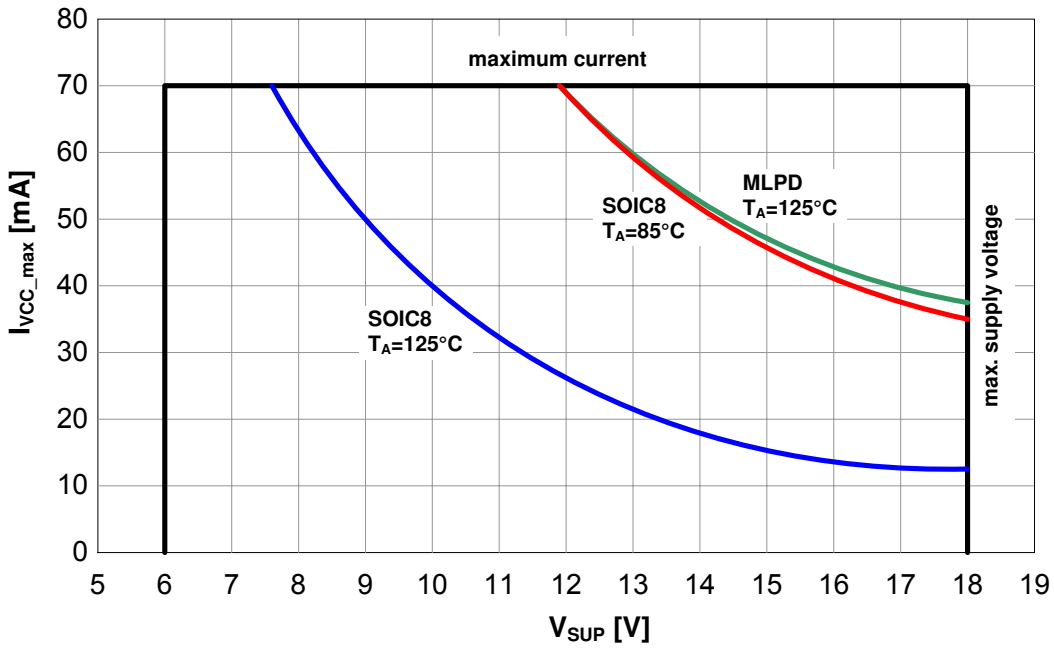


**Figure 17 - Save operating area**

The linear regulator of the TH8062 operates with input voltages up to 18V and can output a current of 70mA. The maximum power dissipation limits the maximum output current at high input voltages and high ambient temperatures. The output current of 70mA at an ambient temperature of $T_A$ = 125°C is only possible with small voltage differences between $V_{SUP}$ and $V_{CC}$. See Figure 17 for safe operating areas for different ambient temperatures.

## 4.2 Low Dropout Regulator

The voltage regulator of theTH8062 is a low dropout regulator (LDO) with a p-MOSFET as driving transistor. This kind of regulator has a standard pole, generated from the internal frequency compensation and an additional pole, which is dependent from the load and the load capacitance. This additional pole can cause an instable behaviour of the regulator! It is required a zero point to compensate this additional pole. It can be realised via an additional load resistor in series with a load capacitor. It is used for this compensation the equivalent series resistance (ESR) of the load capacitor. Every real capacitor is characterized with an ESR value. With the help of this ESR value an additional zero point is implemented into the amplification loop and therefore the result of the negative phase shift is compensated.
Because of this correlation the regulator has a stable operating area which is defined by the load resistance $R_L$, the load capacitor $C_L$ and the corresponding ESR value. The load resistance resp. load current is defined by the application itself and therefore the compensation of the pole can only be done via variation of the load capacitance and ESR value.

### *Input Capacitor on VSUP $C_{IN}$*

An input capacitance of $C_{IN} \geq 4.7\mu F$ is necessary. Higher capacitance values improve the line transient response and the supply noise rejection behaviour. The combination of electrolytic capacitor (e.g.100µF) in parallel with a ceramic RF-capacitor (e.g.100nF) archives good disturbance suppressing.
The input capacitor should be placed as close as possible (< 1cm) to the VSUP pin.