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## To Our Customers

CEL continues to offer industry leading semiconductor products from Japan. We are pleased to add new communication products from THine Electronics to our product portfolio.



## THC63LVD1027

Dual Link LVDS Repeater

#### **General Description**

The THC63LVD1027 LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.

THC63LVD1027 receives the dual link LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

#### **Features**

- 30bits/pixel dual link LVDS Receiver
- 30bits/pixel dual Link LVDS Transmitter
- Operating Temperature Range : -40°C~85°C
- Wide LVDS input skew margin: ± 480ps at 75MHz
- Accurate LVDS output timing: ± 250ps at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI

• Various line rate conversion modes supported Dual link input / Dual link output [clkout=1x clkin] Single link input / Dual link output [clkout=1/2x clkin] Dual link input / Single link output [clkout=2x clkin]

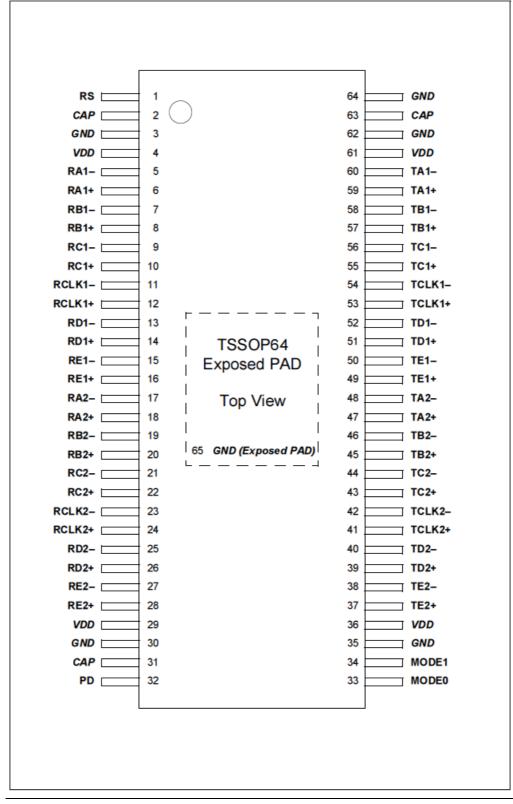
- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

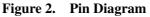
#### **Block Diagram** Dual In / Dual Out Mode THC63LVD1027 THine® THC63LVD1027 85MHz 85MH LVDS-Rx LVDS-Tx 30bit Date 30bit Data Distribution Mode Serialize e-Seriali THC63LVD1027 LVDS LVDS 85MH7 85MHz 1st Link 1st Link Inter-Link Multiplex 85MH: 8 PLL Clock De-Multi plex PLL Single In / Dual Out Mode THC63LVD1027 PLL Cloc Clock 67 5MHz 135MHz LVDS LVDS 67.5MHz 2nd Link 2nd Link LVDS-Rx LVDS-Tx 30bit Data 30bit Data Dual In / Single Out Mode Serialize Seriali LDO THC63LVD1027 Regulato 85MHz 42.5MHz 42.5MHz 3.3v Power Supp D ng Capacito

Figure 1. Block Diagram



#### Pin Diagram







## Pin Description

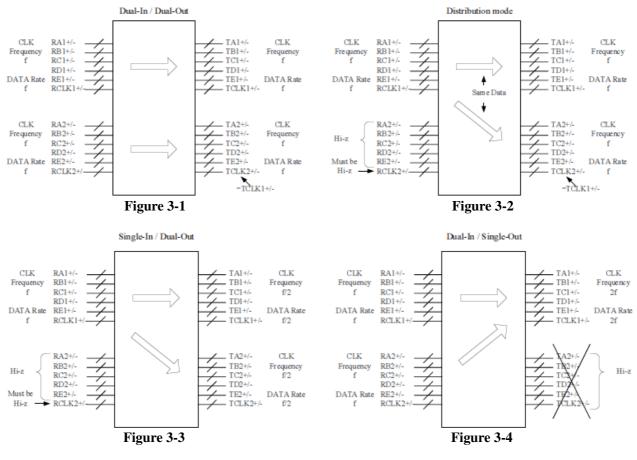
| Pin Name | Direction     | Туре   | Description  |  |  |  |  |
|----------|---------------|--------|--|--|--|--|--|
| RA1+/-   |               |        | LVDS data input for channel A of 1st Link  |  |  |  |  |
| RB1+/-   |               |        | LVDS data input for channel B of 1st Link  |  |  |  |  |
| RC1+/-   | Input         |        | LVDS data input for channel C of 1st Link  |  |  |  |  |
| RD1+/-   | -             |        | LVDS data input for channel D of 1st Link  |  |  |  |  |
| RE1+/-   | -             |        | LVDS data input for channel E of 1st Link  |  |  |  |  |
| RCLK1+/- | Input<br>LVDS |        | LVDS data input for thanker E of 1st Link  |  |  |  |  |
| RA2+/-   |               |        | LVDS clock input for 1st Link  |  |  |  |  |
| RB2+/-   | Input         |        | LVDS data input for channel B of 2nd Link  |  |  |  |  |
| RC2+/-   | -             |        | LVDS data input for channel C of 2nd Link  |  |  |  |  |
|          | -             |        | <b>^</b>   |  |  |  |  |
| RD2+/-   | -             |        | LVDS data input for channel D of 2nd Link  |  |  |  |  |
| RE2+/-   | -             |        | LVDS data input for channel E of 2nd Link  |  |  |  |  |
| RCLK2+/- |               | LVDS   | <b>LVDS clock input for 2nd Link</b><br>In Distribution and Single-in/Dual-out mode,RCLK2+/- must be Hi-Z.<br>(See "Mode selection" below in this page.) |  |  |  |  |
| TA1+/-   |               |        | LVDS data output for channel A of 1st Link   |  |  |  |  |
| TB1+/-   | -             |        | LVDS data output for channel B of 1st Link   |  |  |  |  |
| TC1+/-   | -             |        | LVDS data output for channel C of 1st Link   |  |  |  |  |
| TD1+/-   | -             |        | LVDS data output for channel D of 1st Link   |  |  |  |  |
| TE1+/-   | Output        |        | LVDS data output for channel E of 1st Link   |  |  |  |  |
| TCLK1+/- |               |        | LVDS data output for channel E of 1st Link   |  |  |  |  |
| TA2+/-   |               |        | LVDS data output for channel A of 2nd Link   |  |  |  |  |
| TB2+/-   | -             |        | LVDS data output for channel B of 2nd Link   |  |  |  |  |
|          | -             |        | ·  |  |  |  |  |
| TC2+/-   |               |        | LVDS data output for channel C of 2nd Link   |  |  |  |  |
| TD2+/-   |               |        | LVDS data output for channel D of 2nd Link   |  |  |  |  |
| TE2+/-   |               |        | LVDS data output for channel E of 2nd Link   |  |  |  |  |
| TCLK2+/- |               |        | LVDS clock output for 2nd Link   |  |  |  |  |
| PD       |               |        | Power Down<br>H: Normal operation<br>L: Power down state, all LVDS output signals turn to Hi-Z   |  |  |  |  |
| RS       |               |        | LVDS output swing level selection<br>H: Normal swing<br>L: Reduced swing   |  |  |  |  |
| MODE1    | Input         | LV-TTL | Mode selection   |  |  |  |  |
| MODE0    | r             |        | MODE1 MODE0 RCLK2+/- Description   |  |  |  |  |
|          |               |        | L         L         Clkin         Dual-in/Dual-out mode           L         L         Hi-Z         Distribution mode                                     |  |  |  |  |
|          |               |        | H L Hi-Z Single-in/Dual-out mode   |  |  |  |  |
|          |               |        | L H Clkin Dual-in/Single-out mode  |  |  |  |  |
|          |               |        | H H - Reserved   |  |  |  |  |
|          |               |        | In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z.  |  |  |  |  |
| VDD      | _             |        | 3.3V power supply pins   |  |  |  |  |
| GND      | Power         | -      | Ground pins (Exposed PAD is also Ground)   |  |  |  |  |
| CAP      |               |        | <b>Decoupling capacitor pins</b><br>These pins should be connected to external decoupling capacitors(Ccap).  |  |  |  |  |
|          |               |        | Recommended Ccap is $0.1\mu$ F + $0.01\mu$ F.  |  |  |  |  |



## Mode Setting

| Table 2. Mode Setting |          |              |               |  |  |  |
|-----------------------|----------|--------------|---------------|--|--|--|
| Input/Output          | RCLK2+/- | MODE1        | MODE0         |  |  |  |
|                       |          | (Input mode) | (Output mode) |  |  |  |
|                       |          | H: Single    | H: Single     |  |  |  |
|                       |          | L: Dual      | L: Dual       |  |  |  |
| Dual-In/Dual-Out      | CLK in   | L            | L             |  |  |  |
| (Fig.3-1,14-1)        |          |              |               |  |  |  |
| Distribution          | Hi-Z     | L            | L             |  |  |  |
| (Fig.3-2,14-2)        |          |              |               |  |  |  |
| Single-In/Dual-Out    | Hi-Z     | Н            | L             |  |  |  |
| (Fig.3-3,14-3)        |          |              |               |  |  |  |
| Dual-In/Single-Out    | CLK in   | L            | Н             |  |  |  |
| (Fig.3-4,14-4)        |          |              |               |  |  |  |
| Reserved              | -        | Н            | Н             |  |  |  |

## Signal Flow for Each Setting





#### Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

| PD | RCLK1+/- | RCLK2+/- | Output                      |
|----|----------|----------|-----------------------------|
| L  | *        | *        | All Hi-Z                    |
| Н  | Hi-Z     | *        | All Hi-Z                    |
| Н  | CLK in   | CLK in   | Refer to p.4 Mode Setting # |
| Н  | CLK in   | Hi-Z     | Refer to p.4 Mode Setting # |

#### Table 3. Output Control

\*: Don't care

#: If a particular input data pair is Hi-Z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting Hi-Z state.

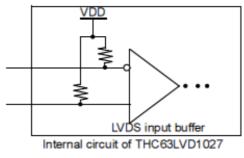


Figure 4. Fail Safe Circuit



## Absolute Maximum Ratings

| Table 4 | Absolute | Maximum    | Rating |
|---------|----------|------------|--------|
|         | Absolute | Maaiiiuiii | Naung  |

|                                  |      | -                    |      |
|----------------------------------|------|----------------------|------|
| Parameter                        | Min  | Max                  | Unit |
| Power Supply Voltage             | -0.3 | +4.0                 | V    |
| LVDS Input Voltage               | -0.3 | V <sub>DD</sub> +0.3 | V    |
| Junction Temperature             | -    | 125                  | °C   |
| Storage Temperature              | -55  | 125                  | °C   |
| Reflow Peak Temperature / Time   | -    | 260 / 10sec          | °C   |
| Maximum Power Dissipation @+25°C | -    | 2.5                  | W    |

## **Operating Conditions**

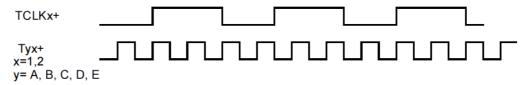
Table 5. Operating Condition

| Symbol                  | Paramete            | Parameter |     |     | Max  | Unit  |  |
|-------------------------|---------------------|-----------|-----|-----|------|-------|--|
| Та                      | Operating Ambient 7 | -40       | 25  | +85 | °C   |       |  |
| V <sub>DD</sub>         | Power Supply Voltag | ge        | 3.0 | 3.3 | 3.6  | V     |  |
|                         | Dual-In/Dual-Out    | Input     | 20  | -   | 85   | MHz   |  |
|                         | Dual-III/Dual-Out   | Output    | 20  | -   | 85   | MITZ  |  |
|                         | Distribution        | Input     | 20  | -   | 85   | MHz   |  |
| Б                       | Distribution        | Output    | 20  | -   | 85   | MITIZ |  |
| <b>F</b> <sub>clk</sub> | Single-In/Dual-Out  | Input     | 40  | -   | 135  | MHz   |  |
|                         | Single-III/Dual-Out | Output    | 20  | -   | 67.5 | MITZ  |  |
|                         | Dual-In/Single-Out  | Input     | 20  | -   | 42.5 | MHz   |  |
|                         | Duai-m/Siligle-Out  | Output    | 40  | -   | 85   | MINZ  |  |

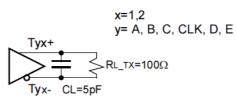


## Power Consumption

|                               |   | Tab                | le 6. Power Cons                                       | umption                 |   |      |   |      |
|-------------------------------|---|--------------------|--|-------------------------|---|------|---|------|
| Symbol                        | Parameter   |                    | Conditions   |                         | Min   | Тур. | Max   | Unit |
|                               |   |                    | CLKIN=40MHz  |                         | -   | -    | 265   |      |
|                               |   | Dual-In/Dual-Out   | CLKIN=65MHz  |                         | -   | -    | 305   |      |
|                               |   | Duai-III/Duai-Out  | CLKIN=75MHz  |                         | -   | -    | 325   | ША   |
|                               |   |                    | CLKIN=85MHz  |                         | -   | -    | 340   |      |
|                               | $\begin{array}{c} \begin{array}{c} \hline \\ \text{CLKIN=40MHz} \\ \hline \\ \text{CLKIN=65MHz} \\ \hline \\ \hline \\ \text{CLKIN=75MHz} \\ \hline \\ \hline \\ \\ \text{CLKIN=85MHz} \end{array} \\ \begin{array}{c} \hline \\ \\ \\ \\ \\ \\ \end{array} \\ \begin{array}{c} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \end{array} \end{array} \\ \begin{array}{c} \hline \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ $ | -                  | -  | 215                     |   |      |   |      |
|                               |   | Distribution       | CLKIN=65MHz  |                         | $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ |      |   |      |
|                               |   | Distribution       | CLKIN=75MHz  | $R_{L} T_x = 100\Omega$ |   | mA   |   |      |
| Operating Current CLKIN=85MHz | 2_14  | -                  | -  | 260                     |   |      |   |      |
| т                             | (Worst Case Pattern)  |                    | CLKIN=40MHz  | CL=5pF<br>RS=VDD        | -   | -    | 175   | mA   |
| <b>I</b> <sub>CCW</sub>       |   |                    | CLKIN=65MHz  |                         | -   | -    | 190   |      |
|                               | Fig 5.  |                    | CLKIN=75MHz  |                         | -   | -    | 200   |      |
|                               |   | Single-In/Dual-Out | $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | 210                     |   |      |   |      |
|                               |   |                    | CLKIN=112MHz   |                         | -   | -    | $\begin{array}{c cccc} - & 265 \\ - & 305 \\ - & 325 \\ - & 340 \\ - & 215 \\ - & 235 \\ - & 245 \\ - & 260 \\ - & 175 \\ - & 190 \\ - & 200 \\ - & 175 \\ - & 190 \\ - & 200 \\ - & 210 \\ - & 230 \\ - & 250 \\ - & 215 \\ - & 235 \\ - & 245 \\ - & 260 \end{array}$ |      |
|                               |   |                    | CLKIN=135MHz   |                         | $\begin{array}{c ccccccccccccccccccccccccccccccccccc$   |      |   |      |
|                               |   |                    | CLKIN=20MHz  |                         | -   | -    | 215   |      |
|                               |   | Dual In/Single Out | CLKIN=32.5MHz  |                         | -   | -    | 235   | mA   |
|                               |   | Dual-In/Single-Out | CLKIN=37.5MHz  |                         | -   | -    | 245   | 1    |
|                               |   |                    | CLKIN=42.5MHz  |                         | -   | -    | 260   |      |
| I <sub>CCS</sub>              | Power Down Current  | -                  | -  | -                       | -   | -    | 8   | mA   |







LVDS Output Load

Figure 6. LVDS Output Load



## **Electrical Characteristics**

## **DC Specifications**

| Symbol              | Parameter                        | Conditions         | Min | Тур | Max | Unit |
|---------------------|----------------------------------|--------------------|-----|-----|-----|------|
| V <sub>CAP</sub>    | Capacitor pin appearance voltage | $C_{CAP}=0.1\mu F$ | -   | 1.8 | -   | V    |
| V <sub>IL</sub>     | LV-TTL Input Low Voltage         | -                  | GND | -   | 0.8 | V    |
| V <sub>IH</sub>     | LV-TTL Input High Voltage        | -                  | 2.0 | -   | VDD | V    |
| I <sub>IN_TTL</sub> | LV-TTL Input Leakage Current     | -                  | -4  | -   | +4  | μΑ   |

#### Table 7. DC Specifications

## LVDS Receiver DC Specifications

#### Table 8. LVDS Receiver DC Specifications

| Symbol             | Parameter                           | Conditions                   | Min  | Тур | Max  | Unit |
|--------------------|-------------------------------------|------------------------------|------|-----|------|------|
| V <sub>IN_RX</sub> | LVDS-Rx Input Voltage Range         | -                            | 0.3  | -   | 2.1  | V    |
| V <sub>IC_RX</sub> | LVDS-Rx Common Voltage              | -                            | 0.6  | 1.2 | 1.8  | v    |
| V <sub>TH_RX</sub> | LVDS-Rx Differential High Threshold | $\mathbf{V} = 1.2\mathbf{V}$ | -    | -   | +100 |      |
| V <sub>TL_RX</sub> | LVDS-Rx Differential Low Threshold  | $V_{IC_{RX}} = 1.2V$         | -100 | -   | -    | mV   |
| V <sub>ID_RX</sub> | LVDS-Rx Differential Input Voltage  | -                            | 100  | -   | 600  |      |
|                    |                                     | PD=VDD                       | -0.3 | -   | +0.3 | mA   |
| I <sub>IN_RX</sub> | LVDS-Rx Input Leakage Current       | PD=GND<br>Vin=GND or VDD     | -10  | -   | +10  | μΑ   |

## LVDS Transmitter DC Specifications

#### **Table 9. LVDS Transmitter DC Specifications**

| Symbol             | Parameter  | (                     | Min                          | Тур   | Max  | Unit  |    |  |
|--------------------|--|-----------------------|------------------------------|-------|------|-------|----|--|
| V <sub>OC_TX</sub> | LVDS-Tx Common Voltage                               |                       | -                            | 1.125 | 1.25 | 1.375 | V  |  |
| $\Delta V_{OC_TX}$ | Change in VOC between complementary output states    | D                     | -                            | -     | -    | 35    | mV |  |
|                    | LVDS-Tx Differential                                 | $R_{L_{TX}} =$        | Normal Swing                 | 250   | 350  | 450   | V  |  |
|                    | Output Threshold                                     | 100Ω                  | Reduced Swing                | 100   | 200  | 300   | mV |  |
| $\Delta V_{OD_TX}$ | Change in VOD between<br>complementary output states |                       | -                            | -     | -    | 35    | mV |  |
| I <sub>OS_TX</sub> | LVDS-Tx Output Short Current                         | V <sub>DD</sub> =3.3V | V <sub>out</sub> =GND        | -24   | -    | -     | mA |  |
| I <sub>OZ_TX</sub> | LVDS-Tx Output Tri-state Current                     | PD=GND                | V <sub>out</sub> =GND to VDD | -10   | -    | +10   | μΑ |  |

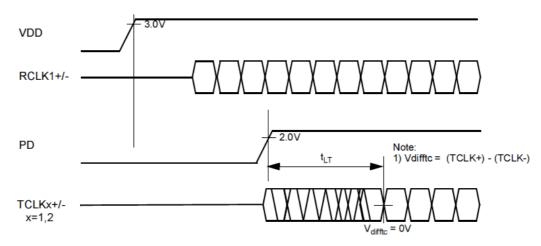


## **AC Specifications**

| Symbol             | Parameter                                    | Conditions         |                      | Min                         | Тур  | Max                         | Unit |
|--------------------|--|--------------------|----------------------|-----------------------------|--|-----------------------------|------|
| t <sub>LT</sub>    | Phase Lock Loop Set Time<br>(Fig 7.)         | -                  | -                    | -                           | -  | 10                          | ms   |
|                    | Dual-In/Dual-Out                             | CLKIN=75MHz        | 9t <sub>RCP</sub> +3 | 9t <sub>RCP</sub> +5        | 9t <sub>RCP</sub> +7                       |                             |      |
| 4                  | <b>t</b> <sub>DL</sub> Data Latency (Fig 8.) | Distribution       | CLKIN=75MHz          | 9t <sub>RCP</sub> +3        | 9t <sub>RCP</sub> +5                       | 9t <sub>RCP</sub> +7        | 20   |
| ι <sub>DL</sub>    |  | Single-In/Dual-Out | CLKIN=75MHz          | (11+2/7)t <sub>RCP</sub> +3 | (11+2/7)t <sub>RCP</sub> +5                | (11+2/7)t <sub>RCP</sub> +7 | ns   |
|                    |  | Dual-In/Single-Out | CLKIN=37.5MHz        | (11+2/7)t <sub>RCP</sub> +3 | (11+2/7)t <sub>RCP</sub> +5                | (11+2/7)t <sub>RCP</sub> +7 |      |
| t <sub>DEH</sub>   | DE Input High Time (Fig 9.)                  |                    | -                    | 2t <sub>RCP</sub>           | -  | -                           |      |
| t <sub>DEL</sub>   | DE Input Low Time (Fig 9.)                   | Single-In/Dual-Out | -                    | 2t <sub>RCP</sub>           | -  | -                           | ns   |
| t <sub>DEINT</sub> | DE Input Period (Fig 9.)                     |                    | -                    | 4t <sub>RCP</sub>           | Must be 2n t <sub>RCP</sub><br>(n=integer) | -                           |      |

### Table 10. AC Specifications

## AC Timing Diagrams



| Figure 7. | Phase | Lock | Loop | Set | Time |
|-----------|-------|------|------|-----|------|
|-----------|-------|------|------|-----|------|



## AC Timing Diagrams(Continued)

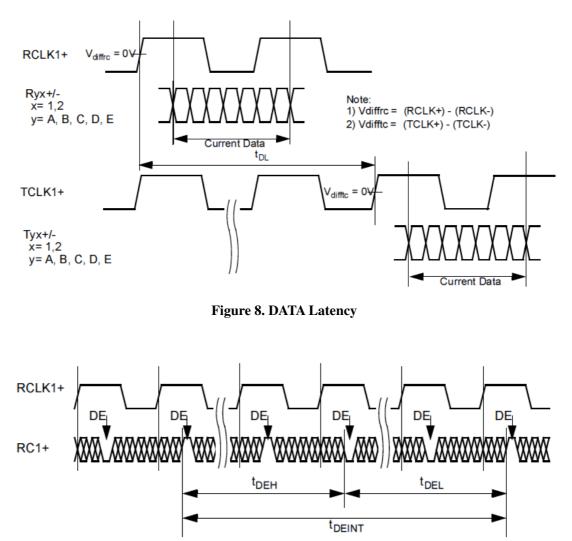


Figure 9. Single Link Input / Dual Link Output Mode RC1(DE) Input Timing



## LVDS Receiver AC Specifications

| Symbol            | Parameter                            | Conditions                  | Min                                    | Тур                 | Max                                    | Unit |
|-------------------|--------------------------------------|-----------------------------|--|---------------------|--|------|
| t <sub>RCP</sub>  | LVDS Clock Period                    | -                           | 7.4                                    | -                   | 50                                     |      |
| t <sub>RCH</sub>  | LVDS Clock High Duration             | -                           | 2/7t <sub>RCP</sub>                    | 4/7t <sub>RCP</sub> | 5/7t <sub>RCP</sub>                    | ns   |
| t <sub>RCL</sub>  | LVDS Clock Low Duration              | -                           | 2/7t <sub>RCP</sub>                    | 3/7t <sub>RCP</sub> | 5/7t <sub>RCP</sub>                    |      |
|                   |                                      | CLKIN=75MHz <sup>(1)</sup>  | 480                                    | -                   | -                                      |      |
| t <sub>RSUP</sub> | LVDS Data Input Setup Margin         | CLKIN=112MHz <sup>(1)</sup> | 250                                    | -                   | -                                      | ps   |
|                   |                                      | CLKIN=135MHz <sup>(1)</sup> | 220                                    | -                   | -                                      |      |
|                   |                                      | CLKIN=75MHz <sup>(1)</sup>  | 480                                    | -                   | -                                      |      |
| t <sub>RHLD</sub> | LVDS Data Input Hold Margin          | CLKIN=112MHz <sup>(1)</sup> | 250                                    | -                   | -                                      | ps   |
|                   |                                      | CLKIN=135MHz <sup>(1)</sup> | 220                                    | -                   | -                                      |      |
| t <sub>RIP6</sub> | LVDS Data Input Position 6           | -                           | 2/7t <sub>RCP</sub> -t <sub>RHLD</sub> | $2/7t_{\rm RCP}$    | $2/7t_{RCP}+t_{RSUP}$                  |      |
| t <sub>RIP5</sub> | LVDS Data Input Position 5           | -                           | 3/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 3/7t <sub>RCP</sub> | 3/7t <sub>RCP</sub> +t <sub>RSUP</sub> |      |
| t <sub>RIP4</sub> | LVDS Data Input Position 4           | -                           | 4/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 4/7t <sub>RCP</sub> | 4/7t <sub>RCP</sub> +t <sub>RSUP</sub> |      |
| t <sub>RIP3</sub> | LVDS Data Input Position 3           | -                           | 5/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 5/7t <sub>RCP</sub> | 5/7t <sub>RCP</sub> +t <sub>RSUP</sub> | ps   |
| t <sub>RIP2</sub> | LVDS Data Input Position 2           | -                           | 6/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 6/7t <sub>RCP</sub> | 6/7t <sub>RCP</sub> +t <sub>RSUP</sub> |      |
| t <sub>RIP1</sub> | LVDS Data Input Position 1           | -                           | 7/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 7/7t <sub>RCP</sub> | 7/7t <sub>RCP</sub> +t <sub>RSUP</sub> |      |
| t <sub>RIP0</sub> | LVDS Data Input Position 0           | -                           | 8/7t <sub>RCP</sub> -t <sub>RHLD</sub> | 8/7t <sub>RCP</sub> | 8/7t <sub>RCP</sub> +t <sub>RSUP</sub> |      |
| t <sub>CK12</sub> | Skew Time Between<br>RCLK1 and RCLK2 | -                           | -0.3 t <sub>RCP</sub>                  | -                   | +0.3 t <sub>RCP</sub>                  | ps   |

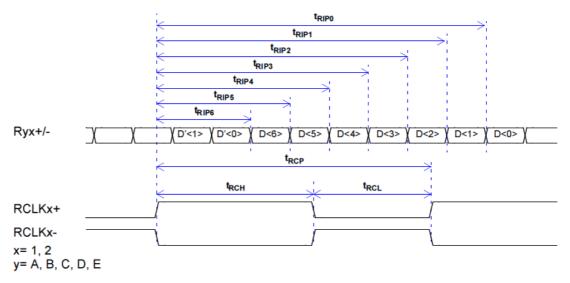
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#### Table 11. LVDS Receiver AC Specifications

(1)  $V_{IC_{RX}}=1.2V$ ,  $t_{RCH}=4/7 t_{RCP}$ 



## LVDS Receiver Input Timing



Ry1+/- skew margin is the one between RCLK1+/- and Ry1+/-. Ry2+/- skew margin is the one between RCLK2+/- and Ry2+/-.

Figure 10. LVDS Receiver Timing

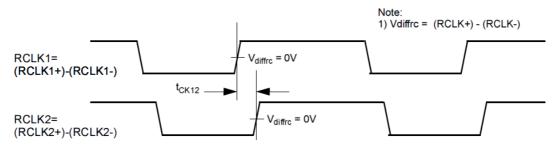


Figure 11. Skew time between RCLK1 and RCLK2



## LVDS Transmitter AC Specifications

| G 1 1             |                                | G IV         | •                                      |                     |  | <b>T</b> T •4 |
|-------------------|--------------------------------|--------------|--|---------------------|--|---------------|
| Symbol            | Parameter                      | Conditions   | Min                                    | Тур                 | Max                                    | Unit          |
| t <sub>TCP</sub>  | LVDS Clock Period              | -            | 11.76                                  | -                   | 50                                     |               |
| t <sub>TCH</sub>  | LVDS Clock High Duration       | -            | -                                      | 4/7t <sub>TCP</sub> | -                                      | ns            |
| t <sub>TCL</sub>  | LVDS Clock Low Duration        | -            | -                                      | 3/7t <sub>TCP</sub> | -                                      |               |
| t <sub>TSUP</sub> | LVDS Data Output Setup         | CLKOUT=75MHz | -                                      | -                   | 250                                    | ps            |
| t <sub>THLD</sub> | LVDS Data Output Hold          | CLKOUT=75MHz | -                                      | -                   | 250                                    | ps            |
| t <sub>TOP6</sub> | LVDS Data Output Position 6    | -            | 2/7t <sub>TCP</sub> -t <sub>THLD</sub> | 2/7t <sub>TCP</sub> | 2/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>TOP5</sub> | LVDS Data Output Position 5    | -            | 3/7t <sub>TCP</sub> -t <sub>THLD</sub> | 3/7t <sub>TCP</sub> | 3/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>TOP4</sub> | LVDS Data Output Position 4    | -            | 4/7t <sub>TCP</sub> -t <sub>THLD</sub> | 4/7t <sub>TCP</sub> | 4/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>TOP3</sub> | LVDS Data Output Position 3    | -            | 5/7t <sub>TCP</sub> -t <sub>THLD</sub> | 5/7t <sub>TCP</sub> | 5/7t <sub>TCP</sub> +t <sub>TSUP</sub> | ps            |
| t <sub>TOP2</sub> | LVDS Data Output Position 2    | -            | 6/7t <sub>TCP</sub> -t <sub>THLD</sub> | 6/7t <sub>TCP</sub> | 6/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>TOP1</sub> | LVDS Data Output Position 1    | -            | 7/7t <sub>TCP</sub> -t <sub>THLD</sub> | 7/7t <sub>TCP</sub> | 7/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>TOP0</sub> | LVDS Data Output Position 0    | -            | 8/7t <sub>TCP</sub> -t <sub>THLD</sub> | 8/7t <sub>TCP</sub> | 8/7t <sub>TCP</sub> +t <sub>TSUP</sub> |               |
| t <sub>LVT</sub>  | LVDS Transition Time (Fig 13.) | Fig.6        | -                                      | 0.6                 | 1.5                                    | ns            |

#### Table 12. LVDS Transmitter AC Specifications



## LVDS Transmitter Output Diagram

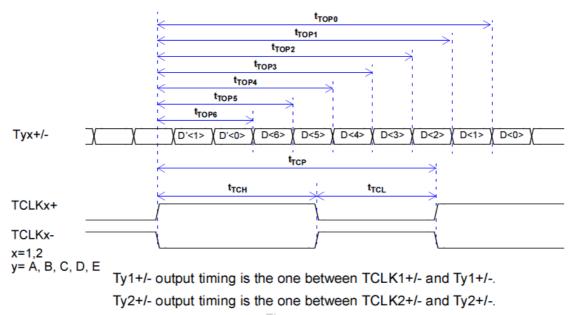
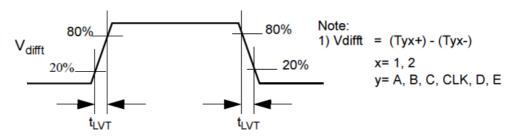


Figure 12. LVDS Transmitter Timing



**Figure 13. LVDS Transition Timing** 



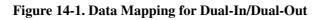
## LVDS Data Mapping

## Dual-In / Dual-Out

## LVDS-Rx Input Mapping

|                  | a process and a second s   |
|------------------|---|
| RCLK1+           |   |
| RA1+/-           | ∬ G1 [4] ∬ R1 [9] ∬ R1 [8] ∬ R1 [7] ∬ R1 [6] ∬ R1 [5] ∬ R1 [4] ∬ G3 [4] ∬ R3 [9] ∬ R3 [8] ∬ R3 [7] ∬ R3 [6] ∬ R3 [5] ∬ R3 [4] ∬   |
| RB1+/-           | X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B3 [5] X B3 [4] X G3 [9] X G3 [8] X G3 [7] X G3 [6] X G3 [5] X   |
| RC1+/-           | DE XVSYNCXHSYNCX B1 [9] X B1 [8] X B1 [7] X B1 [6] X DE XVSYNCXHSYNCX B3 [9] X B3 [8] X B3 [7] X B3 [6] X   |
| RD1+/-           | \data11\ B1 [3] \ B1 [2] \ G1 [3] \ G1 [2] \ R1 [2] \ R1 [3] \ R1 [2] \ data11\ B3 [3] \ B3 [2] \ G3 [3] \ G3 [2] \ R3 [2] \ R3 [2] \   |
| RE1+/-           | data12 (B1 [1] (B1 [0] G1 [1] G1 [0] (R1 [1] R1 [1] R1 [0] data12 B3 [1] B3 [0] G3 [1] G3 [0] (R3 [1] R3 [0] (R3 [1] R3 [0] )   |
| RCLK2+           |   |
| RA2+/-           | G2 [4] X R2 [9] X R2 [8] X R2 [7] X R2 [6] X R2 [5] X R2 [4] X G4 [4] X R4 [9] X R4 [8] X R4 [7] X R4 [6] X R4 [5] X R4 [4] X   |
| RB2+/-           | X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X R2 [5] X B4 [5] X B4 [4] X G4 [9] X G4 [8] X G4 [7] X G4 [6] X G4 [6] X G4 [5] X  |
| RC2+/-           | DE (VSYNC/HSYNC/ B2 [9] / B2 [8] / B2 [7] / B2 [6] / DE /VSYNC/HSYNC/ B4 [9] / B4 [8] / B4 [7] / B4 [6] /   |
| RD2+/-           | $data21 \end{pmatrix}$ B2 [3] $B2$ [2] $G2$ [3] $G2$ [2] $R2$ [3] $R2$ [3] $R2$ [2] $data21 \end{pmatrix}$ B4 [3] $B4$ [2] $G4$ [3] $G4$ [2] $R4$ [3] $R4$ [3] $R4$ [2] $R4$ [3] $R$  |
| RE2+/-           | data22 B2 [1] B2 [0] G2 [1] G2 [0] R2 [0] R2 [1] R2 [0] data22 B4 [1] B4 [0] G4 [1] G4 [0] R4 [0] R4 [0] R4 [0] B4 [0] G4 [1] G4 [0] R4 [0] R4 [0] R4 [0] G4 [0] B4 [0] B4 [0] G4 [0]   |
| TCLK1+           | Output Mapping  |
| TCLK1+<br>TA1+/- |   |
| TB1+/-           |   |
| TC1+/-           |   |
| TD1+/-           |   |
| TE1+/-           | $\int data 11 \int B1 [3] \int B1 [2] \int G1 [3] \int G1 [2] \int R1 [3] \int R1 [2] \int data 11 \int B3 [3] \int B3 [2] \int G3 [3] \int G3 [2] \int R3 [3] \int R3 [2] \int R3 [2]$   |
| <u></u>          | $\frac{1}{2} \det \left( 2 \right) \det \left( 2$ |
| TCLK2+           |   |
| TA2+/-           | (G2 [4] X R2 [9] X R2 [8] X R2 [7] X R2 [6] X R2 [5] X R2 [4] X G4 [4] X R4 [9] X R4 [8] X R4 [7] X R4 [6] X R4 [5] X R4 [4] X  |
| TB2+/-           | X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X G2 [5] X B4 [5] X B4 [4] X G4 [9] X G4 [8] X G4 [7] X G4 [6] X G4 [5] X   |
| TC2+/-           | DE (VSYNC/HSYNC/ B2 [9] / B2 [8] / B2 [7] / B2 [6] / DE /VSYNC/HSYNC/ B4 [9] / B4 [8] / B4 [7] / B4 [6] /   |
| TD2+/-           | $\int data 21 \Big\langle B2 [3] \Big\rangle B2 [2] \Big\rangle G2 [3] \Big\rangle G2 [2] \Big\rangle R2 [3] \Big\rangle R2 [2] \Big\rangle data 21 \Big\rangle B4 [3] \Big\rangle B4 [2] \Big\rangle G4 [3] \Big\rangle G4 [2] \Big\rangle R4 [3] \Big\rangle R4 [3] \Big\rangle R4 [2] \Big\rangle C4 [3] \Big\rangle R4 [3] \Big\rangle $   |
| 241              |   |
| TE2+/-           | $\int data22 \int B2 [1] \int B2 [0] \int G2 [1] \int G2 [0] \int R2 [1] \int R2 [0] \int data22 \int B4 [1] \int B4 [0] \int G4 [1] \int G4 [0] \int R4 [1] \int R4 [0] \int$  |

Data bits "data11, data12, data21, data22" are available for additional data transmission.



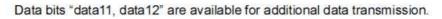


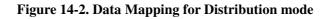
## **Distribution Mode**

In Distribution mode, RCLK2+/- must be Hi-Z.

## LVDS-Rx Input Mapping

| and a survey of the                                      |   |
|--|---|
| RCLK1+   |   |
| RA1+/-   | G1 [4] X R1 [9] X R1 [8] X R1 [7] X R1 [6] X R1 [5] X R1 [4] X G2 [4] X R2 [9] X R2 [8] X R2 [7] X R2 [6] X R2 [5] X R2 [4] X   |
| RB1+/-   | X B1 [5] X B1 [4] X G1 [9] X G1 [8] X G1 [7] X G1 [6] X G1 [5] X B2 [5] X B2 [4] X G2 [9] X G2 [8] X G2 [7] X G2 [6] X G2 [5] X   |
| RC1+/-   | C DE (VSYNC HSYNC B1 [9] ( B1 [8] ( B1 [7] ) B1 [6] DE (VSYNC HSYNC B2 [9] B2 [8] B2 [7] B2 [6]   |
| RD1+/-   | data11 B1 [3] B1 [2] G1 [3] G1 [2] R1 [3] R1 [3] R1 [2] data11 B2 [3] B2 [2] G2 [2] G2 [2] R2 [3] R2 [2]  |
| RE1+/-   | data12 B1 [1] B1 [0] G1 [1] G1 [0] R1 [1] R1 [0] data12 B2 [1] B2 [0] G2 [1] G2 [0] R2 [1] R2 [0]   |
| RCLK2+   | HI-Z  |
| RA2+/-   | no care   |
| RB2+/-   | no care   |
| RC2+/-   | no care   |
| RD2+/-   | no care   |
| RE2+/-   | no care   |
| TCLK1+   |   |
| LVDS-Tx  | Output Mapping  |
| TA1+/-   | G1 [4] X R1 [9] X R1 [8] X R1 [7] X R1 [6] X R1 [5] X R1 [4] X G2 [4] X R2 [9] X R2 [8] X R2 [7] X R2 [6] X R2 [5] X R2 [4] X   |
| TB1+/-   |   |
| <u>21</u>  | (B1 [5])         (B1 [4])         (G1 [9])         (G1 [7])         (G1 [6])         (G1 [5])         (B2 [4])         (G2 [9])         (G2 [8])         (G2 [6])         (G2 [5])  |
| TC1+/-   |   |
| TC1+/-   | (B1 [5])         (B1 [4])         (G1 [9])         (G1 [7])         (G1 [6])         (G1 [5])         (B2 [4])         (G2 [9])         (G2 [7])         (G2 [6])         (G2 [5])  |
|  | $ \begin{array}{c} & \left( B1\left( 5\right) \left( B1\left( 4\right) \right) \left( G1\left( 9\right) \right) \left( G1\left( 8\right) \right) \left( G1\left( 7\right) \right) \left( G1\left( 6\right) \right) \left( G1\left( 5\right) \right) \left( B2\left( 5\right) \right) \left( B2\left( 4\right) \right) \left( G2\left( 8\right) \right) \left( G2\left( 7\right) \right) \left( G2\left( 6\right) \right) \left( G2\left( 5\right) \right) \left( G2\left( 7\right) \right) \left( G2\left( 6\right) \right) \left( G2\left( 5\right) \right) \left( G2\left( 7\right) \right) \left( G2\left( 6\right) \right) \left( G2\left( 7\right) \left($  |
| TD1+/-   | $ \begin{array}{c} B1 \left[ 5 \right] \left\langle B1 \left[ 4 \right] \right\rangle G1 \left[ 9 \right] \left\rangle G1 \left[ 8 \right] \left\rangle G1 \left[ 7 \right] \right\rangle G1 \left[ 6 \right] \left\rangle G1 \left[ 5 \right] \right\rangle B2 \left[ 5 \right] \right\rangle B2 \left[ 4 \right] \left\rangle G2 \left[ 9 \right] \left\rangle G2 \left[ 8 \right] \right\rangle G2 \left[ 7 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \right\rangle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 $ |
| TD1+/-<br>TE1+/-   | $ \begin{array}{c} B1 \left[ 5 \right] \left\langle B1 \left[ 4 \right] \right\rangle G1 \left[ 9 \right] \left\rangle G1 \left[ 8 \right] \left\rangle G1 \left[ 7 \right] \right\rangle G1 \left[ 6 \right] \left\rangle G1 \left[ 5 \right] \right\rangle B2 \left[ 5 \right] \right\rangle B2 \left[ 4 \right] \left\rangle G2 \left[ 9 \right] \left\rangle G2 \left[ 8 \right] \right\rangle G2 \left[ 7 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \right\rangle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 5 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \right\rangle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 \right] \left\langle G2 \left[ 6 $ |
| TD1+/- =<br>TE1+/- =<br>TCLK2+ =                         | B1 [5] (B1 [4] (G1 [9] ) (G1 [8] (G1 [7] ) (G1 [6] ) (G1 [5] ) (B2 [5] ) (B2 [4] ) (G2 [9] ) (G2 [8] ) (G2 [7] ) (G2 [6] ) (G2 [5] )         DE (VSYNC HSYNC ) (B1 [9] ) (B1 [8] ) (B1 [7] ) (B1 [6] ) (DE ) (VSYNC ) (HSYNC ) (B2 [9] ) (B2 [8] ) (B2 [7] ) (B2 [6] )         (data11 ) (B1 [3] ) (B1 [2] ) (G1 [3] ) (G1 [2] ) (R1 [3] ) (R1 [2] ) (data11 ) (B2 [3] ) (B2 [2] ) (G2 [3] ) (G2 [2] ) (R2 [3] ) (R2 [2] )         (data12 ) (B1 [1] ) (B1 [0] ) (G1 [1] ) (G1 [0] ) (R1 [1] ) (R1 [0] ) (data12 ) (B2 [1] ) (B2 [0] ) (G2 [1] ) (G2 [0] ) (R2 [1] ) (R2 [0] )  |
| TD1+/  | B1 [5] (B1 [4] (G1 [9] ) (G1 [8] (G1 [7] ) (G1 [6] ) (G1 [5] ) (B2 [5] ) (B2 [4] ) (G2 [9] ) (G2 [8] ) (G2 [7] ) (G2 [6] ) (G2 [5] )         DE (VSYNC HSYNC ) (D1 [9] (D1 [9] ) (D1 [9] ) (D1 [9] ) (D1 [7] ) (D1 [6] ) (DE (VSYNC ) (HSYNC ) (D2 [9] ) (D2 [8] ) (D2 [7] ) (D2 [6] ) (D2 [7] )  |
| TD1+/  | B1 [5] \ B1 [4] \ G1 [9] \ G1 [8] \ G1 [7] \ G1 [6] \ G1 [5] \ B2 [5] \ B2 [4] \ G2 [9] \ G2 [8] \ G2 [7] \ G2 [6] \ G2 [5] \         DE       \VSYNC \ HSYNC \ B1 [9] \ B1 [8] \ B1 [7] \ B1 [6] \ DE       \VSYNC \ HSYNC \ B2 [9] \ B2 [8] \ B2 [7] \ B2 [6] \         data11 \ B1 [3] \ B1 [2] \ G1 [3] \ G1 [2] \ R1 [3] \ R1 [2] \ data11 \ B2 [3] \ B2 [2] \ G2 [3] \ G2 [2] \ R2 [3] \ R2 [2] \         data12 \ B1 [1] \ B1 [0] \ G1 [1] \ G1 [0] \ R1 [1] \ R1 [0] \ data12 \ B2 [1] \ B2 [0] \ G2 [1] \ G2 [0] \ R2 [1] \ R2 [0] \         G1 [4] \ R1 [9] \ R1 [8] \ R1 [7] \ R1 [6] \ R1 [5] \ R1 [4] \ G2 [4] \ R2 [9] \ R2 [8] \ R2 [7] \ R2 [6] \ R2 [5] \ R2 [4] \         B1 [5] \ B1 [4] \ G1 [9] \ G1 [8] \ G1 [7] \ G1 [6] \ G1 [5] \ B2 [5] \ B2 [4] \ G2 [9] \ G2 [8] \ G2 [7] \ G2 [6] \ G2 [6] \ G2 [5] \  |
| TD1+/-<br>TE1+/-<br>TCLK2+<br>TA2+/-<br>TB2+/-<br>TC2+/- | B1 [5] (B1 [4] (G1 [9]) (G1 [8] (G1 [7]) (G1 [6] (G1 [5]) (B2 [5]) (B2 [4]) (G2 [8]) (G2 [7]) (G2 [6]) (G2 [5])         DE (VSYNC (HSYNC) (B1 [9]) (B1 [8]) (B1 [7]) (B1 [6]) (DE (VSYNC) (HSYNC) (B2 [9]) (B2 [8]) (B2 [7]) (B2 [6]) (DE (VSYNC) (HSYNC) (B2 [9]) (B2 [8]) (B2 [7]) (B2 [6]) (DE (Atanal 1) (B2 [3]) (B2 [2]) (G2 [3]) (G2 [2]) (R2 [3]) (R2 [2]) (Data 11) (B1 [3]) (B1 [2]) (G1 [3]) (G1 [2]) (R1 [3]) (R1 [2]) (data 11) (B2 [3]) (B2 [2]) (G2 [3]) (G2 [2]) (R2 [3]) (R2 [2]) (Data 12) (Data 12) (B2 [3]) (B2 [2]) (G2 [3]) (G2 [2]) (R2 [3]) (   |







#### Single-In / Dual-Out

In Single-in / Dual-out mode, RCLK2+/- must be Hi-Z.

## LVDS-Rx Input Mapping

| LVDS-KX I | nput mappi    | ng              |               | 1             |               |               |                   |
|-----------|---------------|-----------------|---------------|---------------|---------------|---------------|-------------------|
| RCLK1+    |               | \               |               |               |               |               |                   |
| RA1+/-    | G1 [4] R1 [9] | R1 [8] R1 [7]   | R1 [6] R1 [5] | R1 [4] G2 [4] | R2 [9] R2 [8] | R2 [7] R2 [6] | R2 [5] R2 [4]     |
| RB1+/-    | B1 [5] B1 [4] | G1 [9] X G1 [8] | G1 [7] G1 [6] | G1 [5] B2 [5] | B2 [4] G2 [9] | G2 [8] G2 [7] | G2 [6] \ G2 [5]   |
| RC1+/-    |               | HSYNC B1 [9]    | B1 [8] B1 [7] | B1 [6] DE     |               | B2 [9] B2 [8] | B2 [7] X B2 [6] X |
| RD1+/-    | data11 B1 [3] | B1 [2] G1 [3]   | G1 [2] R1 [3] | R1 [2] data11 | B2 [3] 82 [2] | G2 [3] G2 [2] | R2 [3] X R2 [2] X |
| RE1+/-    | data12 B1 [1] | B1 [0] X G1 [1] | G1 [0] R1 [1] | R1 [0] data12 | B2 [1] 82 [0] | G2 [1] G2 [0] | R2 [1] X R2 [0] X |
| RCLK2+    |               |                 |               | Hi-Z          |               |               |                   |
|           |               |                 |               | no care       |               |               |                   |
|           |               |                 |               | no care       |               |               |                   |
| RC2+/-    |               |                 |               | no care       |               |               |                   |
| RD2+/-    |               |                 |               | no care       |               |               |                   |
| RE2+/-    |               |                 |               | no care       |               |               |                   |
| LVDS-Tx C | Dutput Map    | ping            |               |               |               | ſ             |                   |
| TA1+/-    | G1 [4]        | R1 [9]          | R1 [8]        | R1 [7]        |               | R1 [5]        | R1 [4]            |
| TB1+/-    | B1 [5]        | B1 [4]          | G1 [9]        | G1 [8]        | G1 [7]        | G1 [6]        | G1 [5]            |
| TC1+/-    | DE            |                 | HSYNC         | B1 [9]        | (B1 [8]       | B1 [7]        | B1 [6]            |
| TD1+/-    | data11        | (B1 [3]         | B1 [2]        | G1 [3]        | G1 [2]        | R1 [3]        | R1 [2]            |
| TE1+/-    | data12        | B1 [1]          | B1 [0]        | G1 [1]        | G1 [0]        | R1 [1]        | R1 [0]            |
| TCLK2+    |               |                 |               |               |               |               |                   |
| TA2+/     | G2 [4]        | R2 [9]          | R2 [8]        | R2 [7]        | <br>          | R2 [5]        | R2 [4]            |
|           | B2 [5]        | B2 [4]          | G2 [9]        | G2 [8]        | G2 [7]        | G2 [6]        | G2 [5]            |
| TC2+/-    | DE            |                 |               | К В2 [9]      | B2 [8]        | B2 [7]        | B2 [6]            |
| TD2+/-    | data11        | Х В2 [3]        | B2 [2]        | G2 [3]        | G2 [2]        | R2 [3]        | R2 [2]            |
|           |               |                 |               |               |               | 112 [0]       |                   |

(Regardless of the Data Latency)

R2 [1]

Data bits "data11, data12" are available for additional data transmission.

G2 [1]

G2 [0]

B2 [0]

Figure 14-3(a). Data Mapping for Single-In/Dual-Out

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data12

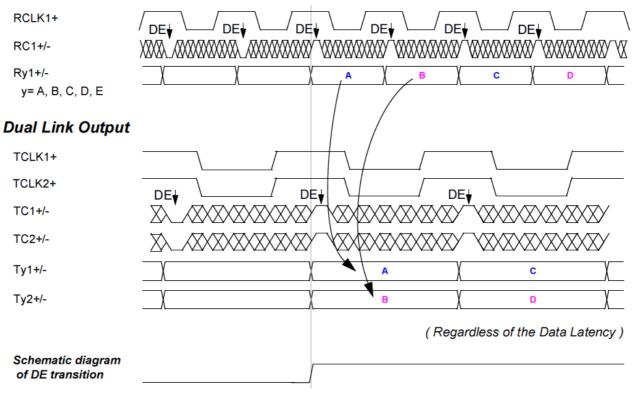
B2 [1]

TE2+/-

R2 [0]



## Single Link Input



Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

Figure 14-3(b). Data Mapping for Single-In/Dual-Out



| LVDS-Rx  | input mappi  | ng   |   |  |   |   |   |
|--|--|--|---|--|---|---|---|
| RCLK1+   |  |  |   |  |   |   |   |
| RA1+/-   | G1 [4]   | R1 [9]   | R1 [8]  | R1 [7]   | R1 [6]  | R1 [5]  | R1 [4]  |
| RB1+/-   | B1 [5]   | B1 [4]   | G1 [9]  | G1 [8]   | G1 [7]  | G1 [6]  | G1 [5]  |
| RC1+/-   | DE   | VSYNC  | HSYNC   | B1 [9]   | B1 [8]  | B1 [7]  | B1 [6]  |
| RD1+/-   | data11   | B1 [3]   | B1 [2]  | G1 [3]   | G1 [2]  | R1 [3]  | R1 [2]  |
| RE1+/-   | data12   | B1 [1]   | B1 [0]  | G1 [1]   | G1 [0]  | R1 [1]  | R1 [0]  |
| RCLK2+   |  |  |   |  | ]   |   |   |
| RA2+/-   | G2 [4]   | R2 [9]   | R2 [8]  | R2 [7]   | R2 [6]  | R2 [5]  | R2 [4]  |
| RB2+/-   | B2 [5]   | B2 [4]   | G2 [9]  | G2 [8]   | G2 [7]  | G2 [6]  | G2 [5]  |
| RC2+/-   | DE   | VSYNC  | HSYNC   | B2 [9]   | B2 [8]  | B2 [7]  | B2 [6]  |
| RD2+/-   | data21   | B2 [3]   | B2 [2]  | G2 [3]   | G2 [2]  | R2 [3]  | R2 [2]  |
| RE2+/-   | data22   | B2 [1]   | B2 [0]  | G2 [1]   | G2 [0]  | R2 [1]  | R2 [0]  |
| LVDS-Tx  | Output Map   | oing   |   |  |   |   |   |
| TCLK1+   |  | \  |   |  |   |   |   |
| T44:4  |  |  |   |  | ·   |   |   |
| TA1+/-   | G1 [4] R1 [9]  | R1 [8] (R1 [7]                                       | R1 [6] R1 [5]   | R1 [4] G2 [4]  | R2 [9] R2 [8]                                     | (R2 [7] (R2 [6]   | R2 [5] R2 [4]   |
| TA1+/-<br>TB1+/-   | (G1 [4] R1 [9]   | (R1 [8] (R1 [7])<br>(G1 [9] (G1 [8])                 | R1 [6] R1 [5]   |  | R2 [9] R2 [8]                                     | (R2 [7] (R2 [6])<br>(G2 [8] (G2 [7])                              | R2 [5] X R2 [4] X G2 [6] X G2 [5] X   |
| =  | X B1 [5] X B1 [4]  |  |   |  |   |   |   |
| TB1+/-   | X B1 [5] X B1 [4]  | G1 [9] G1 [8]  | G1 [7] G1 [6]   | G1 [5] B2 [5]  | B2 [4] G2 [9]                                     | G2 [8] G2 [7]   | G2 [6] \ G2 [5] \   |
| TB1+/-<br>TC1+/-   | B1 [5] B1 [4]  | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]                    | (G1 [5] (B2 [5])<br>(B1 [6] (DE)   |   | (G2 [8] (G2 [7])<br>(B2 [9] (B2 [8])                              | G2 [6] X G2 [5] X<br>B2 [7] X B2 [6] X  |
| TB1+/<br>TC1+/<br>TD1+/  | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | G1 [5] B2 [5]<br>B1 [6] DE<br>R1 [2] data21  | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |
| TB1+/-<br>TC1+/-<br>TD1+/-<br>TE1+/-   | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | G1 [5]     B2 [5]       B1 [6]     DE       (R1 [2])     data21       (R1 [0])     data22                | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |
| TB1+/-<br>TC1+/-<br>TD1+/-<br>TE1+/-<br>TCLK2+                               | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | (G1 [5] (B2 [5])<br>(B1 [6] (DE)<br>(R1 [2] (data21)<br>(R1 [0] (data22)<br>Hi-Z                         | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |
| TB1+/-<br>TC1+/-<br>TD1+/-<br>TE1+/-<br>TCLK2+<br>TA2+/-                     | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | (G1 [5] (B2 [5])<br>(B1 [6] (DE)<br>(R1 [2] (data21)<br>(R1 [0] (data22)<br>Hi-Z<br>Hi-Z                 | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |
| TB1+/-<br>TC1+/-<br>TD1+/-<br>TE1+/-<br>TCLK2+<br>TA2+/-<br>TB2+/-           | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | (G1 [5] (B2 [5])<br>(B1 [6] (DE)<br>(R1 [2] (data21)<br>(R1 [0] (data22)<br>Hi-Z<br>Hi-Z<br>Hi-Z         | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |
| TB1+/-<br>TC1+/-<br>TD1+/-<br>TE1+/-<br>TCLK2+<br>TA2+/-<br>TB2+/-<br>TC2+/- | A         B1 [5]         B1 [4]           A         DE         VSYNC           A         data11         B1 [3] | (G1 [9] (G1 [8]<br>(HSYNC (B1 [9]<br>(B1 [2] (G1 [3] | (G1 [7] (G1 [6]<br>(B1 [8] (B1 [7]<br>(G1 [2] (R1 [3] | (G1 [5] (B2 [5])<br>(B1 [6] (DE)<br>(R1 [2] (data21)<br>(R1 [0] (data22)<br>Hi-Z<br>Hi-Z<br>Hi-Z<br>Hi-Z | B2 [4] (G2 [9])<br>VSYNC HSYNC<br>B2 [3] (B2 [2]) | G2 [8]     G2 [7]       B2 [9]     B2 [8]       G2 [3]     G2 [2] | G2 [6]         G2 [5]           B2 [7]         B2 [6]           R2 [3]         R2 [2] |

## Dual-In / Single-Out LVDS-Rx Input Mapping

(Regardless of the Data Latency)

Data bits "data11, data12, data21, data22" are available for additional data transmission.

Figure 14-4. Data Mapping for Dual-In/Single-Out

#### Notes



## 1) LVDS input pin connection

When LVDS line is not derived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

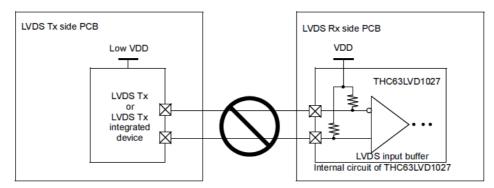


Figure 15. LVDS input pin connection

#### 2) Power On Sequence

Don't input RCLK1+/- and RCLK2+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.



### 3)Cable Connection and Disconnection

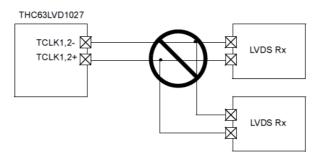
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

#### 4)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

#### 5)Multi Drop Connection

Multi drop connection is not recommended.



#### Figure 16.Multi Drop Connection

#### 6)Asynchronous use

Asynchronous use such as following systems are not recommended. Page.11 tCK12 spec should be kept.

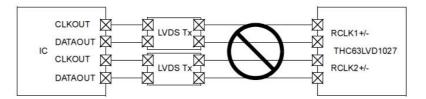


Figure 17-1. Asynchronous Use1

Asynchronous use such as following systems are not recommended.

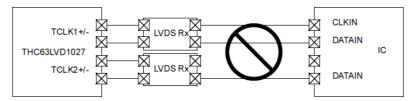
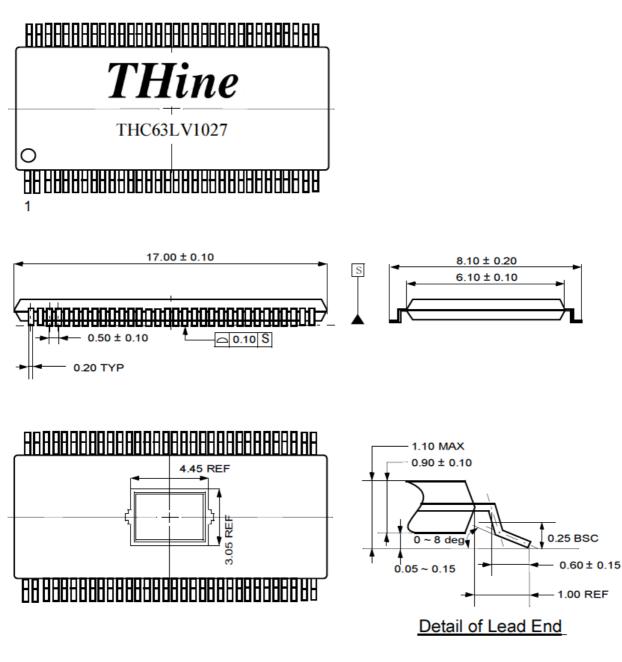


Figure 17-2. Asynchronous Use2



Package



Unit: mm

Exposed PAD is GND and must be soldered to PCB.

Figure 18. Package Diagram



## **Notices and Requests**

- 1. The product specifications described in this material are subject to change without prior notice.
- 2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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- 6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
- 7. Please note that this product is not designed to be radiation-proof.
- 8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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