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THC63LVDM83E

SMALL PACKAGE / 24Bit COLOR LVDS TRANSMITTER

General Description

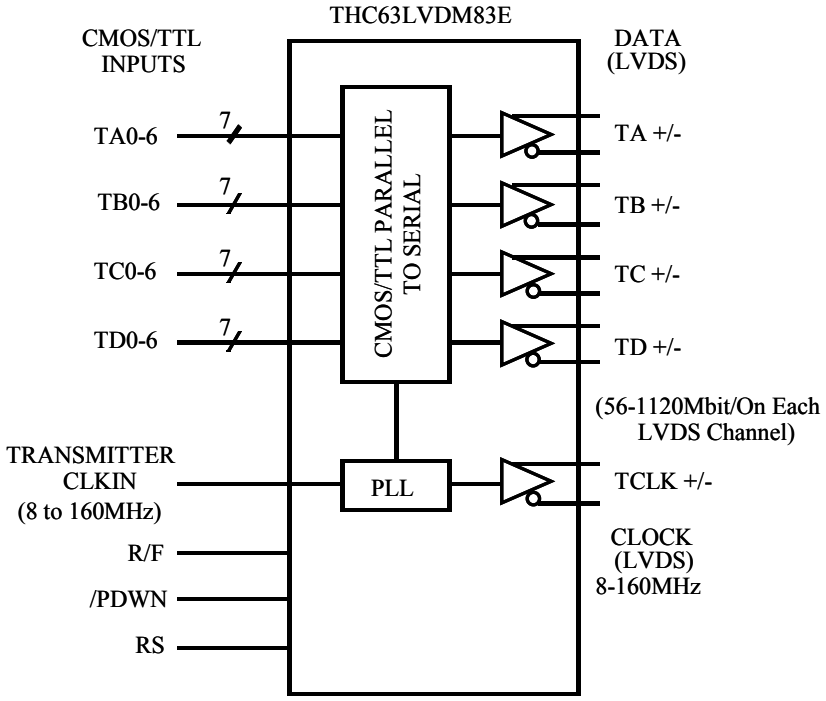
The THC63LVDM83E transmitter is designed to support pixel data transmission between Host and Flat Panel Display up to 1080p/WUXGA resolutions.

The THC63LVDM83E converts 28bits of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 160MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, DE, CONT1) are transmitted at an effective rate of 1120Mbps per LVDS channel.

Features

- 49pin 0.65mm pitch VFBGA Package
- Wide dot clock range: 8-160MHz suited for TV Signal : NTSC(12.27MHz) - 1080p(148.5MHz) PC Signal : QVGA(8MHz) - WUXGA(154MHz)
- 1.2V to 3.3V CMOS inputs are supported.
- LVDS swing is reducible by RS-pin to reduce EMI and power consumption.
- PLL requires no external components.
- On chip jitter filtering.
- Spread Spectrum Clock input tolerant.
- Power down mode.
- Input clock triggering edge is selectable by R/F-pin.
- Operates from a Single 3.3V Supply and 110mW(typ.) at 75MHz.

Block Diagram



Ball Out

TOP VIEW

	1	2	3	4	5	6	7	
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0	A
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+	B
C	TB5	TB0	GND	VCC	RS	TB-	TB+	C
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC-	TC+	D
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+	E
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+	F
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN	G
	1	2	3	4	5	6	7	

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Direction</th><th>Type</th><th>Description</th></tr>
<tr><td>TA+, TA-</td><td>B7, B6</td><td rowspan="5">Output</td><td rowspan="5">LVDS</td><td rowspan="4">LVDS Data Out</td></tr>
<tr><td>TB+, TB-</td><td>C7, C6</td></tr>
<tr><td>TC+, TC-</td><td>D7, D6</td></tr>
<tr><td>TD+, TD-</td><td>F7, F6</td></tr>
<tr><td>TCLK+,
TCLK-</td><td>E7, E6</td><td>LVDS Clock Out</td></tr>
<tr><td>TA0 ~ TA6</td><td>A7,A6,A5,A4,A3,A2,A1</td><td rowspan="8">Input</td><td rowspan="8">LV-CMOS
/TTL</td><td rowspan="4">Pixel Data Input</td></tr>
<tr><td>TB0 ~ TB6</td><td>C2,D2,E2,F2,B1,C1,D1</td></tr>
<tr><td>TC0 ~ TC6</td><td>E1,F1,G1,G2,G3,G4,G5</td></tr>
<tr><td>TD0 ~ TD6</td><td>B5,B4,B3,B2,F3,F4,F5</td></tr>
<tr><td>/PDWN</td><td>G7</td><td>H : Normal operation
L : Power down (all outputs are Hi-Z)</td></tr>
<tr><td>RS</td><td>C5</td><td>LVDS swing mode, VREF select See Fig.5, 6
<table>
<tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr>
<tr><td>VCC</td><td>350mV</td><td>N/A</td></tr>
<tr><td>0.6 ~ 1.4V</td><td>350mV</td><td>RS=VREF</td></tr>
<tr><td>GND</td><td>200mV</td><td>N/A</td></tr>
</table>
VREF is Input Reference Voltage</td></tr>
<tr><td>R/F</td><td>E5</td><td>Input Clock Triggering Edge Select
H : Rising edge
L : Falling edge</td></tr>
<tr><td>CLKIN</td><td>G6</td><td>Input Clock</td></tr>
<tr><td>VCC</td><td>C4</td><td rowspan="4">Power</td><td rowspan="4">---</td><td>Power Supply Pin for CMOS input and digital circuit.</td></tr>
<tr><td>GND</td><td>C3,D3,E3</td><td>Ground Pins for Common.</td></tr>
<tr><td>LVDS VCC</td><td>D4,D5</td><td>Power Supply Pins for LVDS Outputs.</td></tr>
<tr><td>PLL VCC</td><td>E4</td><td>Power Supply Pin for PLL circuit.</td></tr>
</table>

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage	-0.3	+4.0	V
LV-CMOS/TTL Input Voltage	-0.3	VCC + 0.3	V
LVDS Transmitter Output Voltage	-0.3	VCC + 0.3	V
Output Current	-30	30	mA
Junction Temperature		+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature		+260	°C
Reflow Peak Temperature Time		10	sec
Maximum Power Dissipation @+25°C		1.2	W

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
	All Supply Voltage	3.0	3.3	3.6	V
Ta	Operating Ambient Temperature	0	25	+70	°C
	Clock Frequency	8		160	MHz

Power Consumption

VCC = 3.0~3.6V, Ta= 0~+70ºC

Symbol	Parameter	Conditions	Typ*	Max	Units
I_{TCCW}	LVDS Transmitter Operating Current Gray Scale Pattern 16 (Fig.1)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	42 (34)		mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	58 (50)		mA
	LVDS Transmitter Operating Current Worst Case Pattern (Fig.2)	RL=100Ω, CL=5pF, f=85MHz RS=VCC, (RS=GND)	45 (36)	67 (56)	mA
		RL=100Ω, CL=5pF, f=160MHz RS=VCC, (RS=GND)	63 (55)	92 (80)	mA
I_{TCCS}	LVDS Transmitter Power Down Current			10	µA

*Typ values are at VCC=3.3V, Ta = +25ºC

16 Grayscale Pattern

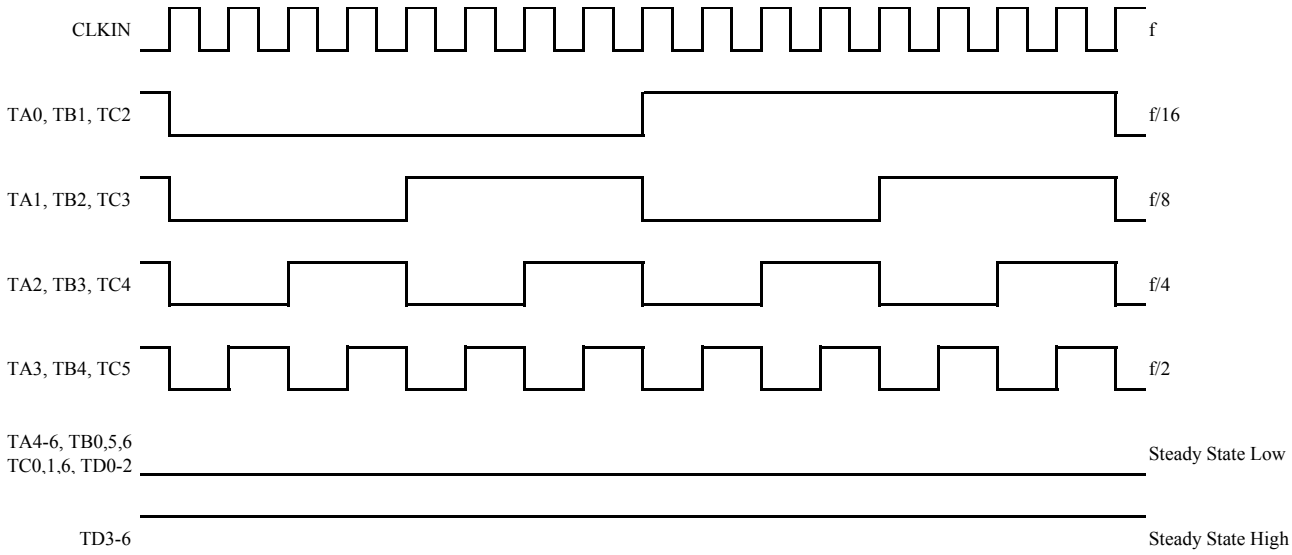
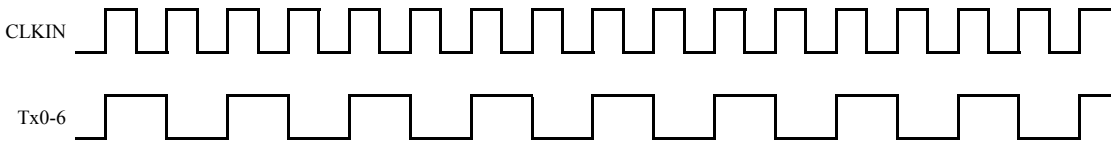


Fig.1 16 Grayscale Pattern

Worst Case Pattern



x=A,B,C,D

Fig.2 Worst Case Pattern

Electrical Characteristics

LV-CMOS/TTL DC Specifications

VCC = 3.0~3.6V, Ta= 0~+70ºC

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	RS=VCC or GND	2.0		VCC	V
V_{IL}	Low Level Input Voltage	RS=VCC or GND	GND		0.8	V
V_{DDQ} [1]	Small Swing Voltage		1.2		2.8	V
V_{REF}	Input Reference Voltage	Small Swing (RS=V_{DDQ}/2)		V_{DDQ}/2		
V_{SH} [2]	Small Swing High Level Input Voltage	$V_{REF=}$ V_{DDQ}/2	V_{DDQ}/2 +100mV			V
V_{SL} [2]	Small Swing Low Level Input Voltage	$V_{REF=}$ V_{DDQ}/2			V_{DDQ}/2 -100mV	V
I_{INC}	Input Current	GND ≤ V_{IN} ≤ VCC			±10	µA

*Typ values are at VCC=3.3V, Ta = +25ºC

Notes : [1] V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.

[2] Small swing signal is applied to TA0-6, TB0-6, TC0-6, TD0-6 and CLKIN.

LVDS Transmitter DC Specifications

VCC = 3.0~3.6V, Ta= 0~+70ºC

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=VCC	250	350	450	mV
			Reduced swing RS=GND	120	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, RL=100Ω				-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=GND, V_{OUT}=GND to VCC				±10	µA

*Typ values are at VCC=3.3V, Ta = +25ºC

LV-CMOS/TTL & LVDS Transmitter AC Specifications VCC = 3.0~3.6V, Ta= 0~+70ºC

Symbol	Parameter	Min	Typ	Max	Units
t_{TCIT}	CLK IN Transition Time			5.0	ns
t_{TCP}	CLK IN Period	6.25	T	125	ns
t_{TCH}	CLK IN High Time	0.35T	0.5T	0.65T	ns
t_{TCL}	CLK IN Low Time	0.35T	0.5T	0.65T	ns
t_{TCD}	CLK IN to TCLK+/- Delay		3T		ns
t_{TS}	LV-CMOS/TTL Data Setup to CLK IN	2.0			ns
t_{TH}	LV-CMOS/TTL Data Hold from CLK IN	0.0			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position0 (T=6.25ns ~ 20ns)	-0.15	0.0	+0.15	ns
t_{Top0}	Output Data Position1 (T=6.25ns ~ 20ns)	T/7-0.15	T/7	T/7+0.15	ns
t_{Top6}	Output Data Position2 (T=6.25ns ~ 20ns)	2T/7-0.15	2T/7	2T/7+0.15	ns
t_{Top5}	Output Data Position3 (T=6.25ns ~ 20ns)	3T/7-0.15	3T/7	3T/7+0.15	ns
t_{Top4}	Output Data Position4 (T=6.25ns ~ 20ns)	4T/7-0.15	4T/7	4T/7+0.15	ns
t_{Top3}	Output Data Position5 (T=6.25ns ~ 20ns)	5T/7-0.15	5T/7	5T/7+0.15	ns
t_{Top2}	Output Data Position6 (T=6.25ns ~ 20ns)	6T/7-0.15	6T/7	6T/7+0.15	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms

*Typ values are at VCC=3.3V, Ta = +25ºC

LV-CMOS/TTL Input

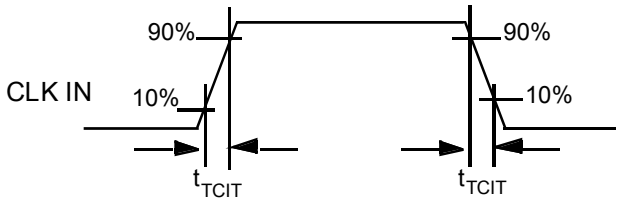
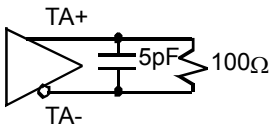


Fig.3 CLKIN Transmission Time

LVDS Output

$V_{Diff} = (TA+) - (TA-)$



LVDS Output Load

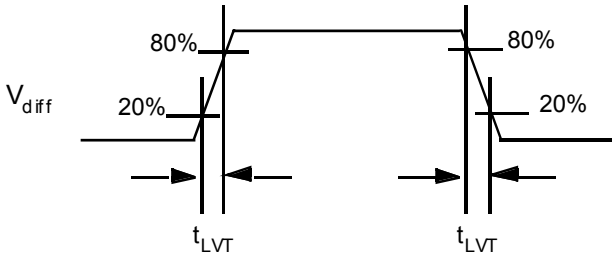
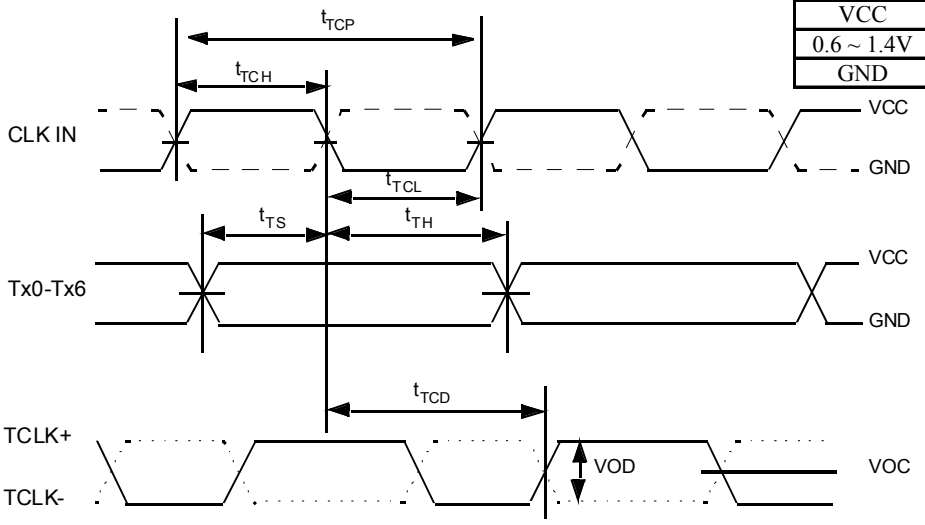


Fig.4 LVDS Output Load and Transmission Time

AC Timing Diagrams

LV-CMOS/TTL Inputs

RS	VOD
VCC	350mV
0.6 ~ 1.4V	
GND	200mV

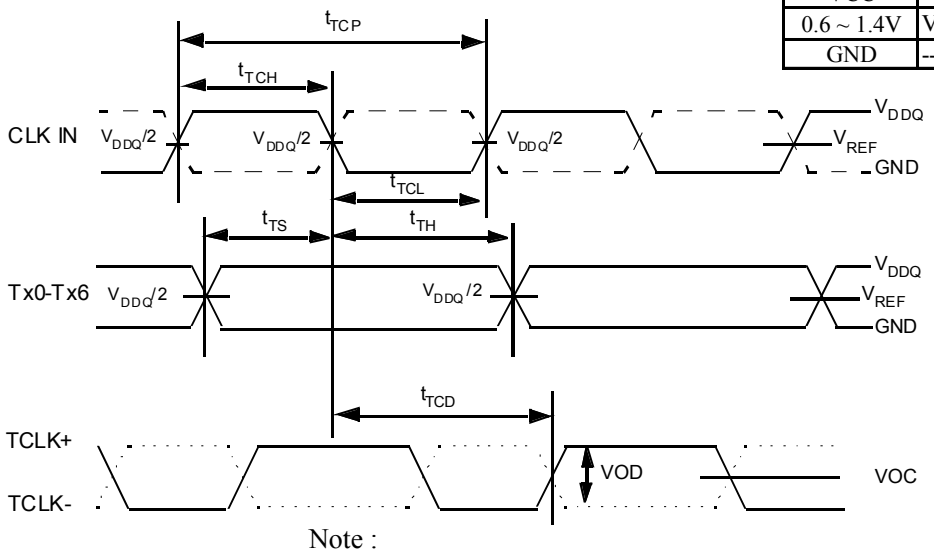


Note :
CLKIN : for R/F=GND, denote as solid line,
for R/F = VCC, denote as dashed line.

Fig.5 CLKIN Period, High/Low Time, Setup/Hold Timing

Small Swing Inputs

RS	VREF
VCC	---
0.6 ~ 1.4V	$V_{DDQ}/2$
GND	---



Note :
CLKIN : for R/F=GND, denote as solid line,
for R/F = VCC, denote as dashed line.

Fig.6 Small Swing Inputs

LVDS Output

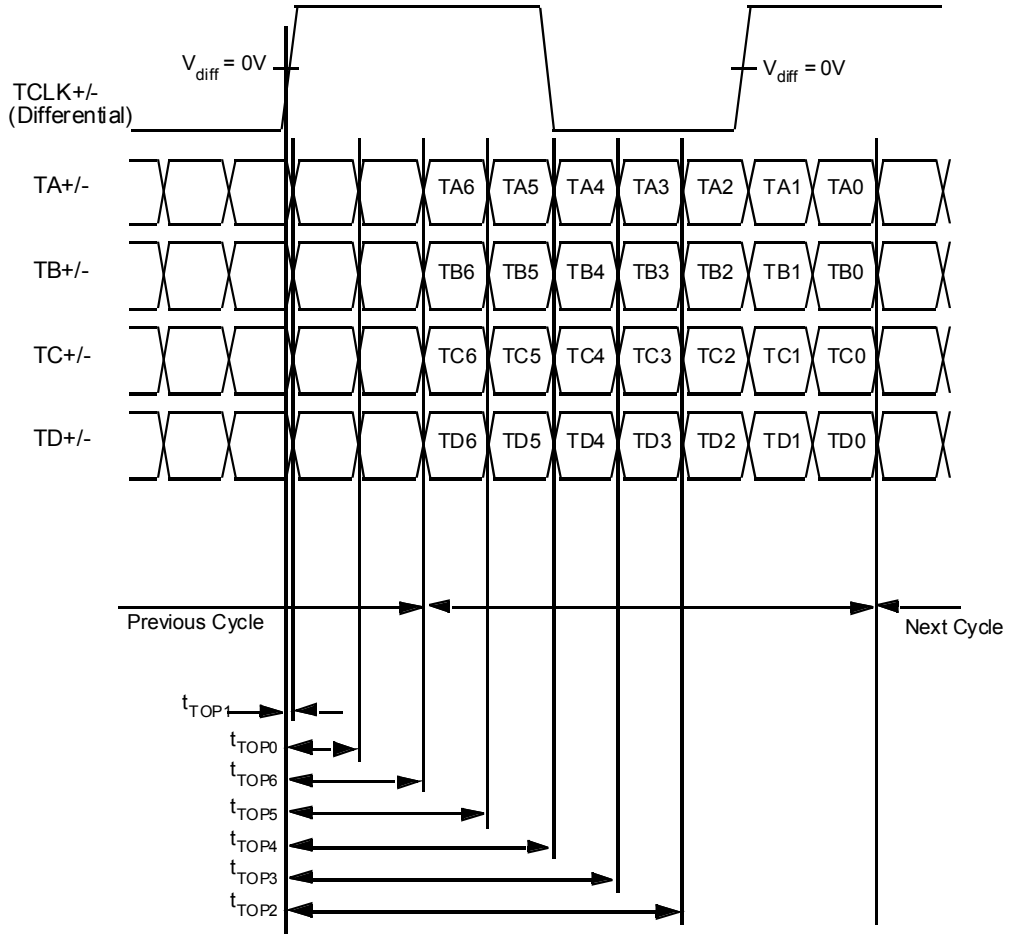


Fig.7 LVDS Output Data Position

Phase Lock Loop Set Time

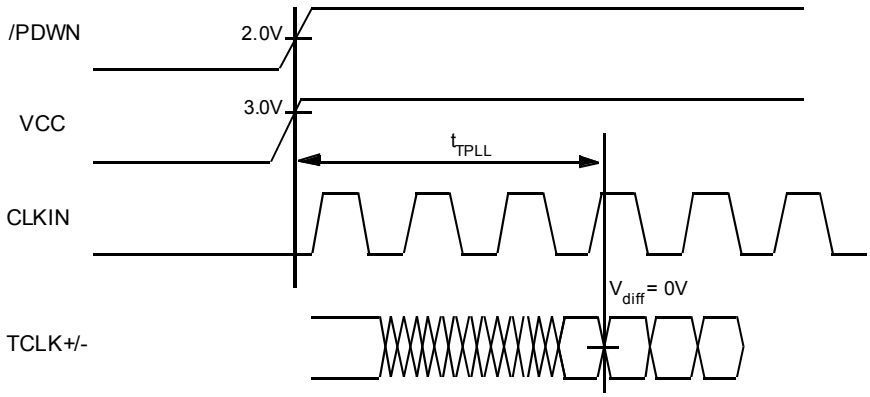
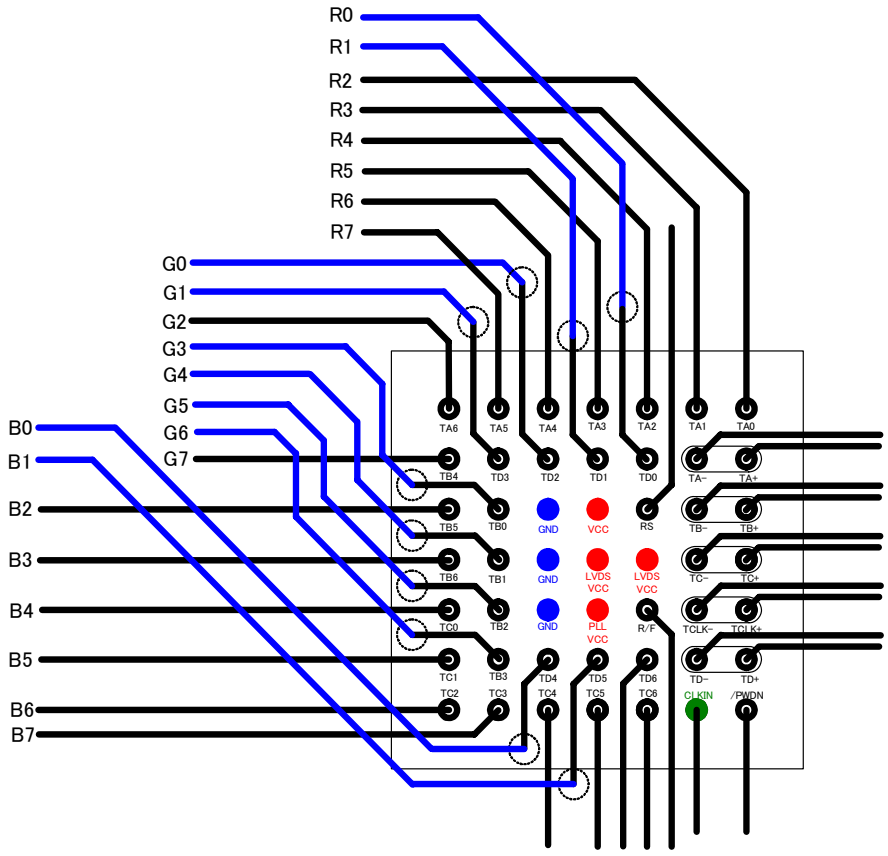


Fig.8 PLL Lock Set Time

Board Layout Example

TOP VIEW

	1	2	3	4	5	6	7	
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0	A
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+	B
C	TB5	TB0	GND	VCC	RS	TB-	TB+	C
D	TB6	TB1	GND	LVDS VCC	LVDS VCC	TC-	TC+	D
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+	E
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+	F
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PDWN	G
	1	2	3	4	5	6	7	



Note

1) Cable Connection and Disconnection

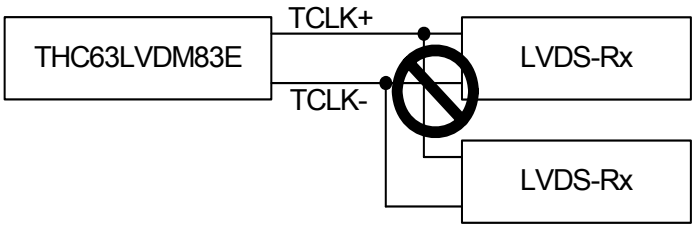
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect the each GND of the PCB which THC63LVDM83E and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

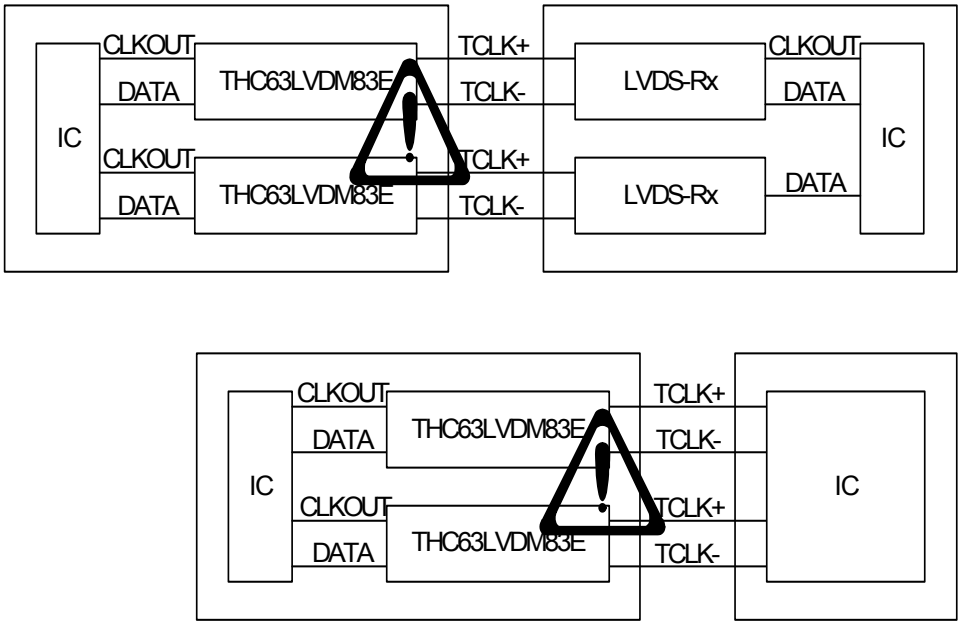
3) Multi Drop Connection

Multi drop connection is not recommended.

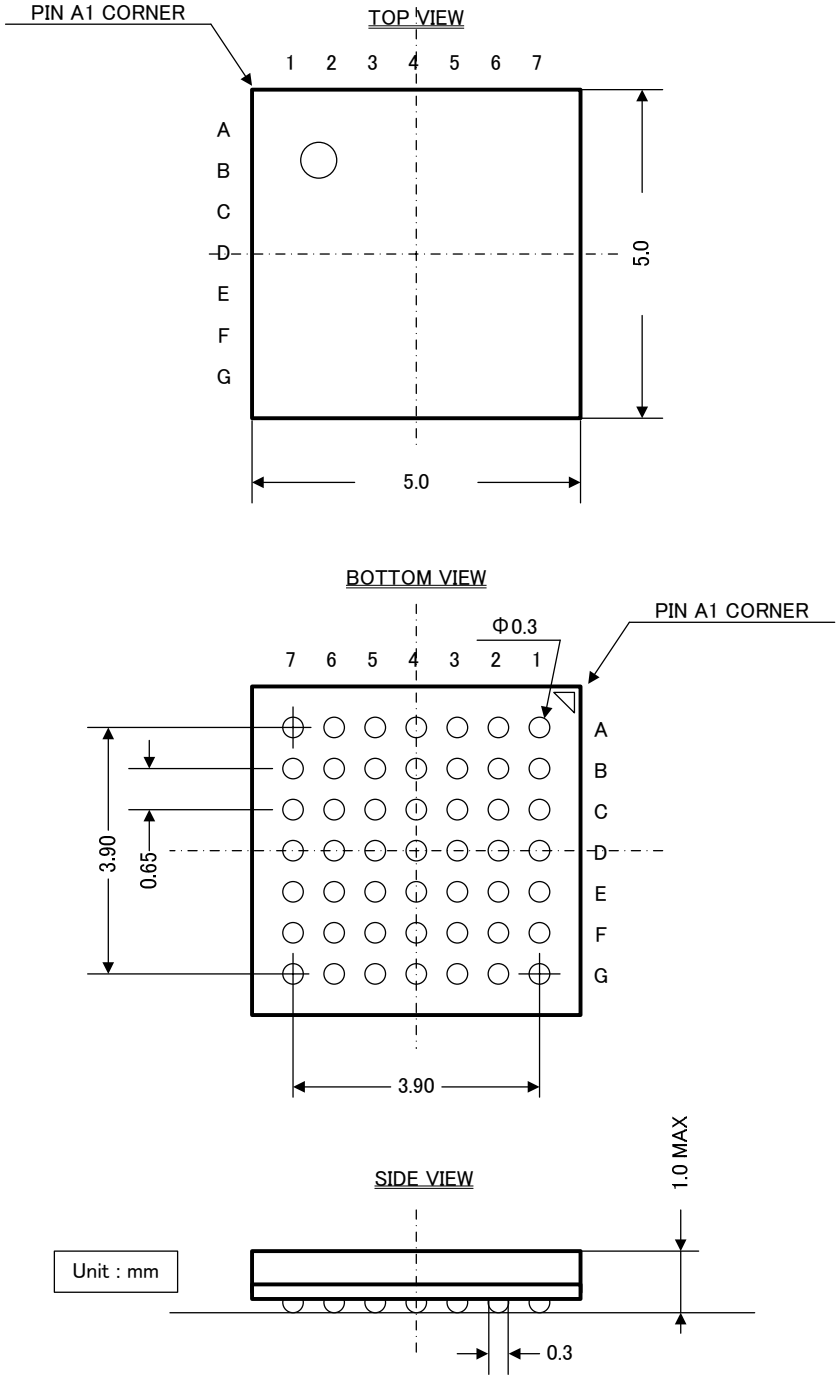


4) Asynchronous use

Asynchronous using such as following systems are not recommended.



Package


PIN A1 CORNER
TOP VIEW
1 2 3 4 5 6 7
A
B
C
D
E
F
G
5.0
5.0
BOTTOM VIEW
Φ0.3
PIN A1 CORNER
7 6 5 4 3 2 1
A
B
C
D
E
F
G
3.90
0.65
3.90
SIDE VIEW
1.0 MAX
Unit : mm
0.3

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1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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