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To Our Customers

CEL continues to offer industry leading semiconductor products from Japan. We are pleased to add new communication products from THine Electronics to our product portfolio.

THC7984

10-bit 3-channel Video Signal Digitizer

General Description

The THC7984 integrates all the functions to digitize analog video signals on a single chip.

Acceptable Signals

PC Graphics (RGB) : VGA-UXGA

- Separate Sync
- Composite Sync
- Sync on Green

Component Video (YPbPr) :

- SDTV (480i / 480p) 2-level Sync
- HDTV (1080i / 720p / 1080p) 3-level Sync
- Protection Signal

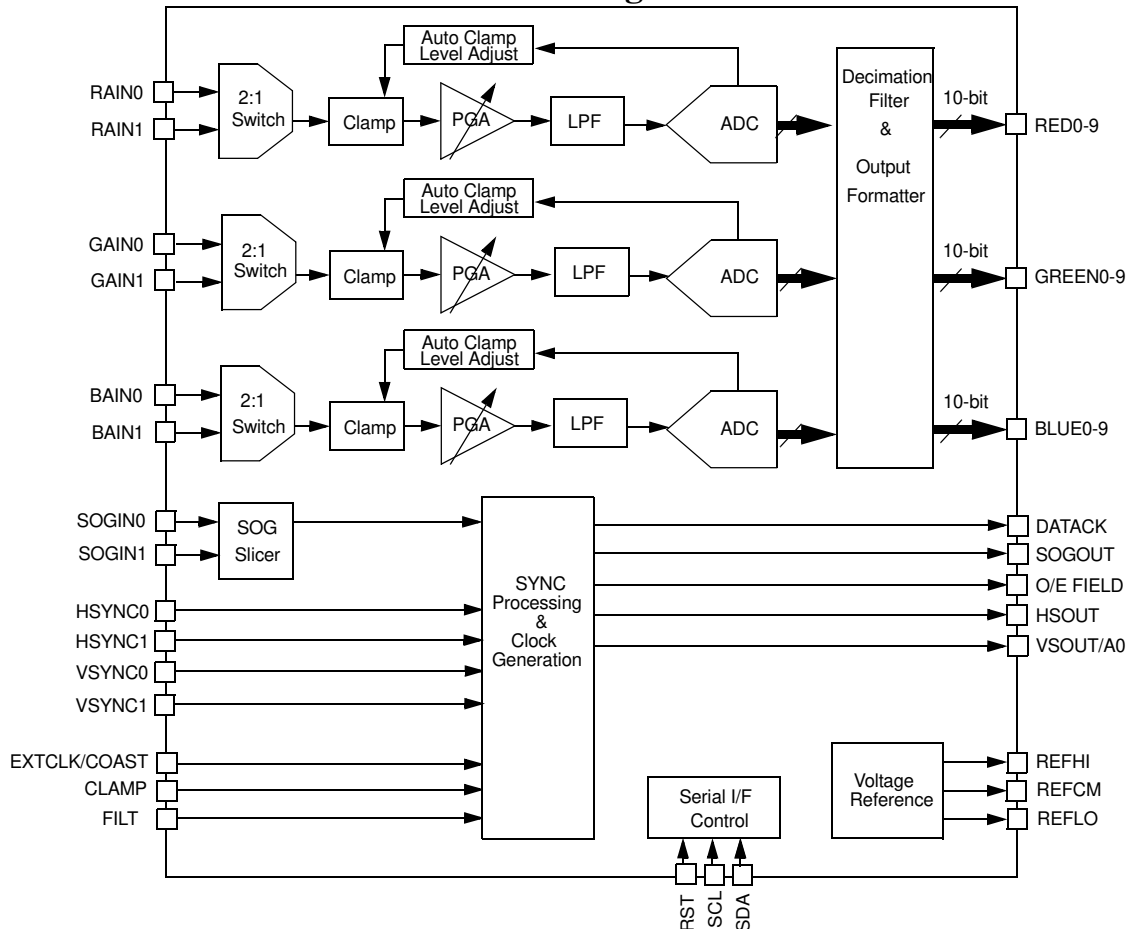
Applications

- LCD TV / PDP TV
- Rear-Projection TV
- LCD Display / PDP Display
- Front Projector etc.

Features

- 170 MSPS 10-bit ADC
- Internal 14-bit ADCs
- Oversampling functions (2x, 4x, and 8x)
- Line-locked PLL with low jitter
- Phase adjustment: 64 steps
- Fine clamp / preamp
- Pedestal / center clamp
- Clamp level auto adjust
- Very low gain mismatch
- Gain adjustment: 2048 steps
- Video Filter (LPF)
- Bandwidth adjustment: 28 steps (6MHz - 310MHz)
- Sync Processor
- 2-level / 3-level sync slicer
- Advanced sync detection / measurement
- Automatic sync processing mode
- IRQ Output
- 2-wire serial interface
- LQFP 80-pin package

Block Diagram



Specifications

VD=1.8V, VDD=3.3V, PVD=1.8V, DAVDD=1.8V, ADC Clock=Maximum Conversion Rate, Full Temperature Range=0° C to 70° C
Analog Input Voltage=0.5 to 1.0Vpp

Parameter	Temp	Test Level	THC7984-17			Unit		
			Min	Typ	Max			
RESOLUTION	Number of Bits			10		Bits		
	LSB Size			0.098		%FS		
DC ACCURACY	25° C	I	Differential Nonlinearity		± 0.75	± 1	LSB	
			Integral Nonlinearity			-1.0/+1.25	LSB	
	Full	VI	Integral Nonlinearity		± 1.5	± 3	LSB	
			No Missing Code		Guaranteed		LSB	
ANALOG INPUT	Full	VI	Minimum Input Voltage			0.5	V p-p	
	Full	VI	Maximum Input Voltage		1.0		V p-p	
	25° C	V	Gain Tempco		100		ppm/° C	
	25° C	IV	Input Bias Current*1			1	µA	
						1	µA	
	Full	VI	Input Offset Voltage		± 1		LSB	
	Full	VI	Input Full-Scale Matching Between Channels		0.2	0.8	%	
	Full	VI	Offset Adjustment Range		50		%FS	
SWITCHING PERFORMANCE	Full	VI	Maximum Conversion Rate		170		MSPS	
	Full	IV	Minimum Conversion Rate			10	MSPS	
	Full	IV	Data Setup Time to Clock*2		0.48Tpixel-2.1		ns	
	Full	IV	Data Hold Time to Clock*2		0.48Tpixel-0.4		ns	
	Full	IV	Duty Cycle, DATA*2		40	50	60	%
	Full	IV	HSYNC Input Frequency		15		110	kHz
	Full	VI	Maximum PLL Clock Rate		170		MHz	
	Full	IV	Minimum PLL Clock Rate				10	MHz
	25° C	V	PLL Jitter*3		500		ps p-p	
	Full	IV	Sampling Phase Tempco		15		ps/° C	
2-WIRE SERIAL INTERFACE	Full	IV	SCL Clock Frequency (fSCL)			100	kHz	
	Full	IV	tBUFF		4.7		µs	
	Full	IV	tSTAH		4.0		µs	
	Full	IV	tDHO		0	3.45	µs	
	Full	IV	tDAL		4.7		µs	
	Full	IV	tDAH		4.0		µs	
	Full	IV	tDSU		250		ns	
	Full	IV	tSTASU		4.7		µs	
	Full	IV	tSTOSU		4.0		µs	
	Full	IV	Tr			1000	ns	
	Full	IV	Tf			150	ns	
	Full	IV	Capacitive Load (Cb)			400	pF	
	Full	IV	Noise margin at the LOW level (VnL)		0.2		V	
	Full	IV	Noise margin at the HIGH level (VnH)		0.25		V	
	DIGITAL INPUTS	Full	VI	Input Voltage, High (VIH)		1.4		V
Full		VI	Input Voltage, Low (VIL)			0.8	V	
Full		V	Input Current, High (IIH)			10	µA	
Full		V	Input Current, Low (IIL)			10	µA	
25° C		V	Input Capacitance			2	pF	
DIGITAL OUTPUTS	Full	VI	Output Voltage, High (VOH)		VDD-0.2		V	
	Full	VI	Output Voltage, Low (VOL)			0.2	V	
	Output Coding				Binary			
POWER SUPPLY	Full	IV	VD Supply Voltage		1.7	1.8	1.9	V
	Full	IV	VDD Supply Voltage		2.3	3.3	3.45	V
	Full	IV	PVD Supply Voltage		1.7	1.8	1.9	V
	Full	IV	DAVDD Supply Voltage		1.7	1.8	1.9	V
	25° C	V	ID Supply Current (VD)				295	mA
	25° C	V	IDD Supply Current (VDD)*4				180	mA
	25° C	V	IPVD Supply Current (PVD)				30	mA
	25° C	V	IDAVDD Supply Current (DAVDD)				65	mA
	Full	VI	Total Power Dissipation				1350	mW
	Full	VI	Power-Down Supply Current			10	20	mA
	Full	VI	Power-Down Dissipation			20	40	mW
THERMAL CHARACTERISTICS	Operating Ambient Temperature		IV	0		70	° C	
	25° C	V	θ JC Junction-to-Case Thermal Resistance		4		° C/W	
	25° C	V	θ JA Junction-to-Ambient Thermal Resistance		37		° C/W	

*1 Input Bias Voltage: 0.05V to VD-0.05V

*2 See "Data/Clock Output Test Condition".

*3 THC7984-17: UXGA@60Hz

*4 Output Load Capacitance per Pin: 15pF

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at +25° C and sample tested at specified temperatures.

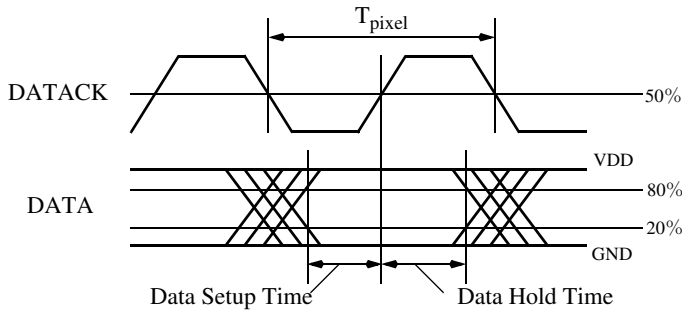
III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

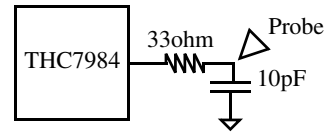
V. Parameter is a typical value only.

VI. 100% production tested at +25° C; guaranteed by design and characterization testing.

< Data Setup/Hold Time to Clock >



< Data /Clock Output Test Condition >



DATAACK: Pixel Clock
 DATAACK Phase: 4
 Output Format: Normal (not DDR)
 Output Drive Strength (VDD=3.3V) : Medium

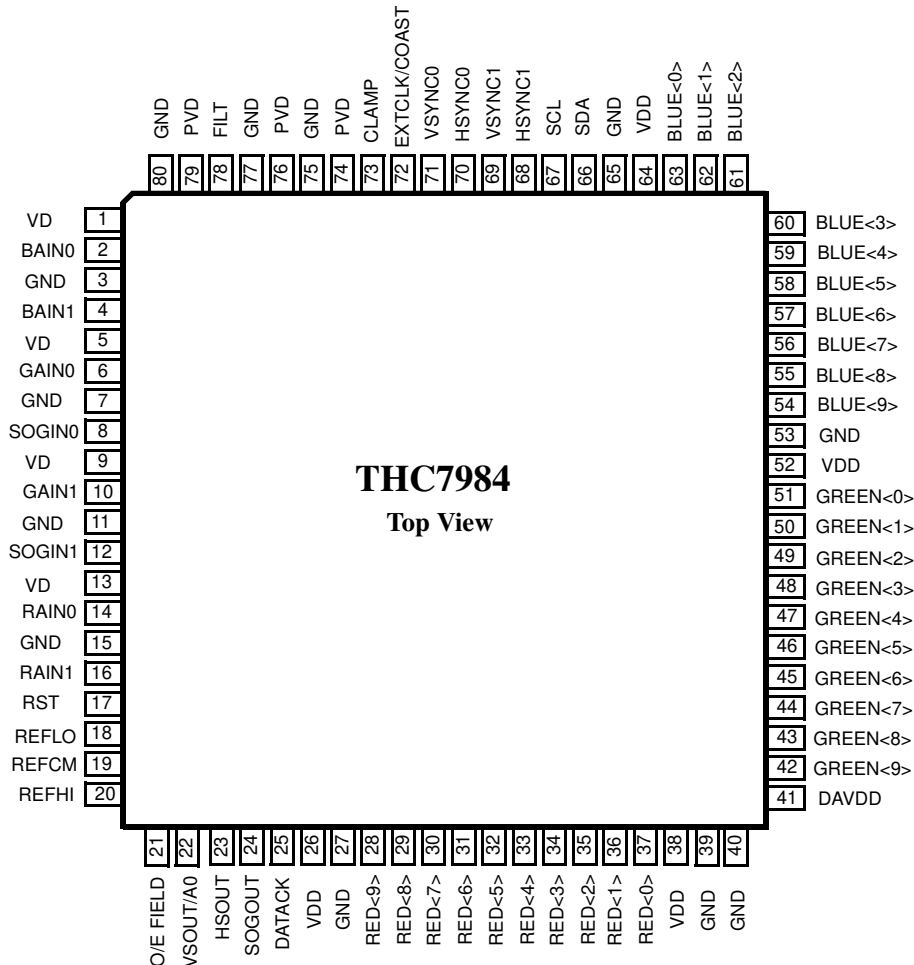
*DATAACK output phase is register programmable.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
VD		2.1	V
VDD		3.8	V
PVD		2.1	V
DAVDD		2.1	V
Analog Inputs	-0.2	VD+0.2 or 2.1*1	V
Digital Inputs	-0.3	PVD+3.6 or 5.5V*1	V
Storage Temperature	-55	150	° C
Maximum Junction Temperature		125	° C

*1 Smaller Value is adopted.

Pin Configuration



Pin List

Pin Name	Type	Function
VD	P	Analog Power Supply
VDD	P	Output Power Supply
PVD	P	PLL Power Supply
DAVDD	P	Digital Core Power Supply
GND	P	Ground
BAIN0	AI	B-ch Analog Input, Port 0
BAIN1	AI	B-ch Analog Input, Port 1
GAIN0	AI	G-ch Analog Input, Port 0
SOGIN0	AI	Sync on Green Input, Port 0
GAIN1	AI	G-ch Analog Input, Port 1
SOGIN1	AI	Sync on Green Input, Port 1
RAIN0	AI	R-ch Analog Input, Port 0
RAIN1	AI	R-ch Analog Input, Port 1
RST	DI	Reset Input Low: Normal Operation High: Power Down (Stand-by) High → Low: Chip Reset
REFLO	-	Connection for External Capacitor
REFCM	-	Connection for External Capacitor
REFHI	-	Connection for External Capacitor
O/E FIELD	DO	Field Parity Output for Interlaced Video <Other Function> Data Enable (DE) Output Sync Processor IRQ Output
VSOUT/A0	DIO	VSYNC Output / Serial Interface Device Address bit 0 (A0)
HSOUT	DO	HSYNC Output
SOGOUT	DO	SOG Slicer Output
DATAACK	DO	Data Clock Output
RED<9:0>	DO	R-ch Data Output
GREEN<9:0>	DO	G-ch Data Output
BLUE<9:0>	DO	B-ch Data Output
SCL	DI	Serial Port Data Clock Input
SDA	DIO	Serial Port Data I/O
HSYNC1	DI	HSYNC Input, Port 1
VSYNC1	DI	VSYNC Input, Port 1
HSYNC0	DI	HSYNC Input, Port 0
VSYNC0	DI	VSYNC Input, Port 0
EXTCLK/COAST	DI	External Clock Input / Coast Signal Input
CLAMP	DI	External Clamp Pulse Input <Other Function> Reference Clock Input for HSYNC Period Measure
FILT	-	Connection for PLL Loop Filter

P:Power AI:Analog Input DI:Digital Input DO:Digital Output DIO:Digital Input/Output

Functional Description

Digital Input

- All digital inputs are 5V tolerant during power-on.

Analog Input

- The THC7984 has two ports that each include three analog inputs for RGB or YPbPr. The input port can be selected by register.
- In case input signals are YPbPr, Y may be input into GAIN0 (or GAIN1) and SOGIN0 (or SOGIN1), Pr into RAIN0 (or RAIN1), and Pb into BAIN0 (or BAIN1).
- The THC7984 accommodates analog signals ranging from 0.5 V_{pp} to 1.0 V_{pp}.

Video Filter (LPF)

The THC7984 has 2 kinds of low-pass filters.

- 5th-order LPF for YPbPr, whose bandwidth is adjustable from 6 MHz to 92 MHz in 24 steps.
- 2nd-order LPF for RGB, whose bandwidth is adjustable in 4 steps (40 MHz, 90 MHz, 170 MHz, and 310 MHz).

Serial Interface

- The THC7984 is controlled by 2-wire serial interface.
- Serial clock SCL supports up to 100 kHz.

Sync Input

- The THC7984 has two ports that each include two digital inputs for the separate sync (HSYNC and VSYNC). The input port can be selected by register.
- The THC7984 can process composite sync (CSYNC). CSYNC may be input into HSYNC0 or HSYNC1.

Digital Output

- The digital outputs can operate from 2.5 V to 3.3 V (VDD).
- The output drive strength is programmable by 2-bit registers (except SDA).

Clamp

- Pedestal clamp for RGB and Y (luminance) clamps black level to 0 with automatic offset cancel.
- Midscale clamp for PbPr clamps to 512 with automatic offset cancel.
- 256-level clamp for Y (luminance) clamps to 256 with automatic offset cancel. It can be used for A/D conversion of Y including sync signal. In this case, input signal needs to be attenuated to put it within the input range of A/D converter.
- Clamp pulses can be input from CLAMP pin when external clamp is selected.

Gain, Offset

- Gain is programmable by 11-bit registers (2048 steps).
- Offset from -256 to +255 can be added to the output code.
- Gain and offset can be adjusted independently.

Reference Voltage

- The THC7984 has Band Gap Reference inside and doesn't require external voltage reference.
- The internal reference voltages (REFHI, REFCM, and REFLO) must be bypassed to stabilize. Each pin (REFHI, REFCM, and REFLO) is connected to ground through a 10 μ F capacitor.

Sampling Clock Generation

- The THC7984 has PLL to generate the sampling clock from HSYNC. The sampling clock frequency range is from 10MHz to 170 MHz.
- PLL divider ratio (the number of horizontal total pixels per line) can be set to the value between 200 to 8191.
- The sampling clock Phase can be adjusted in 64 steps of T/64.
- The external clock can be used as the sampling clock.
- It is required to set VCO Frequency Range and Charge Pump Current according to the input signal format (resolution) .

Oversampling

- Oversampling is the function that enables sampling analog signals with higher rate than the pixel clock and downsampling to the pixel clock rate with decimation filter, which is effective for improving S/N ratio.
- Oversampling ratio can be selected among 1x (normal operation) , 2x, 4x, and 8x. Even if any is selected, output frequency of the output clock and data is same as normal operation.

Output Clock (DATAACK)

- The output clock phase can be selected in 8 steps for the data setup/hold adjustment.
- Divide-by-2 clock can be selected as the output clock for the dual edge data clocking at the subsequent stage. It can not be selected when oversampling.

SOG Slicer

- Sync on Green (SOG) is sliced at the threshold level above the sync tip to extract the sync signal. The threshold level can be set by a register ranging from 15 mV to 240 mV in steps of 15mV.
- Low pass filter prior to the slicer can be used to reduce high frequency noise, which can be disabled by a register.
- The slicer also has hysteresis (about 30mV) , which can be disabled by a register.
- 3-level sync signal can be processed by slicing at the pedestal level.

Sync Processor

Sync Processor implements VSYNC separation from CSYNC, vertical timing generation, and detection and measurement of the sync signals. The various automatic sync-processing modes are realized by utilizing the sync detection and measurement.

The THC7984 can process the copy protection signal.

(1) VSYNC Separation

Extracting VSYNC from Composite sync (CSYNC) or Sync on Green (SOG) .

(2) Vertical Timing Generation

- VSYNC Output Generation
- PLL COAST Generation
- Clamp COAST Generation
- V-Blank of DE Generation

(3) Sync Detection/Measurement

- Input Sync Type Detection (Separate sync, Composite sync, Sync on Green, and No input signal)
- HSYNC, VSYNC Input Polarity Detection
- 3-level Sync Detection
- Interlace Detection
- Vertical Total Line Measurement
- VSYNC Input Pulse Width Measurement
- HSYNC Period Measurement (Reference clock needs to be input into CLAMP pin.)
- SYNC Change Detection
- HSYNC Edge Detection
- Sync Processor IRQ Output

(4) Automatic Sync Processing Mode (Manual Setting Modes are also available)

- Auto Output Mode (All outputs are enabled when input signal is active)
- Input Port Auto Select (Selects the port whose input signal is active)
- Input Sync Type Auto Select (HSYNC Input, VSYNC Input)
- HSYNC, VSYNC Input Polarity Auto Select
- HSYNC, VSYNC Output Polarity Auto Select
- VSYNC Output Timing Auto Setting
- PLL COAST Timing Auto Setting

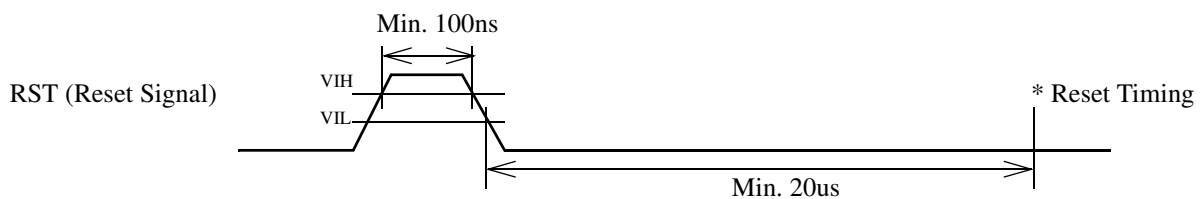
Power Control

- The THC7984 can be set to stand-by mode by a register or RST-pin.
- In stand-by mode, most of the analog circuits are powered down for low power dissipation.
- In stand-by mode, the sync detection and measurement are available nonetheless because SOG Slicer, Sync Processor, and 2-wire serial interface are still power-on.
- The THC7984 is set to stand-by mode when RST-pin is set to High. If unused, RST-pin must be pull-down to ground with a resistor.

Reset

- The logic circuit of the chip is reset when power is applied with RST-pin asserted Low (Power-on Reset) .
 - The reset can be also triggered by RST-pin (Manual Reset) . The reset is triggered when RST-pin falls from High to Low, that means the reset is triggered whenever the THC7984 gets out of stand-by mode by RST-pin.
 - Reset after power-up is necessary to access the serial interface. Please power-up with RST-pin asserted Low or make RST-pin High then Low after power-up. If unused, RST-pin must be pull-down to ground with a resistor.
 - The registers are set to the default values by the reset and the chip becomes stand-by mode and output disable (Hi-Z) .
- For normal operation, the registers must be set to power-on and output enable by the serial interface.

- For Manual Reset, keep RST-pin Low more than 20 us after the transition from High to Low.



Device Address

- The LSB of 7-bit device address of serial interface (A0) is obtained from VSOUT/A0-pin at the reset.

Pull-down to ground with a resistor (10 k Ω) , then Device Address is set to 1001100

Pull-up to VDD with a resistor (10 k Ω) , then Device Address is set to 1001101

- The pull-up resistor must be connected to VDD.

Registers

Register Notation

The register is notated with “R” added to the head of the address in hexadecimal. e.g. R00: Register of address 0x00

The bit position is notated with “[]”. e.g. R04[1:0]: Bit 1 and bit 0 of address 0x04

The register value in hexadecimal is notated with “h” added to the end. e.g. R01=18h

The register value in binary is notated with “b” added to the end. e.g. R04[1:0]=11b

The register value in decimal is notated without suffix. e.g. R15[7:0]=32

Register Classification

< Register Classification >

Sign	Category	Description	Register
R/W	Read/Write	Registers for configuration and adjustment	except below
R	Read Only	Registers which report the result of measurement and detection	R00, R2C~R30, R32~R34
A	Auto	Registers which can be auto-configured - When auto-configuration is enabled, the registers become Read Only and the value auto-configured can be read. - When auto-configuration is disabled, the registers become Read/Write and the value must be set manually.	R12[3], R12[1:0], R13[5], R13[4], R13[2], R13[1], R20[6:0], R21[5:0], R22[6:0], R23[6:0]
EVRC	Event Recorder	Registers which record the event that has occurred in Sync Processor. - 1 is set when the event occurs. - The value is cleared by writing 1 to the register.	R35

Default Value

All registers are set to the default values by the reset (Power-on Reset, Manual Reset) .

Minus Number Setting

Some registers can be configured by two's complement.

< Minus Number Setting >

Function	Register	Range
Clamp Level Offset	R0C/R0D, R0E/R0F, R10/R11	-256 to +255
HSYNC Output Start Position	R14	-128 to +127
VSYNC Output Start Position	R20	-64 to +63

Register Map

Address	Bit	R/W	Default Value	Function	Description
R 00	7	R	0	Revision Code	Can be read 21h
	6	R	0		
	5	R	1		
	4	R	0		
	3	R	0		
	2	R	0		
	1	R	0		
	0	R	1		
R 01	7				
	6				
	5				
	4	R/W	0	Chip Power-On	0: Power-Down (Stand-by Mode) 1: Power-On (Normal Operation)
	3	R/W	0	Auto Output Enable (All outputs become Enable when input signal is active)	0: Disable 1: Enable
	2	R/W	0	Output Enable (Except SOGOUT & IRQ)	0: Disable 1: Enable
	1	R/W	0	SOGOUT Output Enable	0: Disable 1: Enable
	0	R/W	0	Reserved	Must be set to 0 (Default Value)
R 02	7				
	6	R/W	0	Oversampling	00b: 1x(Normal Operation) 01b: 2x 10b: 4x 11b: 8x
	5	R/W	0		
	4	R/W	0	PLL Divider Ratio	Set the number of horizontal total pixels per line
	3	R/W	0		
	2	R/W	1		
	1	R/W	1		
	0	R/W	0		
R 03	7	R/W	1		
	6	R/W	0		
	5	R/W	0		
	4	R/W	1		
	3	R/W	1		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 04	7	R/W	1	Reserved	Must be set to 1 (Default Value)
	6	R/W	1	VCO Frequency Range	00b: 1/8 01b: 1/4 10b: 1/2 11b: 1/1
	5	R/W	1		
	4	R/W	1	Charge Pump Current	000b: 50uA 001b: 100uA 010b: 150uA 011b: 250uA 100b: 350uA 101b: 500uA 110b: 750uA 111b: 1000uA
	3	R/W	0		
	2	R/W	0		
	1	R/W	0	Sampling Clock Source	00b: Internal Clock 01b: Reserved 10b: External Clock (10-20MHz) 11b: External Clock (20-170MHz)
	0	R/W	0		
R 05	7				
	6				
	5	R/W	0	Sampling Clock Phase	Set in 64 steps of T/64 *Bigger values mean more delay.
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 06	7				
	6				
	5				
	4				
	3				
	2	R/W	1	R-ch Gain	Gain = (Register Value + 1024) / 2048 2048 steps from x0.5 to x1.5 *Bigger values mean higher gain.
	1	R/W	0		
	0	R/W	0		
R 07	7	R/W	0		
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		

R 08	7				
	6				
	5				
	4				
	3				
	2	R/W	1	G-ch Gain	Gain = (Register Value + 1024) / 2048 2048 steps from x0.5 to x1.5 *Bigger values mean higher gain.
1	R/W	0			
0	R/W	0			
R 09	7	R/W	0		
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
1	R/W	0			
0	R/W	0			
R 0A	7				
	6				
	5				
	4				
	3				
	2	R/W	1	B-ch Gain	Gain = (Register Value + 1024) / 2048 2048 steps from x0.5 to x1.5 *Bigger values mean higher gain.
1	R/W	0			
0	R/W	0			
R 0B	7	R/W	0		
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
1	R/W	0			
0	R/W	0			
R 0C	7				
	6				
	5				
	4				
	3				
	2				
1					
0	R/W	0	R-ch Clamp Level Offset	1 LSB of offset corresponds to 1 LSB of output code. -256 to +255 *Set in two's complement.	
7	R/W	0			
6	R/W	0			
5	R/W	0			
4	R/W	0			
3	R/W	0			
2	R/W	0			
1	R/W	0			
0	R/W	0			
R 0E	7				
	6				
	5				
	4				
	3				
	2				
1					
0	R/W	0	G-ch Clamp Level Offset	1 LSB of offset corresponds to 1 LSB of output code. -256 to +255 *Set in two's complement.	
7	R/W	0			
6	R/W	0			
5	R/W	0			
4	R/W	0			
3	R/W	0			
2	R/W	0			
1	R/W	0			
0	R/W	0			

R 10	7				
	6				
	5				
	4				
	3				
	2				
	1				
	0	R/W	0	B-ch Clamp Level Offset	1 LSB of offset corresponds to 1 LSB of output code. -256 to +255 *Set in two's complement.
R 11	7	R/W	0		
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 12	7	R/W	0	Reserved	Must be set to 0
	6	R/W	0	Reserved	Must be set to 0
	5	R/W	1	Input Port Automatic Selection Enable	0: Disable 1: Enable
	4	R/W	0	Reserved	Must be set to 0
	3	A	0	Input Port	0: Port-0 1: Port-1
	2	R/W	1	Sync Type Automatic Select Enable	0: Disable 1: Enable
	1	A	0	Sync Type Select	00b: Separate Sync 01b: Composite Sync 10b: Sync on Video (2-level) 11b: Sync on Video (3-level)
	0	A	0		
R 13	7				
	6	R/W	1	HSYNC Input, VSYNC Input Polarity Automatic Selection Enable	0: Disable 1: Enable
	5	A	0	HSYNC Input Polarity	0: Active-Low 1: Active-High
	4	A	0	VSYNC Input Polarity	0: Active-Low 1: Active-High
	3	R/W	1	HSYNC Output, VSYNC Output Polarity Automatic Selection Enable	0: Disable 1: Enable (Output Polarity is conformed to Input Polarity)
	2	A	0	HSYNC Output (HSOUT) Polarity	0: Active-Low 1: Active-High
	1	A	0	VSYNC Output (VSOUT) Polarity	0: Active-Low 1: Active-High
	0	R/W	1	VSYNC Output (VSOUT) Interface Mode	0: Disable 1: Enable
R 14	7	R/W	0	HSYNC Output (HO) Start Position	Set in 1 pixel steps with reference to the leading edge of HSYNC input -128 to +127 *Set in two's complement.
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 15	7	R/W	0	HSYNC Output (HO) Pulse Width	Set in 1 pixel steps 1 to 255
	6	R/W	0		
	5	R/W	1		
	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 16	7				
	6				
	5				
	4	R/W	0	PLL COAST Source	0: Internal PLL COAST 1: External PLL COAST
	3	R/W	1	PLL/Clamp COAST Input Polarity (If COAST Source is External)	0: Active-Low 1: Active-High
	2	R/W	0	Clamp Pulse Source	0: Internal Clamp Pulse 1: External Clamp Pulse
	1	R/W	1	Clamp Pulse Input Polarity (If COAST Source is External)	0: Active-Low 1: Active-High
	0	R/W	0	Clamp COAST Source	0: Internal Clamp COAST 1: External Clamp COAST
R 17	7				
	6	R/W	1	Clamp Pulse Start Reference Edge (Pedestal Clamp, Midscale Clamp)	0: the leading edge of HSYNC Input 1: the trailing edge of HSYNC Input
	5	R/W	0	R-ch Clamp Mode	00b: Pedestal Clamp 01b: Midscale Clamp 10b: Reserved 11b: 256-level clamp
	4	R/W	0		
	3	R/W	0	G-ch Clamp Mode	00b: Pedestal Clamp 01b: Midscale Clamp 10b: Reserved 11b: 256-level clamp
	2	R/W	0		
	1	R/W	0	B-ch Clamp Mode	00b: Pedestal Clamp 01b: Midscale Clamp 10b: Reserved 11b: 256-level clamp
	0	R/W	0		

R 18	7	R/W	0	Clamp Pulse Start Position	Set in 1 pixel steps with the reference edge of HSYNC Input (R17[6]). 0 to 255
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
	3	R/W	1		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 19	7	R/W	0	Clamp Pulse Width	Set in 1 pixel steps 1 to 255
	6	R/W	0		
	5	R/W	0		
	4	R/W	1		
	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	0		
R 1A	7	R/W			
	6	R/W	1	SOG Slicer Hysteresis Enable	0: Disable 1: Enable
	5	R/W	1	SOG Input Filter	00b: Disable 01b: Enable
	4	R/W	0		10b, 11b: Reserved
	3	R/W	0	SOG Slicer threshold	Set in 15mV steps 15mV to 240mV above the Sync Tip
	2	R/W	1		
	1	R/W	0		
	0	R/W	0		
R 1B	7	R/W	0	SOGOUT Output Polarity	0: Active-Low 1: Active-High
	6	R/W	0	SOGOUT Output Signal	00b: Raw HSYNC 01b: Regenerated HSYNC
	5	R/W	0		10b: Filtered HSYNC 11b: Reserved
	4	R/W	1	Preamp Bandwidth (Low Pass Filter)	
	3	R/W	1		
	2	R/W	0		
	1	R/W	1		
	0	R/W	0		
R 1C	7	R/W	0	Output Format	00b: 4: 4: 4 Output 01b: 4: 4: 4 DDR Output
	6	R/W	0		10b: 4: 2: 2 Output 11b: 4: 2: 2 DDR Output
	5	R/W	1	4:2:2 Decimation Filter Enable	0: Disable 1: Enable
	4	R/W	0	Output Clock (DATAACK)	00b: Pixel Clock 01b: 1/2x Pixel Clock
	3	R/W	0		10b: Internal Oscillator (40MHz) 11b: Reserved
	2	R/W	1	Output Clock Phase	Set in 1/8 steps 0 to 7/8T
	1	R/W	0		*Bigger values mean more delay.
	0	R/W	0		
R 1D	7	R/W	1	Reserved	Must be set to 0
	6	R/W	0	Reserved	Must be set to 1
	5	R/W	0	RGB DATA Output Drive Strength	00b: Weak 01b: Medium 10b: Strong 11b: Very Strong
	4	R/W	1		
	3	R/W	0	Sync (SOGOUT/HSOUT/VSOUT/OEFIELD) Output Drive Strength	00b: Weak 01b: Medium 10b: Strong 11b: Very Strong
	2	R/W	1		
	1	R/W	0	Clock Output Drive Strength	00b: Weak 01b: Medium 10b: Strong 11b: Very Strong
	0	R/W	1		
R 1E	7	R/W	0	HSOUT Output Signal	00b: HO 01b: Regenerated HSYNC 10b: Raw HSYNC 11b: Filtered HSYNC
	6	R/W	0		
	5	R/W	0	VSOUT Output Signal	00b: VO 01b: Regenerated VSYNC 10b: Raw VSYNC 11b: Filtered VSYNC
	4	R/W	1		
	3	R/W	0	O/E FIELD Output Signal	000b: FO 001b: Regenerated FIELD 010b: DE 011b: IRQ
	2	R/W	0		100b to 111b: Reserved
	1	R/W	1		
	0	R/W	0	O/E FIELD Output Polarity	0: Odd Field=Low/Even Field=High 1: Odd Field=High/Even Field=Low
R 1F	7				
	6	R/W	0	Reserved	Must be set to 0
	5	R/W	0	Reserved	Must be set to 0
	4	R/W	1	PLL HSYNC Filter Enable	0: Disable (Raw HSYNC) 1: Enable (Filtered HSYNC)
	3	R/W	0	HSYNC Filter Window Width	Set in +/-100ns steps +/-100ns to +/-1600ns
	2	R/W	0		
	1	R/W	1		
	0	R/W	1		*Bigger values mean wider window.

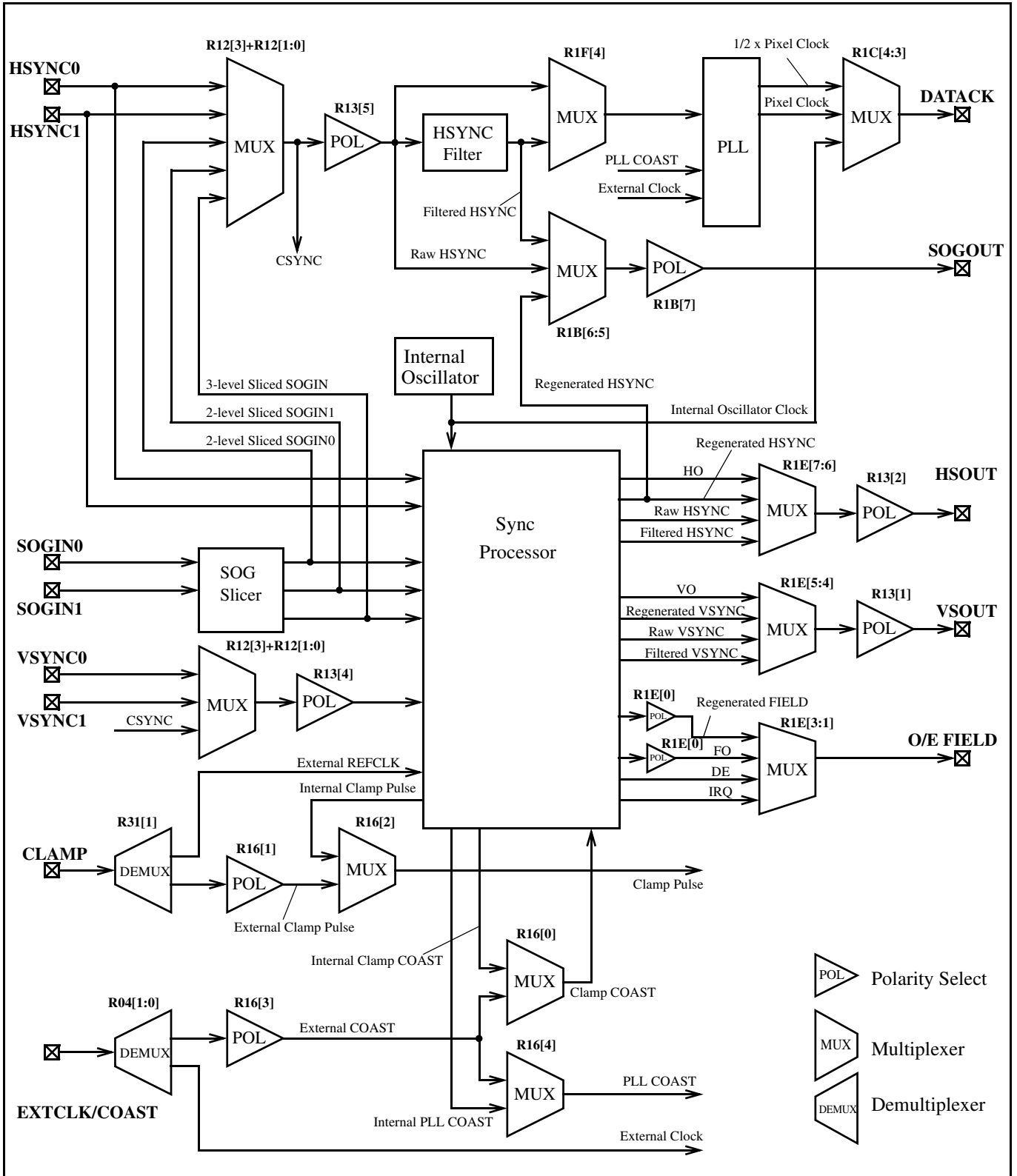
R 20	7	R/W	1	VSYNC Output Timing Automatic Setting Enable (Except Raw VSYNC)	0: Disable 1: Enable		
	6	A	0	VSYNC Output (VO, Regenerated VSYNC) Start Position	Set in 1 line steps -64 to +63 *Set in two's complement. *VSYNC Output Start Position with reference to the leading edge of VSYNC Input.		
	5	A	0				
	4	A	0				
	3	A	0				
	2	A	0				
	1	A	0				
	0	A	0				
R 21	7						
	6						
	5	A	0	VSYNC Output (VO, Regenerated VSYNC) Pulse Width	Set in 1 line steps 1 to 63		
	4	A	0				
	3	A	0				
	2	A	0				
	1	A	0				
	0	A	0				
R 22	7	R/W	1			PLL COAST Timing Automatic Setting Enable	0: Disable 1: Enable
	6	A	0			PLL Pre-Coast (PLL COAST Start Position) *PLL free-runs during PLL COAST	Set in 1 line steps 0 to 127 *PLL COAST Start Position prior to the leading edge of VSYNC Input.
	5	A	0				
	4	A	0				
	3	A	0				
	2	A	0				
	1	A	0				
	0	A	0				
R 23	7						
	6	A	0	PLL Post-Coast (PLL COAST End Position) *PLL free-runs during PLL COAST	Set in 1 line steps 0 to 127 *PLL COAST End Position after the leading edge of VSYNC Input.		
	5	A	0				
	4	A	0				
	3	A	0				
	2	A	0				
	1	A	0				
	0	A	1				
R 24	7						
	6	R/W	0	Clamp Pre-Coast (Clamp COAST Start Position) *Clamp stops during Clamp COAST	Set in 1 line steps 0 to 127 *Clamp COAST Start Position prior to the leading edge of VSYNC Input.		
	5	R/W	0				
	4	R/W	0				
	3	R/W	0				
	2	R/W	1				
	1	R/W	1				
	0	R/W	0				
R 25	7						
	6	R/W	0	Clamp Post-Coast (Clamp COAST End Position) *Clamp stops during Clamp COAST	Set in 1 line steps 0 to 127 *Clamp COAST End Position after the leading edge of VSYNC Input.		
	5	R/W	0				
	4	R/W	1				
	3	R/W	0				
	2	R/W	1				
	1	R/W	0				
	0	R/W	0				
R 26	7						
	6						
	5						
	4						
	3	R/W	0	DE Start Position	Set in 1 pixel steps *DE Start Position after the leading edge of HSYNC Input.		
	2	R/W	0				
	1	R/W	0				
	0	R/W	1				
R 27	7	R/W	0				
	6	R/W	1				
	5	R/W	1				
	4	R/W	1				
	3	R/W	0				
	2	R/W	0				
	1	R/W	0				
	0	R/W	0				

R 28	7				
	6				
	5				
	4				
	3	R/W	0	DE Width	Set in 1 pixel steps
R 29	2	R/W	1		
	1	R/W	0		
	0	R/W	1		
	7	R/W	0		
	6	R/W	0		
	5	R/W	0		
	4	R/W	0		
R 2A	3	R/W	0		
	2	R/W	0		
	1	R/W	0		
	0	R/W	1		
	7	R/W	0	V-Blank Front Porch (DE Low Start Position)	Set in 1 line steps 0 to 127 *V-Blank Start Position prior to the leading edge of VSYNC Output.
	6	R/W	0		
	5	R/W	0		
R 2B	4	R/W	0		
	3	R/W	0		
	2	R/W	0		
	1	R/W	1		
	0	R/W	0		
	7	R/W	0	V-Blank Back Porch (DE Low Start Position)	Set in 1 line steps 0 to 127 *V-Blank End Position after the trailing edge of VSYNC Output.
	6	R/W	1		
R 2C	5	R	1	Reserved	
	4	R	1	Reserved	
	3	R	1	Port-1 Input Sync Type Detection	00b: Separate Sync 01b: Composite Sync 10b: Sync on Video 11b: No Signal
	2	R	1	Port-0 Input Sync Type Detection	00b: Separate Sync 01b: Composite Sync 10b: Sync on Video 11b: No Signal
	1	R	1		
	0	R	1		
	7				
R 2D	6				
	5				
	4				
	3				
	2	R	0	VSYNC Input Polarity Detection	0: Active-Low 1: Active-High
	1	R	0	HSYNC Input Polarity Detection	0: Active-Low 1: Active-High
	0	R	0	Sync on Video 2-level/3-level Detection	0: 2-level 1: 3-level
R 2E	7	R	0	Interlace Detection	0: Progressive 1: Interlace
	6	R	0	Vertical Total Line Measurement	Reports the number of vertical total lines on the active input counted in 1/4 line unit.
	5	R	0		
	4	R	0		
	3	R	0		
	2	R	0		
	1	R	0		
R 2F	0	R	0		
	7	R	0		
	6	R	0		
	5	R	0		
	4	R	0		
	3	R	0		
	2	R	0		

R 30	7	R	0	VSYNC Input Pulse Width Measurement	Reports the number of VSYNC Pulse Width on the active input counted in 1/4 line unit.
	6	R	0		
	5	R	0		
	4	R	0		
	3	R	0		
	2	R	0		
	1	R	0		
	0	R	0		
R 31	7				
	6				
	5				
	4				
	3				
	2	R/W	0	Reserved	Must be set to 0
1	R/W	0	Reference Clock Enable from Clamp-pin for HSYNC Period Measurement	0: Disable 1: Enable	
0	R/W	1	HSYNC Period Measurement Run (Must be stop before reading the result)	0: Stop 1: Run	
R 32	7				
	6				
	5				
	4				
	3	R	0	HSYNC Period Measurement Result	
	2	R	0		
	1	R	0		
	0	R	0		
0	R	0			
R 33	7	R	0		
	6	R	0		
	5	R	0		
	4	R	0		
	3	R	0		
	2	R	0		
	1	R	0		
	0	R	0		
R 34	7	R	0		
	6	R	0		
	5	R	0		
	4	R	0		
	3	R	0		
	2	R	0		
	1	R	0		
	0	R	0		
R 35	7	EVRC	0	Sync Signal Valid Flag	0: Detect 1: Not Detect
	6	EVRC	0	Reserved	
	5	EVRC	0	Reserved	
	4	EVRC	0	Port-1 Input Sync Type Change Detection	0: Detect 1: Not Detect
	3	EVRC	0	Port-0 Input Sync Type Change Detection	0: Detect 1: Not Detect
	2	EVRC	0	Input Signal Format Change Detection	0: Detect 1: Not Detect
	1	EVRC	0	Input HSYNC Missing Edge Detection	0: Detect 1: Not Detect
	0	EVRC	0	Input HSYNC Extraneous Edge Detection	0: Detect 1: Not Detect
R 36	7	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[7])	0: Disable 1: Enable
	6	R/W	0	Reserved	
	5	R/W	0	Reserved	
	4	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[4])	0: Disable 1: Enable
	2	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[3])	0: Disable 1: Enable
	2	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[2])	0: Disable 1: Enable
	1	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[1])	0: Disable 1: Enable
	0	R/W	0	Sync Processor IRQ Output Enable by Event Recorder (R34[0])	0: Disable 1: Enable
R 37	7	R/W	0	Input Signal Format Change Detection	00b: 0.5lines 001b: 1line 010b: 2lines 011b: 4lines
	6	R/W	0	- Threshold of Vertical Total Line Change	100b: 8lines 101b: 16lines 110b: 32lines 111b: Do not watching
	5	R/W	0		
	4	R/W	0	Input Signal Format Change Detection	00b: 0.5lines 01b: 1line 10b: 4lines 11b: Do not watching
	2	R/W	0	- Threshold of VSYNC Input Pulse Width	
	2	R/W	0	Input Signal Format Change Detection	000b: 8 001b: 16 010b: 32 011b: 64
	1	R/W	0	- Threshold of HSYNC Period	100b: 128 101b: 256 110b: 512 111b: Do not watching
	0	R/W	0		

Sync Signal Flow

< Sync Processing Block Diagram >



Register Function

R00 Revision Code 21h can be read

R01[4] Chip Power-On

1: all the circuits power-on for normal operation.

0: the chip is set to stand-by mode. In stand-by mode, several circuits are active for sync monitoring.

Stand-by mode can be triggered by RST-pin.

< Power Control >

R01[4]	RST-pin	Status	ADC/PLL	Serial Interface	SOG Slicer	Sync Processor
1	Low	Normal Operation	Power-On	Power-On	Power-On	Power-On
1	High	Stand-by	Power-Down	Power-On	Power-On	Power-On
0	Low	Stand-by	Power-Down	Power-On	Power-On	Power-On
0	High	Stand-by	Power-Down	Power-On	Power-On	Power-On

* During the stand-by mode, all the output pins except SOGOUT and SDA are disable (Hi-Z) .

R01[3] Auto Output Enable

1: all the output pins are automatically enabled regardless of “Output Enable except SOGOUT (R01[2]) ” or “SOGOUT Output Enable (R01[1]) ” while input sync is detected. Input sync detection is processed in Sync Processor.

* Output Pins are RED<9:0>, GREEN<9:0>, BLUE<9:0>, DATAACK, SOGOUT, HSOUT, VSOUT, and O/E FIELD

R01[2] Output Enable (Except SOGOUT)

1: Output pins except SOGOUT-pin are enabled.

R01[1] SOGOUT Output Enable

1: SOGOUT-pin is enabled.

< Output Control >

R01[3]	R01[2]	R01[1]	Input Signal	Output Signal except SOGOUT	SOGOUT
0	0	0	Inactive	Disable	Disable
0	0	0	Active	Disable	Disable
0	0	1	Inactive	Disable	Enable
0	0	1	Active	Disable	Enable
0	1	0	Inactive	Enable	Disable
0	1	0	Active	Enable	Disable
0	1	1	Inactive	Enable	Enable
0	1	1	Active	Enable	Enable
1	0	0	Inactive	Disable	Disable
1	0	0	Active	Enable	Enable
1	0	1	Inactive	Disable	Enable
1	0	1	Active	Enable	Enable
1	1	0	Inactive	Enable	Disable
1	1	0	Active	Enable	Enable
1	1	1	Inactive	Enable	Enable
1	1	1	Active	Enable	Enable

* When disabled, output pins are Hi-Z.

* SDA-pin is always enabled.

R01[0] Reserved * Must be set to 0 (Default Value: 0)

R02[6:5] Oversampling

Oversampling is the function that enables sampling analog signals with higher rate than the pixel clock and downsampling to the pixel clock rate with the decimation filter.

When setting it as oversampling, setting of the PLL Divider Ratio (R02 [4:0] /R03 [7:0]) and the Charge Pump Current (R04 [4:2]) is unnecessary, but it's necessary to change the VCO frequency range (R04 [6:5]) .

Every time the oversampling setting is increased one step, VCO frequency range also must be increased one step.

00b: Normal operation

01b: 2x Oversampling

10b: 4x Oversampling

11b: 8x Oversampling

(ex) In case of 480i (HSYNC Frequency: 15.75kHz / Pixel Clock: 13.51MHz)

Oversampling(R02[6:5])	VCO Range(R04[6:5])	Charge Pump(R04[4:2])
1x(00b)	1/8(00b)	250uA(011b)
2x(01b)	1/4(01b)	250uA(011b)
4x(10b)	1/2(10b)	250uA(011b)
8x(11b)	1/1(11b)	250uA(011b)

* Under the output of 4:4:4 DDR (R1C[7:6]=01b) or 4:2:2 DDR (R1C[7:6]=11b), the oversampling function can't be used.

* "Internal PLL Divider Ratio" can't be over 8191.

"Internal PLL Divider Ratio" = PLL Divider Ratio setting * Oversampling setting

* Sampling frequency can't be over 170MHz

Sampling frequency = Input HSYNC frequency * PLL Divider Ratio * Oversampling setting

* Even if oversampling setting is changed, the output clock frequency and the output data rate don't change.

* The latency of the data output changes according to the oversampling setting.

R02[4:0]/R03[7:0] PLL Divider Ratio

The internal PLL generates sampling clock from HSYNC.

Set the number of horizontal total pixels per line according to the input signal.

*When the external clock input which is supplied through EXTCLK/COAST-pin is used as sampling clock (R04[1:0]=10b or 11b), PLL Divider Ratio setting is unnecessary.

R04[7] Reserved *Must be set to 1 (Default value: 1)

R04[6:5] VCO Frequency Range *Set according to "Recommended PLL Settings"

R04[4:2] Charge Pump Current *Set according to "Recommended PLL Settings"

R04[1:0] Sampling Clock Source

Set to 00b, when the internal PLL generates sampling clock (pixel clock) from the HSYNC input.

When an external clock input supplied through EXTCLK/COAST-pin is used and the clock frequency is from 10 to 20MHz, set to 10b.

When an external clock input supplied through EXTCLK/COAST-pin is used and the clock frequency is from 20 to 170MHz, set to 11b.

* Even though the external clock is used as sampling clock(R04[1:0]=10b or 11b) , setting like a Recommended PLL Settings are necessary.

* When the external clock is used as sampling clock(R04[1:0]=10b or 11b) , PLL COAST and Clamp COAST can not be input (R16[4]=1, R16[0]=1) .

< Recommended PLL Settings >

	Hsync [kHz]	Pixel Rate	PLL Divider	Sampling Clock: Internal				Sampling Clock: External			
				R04[6:5]	R04[4:2]	R04[1:0]	R04	R04[6:5]	R04[4:2]	R04[1:0]	R04
480i	15.750	13.51	858	00	011	00	8C	00	000	10	82
480p	31.469	27.00	858	01	011	00	AC	01	000	11	A3
720p	45.000	74.25	1650	10	101	00	D4	10	000	11	C3
1080i	33.750	74.25	2200	10	100	00	D0	10	000	11	C3
1080p	67.500	148.50	2200	11	101	00	F4	11	000	11	E3
VGA-60	31.479	25.18	800	01	011	00	AC	01	000	11	A3
VGA-72	37.861	31.50	832	01	100	00	B0	01	000	11	A3
VGA-75	37.500	31.50	840	01	100	00	B0	01	000	11	A3
VGA-85	43.269	36.00	832	01	101	00	B4	01	000	11	A3
SVGA-56	35.156	36.00	1024	01	100	00	B0	01	000	11	A3
SVGA-60	37.879	40.00	1056	01	101	00	B4	01	000	11	A3
SVGA-72	48.077	50.00	1040	10	100	00	D0	10	000	11	C3
SVGA-75	46.875	49.50	1056	10	100	00	D0	10	000	11	C3
SVGA-85	53.674	56.25	1048	10	100	00	D0	10	000	11	C3
XGA-60	48.363	65.00	1344	10	100	00	D0	10	000	11	C3
XGA-70	56.476	75.00	1328	10	101	00	D4	10	000	11	C3
XGA-75	60.023	78.75	1312	10	101	00	D4	10	000	11	C3
XGA-80	64.000	85.50	1336	11	011	00	EC	11	000	11	E3
XGA-85	68.677	94.50	1376	11	100	00	F0	11	000	11	E3
SXGA-60	63.981	108.00	1688	11	100	00	F0	11	000	11	E3
SXGA-75	79.976	135.00	1688	11	101	00	F4	11	000	11	E3
SXGA-85	91.146	157.50	1728	11	101	00	F4	11	000	11	E3
UXGA-60	75.000	162.00	2160	11	101	00	F4	11	000	11	E3

* Other than the settings above, please refer to the other document, "THC7984 PLL Setting Sheet".

R05[5:0] Sampling Clock Phase

The sampling clock phase can be shifted in 64 steps of T/64. Bigger values mean more delay.

* Even the external clock is used as sampling clock(R04[1:0]=10b or 11b) , the clock phase can be shifted.

R06[2:0]/R07[7:0] R-ch (Pr-ch) Gain

R08[2:0]/R09[7:0] G-ch (Y-ch) Gain

R0A[2:0]/R0B[7:0] B-ch (Pb-ch) Gain

The gain can be adjusted from 0.5 to 1.5 in 2048 steps. Bigger value means higher gain.

$$\text{Gain} = (\text{Register Value} + 1024) / 2048$$

Because the full scale of ADC input is 0.7 Vpp (Typical Value) , the gain is set to [0.7 / Video Signal Level*].

* Signal Level without Sync on Video (Vpp)

Example.

Video Signal Level: 0.5 Vpp Gain = 0.7/0.5 =1.4 Register value=1843

Video Signal Level: 0.7 Vpp Gain = 0.7/0.7 =1.0 Register value=1024

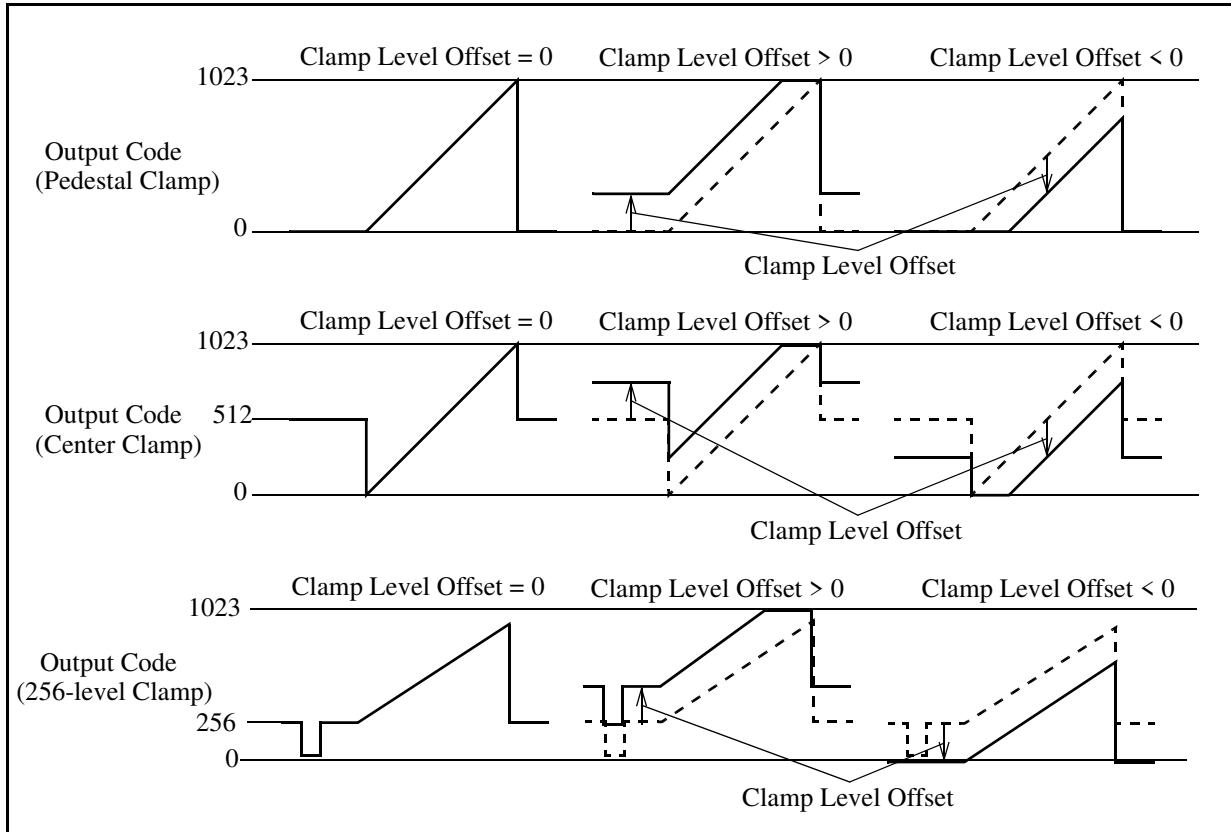
Video Signal Level: 1.0 Vpp Gain = 0.7/1.0 =0.7 Register value=410

* The setting method above is not always necessary for the purpose of contrast adjustment. Bigger gain means higher contrast.

R0C[0]/R0D[7:0] R-ch (Pr-ch) Clamp Level Offset
R0E[0]/R0F[7:0] G-ch (Y-ch) Clamp Level Offset
R10[0]/R11[7:0] B-ch (Pb-ch) Clamp Level Offset

Clamping restores DC level of the video signals. Three clamp modes can be selected; Pedestal clamp, Center clamp (Midscale clamp), and Sync tip clamp (R17[5:4]/R17[3:2]/R17[1:0]).

It's possible to give an offset to the clamp level by the 1LSB unit by a clamp level offset. The register value is configured by two's complement from -256 to +255.

< Clamp Level Offset >


R12[7:6] Reserved *Must be set to 00b (Default value: 00b)

R12[5] Input Port Automatic Selection Enable

1: Selection input port (R12[3]) is done automatically.

Under Automatic setting, with the judgement result of the input SYNC type by Sync Processor, An activated port is selected with the following rules.

- When the selected port is activated, even if the other port becomes activated, selection of port doesn't change.
- Both ports are activate and one port which is selected became inactivate, selection of port changes to the other port.

R12[4] Reserved * Must be set to 0 (Default Value: 0)
R12[3] Input Port Select

0: Port-0 is selected.

Port-0: HSYNC0, VSYNC0, RAIN0, GAIN0, SOGIN0, BAIN0

1: Port-1 is selected.

Port-1: HSYNC1, VSYNC1, RAIN1, GAIN1, SOGIN1, BAIN1

R12[2] Input Sync Type Automatic Select Enable

1: Input Sync Type Select (R12[1:0]) is automatically set.

When Automatic Select is enabled, Input Sync Type Select is determined by sync processor based on the result of Input Sync Type Detection(R2C[6:5]/R2C[4:3]/R2C[0]) .

R12[1:0] Input Sync Type Select

Select the input sync type.

The combination of Input Port Select (R12[3]) and Input Sync Type Select (R12[1:0]) determines the input pin for HSYNC and VSYNC.

< Input Port / Sync Type >

R12[3]	Input Port	R12[1:0]	Sync Type	HSYNC Input Pin	VSYNC Input Pin
0	Port-0	00b	Separate Sync	HSYNC0	VSYNC0
0	Port-0	01b	Composite Sync	HSYNC0	HSYNC0
0	Port-0	10b	Sync on Video (2-level)	SOGIN0	SOGIN0
0	Port-0	11b	Sync on Video (3-level)	SOGIN0*	SOGIN0*
1	Port-1	00b	Separate Sync	HSYNC1	VSYNC1
1	Port-1	01b	Composite Sync	HSYNC1	HSYNC1
1	Port-1	10b	Sync on Video (2-level)	SOGIN1	SOGIN1
1	Port-1	11b	Sync on Video (3-level)	SOGIN1*	SOGIN1*

*3-level sliced (pedestal slice) .

R13[6] HSYNC Input, VSYNC Input Polarity Automatic Select Enable

1: HSYNC Input Polarity (R13[5]) and VSYNC Input Polarity (R13[4]) are automatically set.

When Automatic Select is enabled, the sync input polarity is determined by sync processor based on the result of HSYNC Input Polarity Detection (R2C[1]) and VSYNC Input Polarity Detection (R2C[2]) .

R13[5] HSYNC Input Polarity

HSYNC Input Polarity must be correctly set for normal operation.

Set to 0 when the input polarity is Active-Low.

Set to 1 when the input polarity is Active-High.

* Set to 0 when Input Sync Type Select is set to "Sync on Video (3-level) " (R12[1:0]=11b) .

R13[4] VSYNC Input Polarity

VSYNC Input Polarity must be correctly set for normal operation.

Set to 0 when the input polarity is Active-Low.

Set to 1 when the input polarity is Active-High.

R13[3] HSYNC Output, VSYNC Output Polarity Automatic Select Enable

1: HSYNC Output Polarity (R13[2]) and VSYNC Output Polarity (R13[1]) are automatically set to the same polarity as the input.

When Automatic Select is enabled, the sync output polarity is determined by sync processor based on the result of HSYNC Input Polarity Detection (R2D[1]) and VSYNC Input Polarity Detection (R2D[2]).

R13[2] HSYNC Output (HSOUT) Polarity

Select the HSYNC output polarity of HSOUT-pin.

0: Output polarity is Active-Low.

1: Output polarity is Active-High.

* The polarity of HSYNC available from HSOUT-pin (HO, Regenerated HSYNC) is selected.

R13[1] VSYNC Output (VSOUT) Polarity

Select the VSYNC output polarity of VSOUT-pin.

0: Output polarity is Active-Low.

1: Output polarity is Active-High.

* The polarity of VSYNC available from VSOUT-pin (VO, Regenerated VSYNC, Raw VSYNC) is selected.

R13[0] VSYNC Output (VSOUT) Interlace Mode

Select the output mode of VSYNC available from VSOUT-pin (VO, Regenerated VSYNC) for interlaced video input.

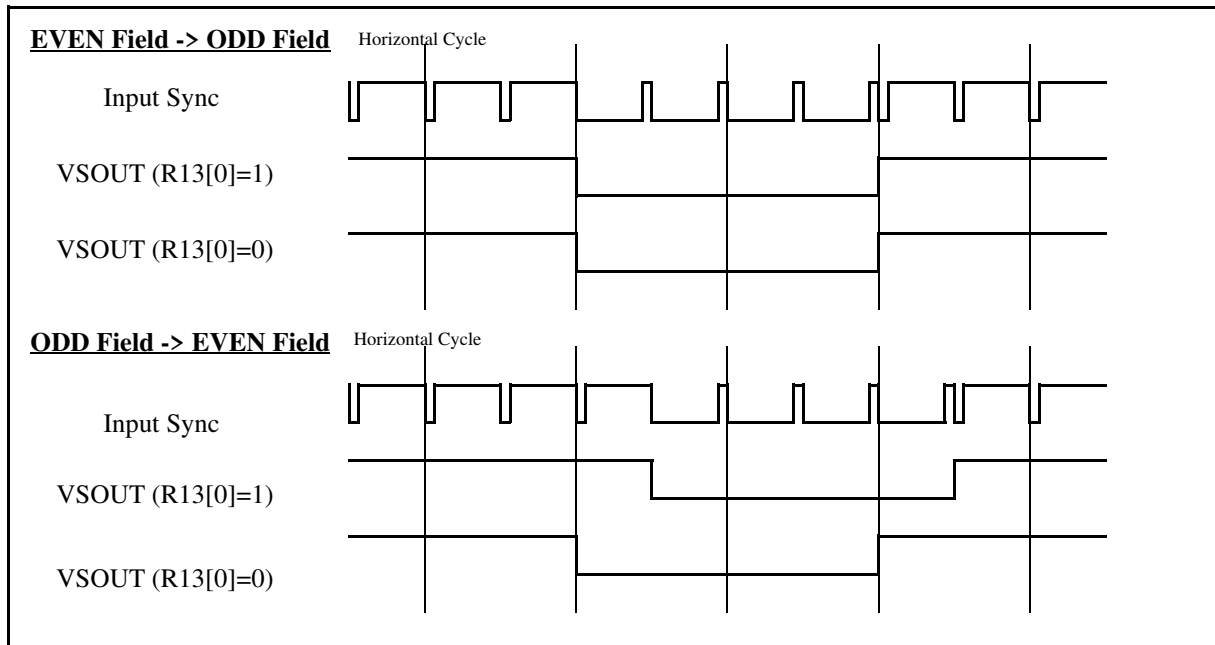
1: VSYNC Output (VO, Regenerated VSYNC) is produced at the center of horizontal period when video field of interlaced video changes from ODD field to EVEN field.

0: VSYNC Output is produced only at the start position of horizontal period. Consequently, the vertical total line number of interlaced video changes by 1 depending on video field.

* The output mode of VSYNC available from VSOUT-pin (VO, Regenerated VSYNC) is selected. Raw VSYNC is not affected by this mode.

* The edge of VSYNC Output always occurs at the start position of horizontal period for non-interlaced video (Detection result: R2E[7]=0). Therefore, R13[0]=0 and R13[0]=1 produce the same result for non-interlaced video.

< VSOUT Interlace Mode >



R14[7:0] HSYNC Output (HO) Start Position

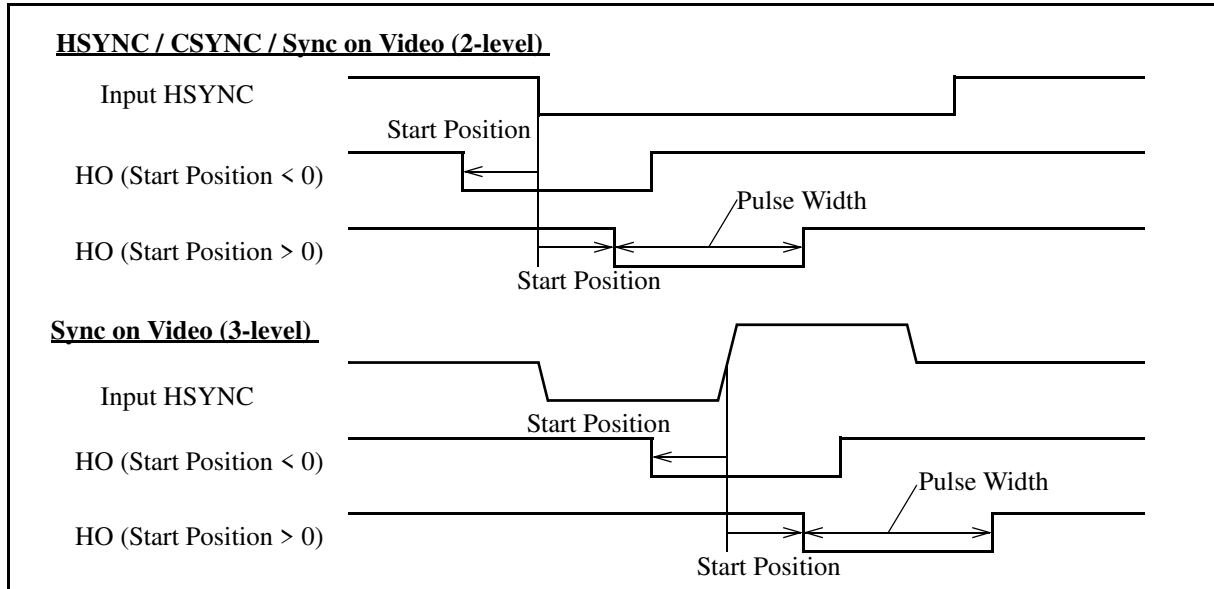
Set the start position of HO available from HSOUT-pin in steps of 1 pixel with reference to the leading edge of the HSYNC (It is the leading edge of the positive pulse when it is 3-level sync) . The register value is configured by two's complement from -128 to +127.

* When the external clock input is used (R04[1:0]=10b or 11b) , minus number is prohibited.

R15[7:0] HSYNC Output (HO) Pulse Width

Set the pulse width of HO available from HSOUT-pin in steps of 1 pixel.

< HO Start Position / Pulse Width >



R16[4] PLL COAST Source

PLL should stop synchronization with the HSYNC input during the vertical blank time including the pulses disturbing PLL lock and the sampling clock generation such as equalization pulses and copy protection signal. PLL COAST signal causes PLL to stop synchronization with the HSYNC input and free-run.

0: PLL COAST signal is internally generated in the device.

1: PLL COAST signal can be externally input from COAST-pin.

* When PLL COAST signal is internally generated, automatic setting mode (R22[7]) is available.

R16[3] PLL COAST Input Polarity

Select the input polarity of PLL COAST signal when externally input (R16[4]=1) .

Set to 0 when the input polarity is Active-Low (PLL free-runs at COAST-pin=Low) .

Set to 1 when the input polarity is Active-High (PLL free-runs at COAST-pin=High) .

R16[2] Clamp Pulse Source

Select the generation source of clamp pulse which is a timing signal of a clamp

0: The clamp pulse is generated internally.

1: Clamp pulse must be inputted through Clamp-pin.

R16[1] Clamp Pulse Input Polarity

Select input polarity when the external clamp pulse is used (R16[2]=1).

0: Input polarity becomes Active-Low.

1: Input polarity becomes Active-High.

R16[0] Clamp COAST Source

It's sometimes necessary to make the clamp suspend while the period which is including the signals that disturb the clamp such as a copy protection signal. The clamp COAST signal is the signal which makes the clamp stop.

0: Internal Clamp COAST

1: External Clamp COAST

R17[6] Clamp Pulse Start Reference Edge

The timing of Clamp pulse is set based on the edge of the HSYNC input. Selecting the edge of the HSYNC input

0: the leading edge of the HSYNC input is referred.

1: the trailing edge of the HSYNC input is referred.

* In case of 3-level sync, the leading edge or trailing edge of the positive pulse is referred.

R17[5:4] R-ch (Pr-ch) Clamp Mode

R17[3:2] G-ch (Y-ch) Clamp Mode

R17[1:0] B-ch (Pb-ch) Clamp Mode

As a clamp method, pedestal clamp, midscale clamp, and 256-level clamp can be selected.

00b: Pedestal clamp for RGB and Y (luminance) clamps black level to 0 with automatic offset cancel (if clamp level offset is set to 0) . The Automatic offset cancel circuitry eliminates any offset errors.

01b: Midscale clamp for PbPr clamps to 512 with automatic offset cancel (if clamp level offset is set to 0) . The Automatic offset cancel circuitry eliminates any offset errors.

10b: Reserved

11b: 256-level clamp clamps to 256 with automatic offset cancel (if clamp level offset is set to 0). The Automatic offset cancel circuitry eliminates any offset errors.

* It's possible to set a clamp pulse on sync part and realize sync tip clamp by a pedestal clamp (R17 [5:4], R17 [3:2] and R17 [1:0] =00b) .

R18[7:0] Clamp Pulse Start Position

Set the clamp pulse start position in steps of 1 pixel with reference to clamp pulse start reference edge (selected by R17[6]) .

R19[7:0] Clamp Pulse Width

Set the clamp pulse width in steps of 1 pixel.

* When the register is set to 0, clamp pulse is not generated.

* Set the end position of clamp pulse (R18[7:0] + R19[7:0]) more than 16 pixels front of active video period because Clamp Offset Cancel is completed after 16 pixels from the clamp pulse.