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THCV235-Q and THCV236-Q

SerDes transmitter and receiver with bi-directional transceiver

General Description

The THCV235-Q and THCV236-Q are designed to support video data transmission between the host and display.

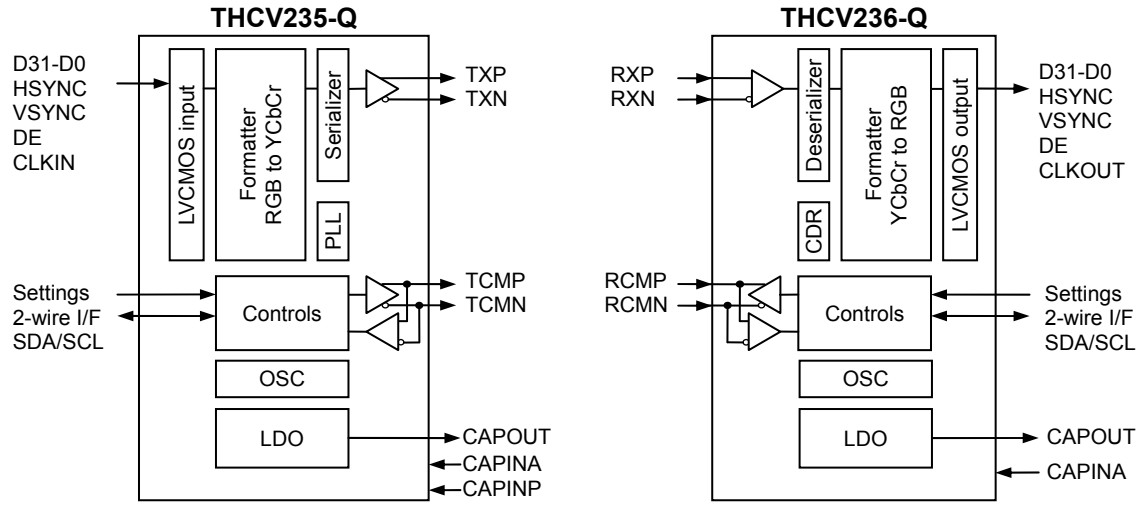
One high-speed lane can carry up to 32bit data and 3bits of synchronizing signals at a pixel clock frequency from 6MHz to 160MHz by converting RGB444 to YCbCr422.

The chipset, which has one high-speed data lane, can transmit video data up to 1080p/60Hz.
The maximum serial data rate is 4.00Gbps/lane.

Features

- Color depth selectable:24/32bit
- RGB ⇔ YCbCr422 color space conversion function
- Wide frequency range
- AC coupling for high-speed lanes
- CDR requires no external frequency reference
- Wide range supply voltage from 1.7V to 3.6V
- Additional spread spectrum on data stream
- 2-wire serial interface bridge function(400kbps)
- Remote side GPIO control and monitoring
- Low speed data bridge function
- QFN64(9mm x 9mm) with exposed pad ground
- Automotive grade product : AEC-Q100 Grade 2 compliant
- ISO/TS16949 compliant
- V-by-One® HS standard version1.4 compliant
- EU RoHS compliant

Block Diagram



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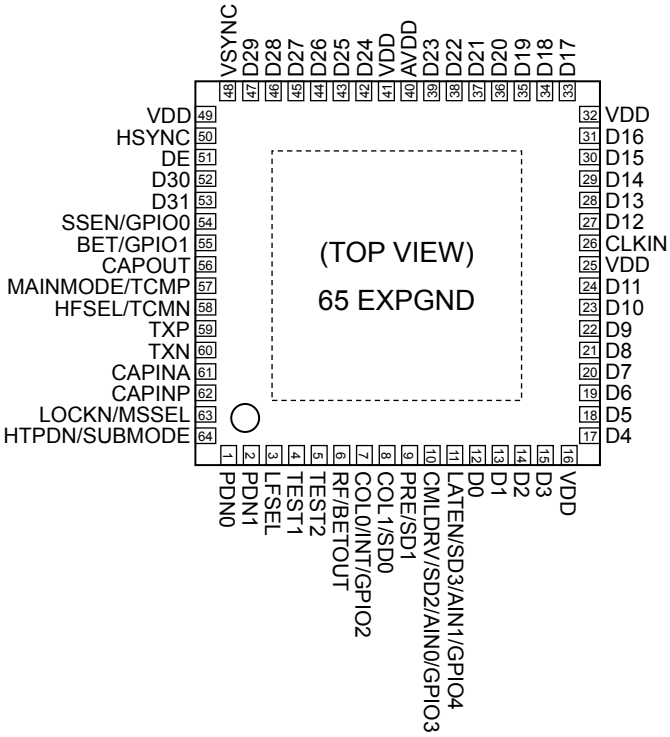
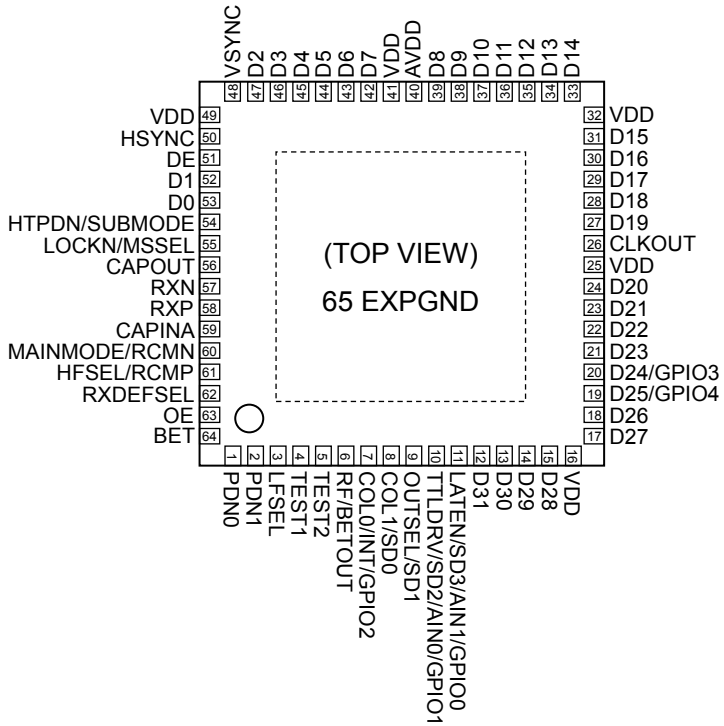
Pin Configuration

THCV235-Q (QFN 64pin)



THCV236-Q (QFN 64pin)



Pin Description

Pin Description for THCV235-Q

Pin Name	Pin No.	Type	Description
TXP	59	CO	High-Speed CML Signal Output(Main-Link)
TXN	60	CO	High-Speed CML Signal Output(Main-Link)
MAINMODE/ TCMP	57	I/CB	MAINMODE : Setting V-by-One® HS Mode or Sync Free Mode when PDN1=0. See page12. 0 : V-by-One® HS Mode 1 : Sync Free Mode TCMP : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HFSEL/TCMN	58	I/CB	HFSEL : High Frequency mode select when PDN1=0. 0 : High Frequency mode Disable 1 : High Frequency mode Enable TCMN : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HTPDN/ SUBMODE	64	IL	HTPDN : Hot Plug Detect Input when PDN1=0. SUBMODE : Sub-Link Mode Select when PDN1=1. 0: 2-wire serial interface(I/F) Mode(default No Clock Stretching mode) 1: Low Speed Data Bridge Mode Forbid the different setting between THCV235-Q and THCV236-Q.
LOCKN/MSSEL	63	IL	LOCKN : Lock Detect Input when PDN1=0. MSSEL : Sub-Link Master/Slave Select when PDN1=1. 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MPU. Forbid the same setting between THCV235-Q and THCV236-Q.
LATEN/SD3/AIN1/ GPIO4	11	B	LATEN : Latch select input under Field BET(Main-Link or Sub-Link). 0 : NOT Latched result 1 : Latched result SD3 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD3 is output. When Sub-Link is Slave (MSSEL=1), SD3 is input. AIN1 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO4 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output or input, no external component is required.

CMLDRV/SD2/ AIN0/GPIO3	10	B	CMLDRV : High-Speed CML Output Drive Strength Select when PDN1=0. 0 : Weak Drive Strength (600mV diff p-p) 1 : Normal Drive Strength (800mV diff p-p) SD2 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD2 is input. When Sub-Link is Slave (MSSEL=1), SD2 is output. AIN0 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO3 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output or input, no external component is required.
PRE/SD1	9	B	PRE : Pre-Emphasis Level Select Input when PDN1=0. 0 : Pre-Emphasis Disable 1 : Pre-Emphasis Enable (when CMLDRV=1. See Table 4) SD1 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD1 is used as SCL input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD1 is input. When SUBMODE=1 and MSSEL=1, SD1 is output.
COL1/SD0	8	B	COL1 : Color Space Converter Enable when PDN1=0 and MAINMODE=0. 0 : Color Space Converter Disable 1 : Color Space Converter Enable Data Width Setting when PDN1=0 and MAINMODE=1. See Table 20. SD0 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD0 is used as SDA input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD0 is input. When SUBMODE=1 and MSSEL=1, SD0 is output.
COL0/INT/GPIO2	7	B	COL0 : Data Width Setting when PDN1=0. See Table 20. INT : Interrupt signal output for Sub-Link when SUBMODE=0 and MSSEL=0. It must be connected with a pull-up resistor to VDD. L : Interrupt occurred H : Steady state GPIO2 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO2 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO2 is used as push pull output or input, no external component is required.

BET/GPIO1	55	BO	BET : Field BET entry when PDN1=0 or Sub-Link is active and Low Speed Data Bridge Mode(PDN1=1, SUBMODE=1). 0 : Normal Operation 1 : Field BET Operation GPIO1 : General Purpose Input/Output when SUBMODE=0. GPIO1 has Open-Drain Output buffer, it must be connected with a pull-up resistor to VDD.
SSEN/GPIO0	54	BO	SSEN : Spread Spectrum Clock Generator(SSCG) Enable when PDN1=0 or Sub-Link is active and Low Speed Data Bridge Mode(PDN1=1, SUBMODE=1). 0 : SSCG Disable 1 : SSCG Enable GPIO0 : General Purpose Input/Output when SUBMODE=0. GPIO0 has Open-Drain Output buffer, it must be connected with a pull-up resistor to VDD.
CLKIN	26	I	Clock Input
D31-D0	53,52,47-42, 39-33,31-27, 24-17,15-12	I	Pixel Data Input
DE	51	I	DE Input
HSYNC	50	I	HSYNC Input
VSYNC	48	I	VSYNC Input
RF/BETOUT	6	B	RF : Input Clock Triggering edge select. See Figure 19. 0 : Falling Edge 1 : Rising Edge BETOUT : Field BET Result Output when Field BET mode
LFSEL	3	I	Low Frequency mode select 0 : Low Frequency mode Disable 1 : Low Frequency mode Enable
PDN1	2	IL	Sub-Link Power Down 0 : Power Down. Main-Link setting by external pin 1 : Normal Operation. Main-Link Setting by 2-wire serial I/F
PDN0	1	IL	Main-Link Power Down 0 : Power Down 1 : Normal Operation
TEST2	5	I	Test pin. Must be tied to Ground for normal operation.
TEST1	4	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	56	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	61	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
CAPINP	62	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	49,41,32,25,16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	40	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	65	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CO : CML Output buffer , CB : CML Bi-directional buffer
I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer
B : LVCMOS Bi-directional buffer , BO : Open-Drain LVCMOS Bi-directional buffer
PWR : Power supply , GND : Ground

Table 1. Pin Sharing Description (THCV235-Q)

Sub-Link State →	Sub-Link Power Down	Low Speed Data Bridge Mode		2-wire serial I/F Mode	
Sub-Link Master/Slave →	-	Master	Slave	Master	Slave
PDN1	**0**	**1**	**1**	**1**	**1**
HTPDN/SUBMODE	*	**1**	**1**	**0**	**0**
LOCKN/MSSEL	*	**0**	**1**	**0**	**1**
BET/GPIO1	**0**	**0**	**0**	*	*
RF/BETOUT	RF				
	BETOUT(*2)				
COL0/INT/GPIO2	COL0	COL0	COL0	INT	GPIO2(*4)
COL1/SD0	COL1	SD0(input)	SD0(output)(*6)	SD0(SDA)	SD0(SDA)
PRE/SD1	PRE	SD1(input)	SD1(output)(*6)	SD1(SCL)	SD1(SCL)
CMLDRV/SD2/AIN0/GPIO3	CMLDRV	SD2(input)	SD2(output)(*6)	AIN0	GPIO3(*5)
LATEN/SD3/AIN1/GPIO4	-(*1)	SD3(output)(*6)	SD3(input)	AIN1	GPIO4(*5)
	LATEN(*3)				
SSEN/GPIO0	SSEN	SSEN	SSEN	GPIO0(*4)	GPIO0(*4)
BET/GPIO1	BET	BET	BET	GPIO1(*4)	GPIO1(*4)
MAINMODE/TCMP	MAINMODE	TCMP			
HFSEL/TCMN	HFSEL	TCMN			
LOCKN/MSSEL	LOCKN	MSSEL			
HTPDN/SUBMODE	HTPDN	SUBMODE			

*1 There is no function. LVCMOS IO has input state. Must be fixed at 0 or 1 input.
*2 When Field BET mode (Main-Link or Sub-Link), it functions as BETOUT output.
*3 When Field BET mode (Main-Link or Sub-Link), it functions as LATEN input.
*4 Programmable GPIO input is default on register setting.
*5 Through GPIO open-drain output is default on register setting.
*6 Low Speed Data Bridge Mode output is LVCMOS push pull buffer.

Pin Description for THCV236-Q

Pin Name	Pin No.	Type	Description
RXP	58	CI	High-Speed CML Signal Input(Main-Link)
RXN	57	CI	High-Speed CML Signal Input(Main-Link)
HFSEL/RCMP	61	CB/I	HFSEL : High Frequency Mode select when PDN1=0. 0 : High Frequency Mode Disable 1 : High Frequency Mode Enable RCMP : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
MAINMODE/ RCMN	60	CB/I	MAINMODE : Setting V-by-One® HS Mode or Sync Free Mode when PDN1=0 0 : V-by-One® HS Mode 1 : Sync Free Mode RCMN : CML Signal Bi-directional Input/Output(Sub-Link) when PDN1=1.
HTPDN/ SUBMODE	54	BO	HTPDN : Hot Plug Detect Output when PDN1=0. Must be connected to Tx HTPDN with 10kΩ pull-up resistor. SUBMODE : Sub-Link Mode Select when PDN1=1. 0 : 2-wire serial I/F Mode (default No Clock Stretching mode) 1 : Low Speed Data Bridge Mode Forbid the different setting between THCV235-Q and THCV236-Q.
LOCKN/ MSSEL	55	BO	LOCKN : Lock Detect Output when PDN1=0. Must be connected to Tx LOCKN with 10kΩ pull-up resistor. MSSEL : Sub-Link Master/Slave Select when PDN1=1. 0 : Sub-Link Master side(inside 2-wire serial I/F is slave) 1 : Sub-Link Slave side(inside 2-wire serial I/F is master) Sub-Link Master is connected to HOST MPU. Forbid the same setting between THCV235-Q and THCV236-Q.
LATEN/SD3/ AIN1/GPIO0	11	B	LATEN : Latch select input under Field BET(Main-Link or Sub-Link). 0 : NOT Latched result 1 : Latched result SD3 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD3 is output. When Sub-Link is Slave (MSSEL=1), SD3 is input. AIN1 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO0 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO0 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO0 is used as push pull output or input, no external component is required.

TTLDRV/SD2/ AIN0/GPIO1	10	B	TTLDRV : TTL Output Drive Strength Select when PDN1=0. 0 : Weak Drive Strength 1 : Normal Drive Strength SD2 : Sub-Link Data Input/Output when PDN1=1 and SUBMODE=1. When Sub-Link is Master (MSSEL=0), SD2 is input. When Sub-Link is Slave (MSSEL=1), SD2 is output. AIN0 : Device ID setting for 2-wire serial I/F when SUBMODE=0 and MSSEL=0. See Table 26. GPIO1 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO1 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO1 is used as push pull output or input, no external component is required.
OUTSEL/SD1	9	B	OUTSEL : Permanent Clock Output Enable when PDN1=0. 0 : Permanent Clock Output Disable 1 : Permanent Clock Output Enable SD1 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD1 is used as SCL input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD1 is input. When SUBMODE=1 and MSSEL=1, SD1 is output.
COL1/SD0	8	B	COL1 : Color Space Converter Enable when PDN1=0 and MAINMODE=0. 0 : Color Space Converter Disable 1 : Color Space Converter Enable Data Width Setting when PDN1=0 and MAINMODE=1. See Table 20. SD0 : Sub-Link Data Input/Output when PDN1=1. When SUBMODE=0, SD0 is used as SDA input/output for 2-wire serial I/F, requires pull-up resistor to VDD. When SUBMODE=1 and MSSEL=0, SD0 is input. When SUBMODE=1 and MSSEL=1, SD0 is output.
COL0/INT/ GPIO2	7	B	COL0 : Data Width Setting when PDN1=0. See Table 20. INT : Interrupt signal output for Sub-Link when SUBMODE=0 and Sub-Link Master. It must be connected with a pull-up resistor to VDD. L : Interrupt occurred H : Steady state GPIO2 : General Purpose Input/Output when SUBMODE=0 and MSSEL=1. When GPIO2 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO2 is used as push pull output or input, no external component is required.
CLKOUT	26	O	Clock Output
D31-D26	12-15,17,18	O	Pixel Data Output

D25/GPIO4	19	B	D25 : Pixel Data Output GPIO4 : General Purpose Input/Output when SUBMODE=0, MSSEL=0 and RXDEFSEL=0. When GPIO4 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO4 is used as push pull output or input, no external component is required.
D24/GPIO3	20	B	D24 : Pixel Data Output GPIO3 : General Purpose Input/Output when SUBMODE=0, MSSEL=0 and RXDEFSEL=0. When GPIO3 is used as Open-Drain Output, it must be connected with a pull-up resistor to VDD. When GPIO3 is used as push pull output or input, no external component is required.
D23-D0	21-24,27-31,33-39, 42-47,52,53	O	Pixel Data Output
DE	51	O	DE Output
HSYNC	50	O	HSYNC Output
VSYNC	48	O	VSYNC Output
OE	63	IL	Output Enable 0 : LVCMOS Output Disable (Hi-Z) except for HTPDN, LOCKN when PDN1=0 and except for BETOUT when BET=1. 1 : LVCMOS Output Enable
BET	64	IL	Field BET entry 0 : Normal Operation 1 : Field BET Operation
RF/BETOUT	6	B	RF : Output Clock Triggering edge select. See Figure 20. 0 : Falling Edge 1 : Rising Edge BETOUT : Field BET Result Output
RXDEFSEL	62	I	Internal Register Default Setting Select. See Table 44, Table 45 0 : for THCV231-Q 1 : for THCV235-Q
LFSEL	3	I	Low Frequency mode select 0 : Low Frequency mode Disable 1 : Low Frequency mode Enable
PDN1	2	IL	Sub-Link Power Down 0 : Power Down. Main-Link setting by external pin 1 : Normal Operation. Main-Link Setting by 2-wire serial I/F
PDN0	1	IL	Main-Link Power Down 0 : Power Down 1 : Normal Operation
TEST2	5	I	Test pin. Must be tied to Ground for normal operation.
TEST1	4	IL	Test pin. Must be tied to Ground for normal operation.
CAPOUT	56	PWR	Decoupling Capacitor Pin, 1.2V output.
CAPINA	59	PWR	Reference Input for Analog Circuit. Must be tied to CAPOUT.
VDD	49,41,32,25,16	PWR	1.7-3.6V Digital Power Supply Pin for LVCMOS I/O
AVDD	40	PWR	1.7-3.6V Analog Power Supply Pin for LDO
EXPGND	65	GND	Exposed Pad Ground. Must be tied to the PCB ground plane through an array of vias.

CI : CML Input buffer , CB : CML Bi-directional buffer
I : LVCMOS Input buffer , IL : Low Speed LVCMOS Input buffer , O: LVCMOS Output buffer
B : LVCMOS Bi-directional buffer , BO : Open-Drain LVCMOS Bi-directional buffer
PWR : Power supply , GND : Ground

Table 2. Pin Sharing Description (THCV236-Q)

Sub-Link State →	Sub-Link Power Down	Low Speed Data Bridge Mode		2-wire serial I/F Mode		
Sub-Link Master/Slave →	-	Master	Slave	Master 1	Master 2	Slave
PDN1	**0**	**1**	**1**	**1**	**1**	**1**
HTPDN/SUBMODE	*	**1**	**1**	**0**	**0**	**0**
LOCKN/MSSEL	*	**0**	**1**	**0**	**0**	**1**
BET	**0**	**0**	**0**	**0**	**0**	**0**
RXDEFSEL	*	*	*	**1**	**0**	*
RF/BETOUT	RF					
	BETOUT(*2)					
COL0/INT/GPIO2	COL0	COL0	COL0	INT	INT	GPIO2(*4)
COL1/SD0	COL1	SD0(input)	SD0(output)(*6)	SD0(SDA)	SD0(SDA)	SD0(SDA)
OUTSEL/SD1	OUTSEL	SD1(input)	SD1(output)(*6)	SD1(SCL)	SD1(SCL)	SD1(SCL)
TTLDRV/SD2/AIN0/GPIO1	TTLDRV	SD2(input)	SD2(output)(*6)	AIN0	AIN0	GPIO1(*4)
LATEN/SD3/AIN1/GPIO0	-(*1)	SD3(output)(*6)	SD3(input)	AIN1	AIN1	GPIO0(*4)
	LATEN(*3)					
D24/GPIO3	D24	D24	D24	D24	GPIO3(*5)	D24
D25/GPIO4	D25	D25	D25	D25	GPIO4(*5)	D25
HTPDN/SUBMODE	HTPDN	SUBMODE				
LOCKN/MSSEL	LOCKN	MSSEL				
MAINMODE/RCMN	MAINMODE	RCMN				
HFSEL/RCMP	HFSEL	RCMP				

*1 There is no function. LVCMOS IO has input state. Must be fixed at 0 or 1 input.
*2 When Field BET mode (Main-Link or Sub-Link), it functions as BETOUT output.
*3 When Field BET mode (Main-Link or Sub-Link), it functions as LATEN input.
*4 Programmable GPIO input is default on register setting.
*5 Through GPIO input is default on register setting.
*6 Low Speed Data Bridge Mode output is LVCMOS push pull buffer.

Functional Overview

With High Speed CML SerDes, proprietary encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV235-Q and THCV236-Q enable transmission of 24/30bit video data, 2bits of user defined data, synchronizing signals HSYNC,VSYNC and DE(Data Enable) as well as any data (up to 35 bit) through Main-Link by single differential pair cable with minimal external components. In addition, the THCV235-Q and THCV236-Q have Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. It does not need any external frequency reference, such as a crystal oscillator. The THCV235-Q - THCV236-Q system is able to watch and control peripheral devices via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of GPIO inputs and internal statuses.

Functional Description

Internal Reference Output/Input Function (CAPOUT, CAPINA, CAPINP)

An internal regulator produces the 1.2V (CAPOUT). This 1.2V linear regulator can't supply any other external loads. Bypass CAPOUT to GND with 10uF.

CAPINP (THCV235-Q only) supplies reference voltage for internal PLL, and CAPINA supplies reference voltage for any internal analog circuit. Bypass CAPINP/CAPINA to GND with 0.1uF to remove high frequency noise. CAPOUT, CAPINA and CAPINP must be tied together.

Power supply AVDD is supposed to be stabilized with de-coupling capacitor and series noise filter (for example, ferrite bead).

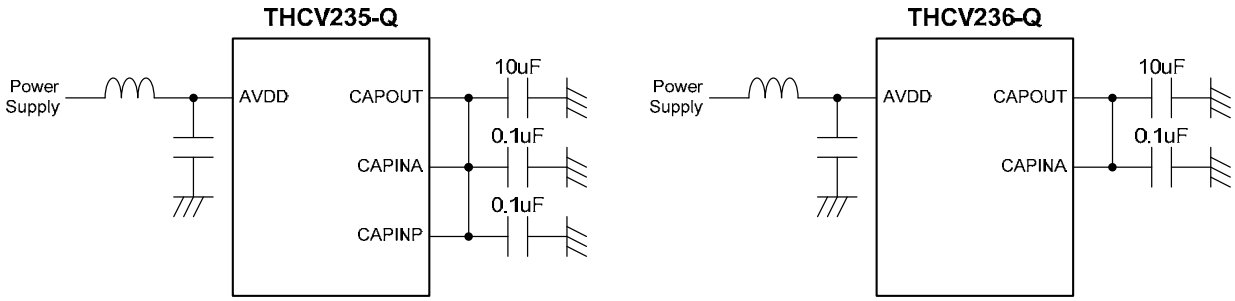


Figure 1. Connection of CAPOUT, CAPINA, CAPINP and Decoupling Capacitor

Power Down (PDN1, PDN0)

PDN1 and PDN0 turn off internal circuitry of Main-Link and Sub-Link separately.

Table 3. Power Down Setting

PDN1	PDN0	Operation
0	0	Both Main-Link and Sub-Link power down
0	1	Only Main-Link is active
1	0	Only Sub-Link is active
1	1	Both Main-Link and Sub-Link active

Main-Link Mode Setting

Two modes of Main-Link operation are available. Mode select is done by MAINMODE pin (when PDN1=0) or MAINMODE register (when PDN1=1).

V-by-One® HS Mode (MAINMODE=0)

V-by-One® HS Mode is compliant with V-by-One® HS standard Version1.4. (See Figure 3 and Table 14)

Sync Free Mode (MAINMODE=1)

Incoming data can be transmitted by Sync Free Mode without DE requirement. (See Table 14)

Color Space Conversion

The THCV235-Q converts RGB444 to YCbCr422 and the THCV236-Q converts back to RGB. This function can only be used in V-by-One® HS mode and enabled by COL1=1 setting. COL1 is external pin (when PDN1=0) or internal register (when PDN1=1). Color space conversion coefficients are compliant with ITU-R BT.709-5.

Pre-emphasis and Drive Select Function (THCV235-Q only)

Pre-emphasis can equalize severe signal degradation caused by long-distance or high-speed transmission. PRE pin or PRE register selects the strength of pre-emphasis. CMLDRV pin or CMLDRV register controls CML Main-Link output swing level. See Table 4 and Table 5.

Table 4. Pre-emphasis and Drive Select function table (PDN1=0)

CMLDRV (pin)	PRE (pin)	Condition	
		Swing Level	Pre-emphasis Level
0	0	600mV diff p-p	0dB
	1		3.5dB
1	*	800mV diff p-p	0dB

Table 5. Pre-emphasis and Drive Select function table (PDN1=1)

CMLDRV[1:0] (register)	PRE (register)	Condition	
		Swing Level	Pre-emphasis Level
00	0	400mV diff p-p	0dB
	1		6dB
01	0	600mV diff p-p	0dB
	1		3.5dB
10	*	800mV diff p-p	0dB
11	*	Forbidden	

Permanent Clock Output (THCV236-Q only)

When there is no input from Main-Link, the THCV236-Q will output internal oscillator clock from CLKOUT pin. This function is controlled by OUTSEL pin or OUTSEL_ENABLE register and OUTSEL_SETTING register. See Table 6 and Table 7.

Table 6. Permanent Clock Output function table (PDN1=0)

OUTSEL (pin)	Output Clock Frequency(*1)
0	-
1	40MHz

*1 typical value

Table 7. Permanent Clock Output function table (PDN1=1)

OUTSEL_ ENABLE (register)	OUTSEL_ SETTING (register)	Output Clock Frequency(*1)
0	*	-
1	00	80MHz
	01	40MHz(default)
	10	20MHz
	11	10MHz

*1 typical value

Spread Spectrum Clock Generator (SSCG)

The THCV235-Q serial data output and the THCV236-Q parallel data and clock outputs are modulated by programmable SSCG. The THCV235-Q SSCG is enabled by SSEN pin or SSEN register. The THCV236-Q SSCG is enabled by only SSEN register. The modulation rate and modulation frequency variation of output spread is controlled through the SSCG control registers on each device. Do not enable spread spectrum for both the THCV235-Q and THCV236-Q at the same time.

Table 8. SSCG enable signal (THCV235-Q)

PDN1	SUBMODE	Mode Entry Signal	Description
0	* (Function as HTPDN)	SSEN (pin)	0:SSCG Disable 1:SSCG Enable
1	0	SSEN (register)	
	1	SSEN (pin)	

Table 9. SSCG enable signal (THCV236-Q)

PDN1	SUBMODE	Mode Entry Signal	Description
*	*	SSEN(register)	0:SSCG Disable 1:SSCG Enable

When customer use the mode and frequency range shown in Table 10, register setting is required according to Table 11.

Table 10. Main-Link mode and frequency range requiring register setting

Mode Setting					Freq.Range[MHz] (SSCG Enable)		Register Setting (*2)
MAINMODE	HFSEL	LFSEL	COL1	COL0	min	max	
0	0	0	(*1)	0	26.6	50	Case1
0	0	0	(*1)	1	33.3	66.6	Case2
0	1	0	(*1)	(*1)	50	100	Case3
1	0	0	0	0	26.6	40	Case1
1	0	0	0	1	26.6	50	Case1
1	0	0	1	0	33.3	66.6	Case2
1	1	0	(*1)	(*1)	50	100	Case3

*1 Don't care
*2 See Table 11

Table 11. SSCG register setting

Step	Register Address(HEX)		Register Value(HEX)				Description
	Sub-Link Master side	Sub-Link Slave side	Case1	Case2	Case3		
					THCV235-Q	THCV236-Q	
1	0x70	0xF0	0x01				Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02		0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x3C	0x30	0x20		Set PLL_SET1
4	0x7C	0xFC	0x35	0x34	0x24		Set PLL_SET2

Modulation frequency f_{mod} can be determined by HFSEL and LFSEL settings, input clock frequency and FMOD register setting (default value 0xD). Refer to following formula.

$$f_{\mathrm{mod}} = \frac{f_{CLKSSCG}}{128 \times FMOD}$$

$f_{CLKSSCG}$ is the frequency listed in Table 12 and Table 13.

Table 12. $f_{CLKSSCG}$ (THCV235-Q)

HFSEL	LFSEL	$f_{CLKSSCG}$
0	0	(1/tTCIP)/2
0	1	1/tTCIP
1	0	(1/tTCIP)/4
1	1	Forbidden Setting

Table 13. $f_{CLKSSCG}$ (THCV236-Q)

HFSEL	LFSEL	$f_{CLKSSCG}$
0	0	(1/tRCP)/2
0	1	1/tRCP
1	0	(1/tRCP)/4
1	1	Forbidden Setting

Up to 0.5 % spread at the 30kHz modulation frequency is stable for most cases. In case of using out of this range, please verify at the actual system.

Data Enable

Figure 2 is the conceptual diagram of the V-by-One® HS mode operation (MAINMODE=0) of the chipset.

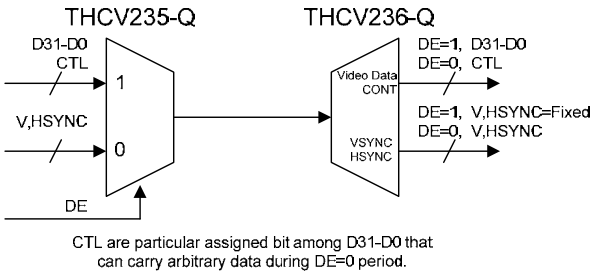
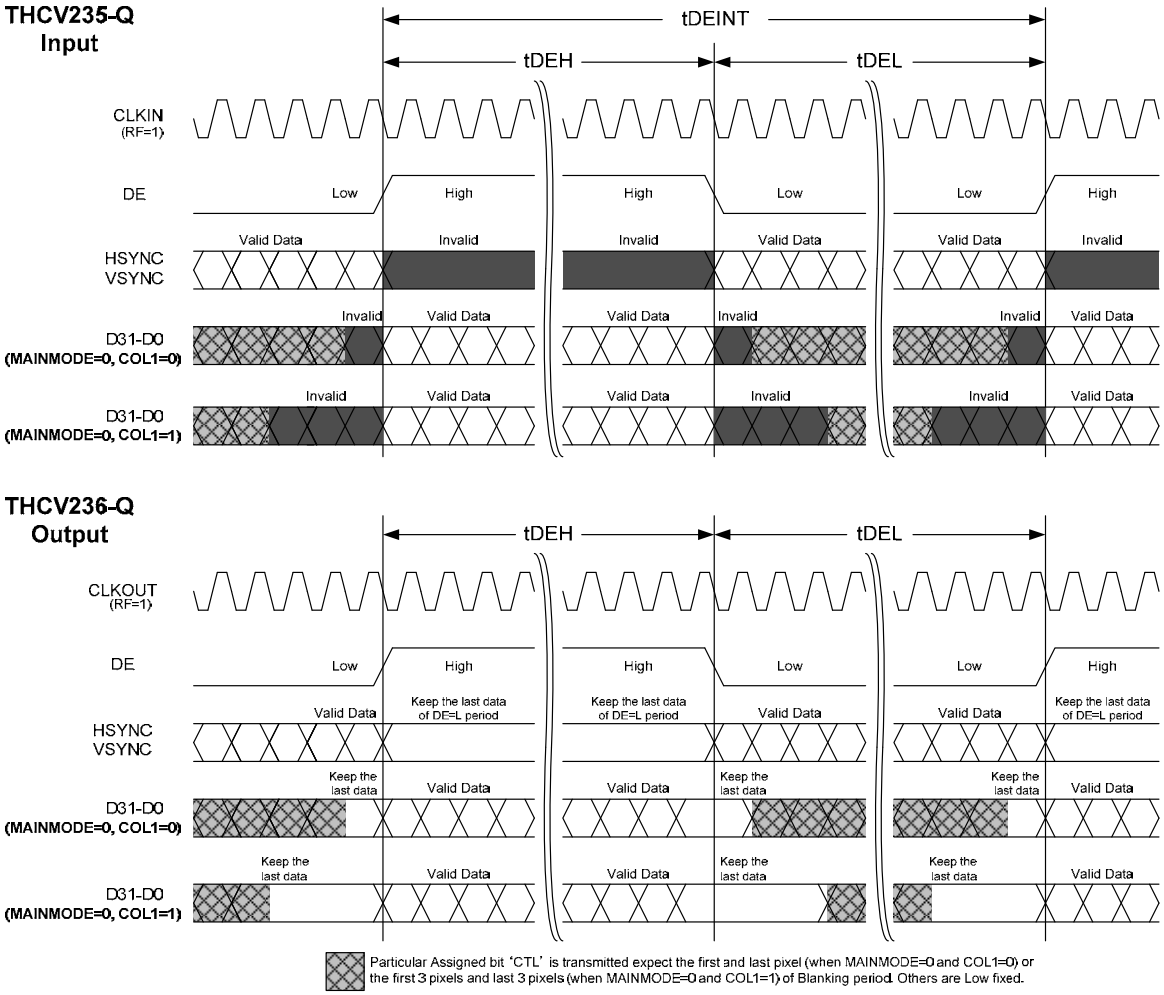


Figure 2. Conceptual Diagram of the Basic Operation of the Chipset in V-by-One® HS mode

There are some requirements for DE. Figure 3 shows the timing diagram of it.



Note: In V-by-One® HS Mode (MAINMODE=0) and High Frequency Mode (HFSEL=1), the period between rising edges of DE (tDEINT), high time of DE (tDEH) should always satisfy following equations.

$$tDEH = tTCIP*(2m)$$
$$tDEINT = tTCIP*(2n)$$
$$m,n=2,3,4,5,6\ldots\ldots$$

Figure 3. Data and Synchronizing Signals Transmission Timing Diagram in V-by-One® HS mode

Table 14. DE Requirement

Symbol	Parameter	Condition	Min	Typ	Max	Unit
tDEH	DE=1 Duration	MAINMODE=0 HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 HFSEL=1	4×tTCIP	-	-	ns
		MAINMODE=1	Don't care			
tDEL	DE=0 Duration	MAINMODE=0 HFSEL=0	2×tTCIP	-	-	ns
		MAINMODE=0 HFSEL=1	4×tTCIP	-	-	ns
		MAINMODE=1	Don't care			

Hot-Plug Function

HTPDN signal indicates connecting condition between the Transmitter and the Receiver. HTPDN of the transmitter side is high when the Receiver is not active or not connected. Then Transmitter can enter into the power down mode. HTPDN is set to low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training.

When PDN1 = 0 (Sub-Link Power Down), HTPDN is transferred to Transmitter by HTPDN pin.
HTPDN is open-drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

HTPDN connection between the Transmitter and the Receiver can be omitted as an application option. In this case, HTPDN at the Transmitter side should always be taken as low.

When PDN1 = 1 (Sub-Link Active), HTPDN is transferred to Transmitter via Sub-Link line.
HTPDN/SUBMODE pin functions as Sub-Link mode select (SUBMODE). HOST MPU can confirm HTPDN state by reading Sub-Link Master register (0x00 bit0 HTPDN).

Lock Detect Function

LOCKN indicates whether the receiver CDR PLL is in the lock state or not. LOCKN at the Transmitter input is set to High by pull-up resistor when Receiver is not active or at the CDR PLL training state. LOCKN is set to low by the Receiver when CDR lock is done. Then the CDR training mode finishes and Transmitter shifts to the normal operation.

When PDN1 = 0 (Sub-Link Power Down), LOCKN is transferred to Transmitter by LOCKN pin. LOCKN is open-drain output at the receiver side. Pull-up resistor is needed at the transmitter side.

When HTPDN is included in an application, the LOCKN signal should only be considered when the HTPDN is pulled low by the Receiver.

When PDN1 = 1 (Sub-Link Active), LOCKN is transferred via Sub-Link line. LOCKN/MSSEL pin functions as Sub-Link Master/Slave select (MSSEL). HOST MPU can confirm LOCKN state by reading Sub-Link Master register (0x00 bit1 LOCKN).

Table 15. HTPDN,LOCKN transmission route setting

PDN1	HTPDN,LOCKN
0	HTPDN, LOCKN are transmitted via external DC signal.
1	HTPDN, LOCKN are transmitted via Sub-Link.

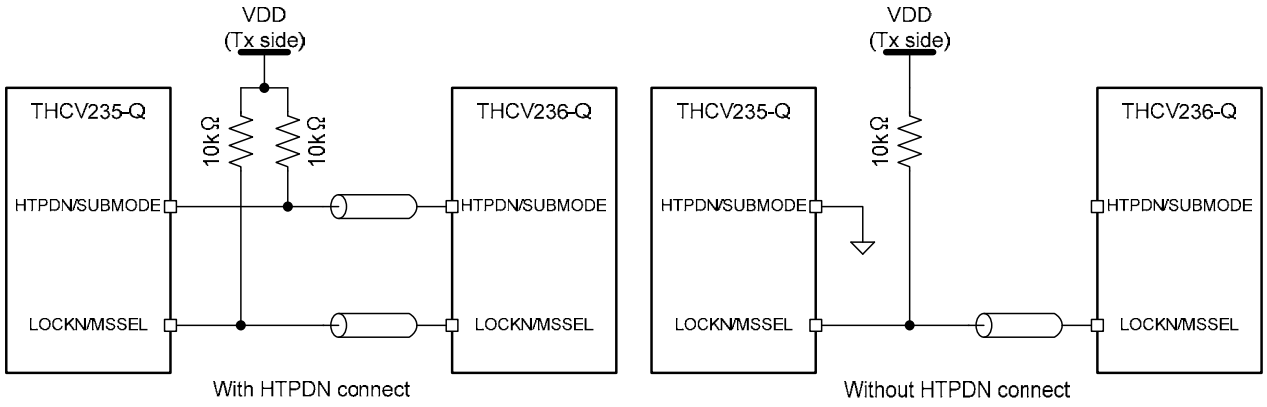


Figure 4. Hot-plug and Lock Detect Scheme when PDN1=0

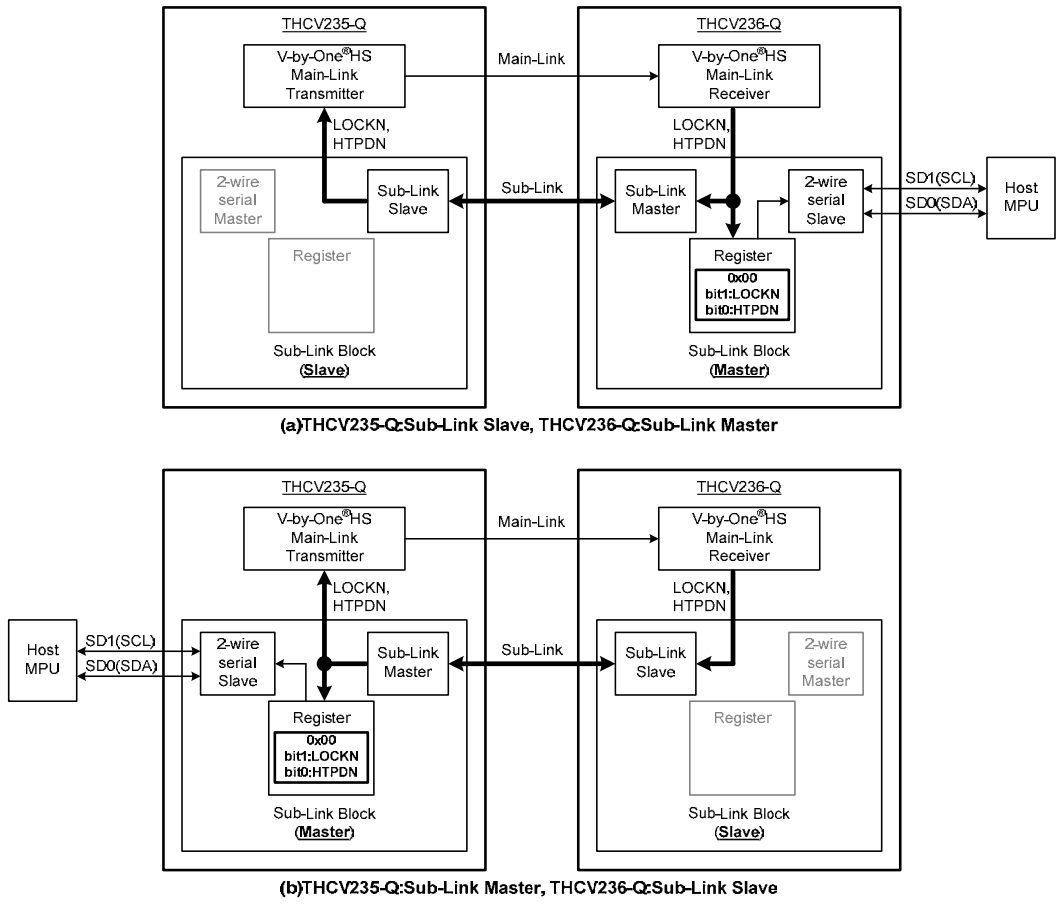


Figure 5. HTPDN,LOCKN transmission route when PDN1=1

Field BET Operation

In order to help users to check validity of CML serial line (Main-Link and Sub-Link), the THCV235-Q and THCV236-Q have an operation mode in which they act as a bit error tester (BET). In Main-Link Field BET mode, the THCV235-Q internally generates test pattern which is then serialized onto the Main-Link CML line. The THCV236-Q also has BET function mode. The THCV236-Q receives the data stream and checks bit errors. The generated data pattern is then 8b/10b encoded, scrambled, and serialized onto the CML channel. As for the THCV236-Q, the internal test pattern check circuit gets enabled and reports result on a certain pin named BETOUT. In Sub-Link Field BET mode, Sub-Link Master device internally generates test pattern which is then serialized onto the Sub-Link CML line. Sub-Link Slave device also has BET function mode. Sub-Link Slave device receives the data stream and checks bit errors. Note that Sub-Link Slave device must be set this mode prior to Sub-Link Master device. Pattern check result is output from BETOUT pin of the Sub-Link Slave device. The BETOUT pin goes LOW whenever bit errors occur, or it stays HIGH when there is no bit error.

In Main-Link Field BET mode, user can select two kinds of check result, latched result or NOT latched result by setting LATEN pin input. The latched result is reset by setting LATEN=0. In Sub-Link Field BET mode, only latched result is available. In order to reset the latched result, please once turn off the power and entry Sub-Link Field BET from power on sequence.

LATEN/SD3/AIN1/GPIO4 pin (THCV235-Q) and LATEN/SD3/AIN1/GPIO0 pin (THCV236-Q) function as LATEN in Field BET mode (Main-Link or Sub-Link).

It is not possible to realize Main-Link Field BET and Sub-Link Field BET at the same time.

Table 16. Main-Link Field BET Operation Settings

THCV235-Q/236-Q Common Setting					THCV236-Q Setting	Condition		
PDN0	PDN1	SUBMODE	BET	BET_SEL	LATEN	Main-Link	Sub-Link	Output Latch Select
1	0	-	1 (*1)	0 (*3)	0	Field BET Operation	Power Down	NOT Latched Result
					1			Latched Result
	1	1	1 (*1)	0 (*3)	0		Normal Operation	NOT Latched Result
					1			Latched Result
		0	1 (*2)	0 (*4)	0			NOT Latched Result
					1			Latched Result

*1 Pin setting
*2 THCV235-Q: Register setting (0x53 bit1), THCV236-Q: Pin setting
*3 When PDN0=1, PDN1=0 and BET=1 or PDN0=1, PDN1=1, SUBMODE=1 and BET=1, BET_SEL is set to 0 automatically.
*4 Register setting (0x53 bit0, Default 0)

Table 17. THCV236-Q Main-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

Table 18. Sub-Link Field BET Operation Setting

THCV235-Q/THCV236-Q Common Setting					THCV235-Q Setting		THCV236-Q Setting		Condition		
PDN0	PDN1	SUBMODE	BET	BET_SEL	MSSEL	LATEN	MSSEL	LATEN	Main-Link	Sub-Link	Output Latch Select
0	1	1	1 (*1)	1 (*3)	0	-	1	1 (*5)	Power Down	Field BET Operation	Latched Result
					1	1 (*5)	0	-			
		0	1 (*2)	1 (*4)	0	-	1	1 (*5)			
					1	1 (*5)	0	-			

*1 Pin setting. Note that BET pin should be 0 at power on sequence.
*2 THCV235-Q: Register setting (0x53 bit1), THCV236-Q: Pin setting. Note that BET pin should be 0 at power on sequence.
*3 When PDN0=0, PDN1=1, SUBMODE=1 and BET=1, BET_SEL is set to 1 automatically.
*4 Register setting (0x53 bit0, Default 0)
*5 Forbidden 0 setting

Table 19. Sub-Link Slave device Sub-Link Field BET Result

BETOUT	Output
L	Bit Error Occurred
H	No Error

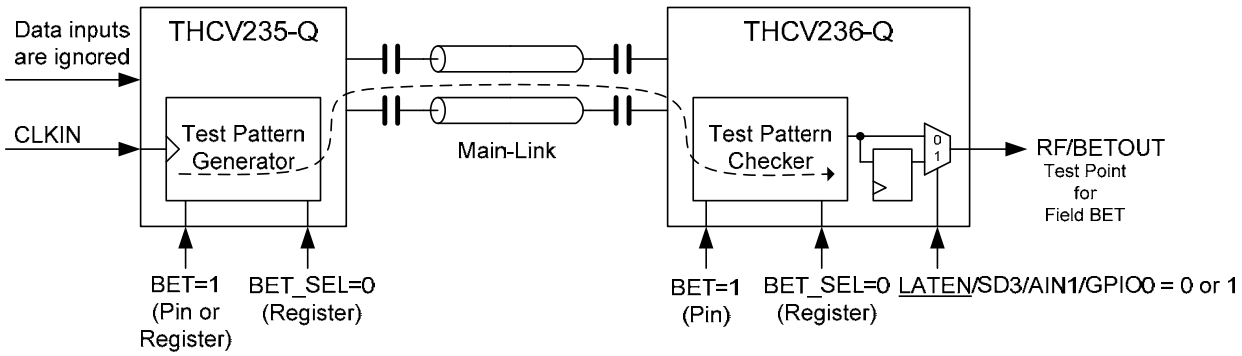


Figure 6. Main-Link Field BET Configuration

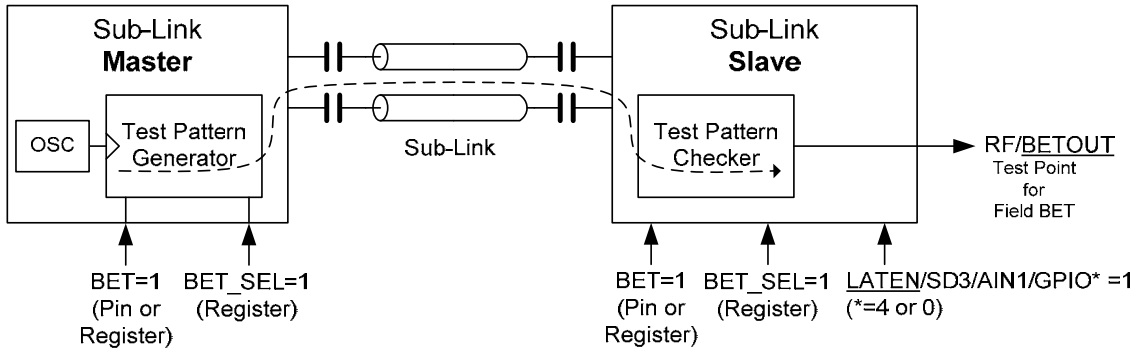


Figure 7. Sub-Link Field BET Configuration

Data Width and Frequency Range Select Function

The THCV235-Q and THCV236-Q support a variety of data width and frequency range. Frequency range is different depending on the mode setting and SSCG enable and disable setting. Refer to Table 20 and Table 21 for details.

Table 20. Main-Link Operation Mode Select (PDN1=1 and SUBMODE=0)

Mode Setting					Freq.Range [MHz]				Main-Link CML Bit Rate	Data Width		Comment
					SSCG Disable		SSCG Enable (*1)					
MAIN MODE	HFSEL	LFSEL	COL1	COL0	min	max	min	max		Data	Sync	
0	0	0	0	0	15	100	26.6	100	x40	32	3	-
0	0	0	0	1	20	133.3	33.3	133.3	x30	24	3	-
0	0	0	1	0	15	100	26.6	100	x40	32	3	Color Space Conversion
0	0	0	1	1	20	133.3	33.3	133.3	x30	24	3	Color Space Conversion
0	0	1	0	0	7.5	15	16.4	32.5	x80	32	3	-
0	0	1	0	1	10	20	19.2	38	x60	24	3	-
0	0	1	1	0	7.5	15	16.4	32.5	x80	32	3	Color Space Conversion
0	0	1	1	1	10	20	19.2	38	x60	24	3	Color Space Conversion
0	1	0	0	0	50	70	50	70	x25	20	3	(*2)
					70	160	70	160				-
0	1	0	0	1	50	70	50	70	x20	16	3	(*2)
					70	160	70	160				-
0	1	0	1	0	50	70	50	70	x25	30	3	Color Space Conversion. (*2)
					70	160	70	160				Color Space Conversion
0	1	0	1	1	50	70	50	70	x20	24	3	Color Space Conversion. (*2)
					70	160	70	160				Color Space Conversion
0	1	1	*	*	-	-	-	-	-	-		Forbidden
1	0	0	0	0	12	80	26.6	80	x50	35		-
1	0	0	0	1	15	100	26.6	100	x40	30		-
1	0	0	1	0	20	133.3	33.3	133.3	x30	22		-
1	0	0	1	1	-	-	-	-	-	-		Forbidden
1	0	1	0	0	6	12	16.4	32.6	x100	35		-
1	0	1	0	1	7.5	15	16.4	32.6	x80	30		-
1	0	1	1	0	10	20	19	38	x60	22		-
1	0	1	1	1	-	-	-	-	-	-		Forbidden
1	1	0	0	0	50	70	50	70	x25	19		(*2)
					70	160	70	160				-
1	1	0	0	1	50	70	50	70	x20	15		(*2)
					70	160	70	160				-
1	1	0	1	0	50	70	50	70	x15	11		(*2)
					70	160	70	160				-
1	1	0	1	1	-	-	-	-	-	-		Forbidden
1	1	1	*	*	-	-	-	-	-	-		Forbidden

*1 Note that register setting is required depending on the mode setting and used frequency range. See Table 10.
*2 Register setting is required. See Table 21.

Table 21. Register setting (HFSEL=1 and Frequency range is from 50MHz to 70MHz)

Step	Register Address(HEX)		Register Value(HEX)		Description
	Sub-Link Master side	Sub-Link Slave side	THCV235-Q	THCV236-Q	
1	0x70	0xF0	0x01		Set 1 to PLL_SET_EN
2	0x76	0xF6	0x02	0x01	Set PLL_SET0
3	0x78	0xF8	0x20		Set PLL_SET1
4	0x7C	0xFC	0x24		Set PLL_SET2

Table 22. Main-Link Operation Mode Select (PDN1=0 or PDN1=1 and SUBMODE=1)

Mode Setting					Freq.Range [MHz]				Main-Link CML Bit Rate	Data Width		Comment
					SSCG Disable		SSCG Enable (THCV235-Q Only)					
MAIN MODE	HFSEL	LFSEL	COL1	COL0	min	max	min	max		Data	Sync	
0	0	0	0	0	15	100	50	100	x40	32	3	-
0	0	0	0	1	20	133.3	66.6	133.3	x30	24	3	-
0	0	0	1	0	15	100	50	100	x40	32	3	Color Space Conversion
0	0	0	1	1	20	133.3	66.6	133.3	x30	24	3	Color Space Conversion
0	0	1	0	0	7.5	15	16.4	32.5	x80	32	3	-
0	0	1	0	1	10	20	19.2	38	x60	24	3	-
0	0	1	1	0	7.5	15	16.4	32.5	x80	32	3	Color Space Conversion
0	0	1	1	1	10	20	19.2	38	x60	24	3	Color Space Conversion
0	1	0	0	0	70	160	100	160	x25	20	3	-
0	1	0	0	1	70	160	100	160	x20	16	3	-
0	1	0	1	0	70	160	100	160	x25	30	3	Color Space Conversion
0	1	0	1	1	70	160	100	160	x20	24	3	Color Space Conversion
0	1	1	*	*	-	-	-	-	-	-		Forbidden
1	0	0	0	0	12	80	40	80	x50	35		-
1	0	0	0	1	15	100	50	100	x40	30		-
1	0	0	1	0	20	133.3	66.6	133.3	x30	22		-
1	0	0	1	1	-	-	-	-	-	-		Forbidden
1	0	1	0	0	6	12	16.4	32.5	x100	35		-
1	0	1	0	1	7.5	15	16.4	32.5	x80	30		-
1	0	1	1	0	10	20	19.2	38	x60	22		-
1	0	1	1	1	-	-	-	-	-	-		Forbidden
1	1	0	0	0	70	160	100	160	x25	19		-
1	1	0	0	1	70	160	100	160	x20	15		-
1	1	0	1	0	70	160	100	160	x15	11		-
1	1	0	1	1	-	-	-	-	-	-		Forbidden
1	1	1	*	*	-	-	-	-	-	-		Forbidden

Data Mapping

Table 23. V-by-One® HS Mode Data Mapping

MAINMODE	0	0	0	0	0	0	0	0	0	0	0	0
HFSEL	0	0	0	0	0	0	0	0	1	1	1	1
LFSEL	0	0	0	0	1	1	1	1	0	0	0	0
COL1	0	0	1	1	0	0	1	1	0	0	1	1
COL0	0	1	0	1	0	1	0	1	0	1	0	1
D0	R2	R0	R2	R0	R2	R0	R2	R0	Cb/Cr2	Cb/Cr0	R2	R0
D1	R3	R1	R3	R1	R3	R1	R3	R1	Cb/Cr3	Cb/Cr1	R3	R1
D2	R4	R2	R4	R2	R4	R2	R4	R2	Cb/Cr4	Cb/Cr2	R4	R2
D3	R5	R3	R5	R3	R5	R3	R5	R3	Cb/Cr5	Cb/Cr3	R5	R3
D4	R6	R4	R6	R4	R6	R4	R6	R4	Cb/Cr6	Cb/Cr4	R6	R4
D5	R7	R5	R7	R5	R7	R5	R7	R5	Cb/Cr7	Cb/Cr5	R7	R5
D6	R8	R6	R8	R6	R8	R6	R8	R6	Cb/Cr8	Cb/Cr6	R8	R6
D7	R9	R7	R9	R7	R9	R7	R9	R7	Cb/Cr9	Cb/Cr7	R9	R7
D8	G2	G0	G2	G0	G2	G0	G2	G0	Y2	Y0	G2	G0
D9	G3	G1	G3	G1	G3	G1	G3	G1	Y3	Y1	G3	G1
D10	G4	G2	G4	G2	G4	G2	G4	G2	Y4	Y2	G4	G2
D11	G5	G3	G5	G3	G5	G3	G5	G3	Y5	Y3	G5	G3
D12	G6	G4	G6	G4	G6	G4	G6	G4	Y6	Y4	G6	G4
D13	G7	G5	G7	G5	G7	G5	G7	G5	Y7	Y5	G7	G5
D14	G8	G6	G8	G6	G8	G6	G8	G6	Y8	Y6	G8	G6
D15	G9	G7	G9	G7	G9	G7	G9	G7	Y9	Y7	G9	G7
D16	B2(*1)	B0(*1)	B2(*1)	B0(*1)	B2(*1)	B0(*1)	B2(*1)	B0(*1)	-	-	B2	B0
D17	B3(*1)	B1(*1)	B3(*1)	B1(*1)	B3(*1)	B1(*1)	B3(*1)	B1(*1)	-	-	B3	B1
D18	B4(*1)	B2(*1)	B4(*1)	B2(*1)	B4(*1)	B2(*1)	B4(*1)	B2(*1)	-	-	B4	B2
D19	B5(*1)	B3(*1)	B5(*1)	B3(*1)	B5(*1)	B3(*1)	B5(*1)	B3(*1)	-	-	B5	B3
D20	B6(*1)	B4(*1)	B6(*1)	B4(*1)	B6(*1)	B4(*1)	B6(*1)	B4(*1)	-	-	B6	B4
D21	B7(*1)	B5(*1)	B7(*1)	B5(*1)	B7(*1)	B5(*1)	B7(*1)	B5(*1)	-	-	B7	B5
D22	B8(*1)	B6(*1)	B8(*1)	B6(*1)	B8(*1)	B6(*1)	B8(*1)	B6(*1)	-	-	B8	B6
D23	B9(*1)	B7(*1)	B9(*1)	B7(*1)	B9(*1)	B7(*1)	B9(*1)	B7(*1)	-	-	B9	B7
D24	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	CONT1 (*1,*2)	-	-	-	-	-
D25	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	CONT2 (*1,*2)	-	-	-	-	-
D26	B0(*1)	-	B0(*1)	-	B0(*1)	-	B0(*1)	-	-	-	B0	-
D27	B1(*1)	-	B1(*1)	-	B1(*1)	-	B1(*1)	-	-	-	B1	-
D28	G0(*1)	-	G0(*1)	-	G0(*1)	-	G0(*1)	-	Y0(*1)	-	G0(*1)	-
D29	G1(*1)	-	G1(*1)	-	G1(*1)	-	G1(*1)	-	Y1(*1)	-	G1(*1)	-
D30	R0(*1)	-	R0(*1)	-	R0(*1)	-	R0(*1)	-	Cb/Cr0(*1)	-	R0(*1)	-
D31	R1(*1)	-	R1(*1)	-	R1(*1)	-	R1(*1)	-	Cb/Cr1(*1)	-	R1(*1)	-
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

*1 CTL bits, which are carried during DE=0 except the first pixel and the last pixel (when COL1=0) or the first 3pixels and the last 3pixels (when COL1=1).
*2 User defined data inputs (THCV235-Q) and outputs (THCV236-Q).

Table 24. Sync Free Mode Data Mapping

MAINMODE	1	1	1	1	1	1	1	1	1	1	1	1
HFSEL	0	0	0	0	0	0	0	0	1	1	1	1
LFSEL	0	0	0	0	1	1	1	1	0	0	0	0
COL1	0	0	1	1	0	0	1	1	0	0	1	1
COL0	0	1	0	1	0	1	0	1	0	1	0	1
D0	D0	D0	D0	-	D0	D0	D0	-	D0/C0	D0/RAW4	D0/YC0	-
D1	D1	D1	D1	-	D1	D1	D1	-	D1/C1	D1/RAW5	D1/YC1	-
D2	D2	D2	D2	-	D2	D2	D2	-	D2/C2	D2/RAW6	D2/YC2	-
D3	D3	D3	D3	-	D3	D3	D3	-	D3/C3	D3/RAW7	D3/YC3	-
D4	D4	D4	D4	-	D4	D4	D4	-	D4/C4	D4/RAW8	D4/YC4	-
D5	D5	D5	D5	-	D5	D5	D5	-	D5/C5	D5/RAW9	D5/YC5	-
D6	D6	D6	D6	-	D6	D6	D6	-	D6/C6	D6/RAW10	D6/YC6	-
D7	D7	D7	D7	-	D7	D7	D7	-	D7/C7	D7/RAW11	D7/YC7	-
D8	D8	D8	D8	-	D8	D8	D8	-	D8/Y0	D8/RAW0	-	-
D9	D9	D9	D9	-	D9	D9	D9	-	D9/Y1	D9/RAW1	-	-
D10	D10	D10	D10	-	D10	D10	D10	-	D10/Y2	D10/RAW2	-	-
D11	D11	D11	D11	-	D11	D11	D11	-	D11/Y3	D11/RAW3	-	-
D12	D12	D12	D12	-	D12	D12	D12	-	D12/Y4	-	-	-
D13	D13	D13	D13	-	D13	D13	D13	-	D13/Y5	-	-	-
D14	D14	D14	D14	-	D14	D14	D14	-	D14/Y6	-	-	-
D15	D15	D15	D15	-	D15	D15	D15	-	D15/Y7	-	-	-
D16	D16	D16	D16	-	D16	D16	D16	-	-	-	-	-
D17	D17	D17	D17	-	D17	D17	D17	-	-	-	-	-
D18	D18	D18	D18	-	D18	D18	D18	-	-	-	-	-
D19	D19	D19	-	-	D19	D19	-	-	-	-	-	-
D20	D20	D20	-	-	D20	D20	-	-	-	-	-	-
D21	D21	D21	-	-	D21	D21	-	-	-	-	-	-
D22	D22	D22	-	-	D22	D22	-	-	-	-	-	-
D23	D23	D23	-	-	D23	D23	-	-	-	-	-	-
D24	D24	D24	-	-	D24	D24	-	-	-	-	-	-
D25	D25	D25	-	-	D25	D25	-	-	-	-	-	-
D26	D26	D26	-	-	D26	D26	-	-	-	-	-	-
D27	D27	-	-	-	D27	-	-	-	-	-	-	-
D28	D28	-	-	-	D28	-	-	-	-	-	-	-
D29	D29	-	-	-	D29	-	-	-	-	-	-	-
D30	D30	-	-	-	D30	-	-	-	-	-	-	-
D31	D31	-	-	-	D31	-	-	-	-	-	-	-
HSYNC(*1)	HSYNC	HSYNC	HSYNC	-	HSYNC	HSYNC	HSYNC	-	HSYNC	HSYNC	HSYNC	-
VSYNC(*1)	VSYNC	VSYNC	VSYNC	-	VSYNC	VSYNC	VSYNC	-	VSYNC	VSYNC	VSYNC	-
DE(*1)	DE	DE	DE	-	DE	DE	DE	-	DE/FIELD	DE	DE	-

*1 Any signal as well as sync signal can be transmitted.