Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

FlashAir™
Wireless LAN Model W-03
Product Specification
Version 3.20

Product Name: FlashAir™ Wireless LAN Model W-03
Product ID: THNSW***GAA-C Series

Memory Application Engineering Department
Memory Division
TOSHIBA CORPORATION – Semiconductor & Storage Products Company

Revision History

Ver/Rev	Date	Written by	Description	Notes
V3.20/D0	28 Aug 2014	Tsuchiya	New Edition	

Contents

1. Introduction

This specification provides an overview of FlashAir™, a Toshiba SDHC card with embedded wireless LAN functionality so that you can review the specification for a host interface design.

You should refer to Section 11, "Requirements and Recommendations for Host Design," when creating a host interface design, etc.

This specification is subject to change without notice for improvement; be sure to consult the latest specification when using FlashAir™.

2. Important Notes

FlashAir™ is a wireless communication device subject to control under the Radio Law of each country. Sales of FlashAir™ and use of its wireless LAN functionality are permitted only in countries and regions where they have been granted official approval.

2.4-GHz-band wireless LAN channels are available from 1ch to 11ch in IEEE 802.11b/g/n mode.

FlashAir™ can be used with SDHC-capable devices that support the FAT32 file system and it supports 8GB, 16GB or 32GB memory capacitor.

3. Product Code (Product and Model Names)

1) TOSHIBA brand model

Product Name: FlashAir™ Wireless LAN Model W-03
Model Name: THNSW008GAA-C (QB8F (8GB Model)
THNSW016GAA-C (QB8F (16GB Model)
THNSW032GAA-C (QB8F (32GB Model)

2) OEM model

Product Name: Wireless LAN SD Memory Card Model W-03
Model Name: THNSW008GAA-C (QB6F (8GB Model)
THNSW016GAA-C (QB6F (16GB Model)
THNSW032GAA-C (QB6F (32GB Model)

* There is no label, which is indicated on Figure 3-1, on OEM model. For the back side, refer to Annex 1-3. Backside Laser Marking, 2) OEM models.

Figure 3-1 SD Card (8GB Model) Design and Appearance

4. Product Overview

FlashAir is a SDHC memory card with embedded wireless LAN functionality.
FlashAir is compliant with the Secure Digital Music Initiative (SDMI) specification and supports content protection compliant with the CPRM specification. FlashAir does not provide content protection by itself; rather, it is realized as an overall system in combination with a host device (e.g., a PC or music player) and application software.

Figure 4-1 shows major use cases of FlashAir.

For example, FlashAir in a digital still camera (DSC) serves as a SD memory card for storing pictures. The wireless LAN functionality of FlashAir allows you to exchange image data with other FlashAir-inserted devices. This means you can easily display pictures in a DSC with a smartphone browser or a browser running on a PC with an embedded wireless LAN module.

Without wireless LAN functionality, you generally need to pull out an SD memory card from one device and insert it to another in order to transfer or copy image data. FlashAir eliminates the need to do this; you can transfer and copy image data more easily.

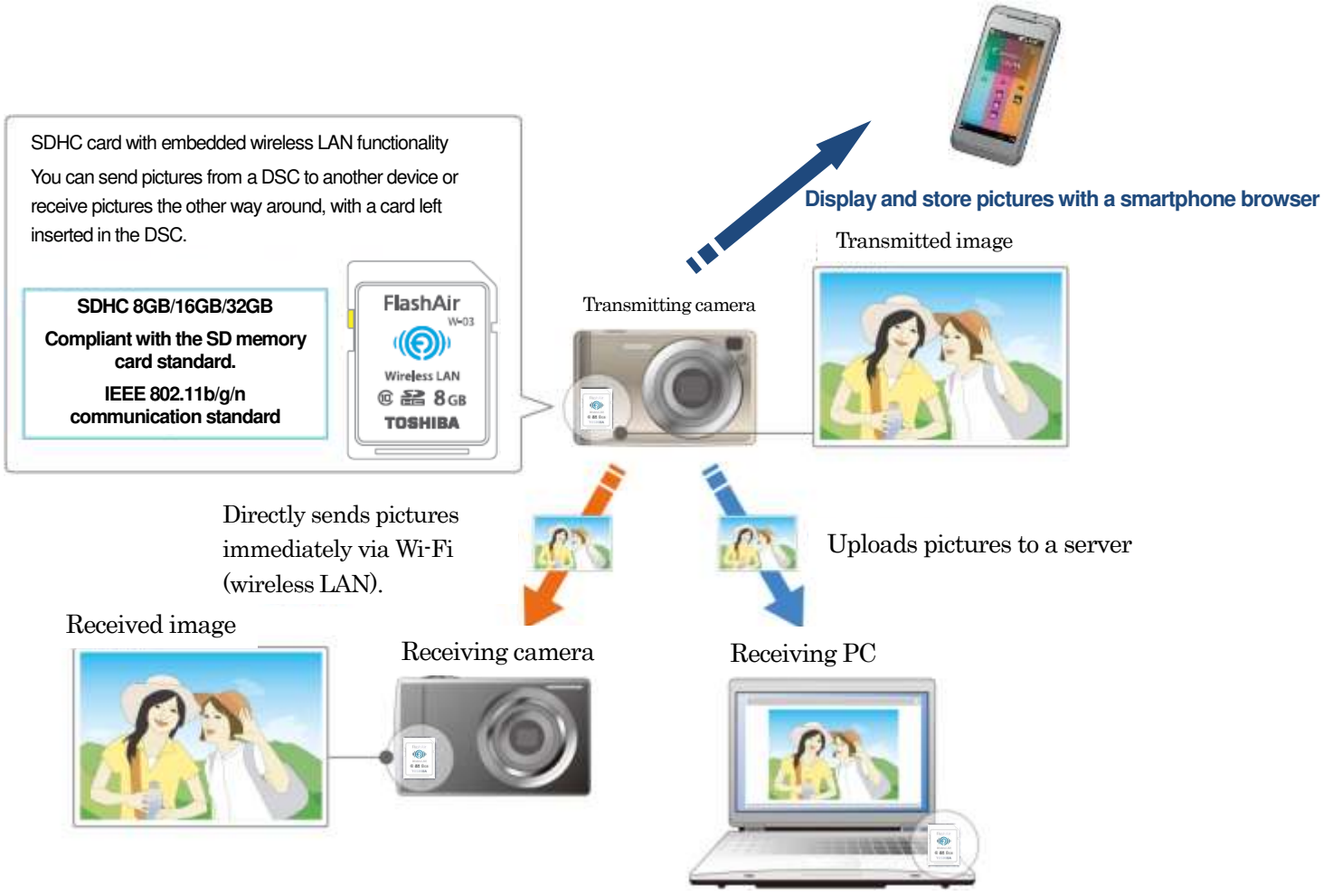

Figure 4-1 Major Use Cases of FlashAir

5. Features

5.1. Design, Content and Logical Format

Table 5.1-1 Design, Content and Logical Format

Design	Toshiba standard design (Figure 3-1)	
Content	None	
Security	Compliant with the SD SECURITY SPECIFICATION, VERSION 3.00 (CPRM-compliant) * CPRM: content Protection for Recordable Media Specification	Media ID and MKB are pre-written.
Logical format	Compliant with the SD FILE SYSTEM SPECIFICATION, VERSION 3.00 (DOS-FAT formatted)	

5.2. Physical and Electrical Features

Table 5.2-1 Physical and Electrical Features

Electrical specification	Operating voltage range: +2.7 to +3.6 V_{DC} Supports SD 1, 4bit mode and SPI mode. * SD PHYSICAL LAYER SPECIFICATION, Version 4.00	
Outline dimensions and weight	32 (H) x 24 (W) x 2.1 (T) mm Weight: Approx. 2 g * Compliant with the SD PHYSICAL LAYER SPECIFICATION, Version 4.00.	
Reliability / durability	* Compliant with the SD PHYSICAL LAYER SPECIFICATION, Version 4.00.	
RoHS	Compliant with the EU RoHS directive (2011 / 65 / EC) specified by the package lable if a package has one that reads "[[G]]/RoHS COMPATIBLE," "[[G]]/RoHS [[Chemical symbol(s) of controlled substance(s)," "RoHS COMPATIBLE" or "RoHS COMPATIBLE, [[Chemical symbol(s) of controlled substance(s)]]>MCV."	
Temperature	Operating	Ta = –25°C to +85°C
	Storage	Tstg = –40°C to +85°C
Humidity (reliability)	Operating	Up to 95% RH (non-condensing) at 25°C
	Storage	Up to 93% RH (non-condensing) at 40°C for 500 h.

5.3. Absolute Maximum Conditions

Parameter	Value
Supply voltage	–0.3V to 4.6V
Input voltage	–0.3V to V_{DD} + 0.3V (≤4.6)

5.4. DC Characteristics

Parameter		Symbol	Condition	Min.	Max.	Unit	Remark
Supply voltage		V_{DD}	-	2.7	3.6	V	
Input voltage	High level	V_H	-	V_{DD}*0.625	V_{DD}+0.3	V	
	Low level	V_L	-	V_{SS}-0.3	V_{DD}*0.25	V	
Output voltage	High level	V_{OH}	V_{DD} = V_{DD} Min. I_{OH} = -2mA	V_{DD}*0.75	-	V	
	Low level	V_{OL}	V_{DD} = V_{DD} Min. I_{OL} = 2mA	-	V_{DD}*0.125	V	
Standby current		I_{CC1}	3.6V 25MHz clock	-	50	mA	
			3.0V Clock stopped	-	30	mA	Ta=25℃
Operating current		I_{CC2}	3.6V / 25MHz 50MHz	-	200	mA	Write
				-	200		Read
				-	200		T_X+Read
				-	200		R_X+Write
Startup time			-	-	500	ms	

5.5. AC Characteristics

Table 5.1-1 shows the AC characteristics of the SD interface in the default speed mode.

Table 5.5-1 SD Device Interface Timing Parameters in the Default Speed Mode

(3.3V power supply = 2.7 to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SDIO clock period	t_{CYCLE}		40	-	-	ns
Command/response data input setup time	$t_{SU\ INPUT}$		5	-	-	ns
Command/response data input hold time	$t_{HO\ INPUT}$		5	-	-	ns
Command/response data output delay (from SDCLK falling edge)	$t_{DLY\ OUTPUT}$		0	-	14	ns

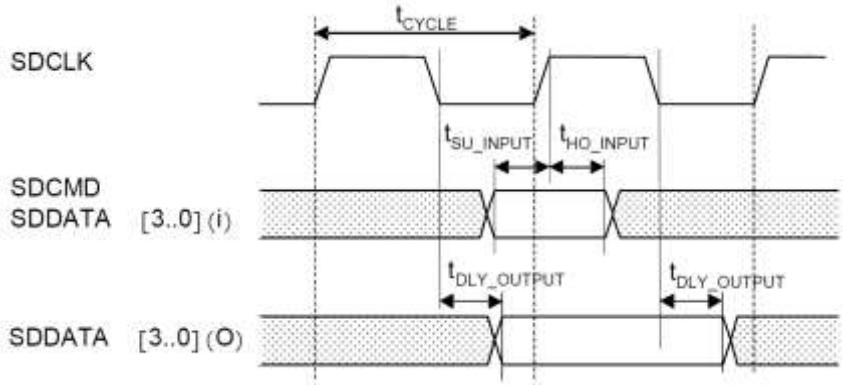

Figure 5.5-1 SD Device Interface Timing in the Default Mode

Table 5.5-2 shows the AC characteristics of the SD interface in high-speed mode.

Table 5.5-2 SD Device Interface Timing Parameters in High-Speed Mode

(3.3V power supply = 2.7 to 3.6 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SDIO clock period	t_{CYCLE}		20	-	-	ns
Command/response data input setup time	$t_{SU\ INPUT}$		6	-	-	ns
Command/response data input hold time	$t_{HO\ INPUT}$		2	-	-	ns
Command/response data output delay (from SDCLK rising edge)	$t_{DLY\ OUTPUT}$		-	-	14	ns
Command/response data output hold time (from SDCLK rising edge)	$t_{HO\ OUTPUT}$		2.5	-	-	ns

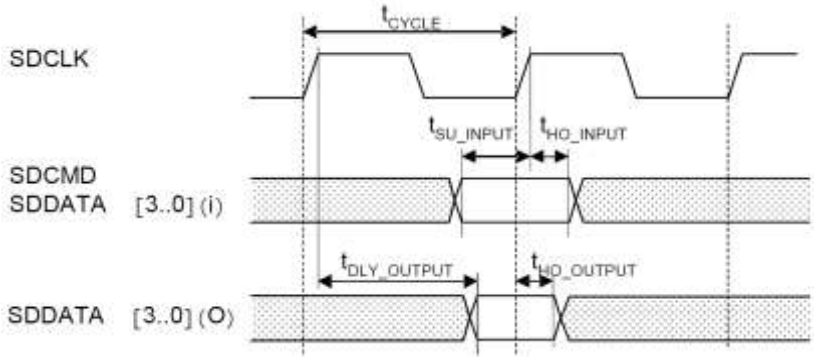

Figure 5.5-2 SD Device Interface Timing in High-Speed Mode

5.6. Key Specifications of the Wireless LAN Functionality

Standard conformity	IEEE 802.11b/g/n (2.4GHz SISO, 20 MHz)
Modulation	DSSS/CCK (1/2/5.5/11 Mbps), OFDM (6 to 72.2 Mbps)
Wireless security	WEP, TKIP, AES (WPA/WPA2)
Wireless QoS	EDCA (WMM)
Other	Infrastructure STA, Infrastructure AP, WPS-enrollee

5.7. Key Specifications of the Network Functionality

Supported protocol	TCP/IP (IPv4)
Server functions	HTTP server, DHCP server, WebDAV
Client functions	HTTP, DHCP, DNS, NETBIOS, Lua

5.8. Case Materials

Polycarbonate and ABS resin
White-colored

5.9. Gold Lead Plating

Surface Au min 0.5 micro meter

6. Standard Conformity and Certification

Standard Conformity

- SD Memory Card Specifications
  - PHYSICAL LAYER SPECIFICATION Ver4.00(Part1) compliant
  - FILE SYSTEM SPECIFICATION Ver3.00(Part2) compliant
  - SECURITY SPECIFICATION Ver3.00(Part3) compliant
  - iSDIO SPECIFICATION Ver1.10(Part E7) compliant
- Wireless certification
  - Japan
    - Certification of construction type for radio equipment (Radio Law) : [R]005-100850
    - Design certification of telecommunications terminal equipment (Telecommunication Business Act) : [T]D14-0133005
  - USA :
    - FCC ID: ZVZP42350FA3
      - RF: FCC PART 15C, OET65C
      - EMC: FCC PART 15B
  - Canada:
    - IC: 9906A-P42350FA3
      - RF: RSS-210, RSS-102
      - EMC: ICES-003
  - Europe:
    - CE0560
      - CE R&TTE RF: EN300 328
      - CE R&TTE Safety: EN60950-1
      - CE R&TTE EMC: EN301 489-1, EN 301 489-17
  - China
    - 8GB Model
      - CMIIT ID : 2014DJ4823
      - valid for five years from 08 Oct, 2014
    - 16GB Model
      - CMIIT ID : 2014DJ4821
      - valid for five years from 08 Oct, 2014
    - 32GB Model
      - CMIIT ID : 2014DJ4822
      - valid for five years from 08 Oct, 2014
  - Taiwan
    - CCAM14LP0220T3
  - Australia
    - RCM
  - New Zealand
    - RCM
  - Korea
    - MSIP-CMM-TSD-THNSW032GAA-C

* For the other countries/regions, to be confirmed to Toshiba sales departments.

7. Physical Feature

Write Protection

The host is responsible for controlling write protection for the SD card. When the Write Protect tab on the SD card is at the LOCK position, the host must not perform any write operation on the SD card.

Sliding the Write Protect tab to the lower position protects the SD card against write access attempts. Upon shipment, the Write Protect tab is set to the upper position to permit write operations to the SD card.

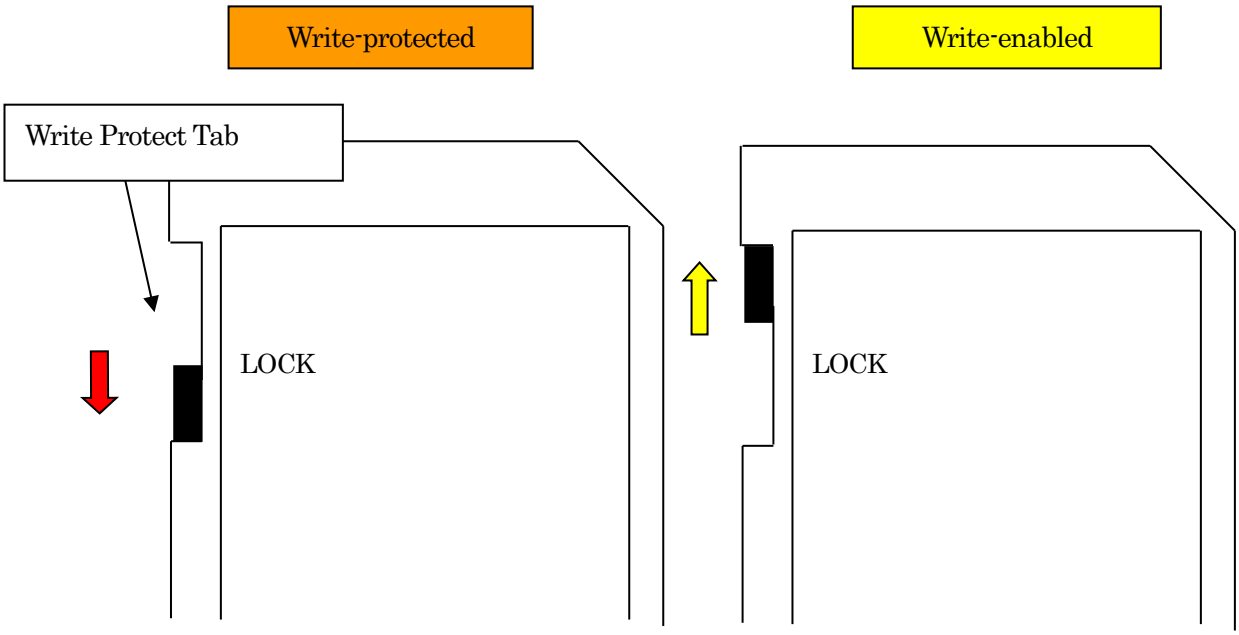

Figure 7-1 Write Protect Tab

8. Electrical Interface Specifications

8.1. SDHC Card Pin Assignment

The pin assignment for the SDHC card is documented below. Figure 8.1-1 shows the pin assignment. Table 8.1-1 lists and briefly describes the SD card pins.

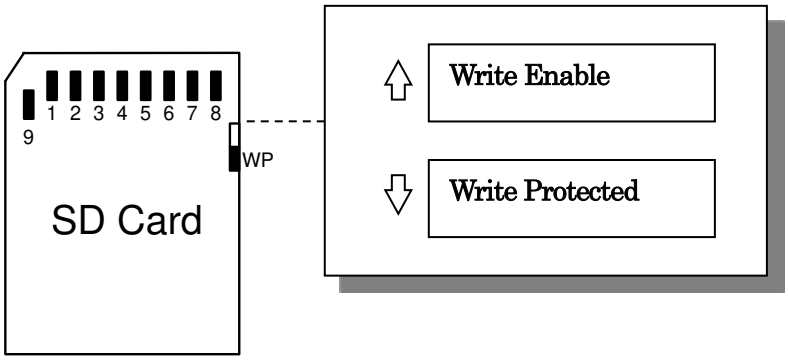

Figure 8.1-1 SDHC Card Pin Assignment

Table 8.1-1 SDHC Card Pin Assignment

Pin #	SD Interface Mode			SPI Interface Mode		
	Pin Name	Type	Description	Pin Name	Type	Description
1	CD/ DAT3	I/O/PP	Card Detect/ Data Line[Bit3]	CS	I	Chip Select (Negative True)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{ss1}	S	Ground	V_{SS}	S	Ground
4	VDD	S	Supply Voltage	V_{DD}	S	Supply Voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{ss2}	S	Ground	V_{SS2}	S	Ground
7	DAT0	I/O/PP	Data Line[Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line[Bit1]	RSV	—	Reserved (*1)
9	DAT2	I/O/PP	Data Line[Bit2]	RSV	—	Reserved (*1)

※S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.

*1 In SPI interface mode, the RSV pins (pins #8 and #9) must be pulled up with a 10- kΩ to 100-kΩ resistor.

8.2. SDHC Card Bus Specifications

The SDHC card supports two access modes: SD mode and SPI mode. In SD mode, the SD card supports parallel data transfers of up to four bits for high-speed access. Compared to SD mode, SPI mode simplifies a host implementation because an SPI interface is available with a multitude of microcontrollers. However, SPI mode is not suitable for applications that require fast transfer rates.

8.2.1. SD Mode

Multiple SDHC memory cards can be connected to a single host, as shown in Figure 8.2.1-1. Multiple SD cards can share the CLK, Vdd and Vss lines, whereas each SD card requires separate command/response and data signals.

The data bus width is programmable for each SDHC memory card. By default, only DAT0 is valid; after reset, the host can change the bus width via ACMD6.

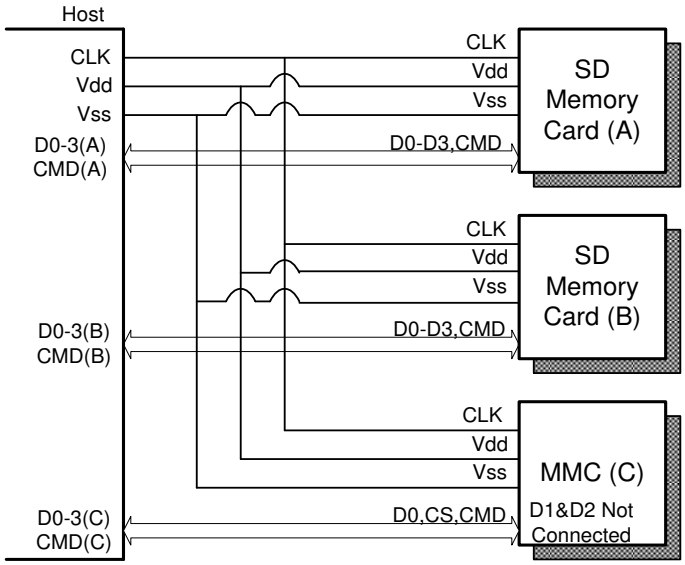

Figure 8.2.1-1 SDHC memory Card Connections (in SD mode)

CLK: Clock signal
CMD: Command/response signal (bidirectional)
DAT 0-DAT3: Data bus (bidirectional)
Vdd, Vss : Vdd and Vss signals

Table 8.2.1-1 List of Commands Supported in SD Mode

(Y: Supported, -: Not supported)

Command	Function	Support	Comment
CMD0	GO_IDLE_STATE	Y	
CMD2	ALL_SEND_CID	Y	
CMD3	SEND_RELATIVE_ADDR	Y	
CMD4	SET_DSR	-	The DSR register is not supported.
CMD6	SWITCH_FUNC	Y	
CMD7	SELECT/DESELECT_CARD	Y	
CMD8	SEND_IF_COND	Y	
CMD9	SEND_CSD	Y	
CMD10	SEND_CID	Y	
CMD12	STOP_TRANSMISSION	Y	
CMD13	SEND_STATUS	Y	
CMD15	GO_INACTIVE_STATE	Y	
CMD16	SET_BLOCKLEN	Y	
CMD17	READ_SINGLE_BLOCK	Y	
CMD18	READ_MULTIPLE_BLOCK	Y	
CMD24	WRITE_BLOCK	Y	
CMD25	WRITE_MULTIPLE_BLOCK	Y	
CMD27	PROGRAM_CSD	Y	
CMD28	SET_WRITE_PROT	-	Write-protect groups are not supported.
CMD29	CLR_WRITE_PROT	-	Write-protect groups are not supported.
CMD30	SEND_WRITE_PROT	-	Write-protect groups are not supported.
CMD32	ERASE_WR_BLK_START	Y	
CMD33	ERASE_WR_BLK_END	Y	
CMD38	ERASE	Y	
CMD42	LOCK_UNLOCK	Y	
CMD48	iSDIO Single block read	Y	
CMD49	iSDIO Single block write	Y	
CMD55	APP_CMD	Y	
CMD56	GEN_CMD	-	An extension command is undefined.
ACMD6	SET_BUS_WIDTH	Y	
ACMD13	SD_STATUS	Y	
ACMD22	SEND_NUM_WR_BLOCKS	Y	
ACMD23	SET_WR_BLK_ERASE_COUNT	Y	
ACMD41	SD_APP_OP_COND	Y	
ACMD42	SET_CLR_CARD_DETECT	Y	
ACMD51	SEND_SCR	Y	
ACMD18	SECURE_READ_MULTI_BLOCK	Y	
ACMD25	SECURE_WRITE_MULTI_BLOCK	Y	
ACMD26	SECURE_WRITE_MKB	Y	
ACMD38	SECURE_ERASE	Y	
ACMD43	GET_MKB	Y	
ACMD44	GET_MID	Y	
ACMD45	SET_CER_RN1	Y	
ACMD46	SET_CER_RN2	Y	
ACMD47	SET_CER_RES2	Y	
ACMD48	SET_CER_RES1	Y	
ACMD49	CHANGE_SECURE_AREA	Y	

- CMD28, CMD29 and CMD30 are optional commands.
- The SDHC card in FlashAir does not contain the DSR register. Therefore, CMD4 is not supported.
- CMD56, an extension command, is undefined.

8.2.2. SPI Mode

The SPI mode of the FlashAir SDHC memory card is designed to allow its connection to a wide range of microcontrollers available on the market and to allow a pool of existing system design resources for MultiMediaCards (MMC) to be reused.

The SPI standard is not a complete data transfer protocol; it only defines the physical connections of a serial bus. In SPI mode, the SDHC memory card provides the same command set as for SD mode.

Since SPI is a widely used serial interface, it simplifies the designing of a host; however, the main drawback of SPI is that it is slow.

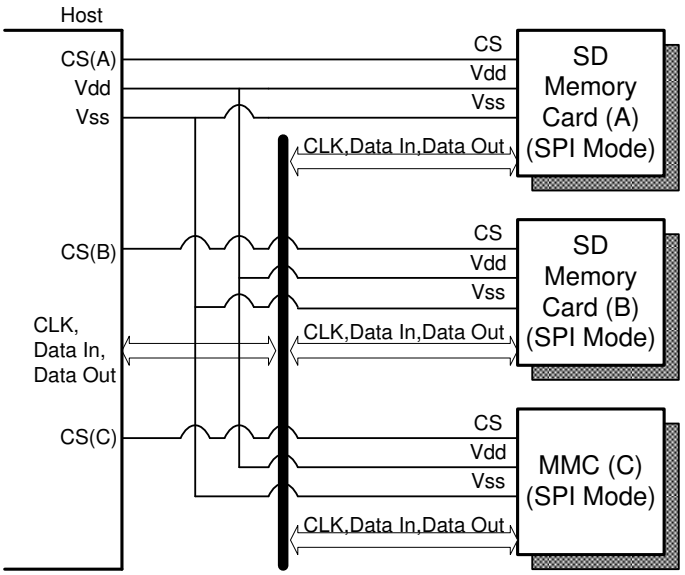

Figure 8.2.2-1 SDHC memory Card Connections (in SPI Mode)

CS: Card Select signal
CLK: Clock signal
Data In: Data signal (from host to card)
Data Out: Data signal (from card to host)
Vdd, Vss: Vdd and Vss signals

Table 8.2.2-1 List of Commands Supported in SPI Mode

(Y: Supported, -: Not supported)

Command	Function	Support	Comment
CMD0	GO_IDLE_STATE	Y	
CMD1	**SEND_OP_CND**	**Y**	**Don't use this command.(See 11.4)**
CMD6	SWITCH_FUNC	Y	
CMD8	SEND_IF_COND	Y	
CMD9	SEND_CSD	Y	
CMD10	SEND_CID	Y	
CMD12	STOP_TRANSMISSION	Y	
CMD13	SEND_STATUS	Y	
CMD16	SET_BLOCKLEN	Y	
CMD17	READ_SINGLE_BLOCK	Y	
CMD18	READ_MULTIPLE_BLOCK	Y	
CMD24	WRITE_BLOCK	Y	
CMD25	WRITE_MULTIPLE_BLOCK	Y	
CMD27	PROGRAM_CSD	Y	
CMD28	SET_WRITE_PROT	-	Write-protect groups are not supported.
CMD29	CLR_WRITE_PROT	-	Write-protect groups are not supported.
CMD30	SEND_WRITE_PROT	-	Write-protect groups are not supported.
CMD32	ERASE_WR_BLK_START_ADDR	Y	
CMD33	ERASE_WR_BLK_END_ADDR	Y	
CMD38	ERASE	Y	
CMD42	LOCK_UNLOCK	Y	
CMD48	iSDIO Single block read	Y	
CMD49	iSDIO Single block write	Y	
CMD55	APP_CMD	Y	
CMD56	GEN_CMD	-	An extension command is undefined.
CMD58	READ_OCR	Y	
CMD59	CRC_ON_OFF	Y	
ACMD6	SET_BUS_WIDTH	Y	
ACMD13	SD_STATUS	Y	
ACMD22	SEND_NUM_WR_BLOCKS	Y	
ACMD23	SET_WR_BLK_ERASE_COUNT	Y	
ACMD41	SD_APP_OP_COND	Y	
ACMD42	SET_CLR_CARD_DETECT	Y	
ACMD51	SEND_SCR	Y	
ACMD18	SECURE_READ_MULTI_BLOCK	Y	
ACMD25	SECURE_WRITE_MULTI_BLOCK	Y	
ACMD26	SECURE_WRITE_MKB	Y	
ACMD38	SECURE_ERASE	Y	
ACMD43	GET_MKB	Y	
ACMD44	GET_MID	Y	
ACMD45	SET_CER_RN1	Y	
ACMD46	SET_CER_RN2	Y	
ACMD47	SET_CER_RES2	Y	
ACMD48	SET_CER_RES1	Y	
ACMD49	CHANGE_SECURE_AREA	Y	

- CMD28, CMD29 and CMD30 are optional commands.
- CMD56, an extension command, is undefined.
- SPI mode is supporting the commands of SD Specification Version 2.00 level.

8.3. SDHC memory Card Initialization

This section describes the procedure for initializing the SDHC memory card. Figure 8.3-1 shows its flowcharts.

(1) After power-on, apply at least 74 dummy clock cycles. At this time, the operating voltage can be supplied from the beginning.
(2) Select an operating mode (SD or SPI mode) of the SDHC memory card as follows. To use the SD card in SPI mode, the host should issue CMD0 by driving pin 1, CD/DAT3, Low. This causes an initialization to start in SPI mode. A High on pin 1, CD/DAT3, causes an initialization to start in SD mode. (When pin 1 is not driven by the host, it is pulled High by an internal pull-up resistor.) Thereafter, the SD card remains in the selected operating mode until CMD0 is issued again or the SD card is rebooted.
(3) Send the ACMD41 with Arg = 0 and identify the operating voltage range of the Card.
(4) Apply the indicated operating voltage to the card.
Reissue ACMD41 with apply voltage storing and repeat ACMD41 until the busy bit is cleared.
(Bit 31 Busy = 1) If response time out occurred, host can recognize not SDHC Card.
(5) Issue the CMD2 and get the Card ID (CID).
Issue the CMD3 and get the RCA. (RCA value is randomly changed by access, not equal zero)
(6) Issue the CMD7 and move to the transfer state.
If necessary, Host may issue the ACMD42 and disabled the pull up resistor for Card detect.
(7) Issue the ACMD13 and poll the Card status as SD Memory Card. Check SD_CARD_TYPE value. If significant 8 bits are “all zero”, that means SD Card. If it is not, stop initialization.
(8) Issue CMD7 and move to standby state. Issue CMD9 and get CSD. Issue CMD10 and get CID.
(9) Back to the Transfer state with CMD7. Issue ACMD6 and choose the appropriate bus-width.

Then the Host can access the Data between the SD card as a storage device.

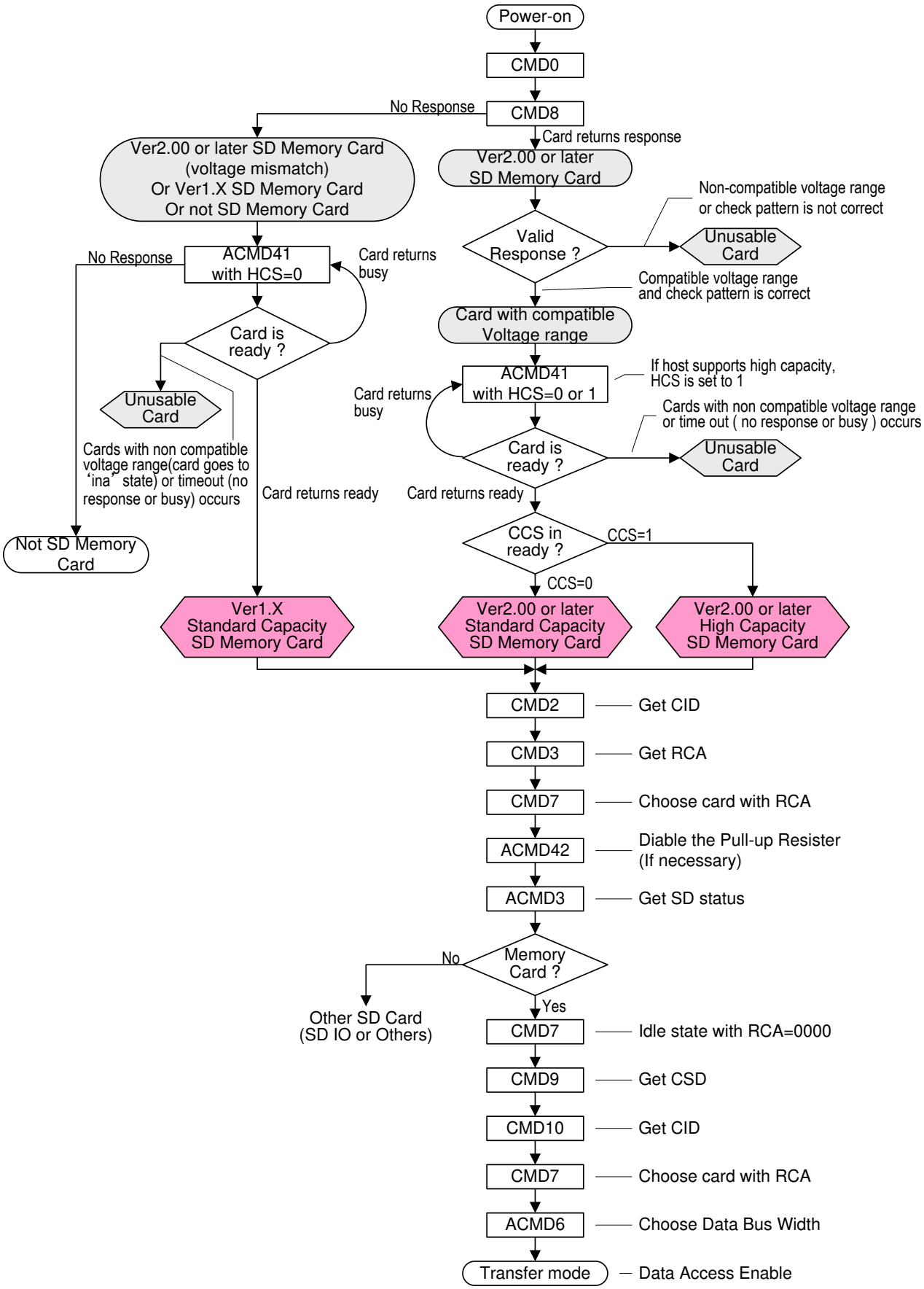

Figure 8.3-1 Flowchart for SD Card Initialization

8.4. Electrical Specification of the SDHC memory Card

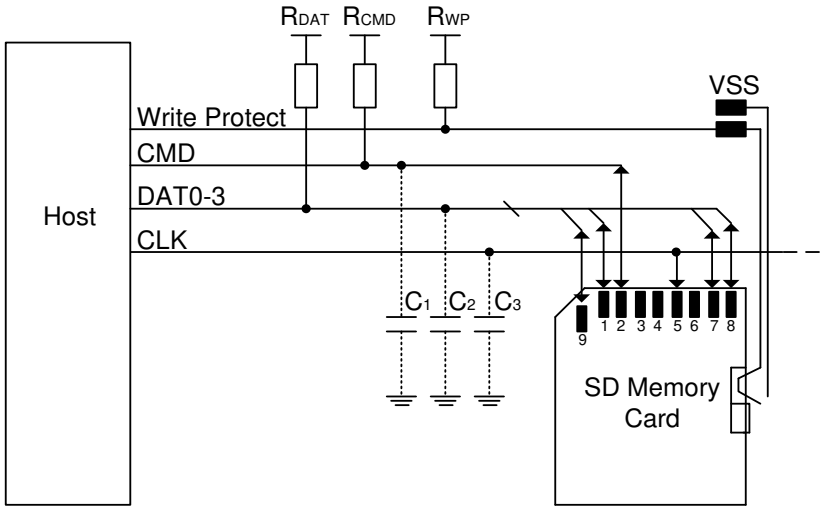

Figure 8.4-1 SD Card Connections

9. SDHC memory Card Internals

9.1. Security Information

The Media ID and MKB (Media Key Block) contain Toshiba-standard data compliant with the Content Protection for Recordable Media (CPRM) Specification.

Note: The security information is NOT Development information for evaluation.
Host System shall be compliance with the CPRM to use the security function.
This information is kept as confidential because of security reasons.

9.2. Registers in the SDHC memory Card

The SD card contains six registers (OCR, CID, CSD, RCA, DSR and SCR) listed in Table 9.2-1, of which FlashAir does not support the DSR register.

The subsections that follow describe each of these registers and the SD Status values.

Table 9.2-1 Internal Registers of the SD Card

Name	Bit Width	Description
OCR	32	Operating Conditions Register (OCR). Contains the operating voltage range and the SD card busy flag.
CID	128	Card Identification (CID) register. Contains an SD card identification number.
CSD	128	Card Specific Data (CSD) register
RCA	16	Relative Card Address (RCA) register. Contains the card address used for SD card identification.
DSR	16	Driver Stage Register (not supported)
SCR	64	SD Card Configuration Register (SCR)
SD Status	512	SD card status

9.2.1. OCR Register

The OCR is a 32-bit read-only register that shows the operating voltage range of the SD card and informs the host whether the SD initialization procedure is finished after power-on. Table 9.2.1-1 describes the structure of the OCR register.

Table 9.2.1-1 OCR Register

OCR bit position	VDD voltage window	Default		
		8 GB	16GB	32GB
31	Card power up status bit (busy)	"0" = busy "1" = ready		
30	Card Capacity Status	"0" = SD Memory Card "1" = SDHC Memory Card		
29-24	Reserved	All '0'		
24	Switching to 1.8V Accepted(S18A)	0		
23	3.6 - 3.5	1		
22	3.5 - 3.4	1		
21	3.4 - 3.3	1		
20	3.3 - 3.2	1		
19	3.2 - 3.1	1		
18	3.1 - 3.0	1		
17	3.0 - 2.9	1		
16	2.9 - 2.8	1		
15	2.8 - 2.7	1		
14	Reserved	0		
13	Reserved	0		
12	Reserved	0		
11	Reserved	0		
10	Reserved	0		
9	Reserved	0		
8	Reserved	0		
7	Reserved for Low Voltage Range	0		
6	Reserved	0		
5	Reserved	0		
4	Reserved	0		
3-0	reserved	All '0'		

Bits 23 to 4 show the operating voltage range of the SDHC memory card.

Bit 31 informs the host whether the SD initialization procedure is finished during power-up. This bit is set to 1 when the SDHC memory card has finished the initialization procedure after receiving an initialization command upon power-on.

9.2.2. CID Register

The 128-bit CID register contains information for SD card identification.
This information is used during the card identification phase.
Table 9.2.2-1 describes the structure of the CID register.

Table 9.2.2-1 CID Register

Field	Width	CID-slice	Default		
			8 GB	16GB	32GB
MID	8	[127:120]	0x02		
OID	16	[119:104]	"TM"(0x544D)		
PNM	40	[103:64]	"SW08G"	"SW16G"	"SW32G"
PRV	8	[63:56]	0x48	0x40	0x40
PSN	32	[55:24]	(Note 1) (Product serial number)		
-	4	[23:20]	All '0'		
MDT	12	[19:8]	(Note 1) (Manufacture date)		
CRC	7	[7:1]	(Note 2) (CRC)		
-	1	[0:0]	1b		

Note 1: Specific to an SD card
Note 2: Computed from the contents of the CID register

・MID
8-bit binary manufacturer ID assigned by the SDA.
→ 0x02 in the FlashAir SDHC memory card

・OID
16-bit binary value that identifies the SD card OEM and/or the card contents. The OID is assigned by the SDA.
→ The ASCII string "TM" in FlashAir SDHC memory card

・PNM
String that denotes a product name
→ The product name of the FlashAir SDHC memory card is as follows:

8GB: "SW08G" (0x5357303847)
16GB: "SW16G" (0x5357313647)
32GB: "SW32G" (0x5357333247)

・PRV
Product revision
→ The PRV value is updated for each revision of the SDHC memory card.

・PSN
32-bit binary product serial number
→ Contains a unique number for each SDHC memory card.

・MDT

Year and month of manufacture

[3:0]: Month. The digit 1 denotes January.

[11:4]: Year. The digit 0 denotes 2000.

→ Contains a unique number for each SDHC memory card.

・CRC

CRC checksum value calculated over the contents of the CID register