



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

Copyright © 1997, Power Innovations Limited, UK

MARCH 1994 - REVISED SEPTEMBER 1997

TELECOMMUNICATION SYSTEM SECONDARY PROTECTION

- **Ion-Implanted Breakdown Region**
Precise and Stable Voltage
Low Voltage Overshoot under Surge

DEVICE	V _{DRM} V	V _(BO) V
'2072F3	58	72
'2082F3	66	82

- **Planar Passivated Junctions**
Low Off-State Current < 10 µA
- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I _{TSP} A
2/10 µs	FCC Part 68	80
8/20 µs	ANSI C62.41	70
10/160 µs	FCC Part 68	60
10/560 µs	FCC Part 68	45
0.5/700 µs	RLM 88	38
10/700 µs	FTZ R12	50
	VDE 0433	50
	CCITT IX K17/K20	50
10/1000 µs	REA PE-60	35

- **Surface Mount and Through-Hole Options**

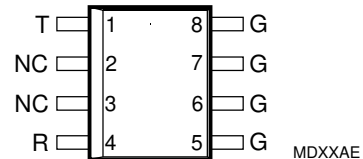
PACKAGE	PART # SUFFIX
Small-outline	D
Small-outline taped and reeled	DR
Plastic DIP	P
Single-in-line	SL

- **UL Recognized, E132482**

description

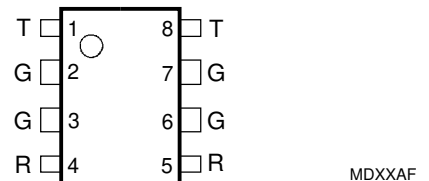
These low voltage dual symmetrical transient voltage suppressor devices are designed to protect ISDN applications against transients caused by lightning strikes and a.c. power lines. Offered in two voltage variants to meet battery and protection requirements they are guaranteed to suppress and withstand the listed international lightning surges in both polarities. Transients are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents d.c. latchup as the current subsides.

**D PACKAGE
(TOP VIEW)**



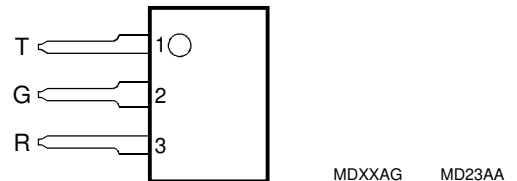
NC - No internal connection

**P PACKAGE
(TOP VIEW)**

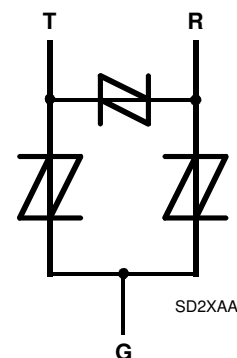


Specified T terminal ratings require connection of pins 1 and 8.
Specified R terminal ratings require connection of pins 4 and 5.

**SL PACKAGE
(TOP VIEW)**



device symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation

PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.

TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

MARCH 1994 - REVISED SEPTEMBER 1997

description (Continued)

The small-outline 8-pin assignment has been carefully chosen for the TISP series to maximise the inter-pin clearance and creepage distances which are used by standards (e.g. IEC950) to establish voltage withstand ratings.

absolute maximum ratings

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage ($0^{\circ}\text{C} < T_J < 70^{\circ}\text{C}$)	'2072F3 '2082F3	V_{DRM}	± 58 ± 66	V
Non-repetitive peak on-state pulse current (see Notes 1, 2 and 3)				
1/2 μs (Gas tube differential transient, open-circuit voltage wave shape 1/2 μs)			120	
2/10 μs (FCC Part 68, open-circuit voltage wave shape 2/10 μs)			80	
8/20 μs (ANSI C62.41, open-circuit voltage wave shape 1.2/50 μs)			70	
10/160 μs (FCC Part 68, open-circuit voltage wave shape 10/160 μs)			60	
5/200 μs (VDE 0433, open-circuit voltage wave shape 2 kV, 10/700 μs)		I_{TSP}	50	A
0.5/310 μs (RLM 88, open-circuit voltage wave shape 1.5 kV, 0.5/700 μs)			38	
5/310 μs (CCITT IX K17/K20, open-circuit voltage wave shape 2 kV, 10/700 μs)			50	
5/310 μs (FTZ R12, open-circuit voltage wave shape 2 kV, 10/700 μs)			50	
10/560 μs (FCC Part 68, open-circuit voltage wave shape 10/560 μs)			45	
10/1000 μs (REA PE-60, open-circuit voltage wave shape 10/1000 μs)			35	
Non-repetitive peak on-state current (see Notes 2 and 3)	D Package P Package SL Package	I_{TSM}	4 6 6	A rms
50 Hz, 1 s				
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value < 38 A		di_F/dt	250	A/ μs
Junction temperature		T_J	-40 to +150	$^{\circ}\text{C}$
Storage temperature range		T_{stg}	-40 to +150	$^{\circ}\text{C}$

- NOTES: 1. Further details on surge wave shapes are contained in the Applications Information section.
 2. Initially the TISP must be in thermal equilibrium with $0^{\circ}\text{C} < T_J < 70^{\circ}\text{C}$. The surge may be repeated after the TISP returns to its initial conditions.
 3. Above 70°C , derate linearly to zero at 150°C lead temperature.

electrical characteristics for the T and R terminals, $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	TISP2072F3		TISP2082F3		UNIT
		MIN	MAX	MIN	MAX	
I_{DRM} Repetitive peak off-state current	$V_D = \pm V_{\text{DRM}}, 0^{\circ}\text{C} < T_J < 70^{\circ}\text{C}$		± 10		± 10	μA
I_D Off-state current	$V_D = \pm 50\text{ V}$		± 10		± 10	μA
C_{off} Off-state capacitance	$f = 100\text{ kHz}, V_d = 100\text{ mV}, V_D = 0,$ Third terminal voltage = 0 (see Notes 4 and 5)	32†	55	32†	55	pF

- NOTES: 4. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.
 5. Further details on capacitance are given in the Applications Information section.

† Typical value of the parameter, not a limit value.

electrical characteristics for the T and G or the R and G terminals, $T_J = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	TISP2072F3		TISP2082F3		UNIT
		MIN	MAX	MIN	MAX	
I_{DRM} Repetitive peak off-state current	$V_D = \pm V_{\text{DRM}}, 0^{\circ}\text{C} < T_J < 70^{\circ}\text{C}$		± 10		± 10	μA

PRODUCT INFORMATION

TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

MARCH 1994 - REVISED SEPTEMBER 1997

electrical characteristics for the T and G or the R and G terminals, $T_J = 25^\circ\text{C}$ (Continued)

PARAMETER	TEST CONDITIONS	TISP2072F3		TISP2082F3		UNIT
		MIN	MAX	MIN	MAX	
$V_{(BO)}$ Breakover voltage	$dv/dt = \pm 250 \text{ V/ms}$, Source Resistance = 300Ω		± 72		± 82	V
$V_{(BO)}$ Impulse breakover voltage	$dv/dt = \pm 1000 \text{ V}/\mu\text{s}$, $di/dt < 20 \text{ A}/\mu\text{s}$ Source Resistance = 50Ω		$\pm 84^\dagger$		$\pm 94^\dagger$	V
$I_{(BO)}$ Breakover current	$dv/dt = \pm 250 \text{ V/ms}$, Source Resistance = 300Ω	± 0.15	± 0.6	± 0.15	± 0.6	A
V_T On-state voltage	$I_T = \pm 5 \text{ A}$, $t_W = 100 \mu\text{s}$		± 3		± 3	V
I_H Holding current	$di/dt = -/+30 \text{ mA/ms}$	± 0.15		± 0.15		A
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value $< 0.85V_{(BR)MIN}$	± 5		± 5		$\text{kV}/\mu\text{s}$
I_D Off-state current	$V_D = \pm 50 \text{ V}$		± 10		± 10	μA
C_{off} Off-state capacitance	$f = 100 \text{ kHz}$, $V_d = 100 \text{ mV}$ $V_D = 0$, Third terminal voltage = 0 $V_D = -5 \text{ V}$ (see Notes 6 and 7) $V_D = -50 \text{ V}$	77^\dagger	130	77^\dagger	130	μF
		42^\dagger	70	42^\dagger	70	μF
		19^\dagger	30	19^\dagger	30	μF

NOTES: 6 These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.
7. Further details on capacitance are given in the Applications Information section.

PARAMETER MEASUREMENT INFORMATION

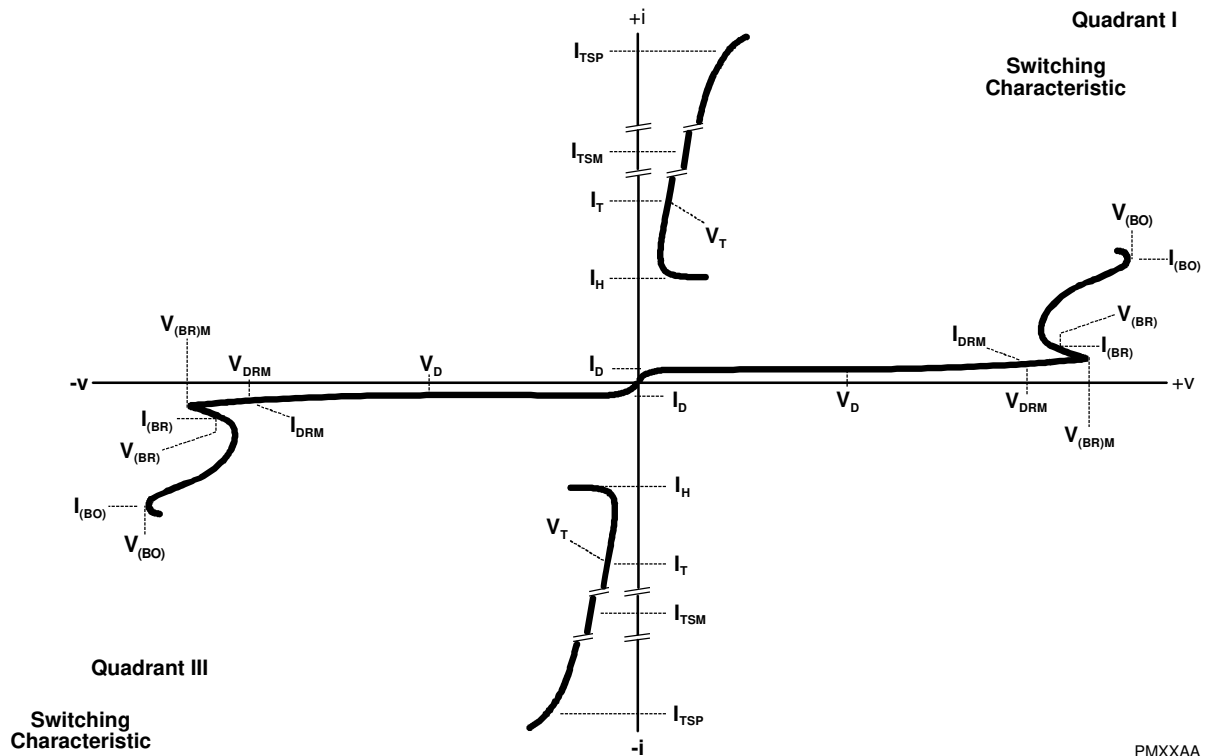


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR ANY PAIR OF TERMINALS

The high level characteristics for terminals R and T are not guaranteed.

TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

MARCH 1994 - REVISED SEPTEMBER 1997

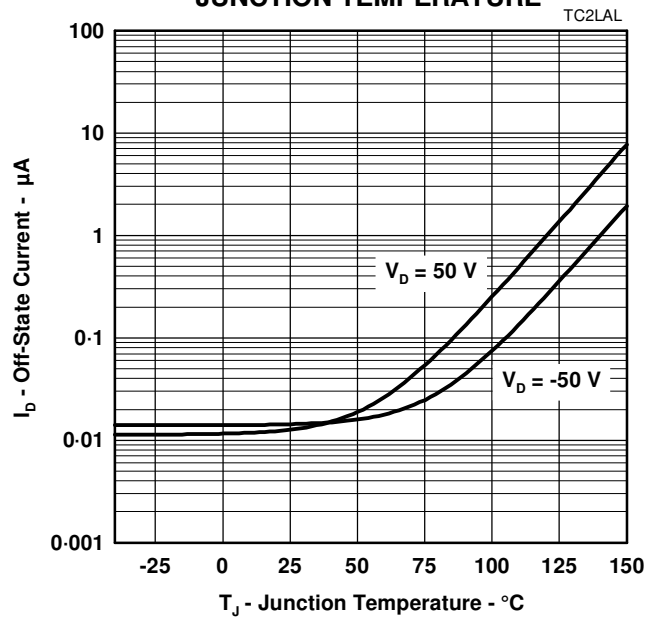
† Typical value of the parameter, not a limit value.

thermal characteristics

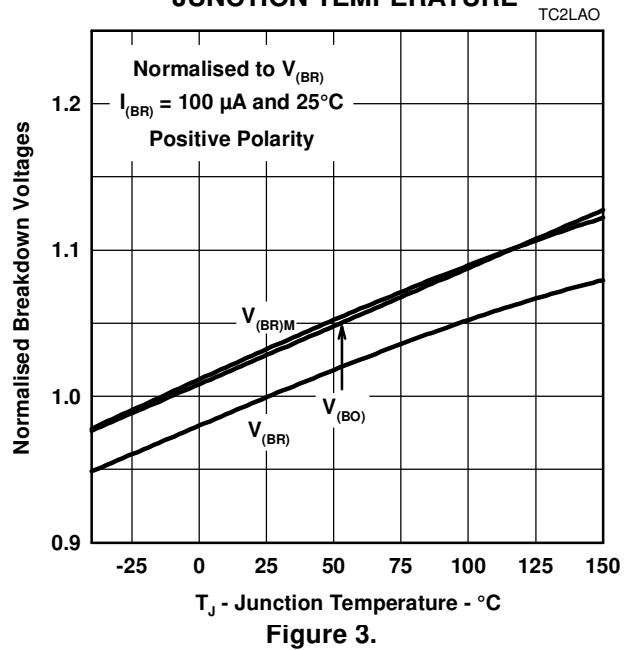
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction to free air thermal resistance	D Package			160	°C/W
	P Package			100	
	SL Package			105	

TYPICAL CHARACTERISTICS T and G, or R and G terminals

OFF-STATE CURRENT
vs
JUNCTION TEMPERATURE



NORMALISED BREAKDOWN VOLTAGES
vs
JUNCTION TEMPERATURE



PRODUCT INFORMATION

TYPICAL CHARACTERISTICS
 T and G, or R and G terminals

NORMALISED BREAKDOWN VOLTAGES

VS

JUNCTION TEMPERATURE

TC2LAP

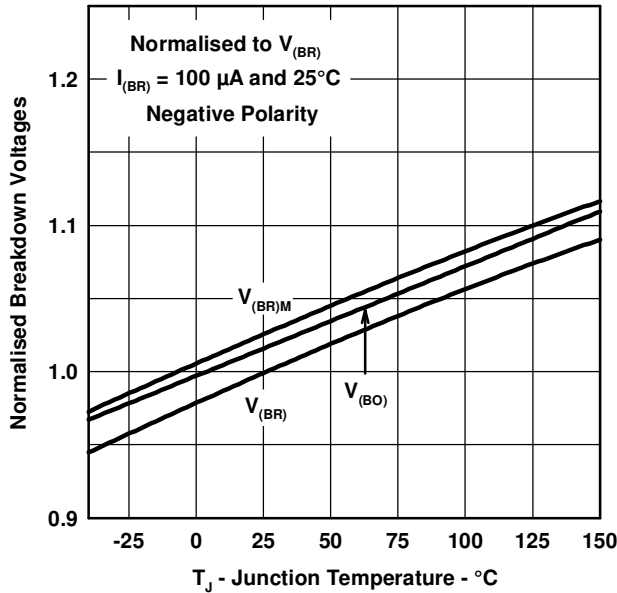


Figure 4.

ON-STATE CURRENT

VS

ON-STATE VOLTAGE

TC2MAQ

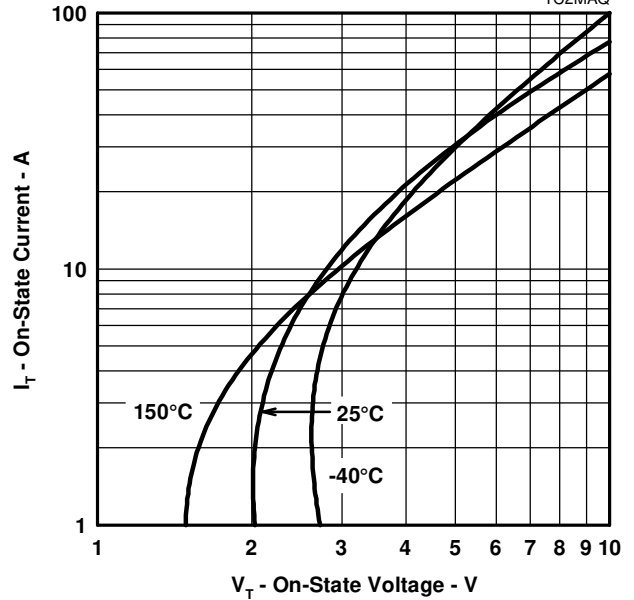


Figure 5.

HOLDING CURRENT & BREAKOVER CURRENT

VS

JUNCTION TEMPERATURE

TC2LAM

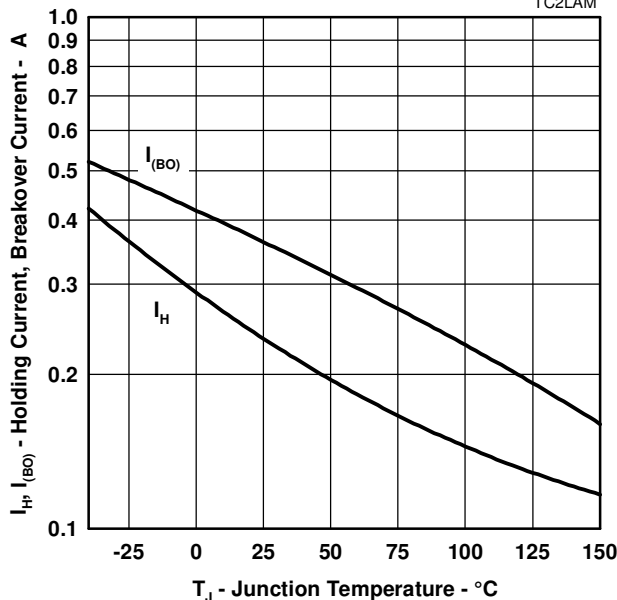


Figure 6.

NORMALISED BREAKOVER VOLTAGE

VS

RATE OF RISE OF PRINCIPLE CURRENT

TC2LAM

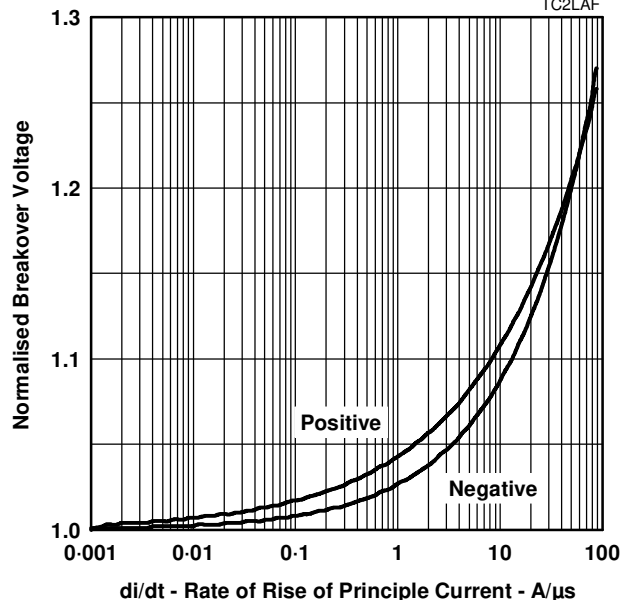


Figure 7.

**TISP2072F3, TISP2082F3
DUAL SYMMETRICAL TRANSIENT
VOLTAGE SUPPRESSORS**

MARCH 1994 - REVISED SEPTEMBER 1997

**TYPICAL CHARACTERISTICS
T and G, or R and G terminals**

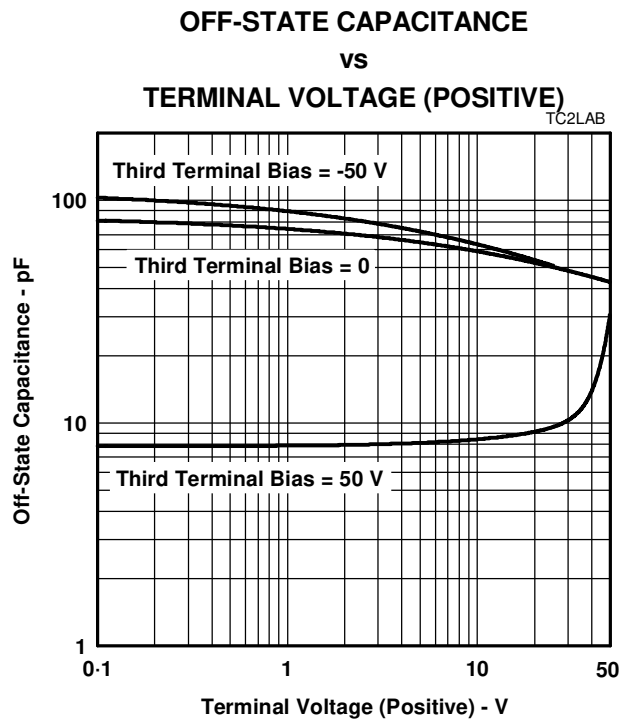


Figure 8.

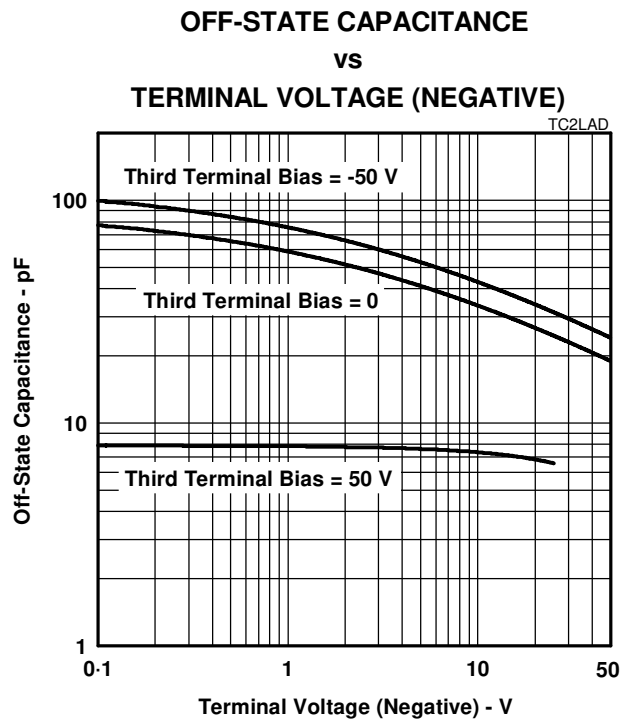


Figure 9.

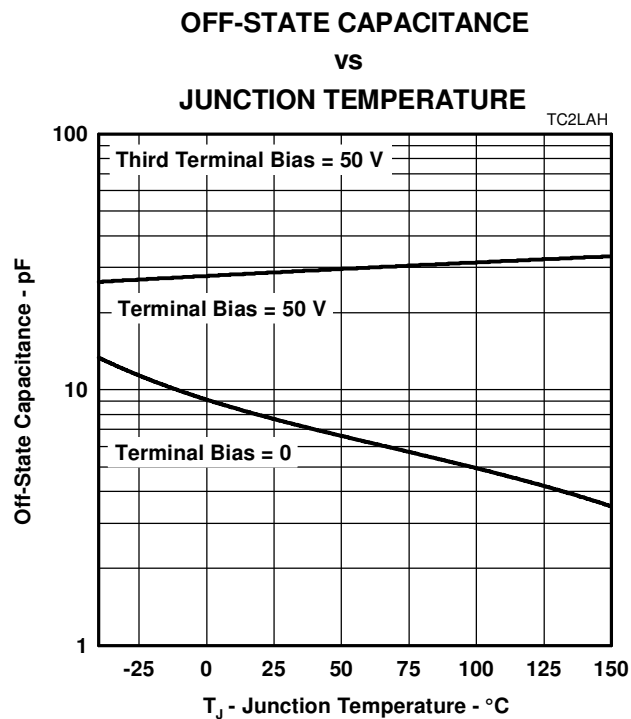


Figure 10.

TYPICAL CHARACTERISTICS
 T and G, or R and G terminals

OFF-STATE CAPACITANCE
 vs
 JUNCTION TEMPERATURE

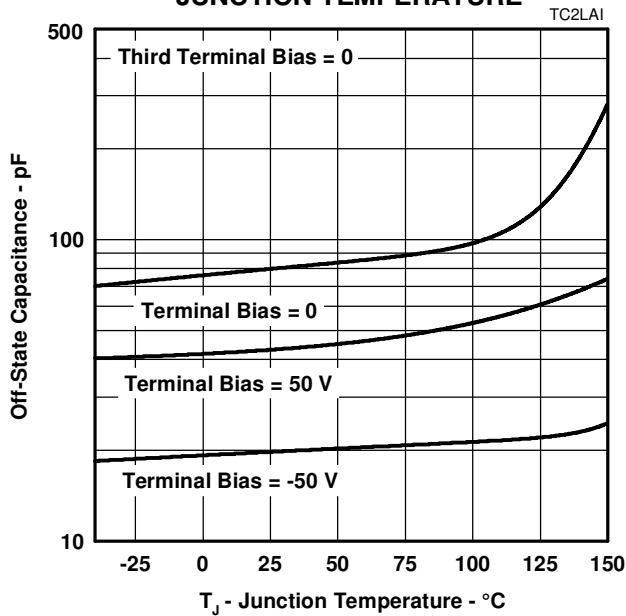


Figure 11.

OFF-STATE CAPACITANCE
 vs
 JUNCTION TEMPERATURE

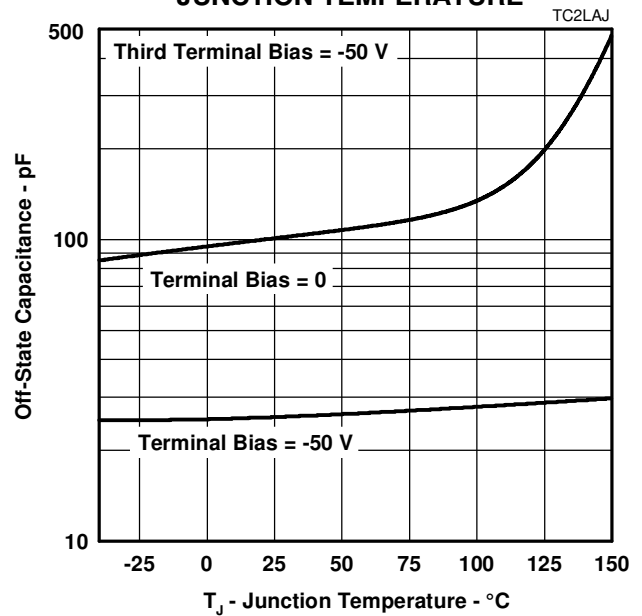


Figure 12.

SURGE CURRENT
 vs
 DECAY TIME

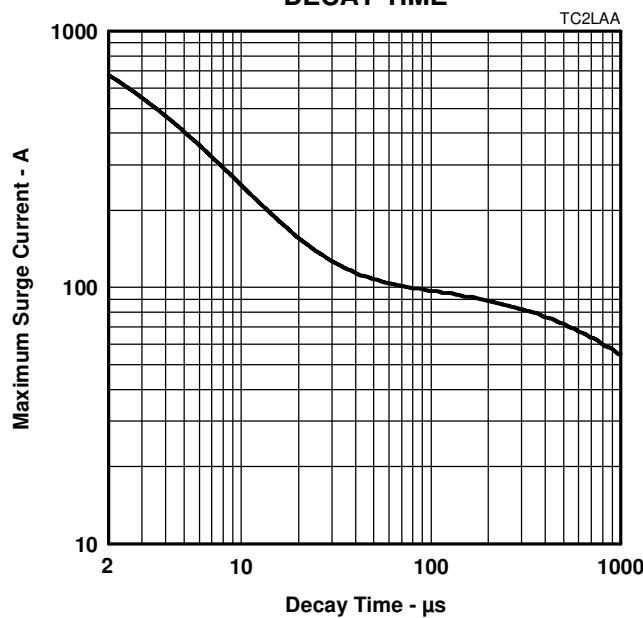


Figure 13.

**TISP2072F3, TISP2082F3
DUAL SYMMETRICAL TRANSIENT
VOLTAGE SUPPRESSORS**

MARCH 1994 - REVISED SEPTEMBER 1997

**TYPICAL CHARACTERISTICS
T and R terminals**

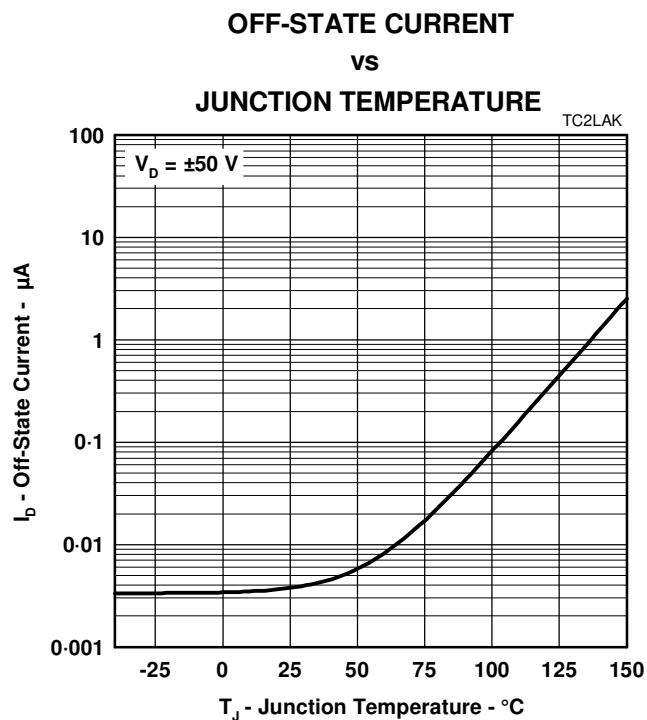


Figure 14.

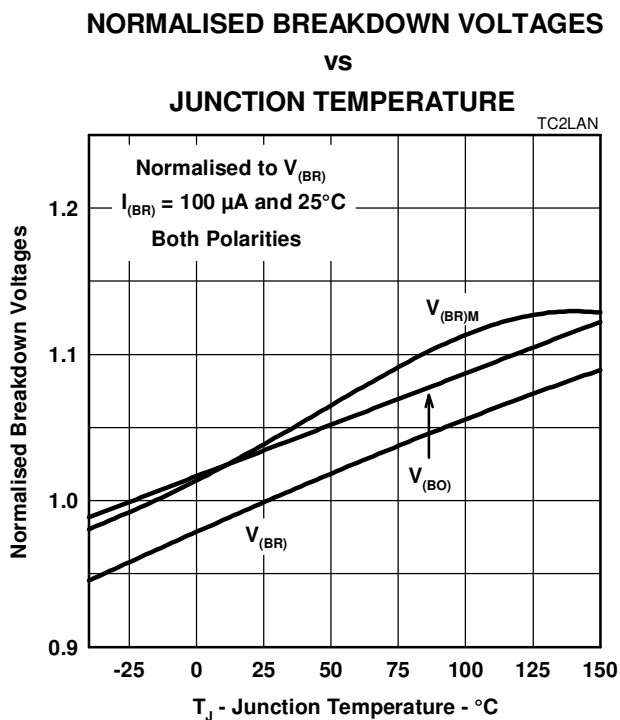


Figure 15.

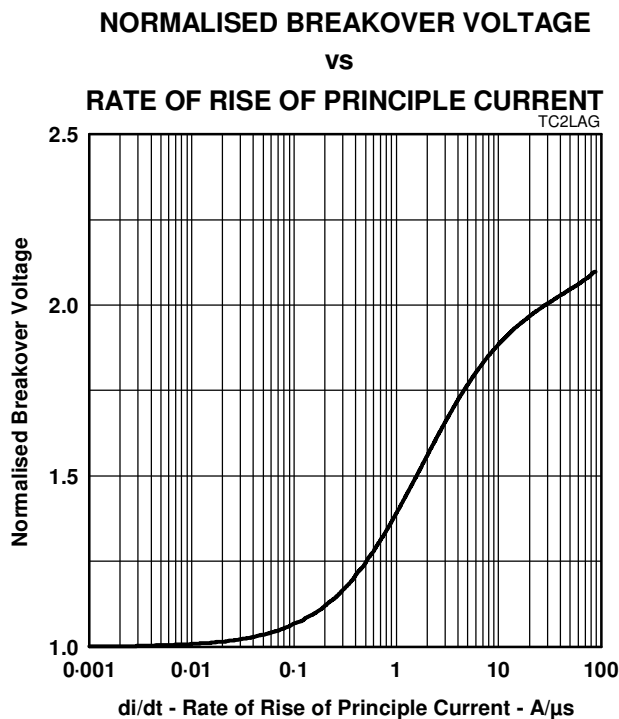


Figure 16.

PRODUCT INFORMATION

TYPICAL CHARACTERISTICS
 T and R terminals

OFF-STATE CAPACITANCE

VS

TERMINAL VOLTAGE (POSITIVE)

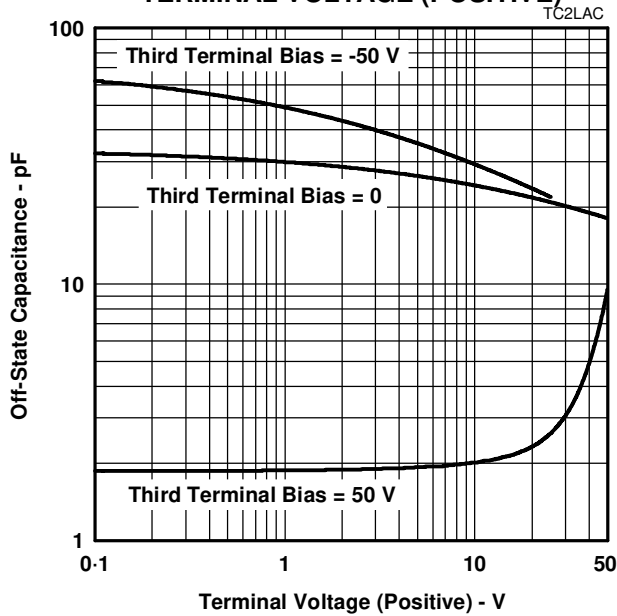


Figure 17.

OFF-STATE CAPACITANCE

VS

TERMINAL VOLTAGE (NEGATIVE)

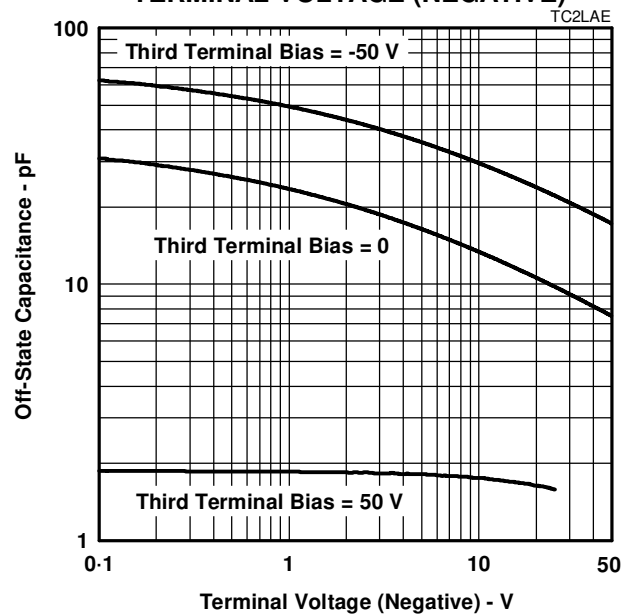


Figure 18.

THERMAL INFORMATION

MAXIMUM NON-RECURRING 50 Hz CURRENT

VS

CURRENT DURATION

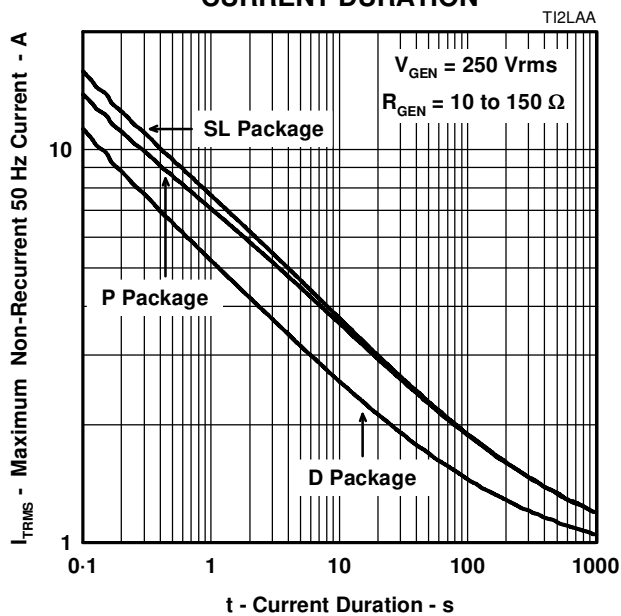


Figure 19.

THERMAL RESPONSE

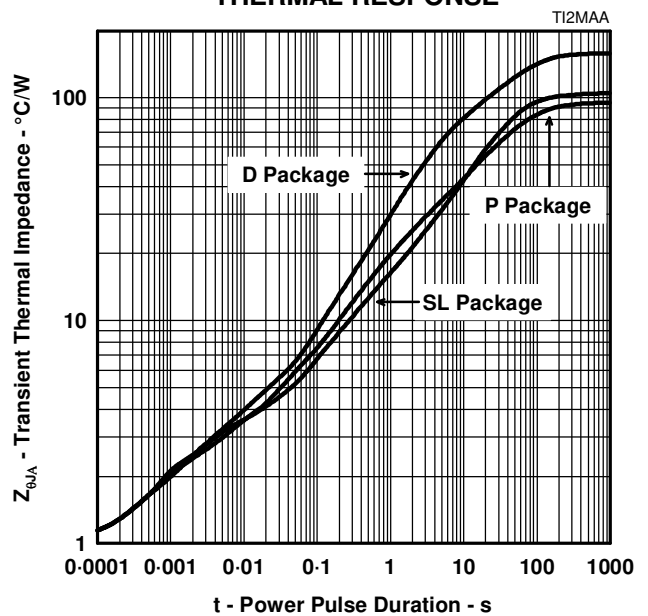


Figure 20.

TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

MARCH 1994 - REVISED SEPTEMBER 1997

APPLICATIONS INFORMATION

electrical characteristics

The electrical characteristics of a TISP are strongly dependent on junction temperature, T_J . Hence a characteristic value will depend on the junction temperature at the instant of measurement. The values given in this data sheet were measured on commercial testers, which generally minimise the temperature rise caused by testing. Application values may be calculated from the parameters' temperature curves, the power dissipated and the thermal response curve (Z_{θ}).

lightning surge

wave shape notation

Most lightning tests, used for equipment verification, specify a unidirectional sawtooth waveform which has an exponential rise and an exponential decay. Wave shapes are classified in terms of peak amplitude (voltage or current), rise time and a decay time to 50% of the maximum amplitude. The notation used for the wave shape is *amplitude, rise time/decay time*. A 50A, 5/310 μ s wave shape would have a peak current value of 50 A, a rise time of 5 μ s and a decay time of 310 μ s. The TISP surge current graph comprehends the wave shapes of commonly used surges.

generators

There are three categories of surge generator type, single wave shape, combination wave shape and circuit defined. Single wave shape generators have essentially the same wave shape for the open circuit voltage and short circuit current (e.g. 10/1000 μ s open circuit voltage and short circuit current). Combination generators have two wave shapes, one for the open circuit voltage and the other for the short circuit current (e.g. 1.2/50 μ s open circuit voltage and 8/20 μ s short circuit current) Circuit specified generators usually equate to a combination generator, although typically only the open circuit voltage waveshape is referenced (e.g. a 10/700 μ s open circuit voltage generator typically produces a 5/310 μ s short circuit current). If the combination or circuit defined generators operate into a finite resistance the wave shape produced is intermediate between the open circuit and short circuit values.

current rating

When the TISP switches into the on-state it has a very low impedance. As a result, although the surge wave shape may be defined in terms of open circuit voltage, it is the current wave shape that must be used to assess the required TISP surge capability. As an example, the CCITT IX K17 1.5 kV, 10/700 μ s surge is changed to a 38 A, 5/310 μ s waveshape when driving into a short circuit. Thus the TISP surge current capability, when directly connected to the generator, will be found for the CCITT IX K17 waveform at 310 μ s on the surge graph and not 700 μ s. Some common short circuit equivalents are tabulated below:

STANDARD	OPEN CIRCUIT VOLTAGE	SHORT CIRCUIT CURRENT
CCITT IX K17	1.5 kV, 10/700 μ s	38 A, 5/310 μ s
CCITT IX K20	1 kV, 10/700 μ s	25 A, 5/310 μ s
RLM88	1.5 kV, 0.5/700 μ s	38 A, 0.2/310 μ s
VDE 0433	2.0 kV, 10/700 μ s	50 A, 5/200 μ s
FTZ R12	2.0 kV, 10/700 μ s	50 A, 5/310 μ s

Any series resistance in the protected equipment will reduce the peak circuit current to less than the generators' short circuit value. A 2 kV open circuit voltage, 50 A short circuit current generator has an effective output impedance of 40 Ω (2000/50). If the equipment has a series resistance of 25 Ω then the surge current requirement of the TISP becomes 31 A (2000/65) and not 50 A.

PRODUCT INFORMATION

APPLICATIONS INFORMATION

protection voltage

The protection voltage, ($V_{(BO)}$), increases under lightning surge conditions due to thyristor regeneration. This increase is dependent on the rate of current rise, di/dt , when the TISP is clamping the voltage in its breakdown region. The $V_{(BO)}$ value under surge conditions can be estimated by multiplying the 50 Hz rate $V_{(BO)}$ (250 V/ms) value by the normalised increase at the surge's di/dt (Figure 7.) . An estimate of the di/dt can be made from the surge generator voltage rate of rise, dv/dt , and the circuit resistance.

As an example, the CCITT IX K17 1.5 kV, 10/700 μ s surge has an average dv/dt of 150 V/ μ s, but, as the rise is exponential, the initial dv/dt is higher, being in the region of 450 V/ μ s. The instantaneous generator output resistance is 25 Ω . If the equipment has an additional series resistance of 20 Ω , the total series resistance becomes 45 Ω . The maximum di/dt then can be estimated as 450/45 = 10 A/ μ s. In practice the measured di/dt and protection voltage increase will be lower due to inductive effects and the finite slope resistance of the TISP breakdown region.

capacitance

off-state capacitance

The off-state capacitance of a TISP is sensitive to junction temperature, T_J , and the bias voltage, comprising of the dc voltage, V_D , and the ac voltage, V_d . All the capacitance values in this data sheet are measured with an ac voltage of 100 mV. The typical 25°C variation of capacitance value with ac bias is shown in Figure 21. When $V_D \gg V_d$ the capacitance value is independent on the value of V_d . The capacitance is essentially constant over the range of normal telecommunication frequencies.

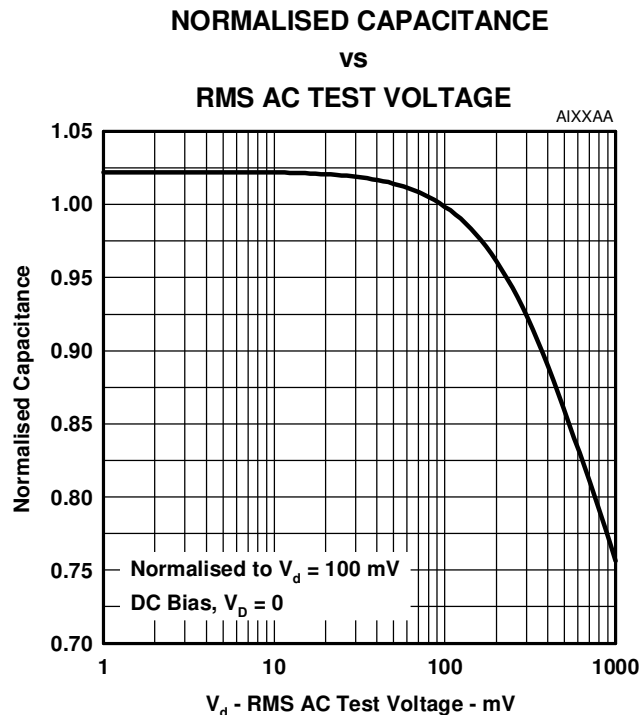


Figure 21.

**TISP2072F3, TISP2082F3
DUAL SYMMETRICAL TRANSIENT
VOLTAGE SUPPRESSORS**

MARCH 1994 - REVISED SEPTEMBER 1997

APPLICATIONS INFORMATION

longitudinal balance

Figure 22 shows a three terminal TISP with its equivalent "delta" capacitance. Each capacitance, C_{TG} , C_{RG} and C_{TR} , is the true terminal pair capacitance measured with a three terminal or guarded capacitance bridge. If wire R is biased at a larger potential than wire T then $C_{TG} > C_{RG}$. Capacitance C_{TG} is equivalent to a capacitance of C_{RG} in parallel with the capacitive difference of $(C_{TG} - C_{RG})$. The line capacitive unbalance is due to $(C_{TG} - C_{RG})$ and the capacitance shunting the line is $C_{TR} + C_{RG}/2$.

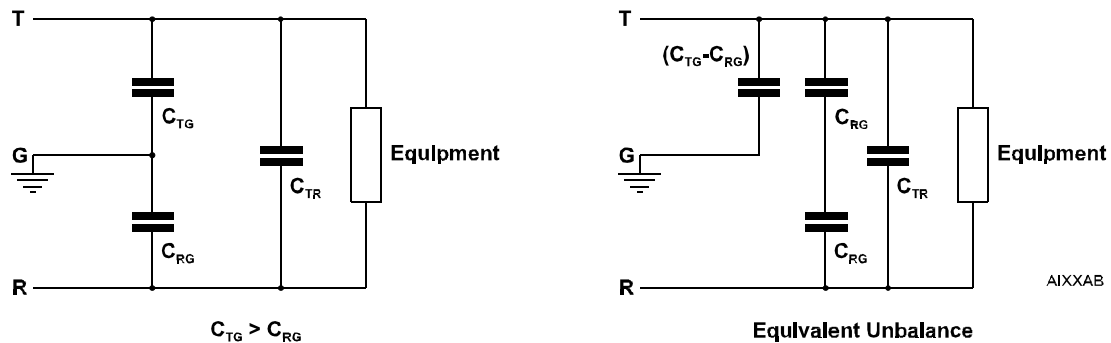


Figure 22.

All capacitance measurements in this data sheet are three terminal guarded to allow the designer to accurately assess capacitive unbalance effects. Simple two terminal capacitance meters (unguarded third terminal) give false readings as the shunt capacitance via the third terminal is included.

PRODUCT INFORMATION

TISP2072F3, TISP2082F3 DUAL SYMMETRICAL TRANSIENT VOLTAGE SUPPRESSORS

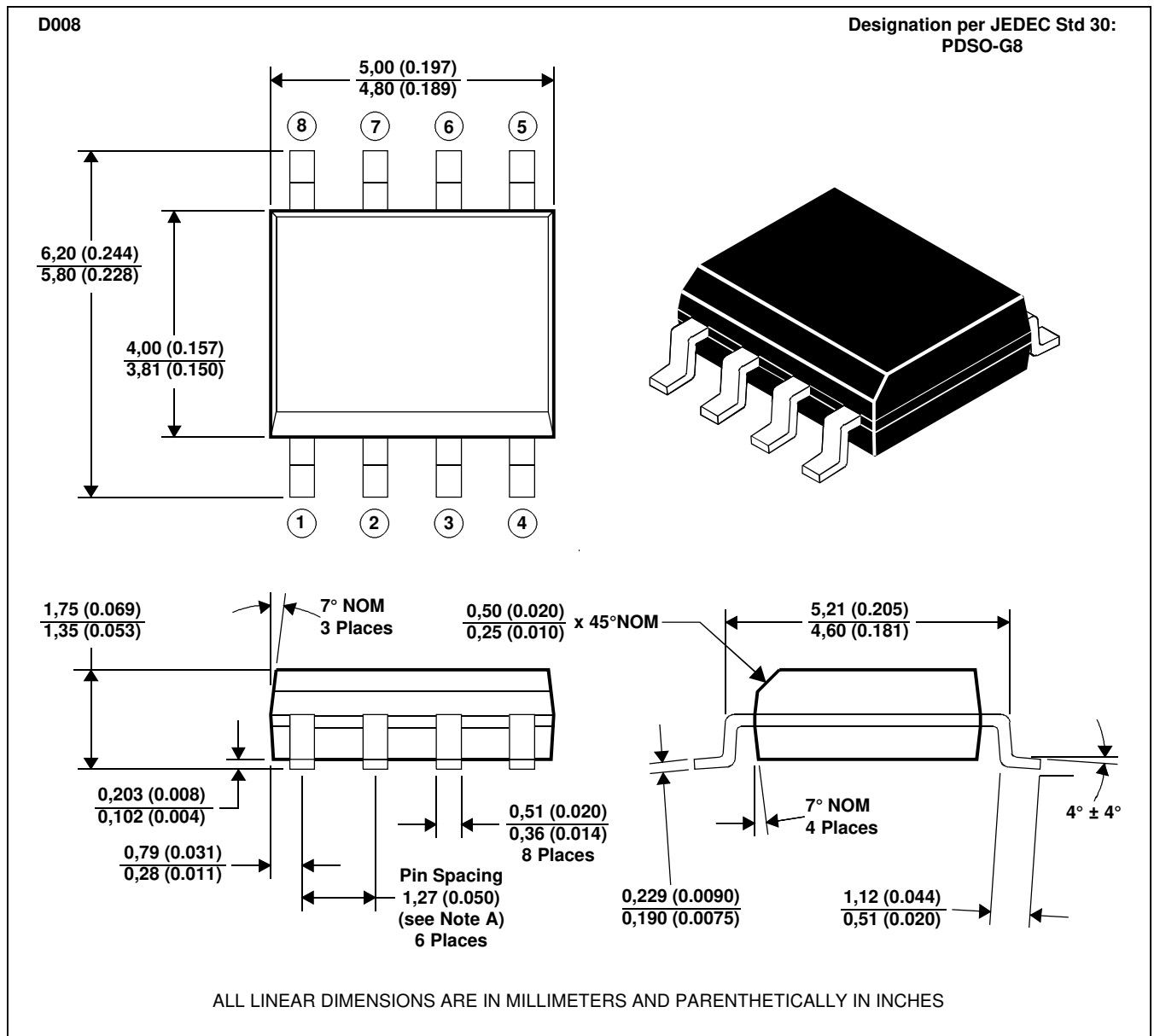
MARCH 1994 - REVISED SEPTEMBER 1997

MECHANICAL DATA

D008

plastic small-outline package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002).

MDXXAA

TISP2072F3, TISP2082F3
DUAL SYMMETRICAL TRANSIENT
VOLTAGE SUPPRESSORS

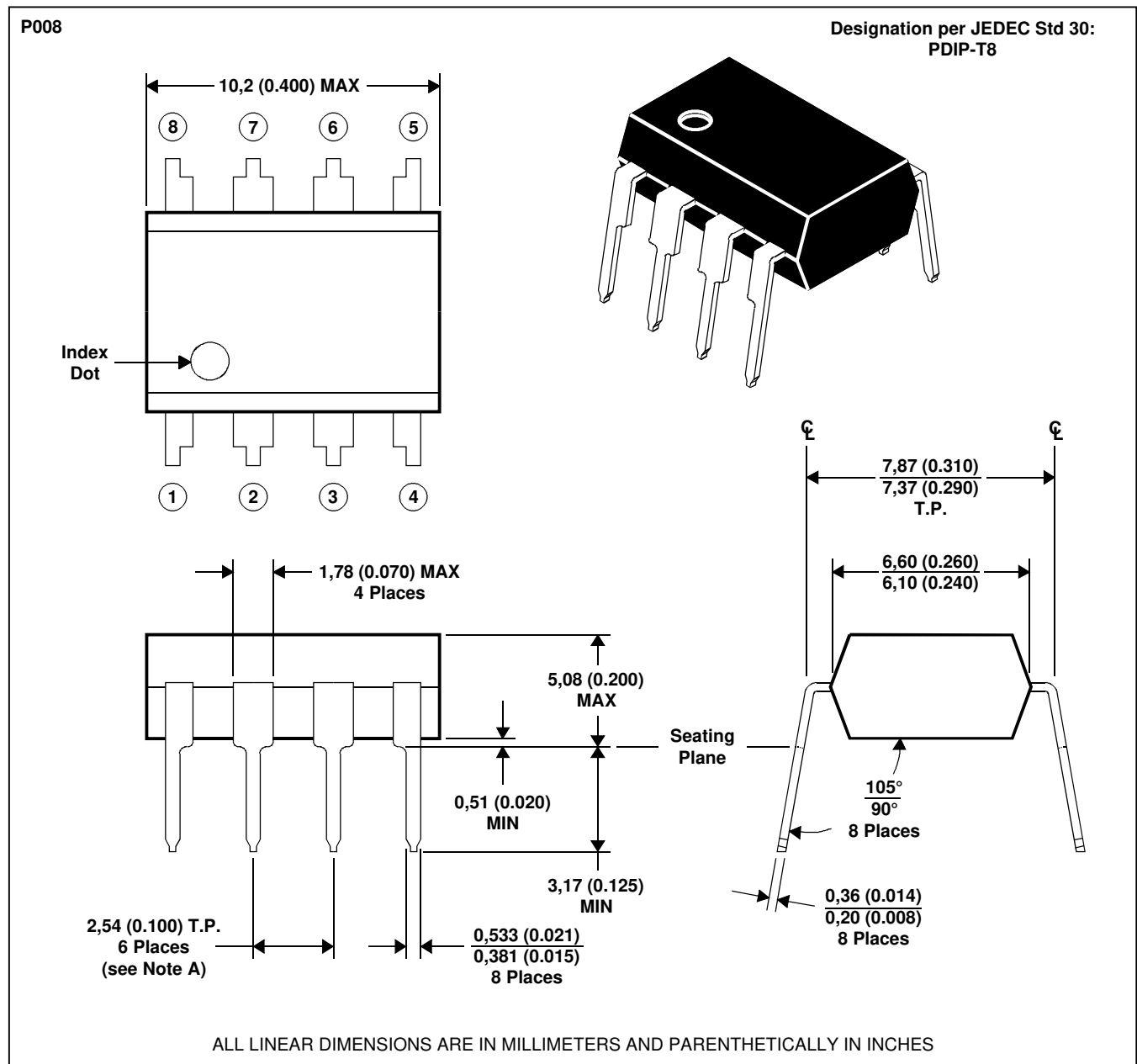
MARCH 1994 - REVISED SEPTEMBER 1997

MECHANICAL DATA

P008

plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position

MDXXABA

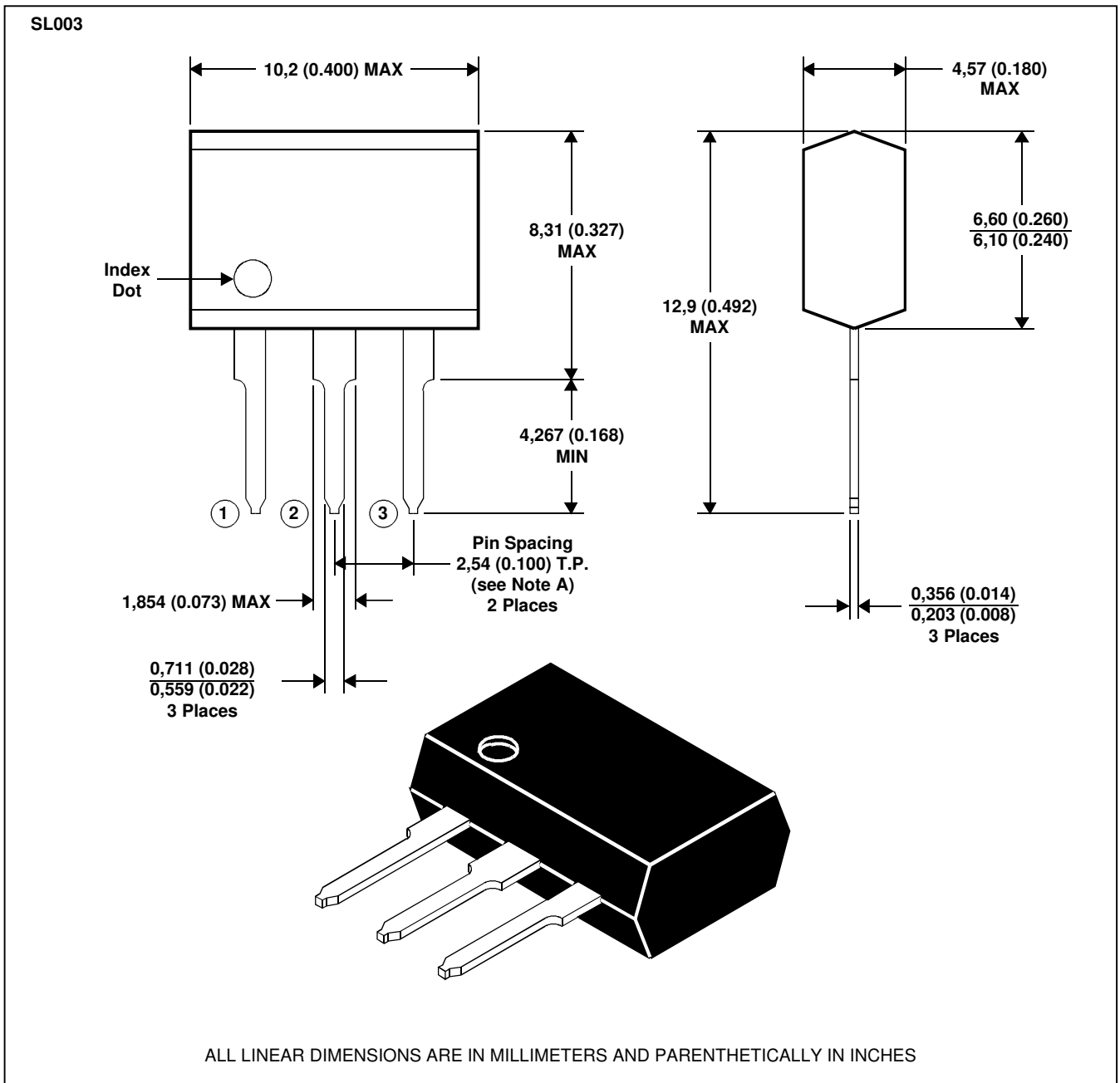
PRODUCT INFORMATION

MECHANICAL DATA

SL003

3-pin plastic single-in-line package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
 B. Body molding flash of up to 0,15 (0.006) may occur in the package lead plane.

MDXXAD

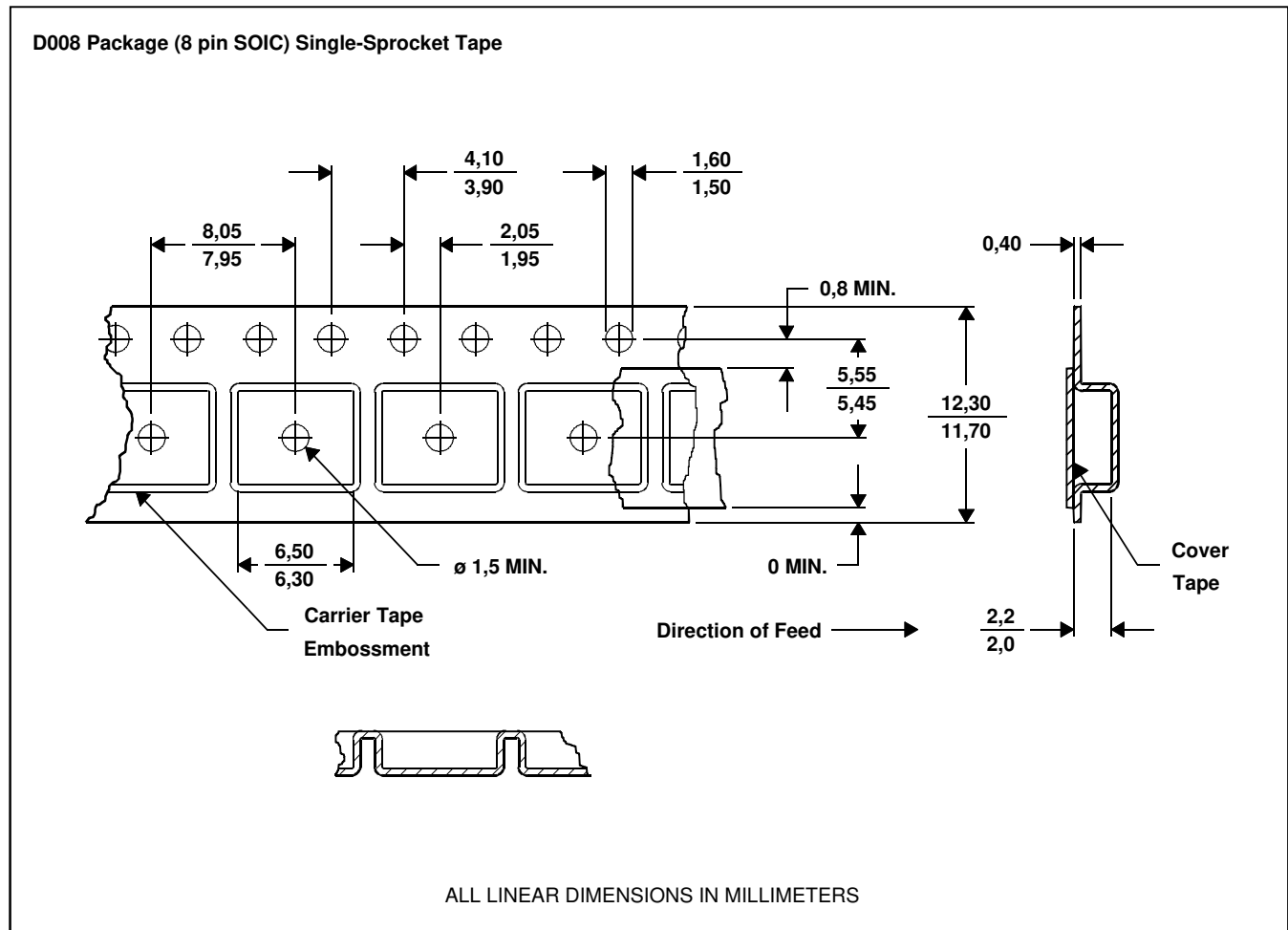
**TISP2072F3, TISP2082F3
DUAL SYMMETRICAL TRANSIENT
VOLTAGE SUPPRESSORS**

MARCH 1994 - REVISED SEPTEMBER 1997

MECHANICAL DATA

D008

tape dimensions



NOTES: A. Taped devices are supplied on a reel of the following dimensions:-

MDXXAT

Reel diameter: 330 +0,0/-4,0 mm
 Reel hub diameter: 100 ±2,0 mm
 Reel axial hole: 13,0 ±0,2 mm

B. 2500 devices are on a reel.

PRODUCT INFORMATION

IMPORTANT NOTICE

Power Innovations Limited (PI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to verify, before placing orders, that the information being relied on is current.

PI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with PI's standard warranty. Testing and other quality control techniques are utilized to the extent PI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except as mandated by government requirements.

PI accepts no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor is any license, either express or implied, granted under any patent right, copyright, design right, or other intellectual property right of PI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

PI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS.

Copyright © 1997, Power Innovations Limited