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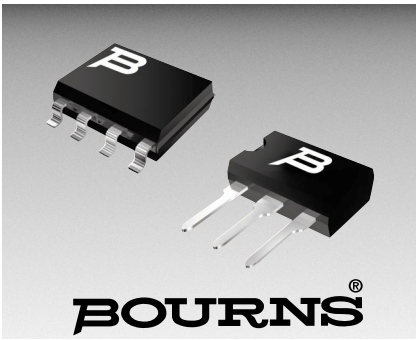
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LOW-VOLTAGE DUAL BIDIRECTIONAL THYRISTOR
OVERVOLTAGE PROTECTORS



TISP30xxF3 (LV) Overvoltage Protector Series

Ion-Implanted Breakdown Region
Precise and Stable Voltage
Low Voltage Overshoot under Surge

DEVICE	V _{DRM} V	V _(BO) V
'3072F3	58	72
'3082F3	66	82

Planar Passivated Junctions
Low Off-State Current <10 μA

Rated for International Surge Wave Shapes

Waveshape	Standard	I _{TSP} A
2/10 μs	GR-1089-CORE	80
8/20 μs	IEC 61000-4-5	70
10/160 μs	FCC Part 68	60
10/700 μs	ITU-T K.20/21 FCC Part 68	50
10/560 μs	FCC Part 68	45
10/1000 μs	GR-1089-CORE	35

 **UL Recognized Component**

Description

These low-voltage dual bidirectional thyristor protectors are designed to protect ISDN applications against transients caused by lightning strikes and a.c. power lines. Offered in two voltage variants to meet battery and protection requirements, they are guaranteed to suppress and withstand the listed international lightning surges in both polarities. Transients are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current prevents d.c. latchup as the current subsides.

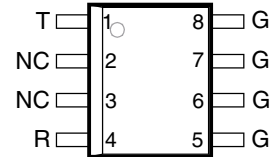
These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation.

How To Order

Device	Package	Carrier	Order As
TISP30xxF3	D, Small-outline	Tape And Reeled	TISP30xxF3DR
	P, Plastic Dip	Tube	TISP30xxF3P
	SL, Single-in-line	Tube	TISP30xxF3SL

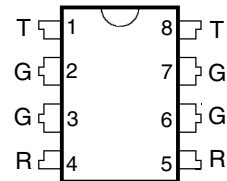
Insert xx value corresponding to protection voltages of 72 and 82

D Package (Top View)



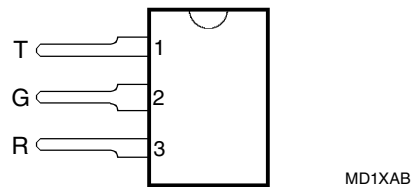
NC - No internal connection

P Package (Top View)

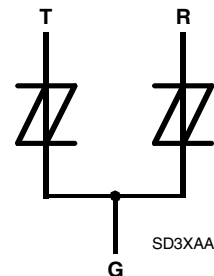


Specified T terminal ratings require connection of pins 1 and 8.
Specified R terminal ratings require connection of pins 4 and 5.

SL Package (Top View)



Device Symbol



Terminals T, R and G correspond to the alternative line designators of A, B and C

TISP30xxF3 (LV) Overvoltage Protector Series



Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, $0\text{ }^\circ\text{C} < T_A < 70\text{ }^\circ\text{C}$	'3072F3 '3082F3	± 58 ± 66	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)	I_{PPSM}	A	1/2 (Gas tube differential transient, 1/2 voltage wave shape)
1/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)			120
2/10 (Telcordia GR-1089-CORE, 2/10 voltage wave shape)			80
1/20 (ITU-T K.22, 1.2/50 voltage wave shape, 25 Ω resistor)			50
8/20 (IEC 61000-4-5, combination wave generator, 1.2/50 voltage wave shape)			70
10/160 (FCC Part 68, 10/160 voltage wave shape)			60
4/250 (ITU-T K.20/21, 10/700 voltage wave shape, simultaneous)			55
0.2/310 (CNET I 31-24, 0.5/700 voltage wave shape)			38
5/310 (ITU-T K.20/21, 10/700 voltage wave shape, single)			50
5/320 (FCC Part 68, 9/720 voltage wave shape, single)			50
10/560 (FCC Part 68, 10/560 voltage wave shape)			45
10/1000 (Telcordia GR-1089-CORE, 10/1000 voltage wave shape)	35		
Non-repetitive peak on-state current, $0\text{ }^\circ\text{C} < T_A < 70\text{ }^\circ\text{C}$ (see Notes 1 and 3) 50 Hz, 1 s	D Package P Package SL Package	4.3 5.7 7.1	A
Initial rate of rise of on-state current, Linear current ramp, Maximum ramp value $< 38\text{ A}$	di_T/dt	250	A/ μs
Junction temperature	T_J	-65 to +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

- NOTES: 1. Further details on surge wave shapes are contained in the Applications Information section.
 2. Initially the TISP[®] must be in thermal equilibrium with $0\text{ }^\circ\text{C} < T_J < 70\text{ }^\circ\text{C}$. The surge may be repeated after the TISP[®] returns to its initial conditions.
 3. Above $70\text{ }^\circ\text{C}$, derate linearly to zero at $150\text{ }^\circ\text{C}$ lead temperature.

Electrical Characteristics for the T and R terminals, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_D = \pm 2V_{DRM}$, $0\text{ }^\circ\text{C} < T_A < 70\text{ }^\circ\text{C}$			± 10	μA
I_D Off-state current	$V_D = \pm 50\text{ V}$			± 10	μA
C_{off} Off-state capacitance	$f = 100\text{ kHz}$, $V_d = 100\text{ mV}$, $V_D = 0$, Third terminal voltage = -50 V to $+50\text{ V}$ (see Notes 4 and 5)	D Package	0.05	0.15	pF
		P Package	0.065	0.2	
		SL Package	0.03	0.1	

- NOTES: 4. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.
 5. Further details on capacitance are given in the Applications Information section.

TISP30xxF3 (LV) Overvoltage Protector Series

BOURNS[®]

Electrical Characteristics for T and G or R and G Terminals, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_D = \pm V_{\text{DRM}}$, $0\text{ }^\circ\text{C} < T_A < 70\text{ }^\circ\text{C}$			± 10	μA
$V_{\text{(BO)}}$ Breakover voltage	$dv/dt = \pm 250\text{ V/ms}$, $R_{\text{SOURCE}} = 300\ \Omega$			± 72 ± 82	V
$V_{\text{(BO)}}$ Impulse breakover voltage	$dv/dt \leq \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $R_{\text{SOURCE}} = 50\ \Omega$		± 86 ± 96		V
$I_{\text{(BO)}}$ Breakover current	$dv/dt = \pm 250\text{ V/ms}$, $R_{\text{SOURCE}} = 300\ \Omega$	± 0.1		± 0.6	A
V_T On-state voltage	$I_T = \pm 5\text{ A}$, $t_W = 100\ \mu\text{s}$			± 3	V
I_H Holding current	$I_T = \pm 5\text{ A}$, $di/dt = -/+30\text{ mA/ms}$	± 0.15			A
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value $< 0.85V_{\text{DRM}}$	± 5			$\text{kV}/\mu\text{s}$
I_D Off-state current	$V_D = \pm 50\text{ V}$			± 10	μA
C_{off} Off-state capacitance	$f = 1\text{ MHz}$, $V_d = 0.1\text{ V r.m.s.}$, $V_D = 0$ $f = 1\text{ MHz}$, $V_d = 0.1\text{ V r.m.s.}$, $V_D = -5\text{ V}$ $f = 1\text{ MHz}$, $V_d = 0.1\text{ V r.m.s.}$, $V_D = -50\text{ V}$ (see Notes 5 and 6)		82 49 25	140 85 40	pF

NOTES: 6. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The third terminal is connected to the guard terminal of the bridge.

7. Further details on capacitance are given in the Applications Information section.

Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta\text{JA}}$ Junction to free air thermal resistance	$P_{\text{tot}} = 0.8\text{ W}$, $T_A = 25\text{ }^\circ\text{C}$ 5 cm^2 , FR4 PCB	D Package		160	$^\circ\text{C}/\text{W}$
		P Package		100	
		SL Package		135	

Parameter Measurement Information

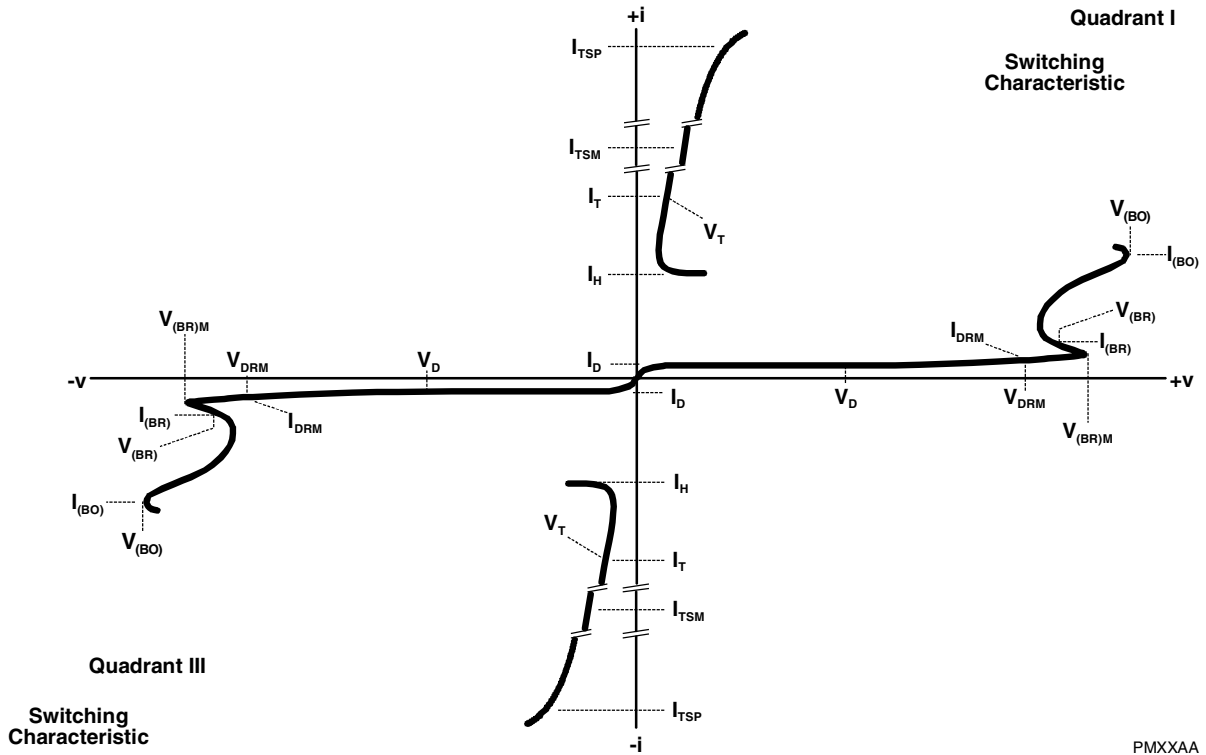


Figure 1. Voltage-Current Characteristics for any Terminal Pair

PMXXAA

Typical Characteristics - R and G or T and G Terminals

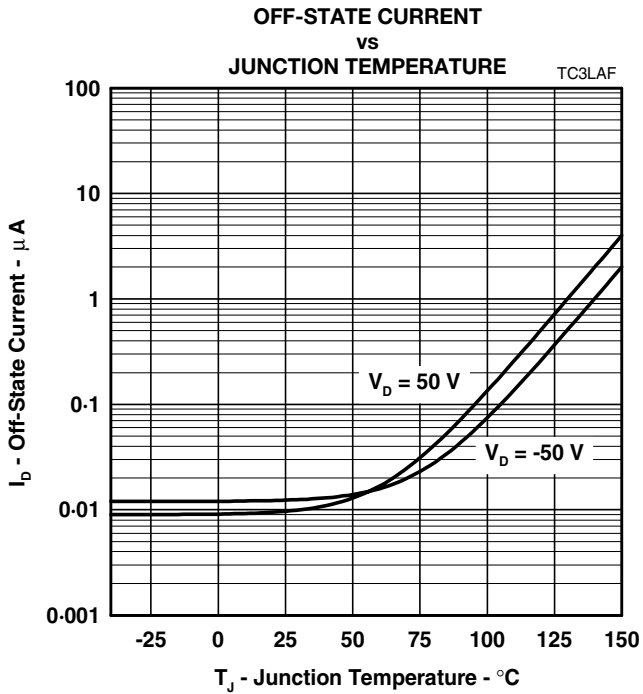


Figure 2.

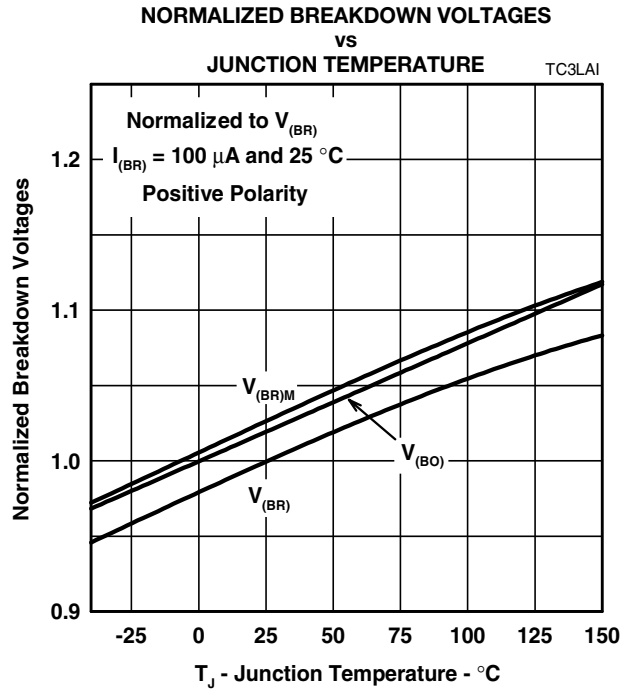


Figure 3.

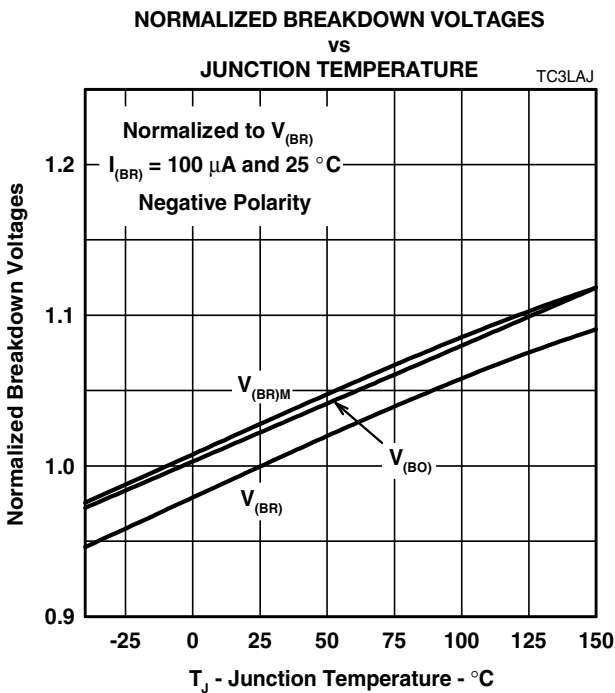


Figure 4.

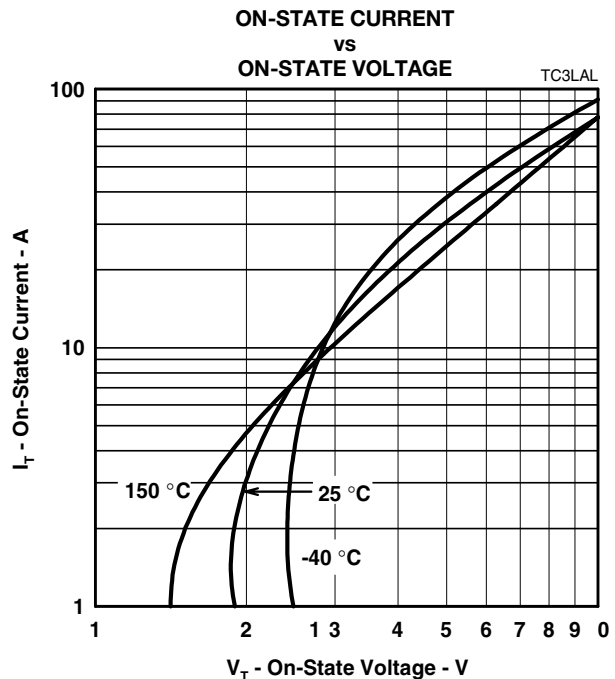


Figure 5.

Typical Characteristics - R and G or T and G Terminals

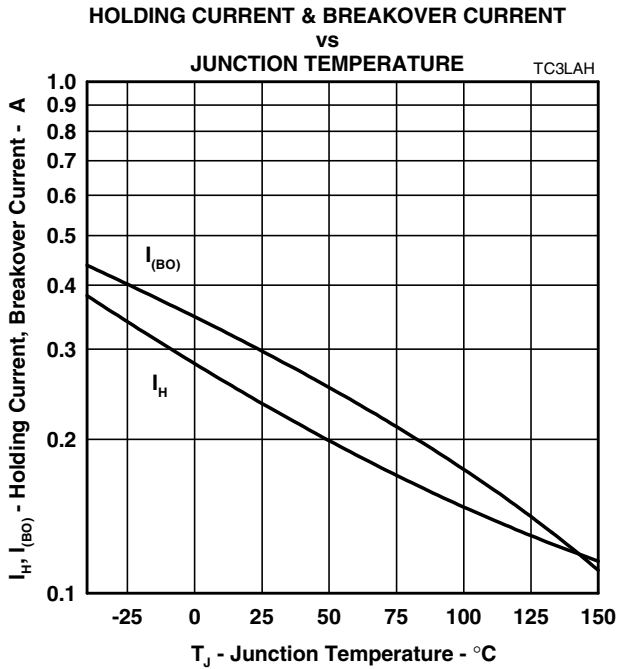


Figure 6.

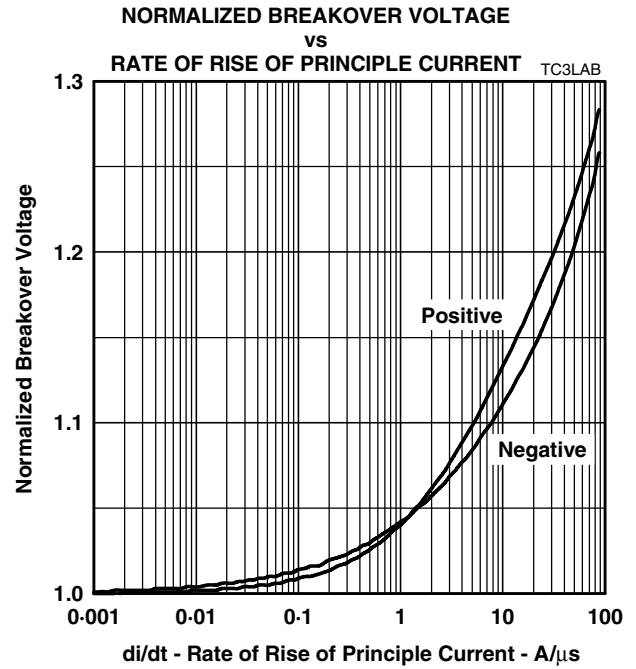


Figure 7.

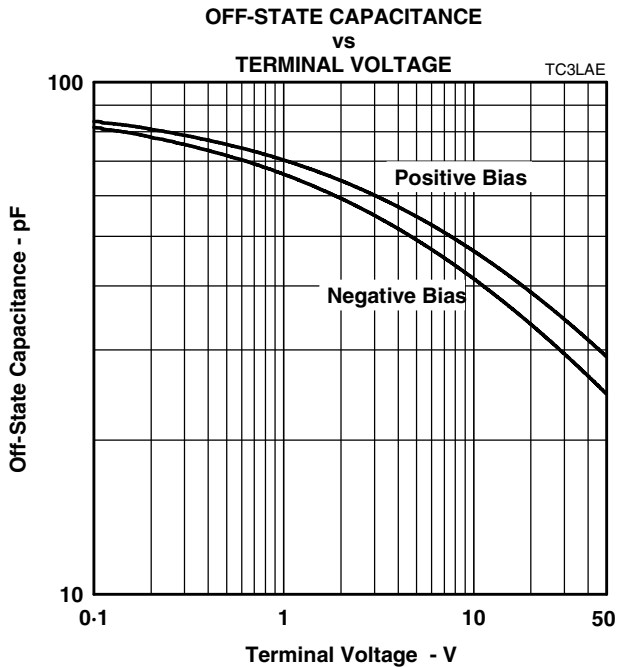


Figure 8.

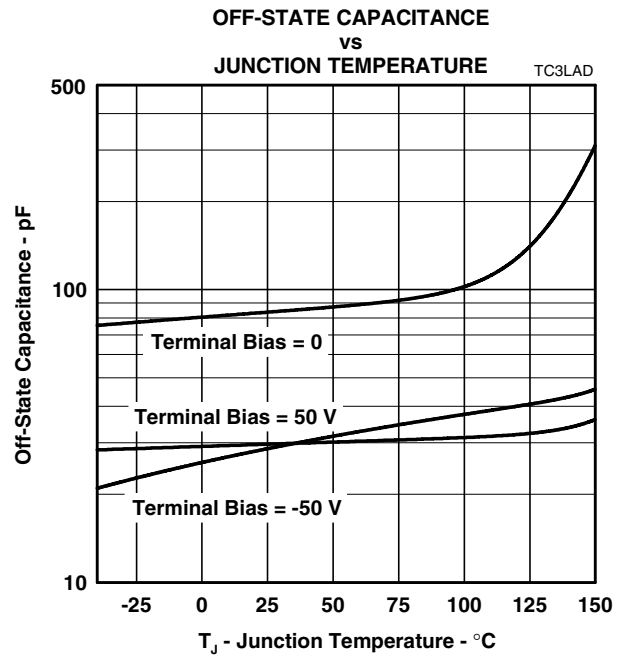


Figure 9.

Typical Characteristics - R and G or T and G Terminals

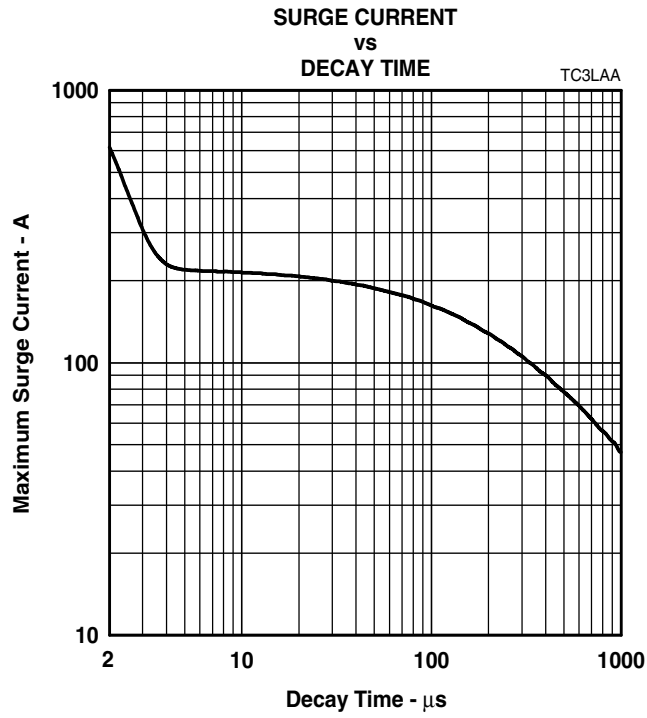


Figure 10.

Typical Characteristics - R and T Terminals

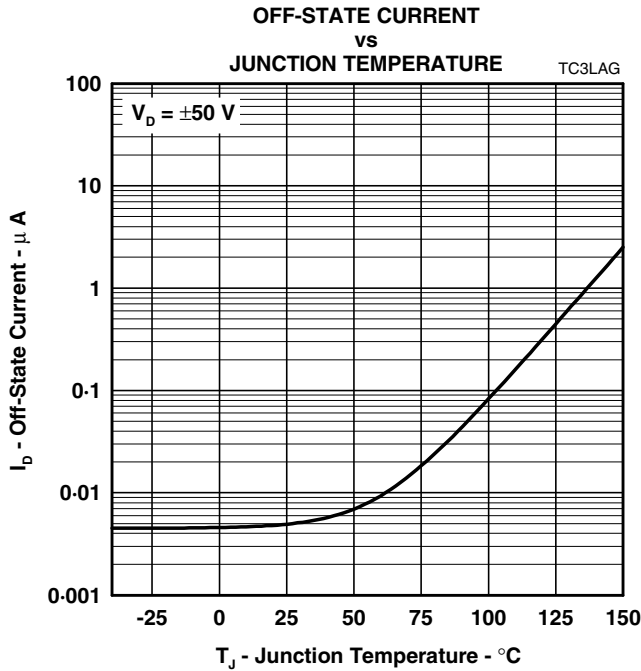


Figure 11.

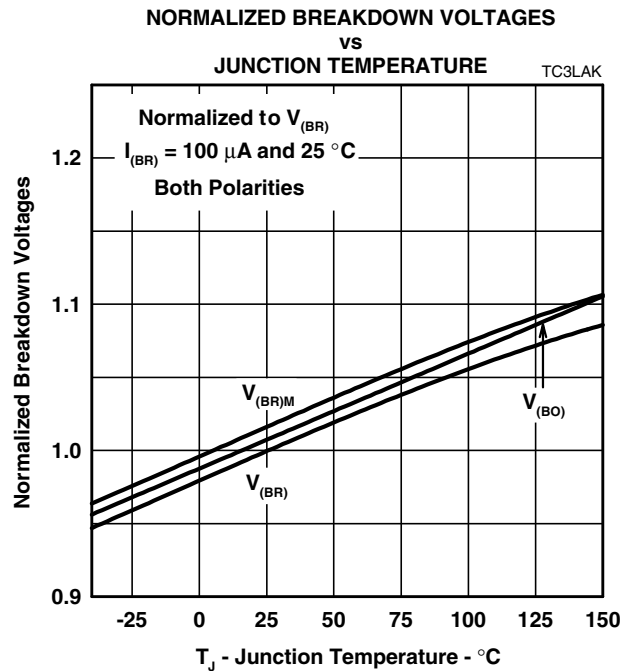


Figure 12.

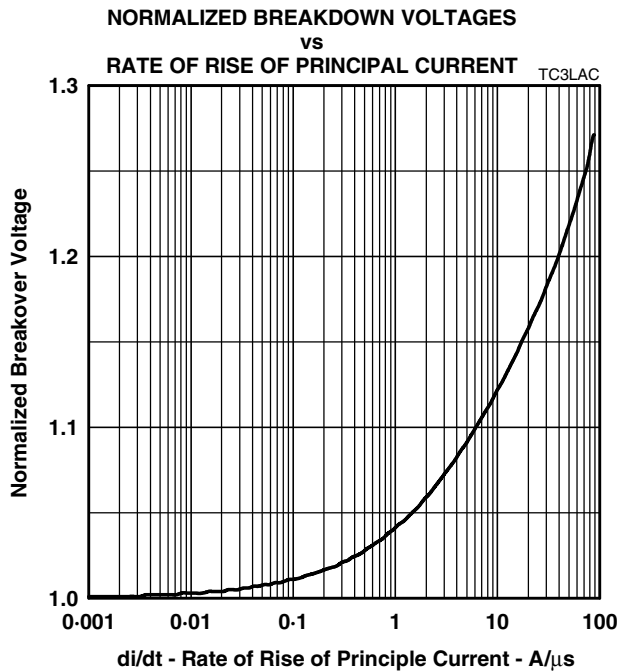


Figure 13.

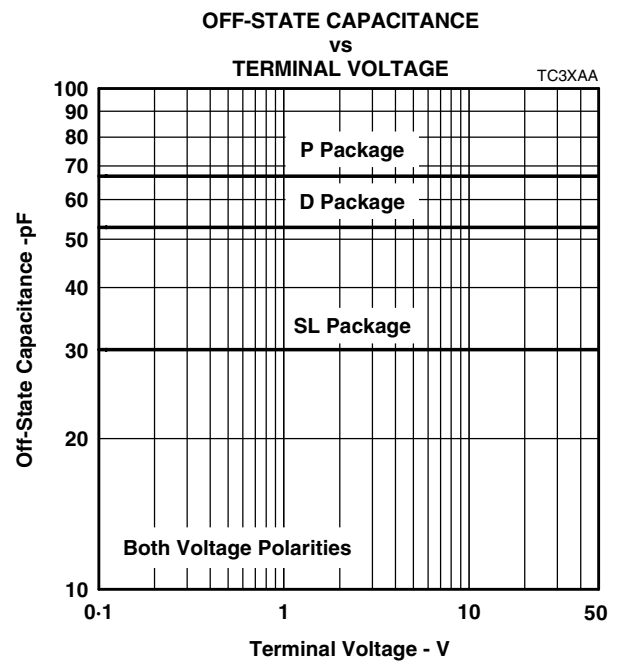
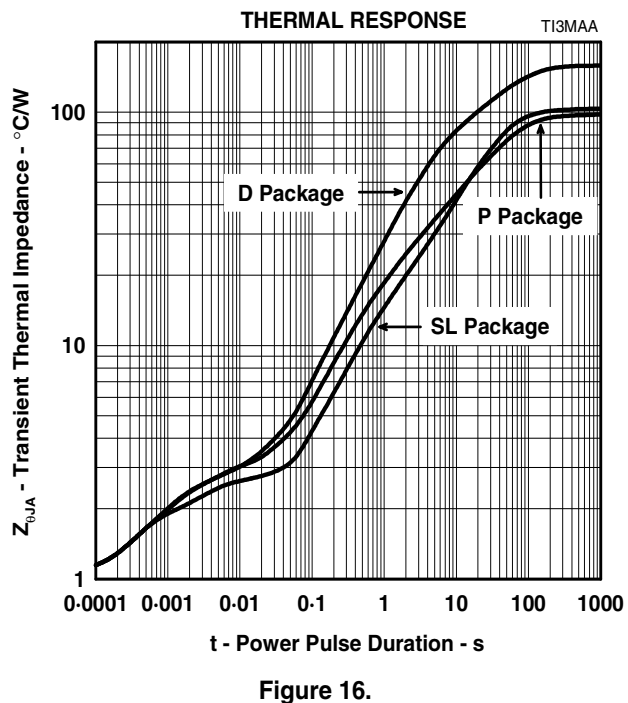
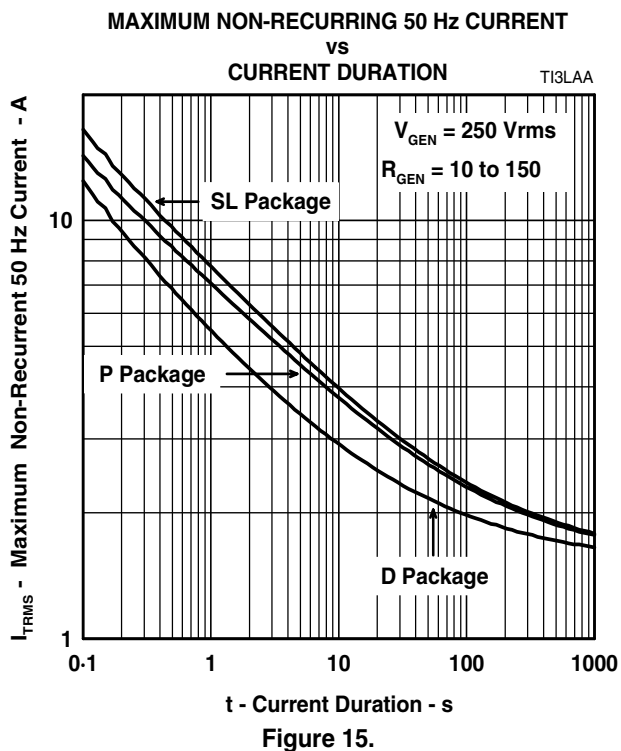


Figure 14.

Thermal Information



APPLICATIONS INFORMATION

Electrical Characteristics

The electrical characteristics of a TISP[®] device are strongly dependent on junction temperature, T_J . Hence, a characteristic value will depend on the junction temperature at the instant of measurement. The values given in this data sheet were measured on commercial testers, which generally minimize the temperature rise caused by testing. Application values may be calculated from the parameters' temperature coefficient, the power dissipated and the thermal response curve, Z_{θ} (see M. J. Maytum, "Transient Suppressor Dynamic Parameters." TI Technical Journal, vol. 6, No. 4, pp.63-70, July-August 1989).

Lightning Surge

Wave Shape Notation

Most lightning tests, used for equipment verification, specify a unidirectional sawtooth waveform which has an exponential rise and an exponential decay. Wave shapes are classified in terms of peak amplitude (voltage or current), rise time and a decay time to 50% of the maximum amplitude. The notation used for the wave shape is *amplitude, rise time/decay time*. A 50 A, 5/310 μ s wave shape would have a peak current value of 50 A, a rise time of 5 μ s and a decay time of 310 μ s. The TISP[®] device surge current graph comprehends the wave shapes of commonly used surges.

Generators

There are three categories of surge generator type, single wave shape, combination wave shape and circuit defined. Single wave shape generators have essentially the same wave shape for the open circuit voltage and short circuit current (e.g., 10/1000 μ s open circuit voltage and short circuit current). Combination generators have two wave shapes, one for the open circuit voltage and the other for the short circuit current (e.g., 1.2/50 μ s open circuit voltage and 8/20 μ s short circuit current). Circuit specified generators usually equate to a combination generator, although typically only the open circuit voltage waveshape is referenced (e.g. a 10/700 μ s open circuit voltage generator typically produces a 5/310 μ s short circuit current). If the combination or circuit defined generators operate into a finite resistance, the wave shape produced is intermediate between the open circuit and short circuit values.

Current Rating

When the TISP[®] device switches into the on-state, it has a very low impedance. As a result, although the surge wave shape may be defined in terms of open circuit voltage, it is the current wave shape that must be used to assess the required TISP[®] surge capability. As an example, the ITU-T K.21 1.5 kV, 10/700 μ s open circuit voltage surge is changed to a 38 A, 5/310 μ s current waveshape when driving into a short circuit. Thus, the TISP[®] surge current capability, when directly connected to the generator, will be found for the ITU-T K.21 waveform at 310 μ s on the surge graph and not 700 μ s. Some common short circuit equivalents are tabulated below:

Standard	Open Circuit Voltage	Short Circuit Current
ITU-T K.21	1.5 kV, 10/700 μ s	37.5 A, 5/310 μ s
ITU-T K.20	1 kV, 10/700 μ s	25 A, 5/310 μ s
IEC 61000-4-5, combination wave generator	1.0 kV, 1.2/50 μ s	500 A, 8/20 μ s
Telcordia GR-1089-CORE	1.0 kV, 10/1000 μ s	100 A, 10/1000 μ s
Telcordia GR-1089-CORE	2.5 kV, 2/10 μ s	500 A, 2/10 μ s
FCC Part 68, Type A	1.5 kV, <10/>160 μ s	200 A, <10/>160 μ s
FCC Part 68, Type A	800 V, <10/>560 μ s	100 A, <10/>160 μ s
FCC Part 68, Type B	1.5 kV, 9/720 μ s	37.5 A, 5/320 μ s

Any series resistance in the protected equipment will reduce the peak circuit current to less than the generators' short circuit value. A 1 kV open circuit voltage, 100 A short circuit current generator has an effective output impedance of 10 Ω (1000/100). If the equipment has a series resistance of 25 Ω , then the surge current requirement of the TISP[®] device becomes 29 A (1000/35) and not 100 A.

APPLICATIONS INFORMATION

Protection Voltage

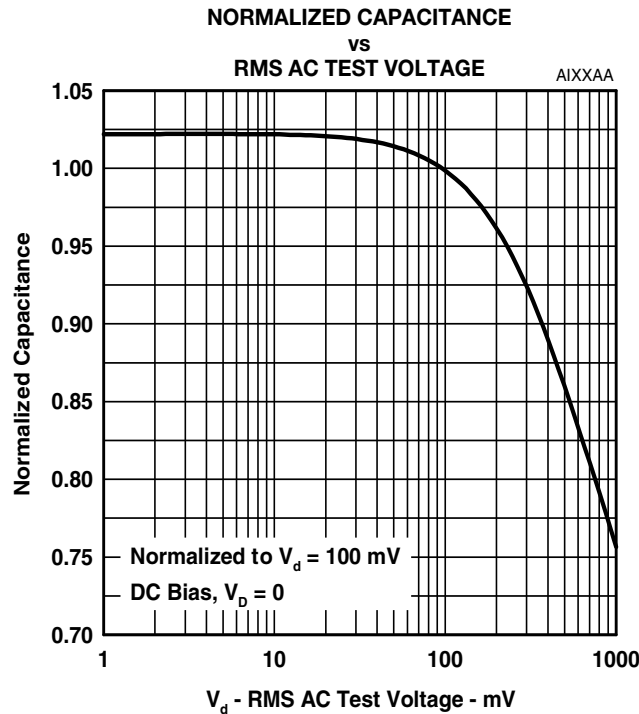
The protection voltage, ($V_{(BO)}$), increases under lightning surge conditions due to thyristor regeneration. This increase is dependent on the rate of current rise, di/dt , when the TISP[®] device is clamping the voltage in its breakdown region. The $V_{(BO)}$ value under surge conditions can be estimated by multiplying the 50 Hz rate $V_{(BO)}$ (250 V/ms) value by the normalized increase at the surge's di/dt (Figure 7). An estimate of the di/dt can be made from the surge generator voltage rate of rise, dv/dt , and the circuit resistance.

As an example, the ITU-T K.21 1.5 kV, 10/700 μ s surge has an average dv/dt of 150 V/ μ s, but, as the rise is exponential, the initial dv/dt is higher, being in the region of 450 V/ μ s. The instantaneous generator output resistance is 25 Ω . If the equipment has an additional series resistance of 20 Ω , the total series resistance becomes 45 Ω . The maximum di/dt then can be estimated as 450/45 = 10 A/ μ s. In practice, the measured di/dt and protection voltage increase will be lower due to inductive effects and the finite slope resistance of the TISP[®] breakdown region.

Capacitance

Off-state Capacitance

The off-state capacitance of a TISP[®] device is sensitive to junction temperature, T_J , and the bias voltage, comprising of the d.c. voltage, V_D , and the a.c. voltage, V_d . All the capacitance values in this data sheet are measured with an a.c. voltage of 100 mV. The typical 25 $^{\circ}$ C variation of capacitance value with a.c. bias is shown in Figure 17. When $V_D \gg V_d$, the capacitance value is independent on the value of V_d . The capacitance is essentially constant over the range of normal telecommunication frequencies.



APPLICATIONS INFORMATION

Longitudinal Balance

Figure 18 shows a three terminal TISP® device with its equivalent “delta” capacitance. Each capacitance, C_{TG} , C_{RG} and C_{TR} , is the true terminal pair capacitance measured with a three terminal or guarded capacitance bridge. If wire R is biased at a larger potential than wire T, then $C_{TG} > C_{RG}$. Capacitance C_{TG} is equivalent to a capacitance of C_{RG} in parallel with the capacitive difference of $(C_{TG} - C_{RG})$. The line capacitive unbalance is due to $(C_{TG} - C_{RG})$ and the capacitance shunting the line is $C_{TR} + C_{RG}/2$.

All capacitance measurements in this data sheet are three terminal guarded to allow the designer to accurately assess capacitive unbalance effects. Simple two terminal capacitance meters (unguarded third terminal) give false readings as the shunt capacitance via the third terminal is included.

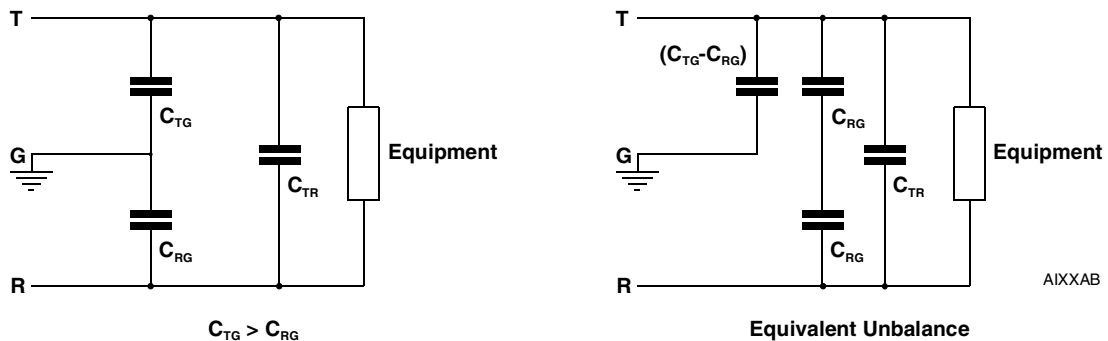
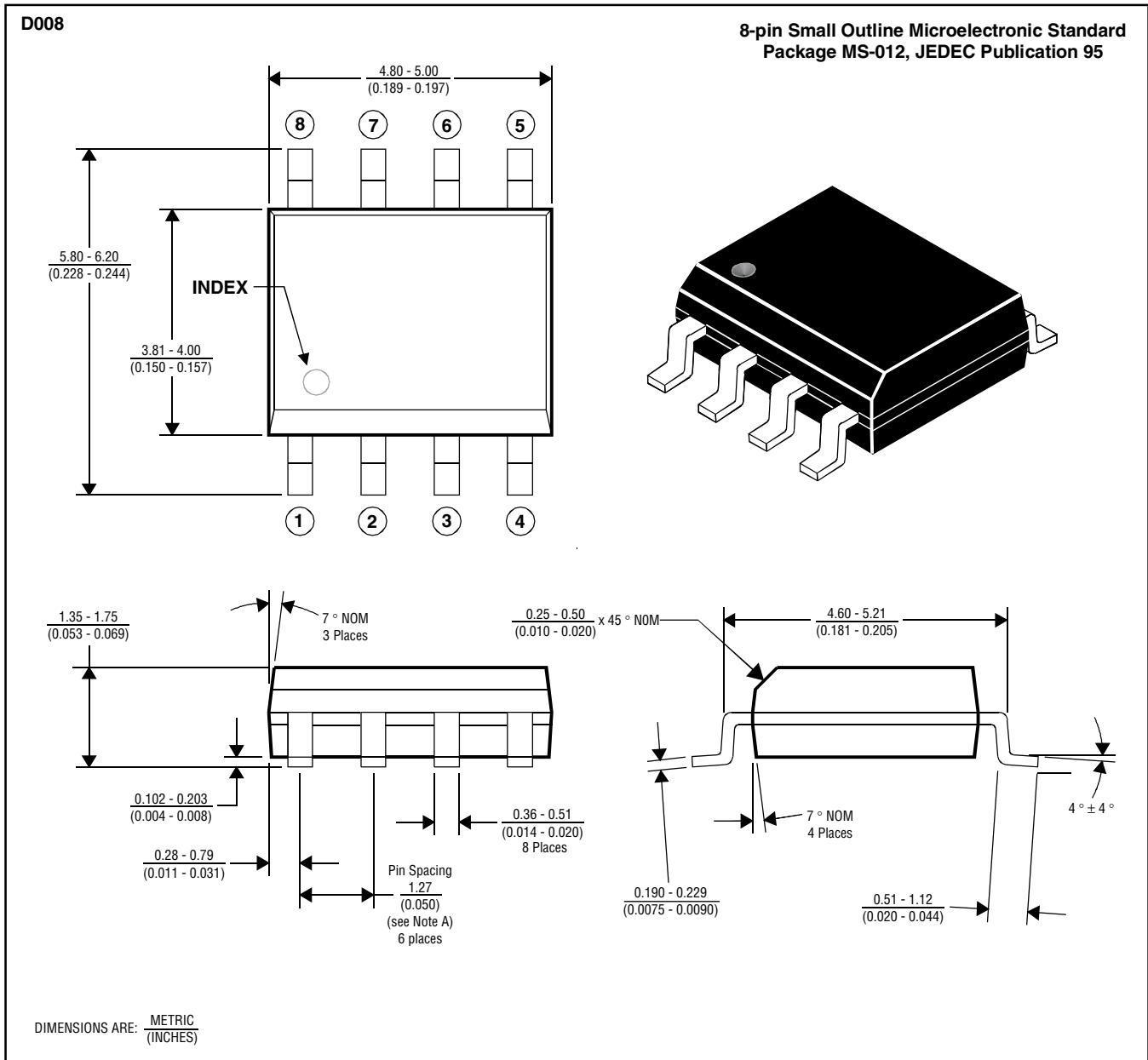


Figure 18.

MECHANICAL DATA

D008 Plastic Small-outline Package

This small-outline package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

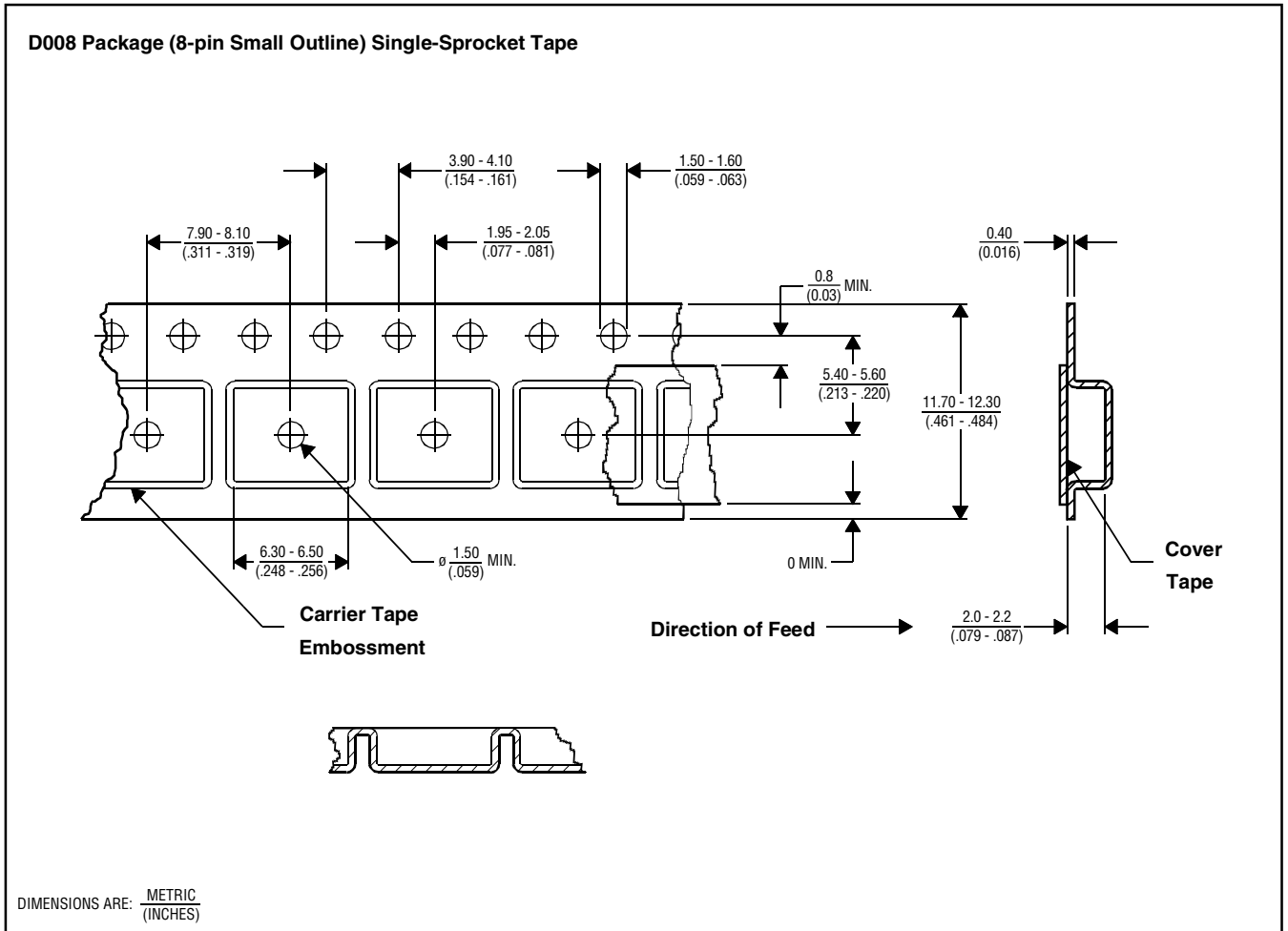


- NOTES: A. Leads are within 0.25 (0.010) radius of true position at maximum material condition.
 B. Body dimensions do not include mold flash or protrusion.
 C. Mold flash or protrusion shall not exceed 0.15 (0.006).
 D. Lead tips to be planar within ±0.051 (0.002).

MDXXAAC

MECHANICAL DATA

D008 Tape Dimensions



NOTES: A. Taped devices are supplied on a reel of the following dimensions:-

MDXXATB

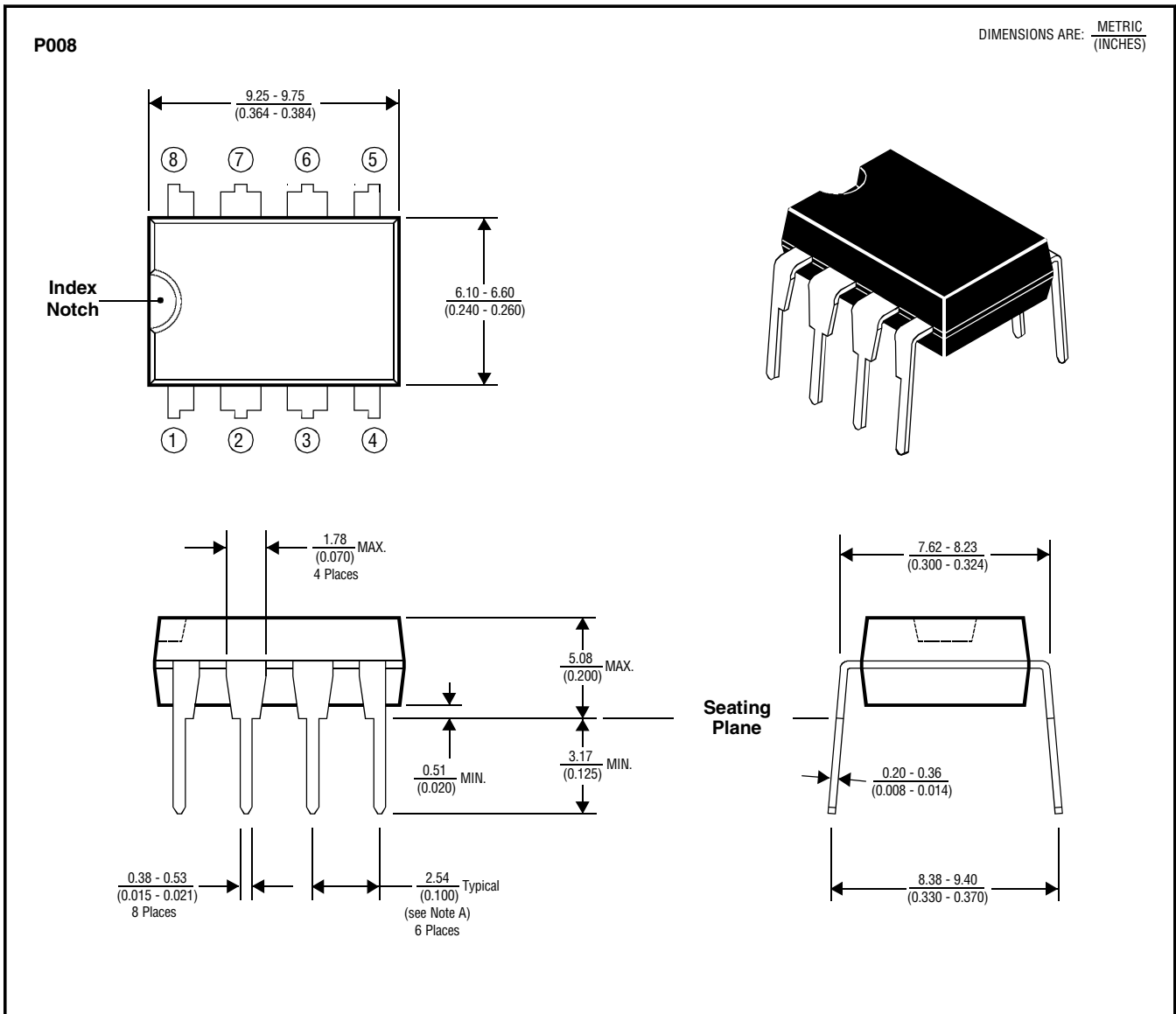
Reel diameter:	$\frac{330 \pm 0.0/-4.0}{(12.992 \pm 0.0/-1.57)}$
Reel hub diameter:	$\frac{100 \pm 2.0}{(3.937 \pm .079)}$
Reel axial hole:	$\frac{13.0 \pm 0.2}{(.512 \pm .008)}$

B. 2500 devices are on a reel.

MECHANICAL DATA

D008 Plastic Dual-in-Line Package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. The package is intended for insertion in mounting-hole rows on 7.62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



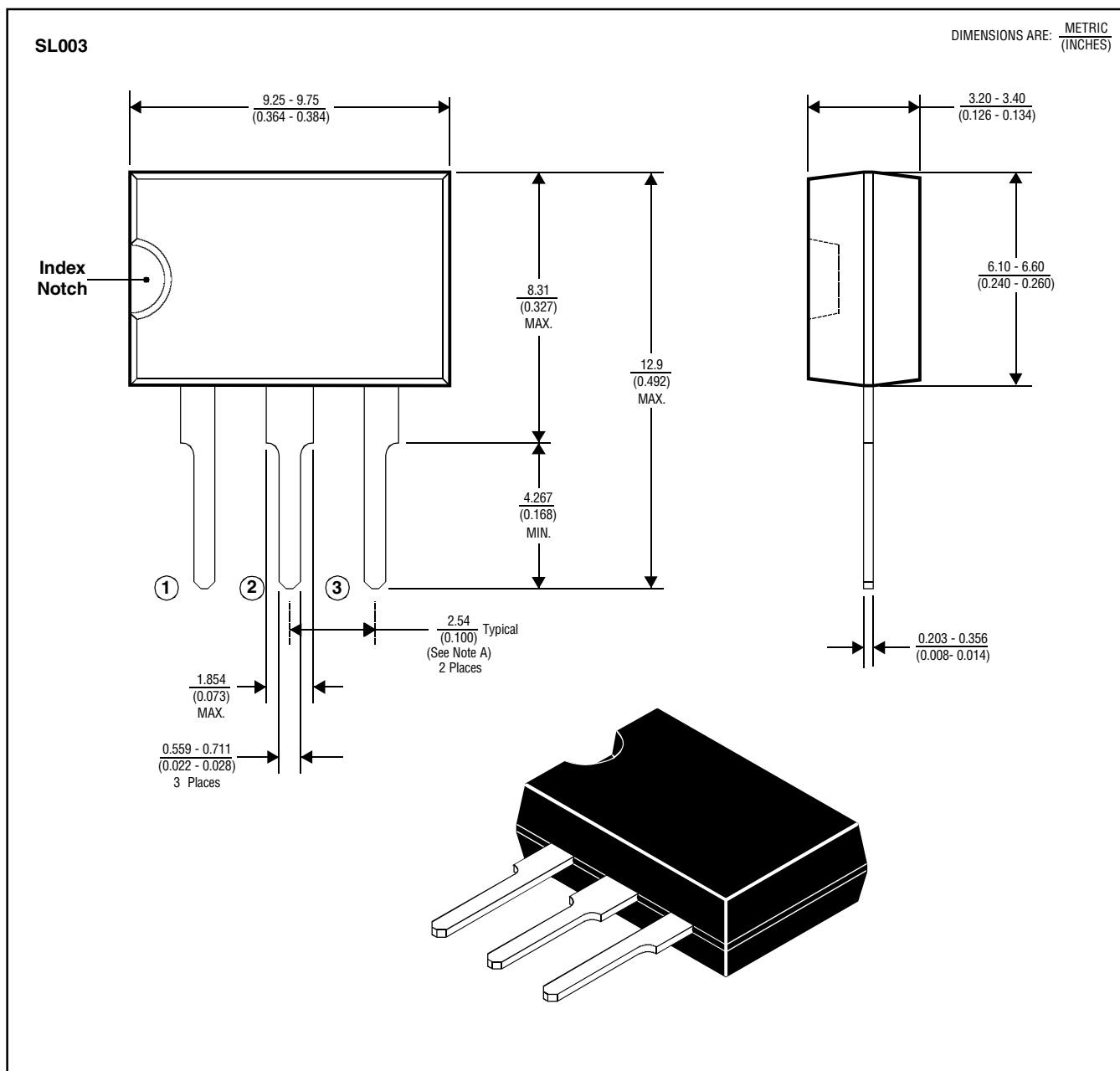
- NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
 B. Dimensions fall within JEDEC MS001 - R-PDIP-T, 0.300" Dual-In-Line Plastic Family.

MDXXCF

MECHANICAL DATA

SL003 3-pin Plastic Single-In-Line Package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.
 B. Body molding flash of up to 0.15 (0.006) may occur in the package lead plane.

MDXXCE