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TJA1086G

FlexRay active star coupler

Rev. 1 — 13 July 2017 Product data sheet

1. General description

The TJA1086G is a FlexRay active star coupler that connects two branches of a FlexRay network. The TJA1086G is compliant with the FlexRay electrical physical layer specification V3.0.1/ISO17458-4 (see Ref. 1 and Ref. 2).

Several TJA1085G and TJA1086G devices can be connected via their TRXD0/1 interfaces to increase the number of branches in the network. A dedicated Communication Controller (CC) interface allows for integration into an ECU. The TJA1086G supports low-power management by offering bus wake-up capability along with battery supply and voltage regulator control. The TJA1086G meets industry standards for EMC/ESD performance and provides enhanced bus error detection, low current consumption and unmatched asymmetric delay performance.

2. Features and benefits

2.1 General

- Compliant with FlexRay Electrical Physical Layer specification V3.0.1/ISO17458-4
- Automotive product qualification in accordance with AEC-Q100
- Data transfer rates from 2.5 Mbit/s to 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential voltage
- Low-power management for battery-supplied ECUs
- Very low current consumption in AS_Sleep mode
- Leadless HVQFN44 package with improved Automated Optical Inspection (AOI) capability

2.2 Functional

- Supports autonomous active star operation independent of the host ensuring the TJA1086G remains active even if the host fails or is switched off
- Branches can be independently configured
- Branch extension via TRXD0/1 inner star interface
- 16-bit bidirectional SPI interface up to 2 Mbit/s for host communication
- Full host control over branch status
- Enhanced wake-up capability:
  - Remote wake-up via wake-up pattern and dedicated FlexRay data frames
  - Local wake-up via pin LWU
  - Wake-up source recognition
  - configurable per branch
- Enhanced supply voltage monitoring on V_{IO}, V_{CC}, V_{BUF} and V_{BAT}

- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Can be used in 14 V, 24 V and 48 V powered systems
- Enhanced bus error detection - detects short-circuit conditions on the bus
- Instant transmitter shut-down interface (BGE pin)
- Selective branch shut-down (partial networking)

2.3 Robustness

- Bus pins protected against ±8 kV ESD pulses according to HBM and ±6 kV ESD pulses according to IEC61000-4-2
- All pins protected against ±1000 V ESD according to CDM
- All pins protected against ±200 V ESD according to MM
- No reverse currents from the digital input pins to V_{IO} or V_{CC} when the TJA1086G is not powered up
- Bus pins short-circuit proof to battery voltage (14 V, 24 V or 48 V) and ground
- Overtemperature detection and protection
- Bus pins protected against transients in automotive environment (according to ISO 7637 class C)

2.4 Active star functional classes

- Active star - communication controller interface
- Active star - bus guardian interface
- Active star - voltage regulator control
- Active star - logic level adaptation
- Active star - host interface
- Active star - increased voltage amplitude transmitter

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	-	5.25	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	V_{CC1}/V_{CC2} connected on pcb	4.45	-	4.715	V
I_{CC}	supply current	AS_Normal mode; $V_{BGE} = V_{IO}$; $V_{TXEN} = 0$ V; $R_{bus} = 45\ \Omega$	-	95	120	mA
V_{BAT}	battery supply voltage		4.75	-	60	V
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}		4.45	-	4.715	V
I_{BAT}	battery supply current	AS_Sleep mode; wake-up enabled on all branches; $T_{vj} \leq 85$ °C	-	38	70	µA
		normal power modes	-	0.1	1	mA
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.25	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.55	-	2.765	V
I_{IO}	supply current on pin V_{IO}	normal power modes	-	-	1	mA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins BP and BM to ground	–6	-	+6	kV

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1086GHN	HVQFN44	plastic thermal enhanced very thin quad flat package; no leads; 44 terminals; body 9 × 9 × 0.85 mm	SOT1113-1

5. Block diagram

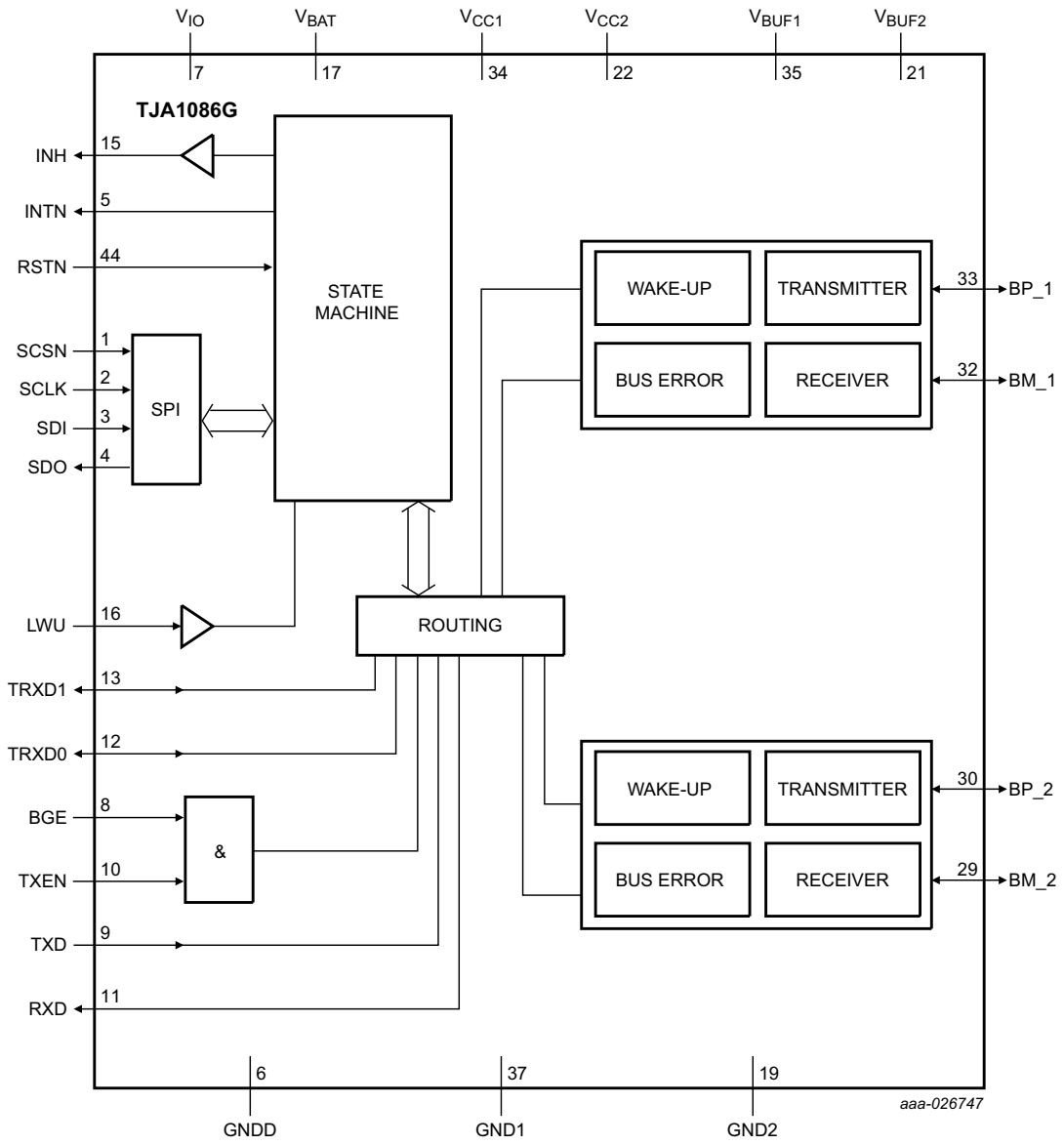
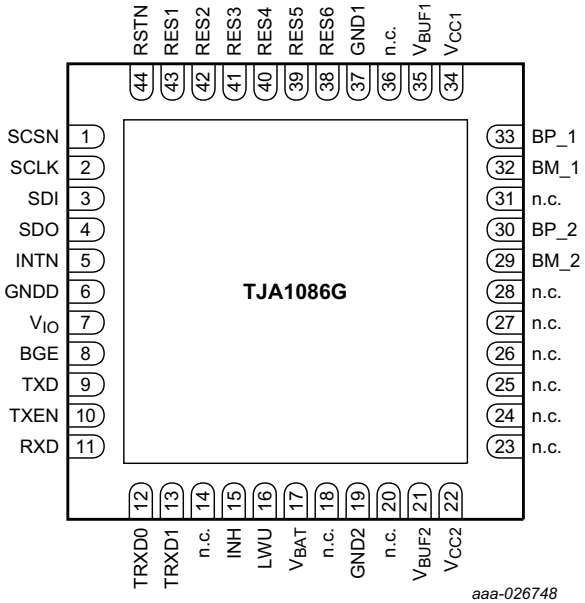


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
SCSN	1	I	SPI chip select input; internal pull-up
SCLK	2	I	SPI clock signal; internal pull-down
SDI	3	I	SPI data input; internal pull-down
SDO	4	O	SPI data output; 3-state output
INTN	5	O	interrupt output; open-drain output, low-side driver
GNDD	6	G	ground for digital circuits[2]
V_{IO}	7	P	supply voltage for V_{IO} voltage level adaptation
BGE	8	I	bus guardian enable input; internal pull-down
TXD	9	I	transmit data input; internal pull-down
TXEN	10	I	transmitter enable input; internal pull-up
RXD	11	O	receive data output
TRXD0	12	IO	data bus line 0 for inner star connection
TRXD1	13	IO	data bus line 1 for inner star connection
n.c.	14	-	not connected; to be connected to GND in application
INH	15	O	inhibit output; for switching external voltage regulator

Table 3. Pin description *...continued*

Symbol	Pin	Type[1]	Description
LWU	16	I	local wake-up input; internal pull-up or pull-down (depends on voltage at pin LWU)
V_{BAT}	17	P	battery supply voltage
n.c.	18	-	not connected; to be connected to GND in application
GND2	19	G	ground connection 2[2]
n.c.	20	-	not connected; to be connected to GND in application
V_{BUF2}	21	P	buffer supply voltage 2[3]
V_{CC2}	22	P	supply voltage 2[4]
n.c.	23	-	not connected; to be left open in the application
n.c.	24	-	not connected; to be left open in the application
n.c.	25	-	not connected; to be connected to GND in application
n.c.	26	-	not connected; to be left open in the application
n.c.	27	-	not connected; to be left open in the application
n.c.	28	-	not connected; to be connected to GND in application
BM_2	29	IO	bus line minus for branch 2[5]
BP_2	30	IO	bus line plus for branch 2[6]
n.c.	31	-	not connected; to be connected to GND in application
BM_1	32	IO	bus line minus for branch 1[5]
BP_1	33	IO	bus line plus for branch 1[6]
V_{CC1}	34	P	supply voltage 1[4]
V_{BUF1}	35	P	buffer supply voltage 1[3]
n.c.	36	-	not connected; to be connected to GND in application
GND1	37	G	ground connection 1[2]
RES6	38	-	reserved; to be connected to GND in application
RES5	39	-	reserved; to be connected to GND in application
RES4	40	-	reserved; to be connected to GND in application
RES3	41	-	reserved; to be connected to GND in application
RES2	42	-	reserved; to be connected to GND in application
RES1	43	-	reserved; to be connected to GND in application
RSTN	44	I	reset input; internal pull-up

[1] IO: input/output; O: output; I: input; P: power supply; G: ground.

[2] GND1, GND2, GNDD and the exposed center pad of HVQFN44 package must be connected together on the PCB; references in the data sheet to GND can be assumed to encompass GND1, GND2, GNDD and the exposed center pad of HVQFN4 unless stated otherwise.

[3] V_{BUF1} and V_{BUF2} must be connected together on the PCB; note that references in the data sheet to V_{BUF} can be assumed to encompass V_{BUF1} and V_{BUF2} unless stated otherwise.

[4] V_{CC1} and V_{CC2} must be connected together on the PCB; note that references in the data sheet to V_{CC} can be assumed to encompass V_{CC1} and V_{CC2} unless stated otherwise.

[5] References in the data sheet to BM (e.g. pin BM or V_{BM}) can be assumed to encompass BM_1 and BM_2 unless stated otherwise.

[6] References in the data sheet to BP (e.g. pin BP or V_{BP}) can be assumed to encompass BP_1 and BP_2 unless stated otherwise.

7. Functional description

7.1 Supply voltage

The TJA1086G state machine is adequately supplied if at least one of V_{BAT}, V_{CC} or V_{BUF} is available. The internal supply voltage to the state machine is denoted by V_{DIG}. V_{BUF} is an auxiliary supply and is only needed for forwarding the wake-up pattern when V_{CC} is not available.

7.2 Host Control (HC) and Autonomous Power (AP) modes - APM flag

The APM flag determines whether the TJA1086G is host-controlled or is operating in Autonomous Power mode. It is in AP mode by default.

The TJA1086G sets the APM flag:

- at power-on
- when a wake-up event is detected (on TXRD0/1, local or remote)
- when a V_{CC} undervoltage event is detected in AS_Normal mode
- when a V_{IO} undervoltage event lasts longer than $t_{to(uvd)(VIO)}$

The host can set or reset the APM flag at any time.

7.3 Signal router

The signal router transfers data received on an input channel to all channels configured as outputs. If data is being received on more than one input channel at the same time, the channel that was first to signal activity is selected and data on the other channel/s is ignored. Whether or not the data on an output channel is transmitted depends on whether the output channel is enabled or disabled.

The TJA1086G contains the following data input channels:

- Branches 1 and 2
- TRXD0/1 interface (inner star interface)
- TXD/TXEN interface

The TJA1086G contains the following data output channels:

- Branches 1 and 2
- TRXD0/1 interface
- RXD pin

7.3.1 TRXD collision

When the TRXD0/1 interface is configured as an output channel, a TRXD collision is detected (COLL_TRXD = 1) if pins TRXD0 and TRXD1 are both LOW for longer than $t_{det(col)(TRXD)}$, generating a CLAMP_ERROR interrupt.

When a TRXD collision is detected, the TJA1086G transmits a DATA_0 to all other active output channels (irrespective of the actual data on the selected input channel), until the selected input channel detects idle state.

7.4 Wake-up

The TJA1086G supports the following wake-up mechanisms:

- Remote wake-up via the bus (wake-up pattern or dedicated wake-up frame)
- Local wake-up via pin LWU
- Activity on the inner star interface (pins TRXD0 and TRXD1)

Any wake-up event will generate a WU interrupt. A remote wake-up on a branch will generate an EVENT_BRx interrupt to indicate the branch where the wake-up pattern or dedicated data frame was detected.

The host can identify the wake-up source by polling the General Status register (WU_TRXD = 1 for a TRXD0/1 wake-up; WU_LOCAL = 1 for a local wake-up) and the Branch Status register (WU_BRx = 1 for a remote wake-up).

7.4.1 Remote wake-up

When the TJA1086G is in AS_Standby or AS_Sleep, both branches are monitored for wake-up events. When a valid wake-up pattern or data frame is detected on one of the branches, the relevant WU_BRx status bit is set and the wake-up pattern/data frame is forwarded to the other branch (if enabled).

A remote wake-up event occurring during an AS_Normal-to-AS_Standby or AS_Normal-to-AS_Sleep transition will also be detected, setting the relevant WU_BRx status bit and generating WU and EVENT_BRx interrupts.

7.4.1.1 Bus wake-up via wake-up pattern

A wake-up pattern consists of at least two consecutive wake-up symbols. A wake-up symbol consists of a DATA_0 phase lasting longer than $t_{det(wake)DATA\_0}$, followed by an idle phase lasting longer than $t_{det(wake)idle}$, provided both wake-up symbols occur within a time span of $t_{det(wake)tot}$ (see Figure 3). The transceiver also wakes up if the idle phases are replaced by DATA_1 phases.

A wake-up event is not detected if an invalid wake-up pattern is received. See Ref. 1 for more details on invalid wake-up patterns.

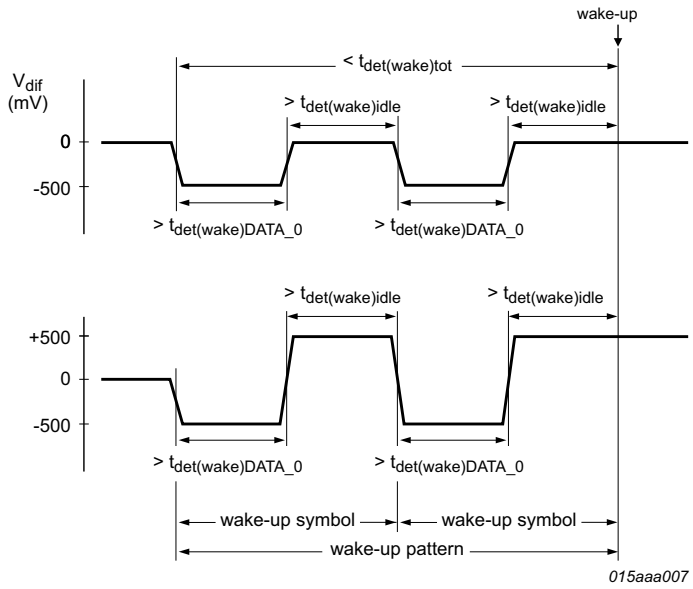


Fig 3. Bus wake-up timing

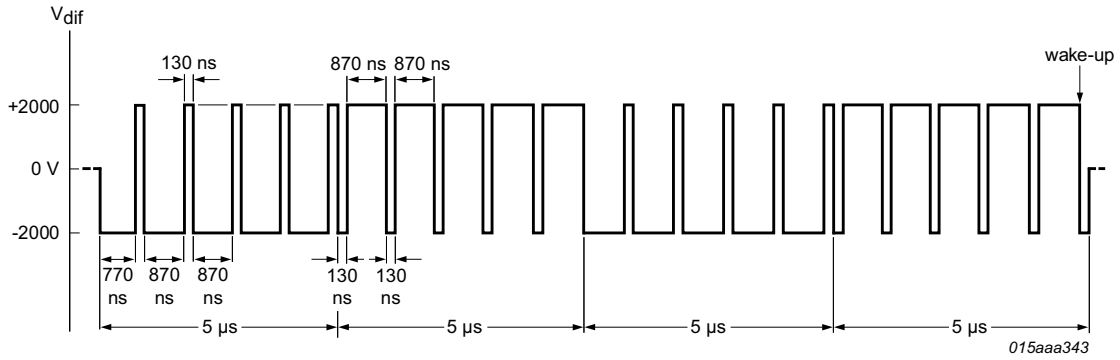
See Ref. 1 for more details of the wake-up mechanism.

7.4.1.2 Bus wake-up via dedicated FlexRay data frame

The TJA1086G detects a wake-up event when a dedicated data frame emulating a valid wake-up pattern, as shown in Figure 4, is received.

The Data_0 and Data_1 phases of the emulated wake-up symbol are interrupted by the Byte Start Sequence (BSS) preceding each byte in the data frame. With a data rate of 10 Mbit/s, the interruption has a maximum duration of 130 ns and does not prevent the transceiver from recognizing the wake-up pattern in the payload.

For longer interruptions at lower data rates (5 Mbit/s and 2.5 Mbit/s), the wake-up pattern should be used (see Section 7.4.1.1).



The duration of each interruption is 130 ns.

The transition time from DATA_0 to DATA_1 and vice versa is about 20 ns.

The TJA1086G wake-up flag is set on receipt of the following frame payload:

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

Fig 4. Minimum bus pattern for bus wake-up via dedicated FlexRay data frame

7.4.2 Local wake-up via pin LWU

Local wake-up is detected when the voltage on pin LWU is lower than $V_{th(wake)(LWU)}$ for longer than $t_{det(wake)(LWU)}$ (falling edge on pin LWU). When local wake-up is detected, the WU_LOCAL status bit is set and a WU interrupt is generated. At the same time, the internal biasing of this pin is switched to pull-down.

If the voltage on pin LWU rises and remains above $V_{th(wake)(LWU)}$ for longer than $t_{det(wake)(LWU)}$ (rising edge on pin LWU), local wake-up is not detected and the biasing on pin LWU is switched to pull-up.

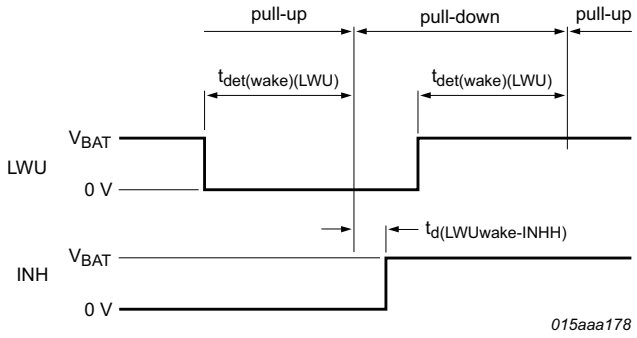


Fig 5. Local wake-up timing on pin LWU

7.4.3 Wake-up via the TRXD0/1 interface

If the voltage on pin TRXD0 or pin TRXD1 is LOW for longer than $t_{det(wake)(TRXD)}$, a WU interrupt is generated and the WU_TRXD status bit is set.

7.5 Communication controller interface

7.5.1 Bus activity and idle detection

The following mechanisms for activity and idle detection are valid in normal power modes:

- If the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$, activity is detected on the bus lines
- If, after bus activity detection, the differential voltage on the bus lines is higher than $V_{IH(dif)}$, pin RXD will go HIGH
- If, after bus activity detection, the differential voltage on the bus lines is lower than $V_{IL(dif)}$, pin RXD will go LOW
- If the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$, then idle is detected on the bus lines (pin RXD is switched HIGH or remains HIGH)

Additionally, activity and idle can be detected:

- if pin TXEN is LOW for longer than $t_{det(act)(TXEN)}$, activity is detected on pin TXEN
- if pin TXEN is HIGH for longer than $t_{det(idle)(TXEN)}$, idle is detected on pin TXEN
- if pin TRXD0 or TRXD1 is LOW for longer than $t_{det(act)(TRXD)}$, activity is detected on the TRXD0/1 interface
- if pins TRXD0 and TRXD1 are both HIGH for longer than $t_{det(idle)(TRXD)}$, idle is detected on the TRXD0/1 interface

Table 4. Transmitter input signals: TXD, TXEN and BGE[1]

TXD	TXEN	BGE	V_{IO} UV detected	RXD	Bus	TRXD0	TRXD1	Operating mode
X	H	X	no	HIGH	idle	high ohmic[2]	high ohmic[2]	AS_Normal
X	X	L	no	HIGH	idle	high ohmic[2]	high ohmic[2]	AS_Normal
L	L	H	no	LOW	DATA_0	LOW	high ohmic[2]	AS_Normal
H	L	H	no	HIGH	DATA_1	high ohmic[2]	LOW	AS_Normal
X	X	X	no	HIGH	idle	high ohmic[2]	high ohmic[2]	AS_Standby,[3] AS_Sleep[3]
X	X	X	yes	LOW	idle	high ohmic[2]	high ohmic[2]	AS_Normal, AS_Standby,[3] AS_Sleep[3]
X	X	X	X	HIGH	float	high ohmic[2]	high ohmic[2]	AS_PowerOff, AS_Reset

[1] The transmitter is activated by a falling edge on pin TXD while TXEN is LOW and BGE is HIGH.

[2] Internal pull-up resistor (R_{pu}) to V_{BUF}.

[3] BP and BM biased to GND.

Table 5. Bus as input

Bus	V_{IO} UV detected	RXD	TRXD0	TRXD1	Operating mode
DATA_0	no	LOW	LOW	high ohmic[1]	AS_Normal
DATA_1	no	HIGH	high ohmic[1]	LOW	AS_Normal
idle	no	HIGH	high ohmic[1]	high ohmic[1]	AS_Normal
X	no	HIGH	high ohmic[1]	high ohmic[1]	AS_Standby, AS_Sleep

Table 5. Bus as input

Bus	V_{IO} UV detected	RXD	TRXD0	TRXD1	Operating mode
DATA_0	yes	LOW	LOW	high ohmic[1]	AS_Normal
DATA_1	yes	LOW	high ohmic[1]	LOW	AS_Normal
idle	yes	LOW	high ohmic[1]	high ohmic[1]	AS_Normal
X	yes	LOW	high ohmic[1]	high ohmic[1]	AS_Standby, AS_Sleep
X	X	HIGH	high ohmic[1]	high ohmic[1]	AS_PowerOff, AS_Reset

[1] Internal pull-up resistor (R_{pu}) to V_{BUF}.

Table 6. TRXD0/1 interface configured as input

TRXD0	TRXD1	V_{IO} UV detected	RXD	Bus	Operating mode
X	falling edge	no	HIGH	DATA_1	AS_Normal[1]
HIGH	HIGH	no	HIGH	idle	AS_Normal
falling edge	X	X	LOW	DATA_0	AS_Normal[1]
X	falling edge	yes	LOW	DATA_1	AS_Normal[1]
HIGH	HIGH	yes	LOW	idle	AS_Normal
LOW	LOW	X	LOW	DATA_0	collision detected on TRXD0/1

[1] Activity detected on TRXD0/TRXD1.

7.6 Bus error detection

The TJA1086G provides bus error detection on each branch during data transmission. When a transmit error (TxE_BRx = 1) is detected on a branch, an EVENT_BRx interrupt is generated to notify the host.

The following conditions trigger bus error detection:

- Short circuit BP to BM
- Short-circuit BP to GND
- Short-circuit BM to GND
- Short-circuit BP to V_{CC} or V_{BAT}
- Short-circuit BM to V_{CC} or V_{BAT}

7.7 Interrupt generation

Interrupts are generated when specific events take place or associated status bits in the General or Branch X status registers are set. When an interrupt is generated, the relevant interrupt status bit is set in the Interrupt Status register (see Table 10) and pin INTN is forced LOW.

Some interrupt status bits (PWON, WU, SPI_ERROR and HC_ERROR) are reset immediately after the Interrupt Status register has been read successfully (i.e. a rising edge on SCSN with no SPI_ERROR).

The UV_ERROR, CLAMP_ERROR, TEMP_ERROR and EVENT_BRx status bits are reset after the flag (or flags) that triggered the interrupt has been reset and a successful read operation had been performed (these two events can occur in any order). Resetting these bits triggers a further falling edge on INTN to indicate to the host that the issue that triggered the interrupt has been resolved (except in the case of EVENT_BRx if a branch wake-up event triggered the interrupt). See Section 7.10.2.3 for further details.

INTN signaling conforms to the FlexRay Electrical Physical Layer specification V3.0.1 (see Ref. 1).

7.8 Operating modes

The TJA1086G features five operating modes.

AS_PowerOff, AS_Sleep and AS_Standby are low-power modes in which the transceiver is unable to transmit or receive data streams on the bus. In AS_PowerOff mode, only power-on reset detection is active. The SPI, the low-power receiver and wake-up detection are active in AS_Sleep mode. Undervoltage detection is enabled on V_{CC}, V_{BAT} and V_{BUF} in AS_Standby and AS_Normal modes. V_{IO} undervoltage detection is always enabled, except when the TJA1086G is in AS_PowerOff mode.

In AS_Normal mode, the TJA1086G can transmit and receive data streams on the bus.

Pin INH is HIGH in AS_Normal, AS_Standby and AS_Reset, and floating in AS_PowerOff and AS_Sleep.

The dStarGoToSleep timer is started when the TJA1086G switches to AS_Standby or AS_Normal, or when idle is detected on the bus. The timer is halted and reset when activity is detected on the bus.

7.8.1 Operating mode transitions

7.8.1.1 AS_PowerOff

The TJA1086G switches to AS_PowerOff from any mode if the internal supply to the state machine, V_{DIG}, falls below the power-on detection threshold voltage ($V_{th(det)POR}$). It remains in AS_PowerOff until V_{DIG} rises above the power-on recovery threshold voltage ($V_{th(rec)POR}$), when it switches to AS_Standby. Pins INTN and SDO are switched to a high-impedance state in AS_PowerOff mode.

7.8.1.2 AS_Reset

The TJA1086G switches to AS_Reset from any mode if pin RSTN goes LOW with no undervoltage detected on V_{IO}. It remains in AS_Reset until pin RSTN goes HIGH, when it switches to AS_Standby.

7.8.1.3 AS_Standby

The TJA1086G switches to AS_Standby:

- from AS_PowerOff when V_{DIG} rises above the power-on recovery threshold voltage ($V_{th(rec)POR}$)
- from AS_Reset when pin RSTN goes HIGH
- from AS_Normal when a V_{CC} undervoltage event is detected ($V_{CC} < V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$)

- from AS_Normal in response to a host ‘AS_Standby’ command (HC mode)
- from AS_Sleep in response to a host ‘AS_Standby’ command (HC mode)
- from AS_Sleep when a wake-up event is detected

The TJA1086G switches from AS_Standby:

- to AS_Normal when a wake-up event is detected, provided $V_{BUF} > V_{uvr(VBUF)}$
- to AS_Normal when a V_{CC} undervoltage recovery event is detected ($V_{CC} > V_{uvr(VCC)}$ for longer than $t_{rec(uv)(VCC)}$), provided $V_{BUF} > V_{uvr(BUF)}$
- to AS_Normal in response to a host ‘AS_Normal’ command (HC mode)
- to AS_Sleep if the dStarGoToSleep timer expires (AP mode)
- to AS_Sleep if a V_{CC} undervoltage event lasts longer than $t_{to(uvd)(VCC)}$ (HC mode)
- to AS_Sleep in response to a host ‘AS_Sleep’ command (HC mode)

7.8.1.4 AS_Sleep

A wake-up event will trigger a transition to AS_Standby (followed by a transition to AS_Normal if $V_{BUF} > V_{uvr(VBUF)}$).

The TJA1086G switches to AS_Sleep:

- from AS_Standby in response to a host ‘AS_Sleep’ command (HC mode)
- from AS_Standby if the dStarGoToSleep timer expires (AP mode)
- from AS_Standby if a V_{CC} undervoltage event lasts longer than $t_{to(uvd)(VCC)}$ (HC mode)
- from AS_Normal in response to a host ‘AS_Sleep’ command (HC mode)
- from AS_Normal if the dStarGoToSleep timer expires (AP mode)

The TJA1086G switches from AS_Sleep:

- to AS_Standby in response to a host ‘AS_Standby’ command (HC mode)
- to AS_Standby when a wake-up event is detected.
- to AS_Normal in response to a host ‘AS_Normal’ command (HC mode)

7.8.1.5 AS_Normal

The TJA1086G switches to AS_Normal:

- from AS_Standby if a V_{CC} undervoltage recovery event is detected ($V_{CC} > V_{uvr(VCC)}$ for longer than $t_{rec(uv)(VCC)}$), provided $V_{BUF} > V_{uvr(BUF)}$
- from AS_Standby if a wake-up event is detected, provided $V_{BUF} > V_{uvr(VBUF)}$ for longer than $t_{rec(uv)(VBUF)}$
- from AS_Standby or AS_Sleep in response to a host ‘AS_Normal’ command

The TJA1086G switches from AS_Normal:

- to AS_Standby when a V_{CC} undervoltage event is detected ($V_{CC} < V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$)

- if the TJA1086G is in HC mode, it will switch from AS_Standby to AS_Sleep if the V_{CC} undervoltage persists for longer than $t_{to(uvd)(VCC)}$
- if the TJA1086G is in AP mode, it will switch to AS_Sleep when the dStarGoToSleep timer expires

- to AS_Standby in response to a host ‘AS_Standby’ command (HC mode)
- to AS_Sleep in response to a host ‘AS_Sleep’ command (HC mode)
- to AS_Sleep if the dStarGoToSleep timer expires (AP mode)

7.8.1.6 Operating mode transition diagram

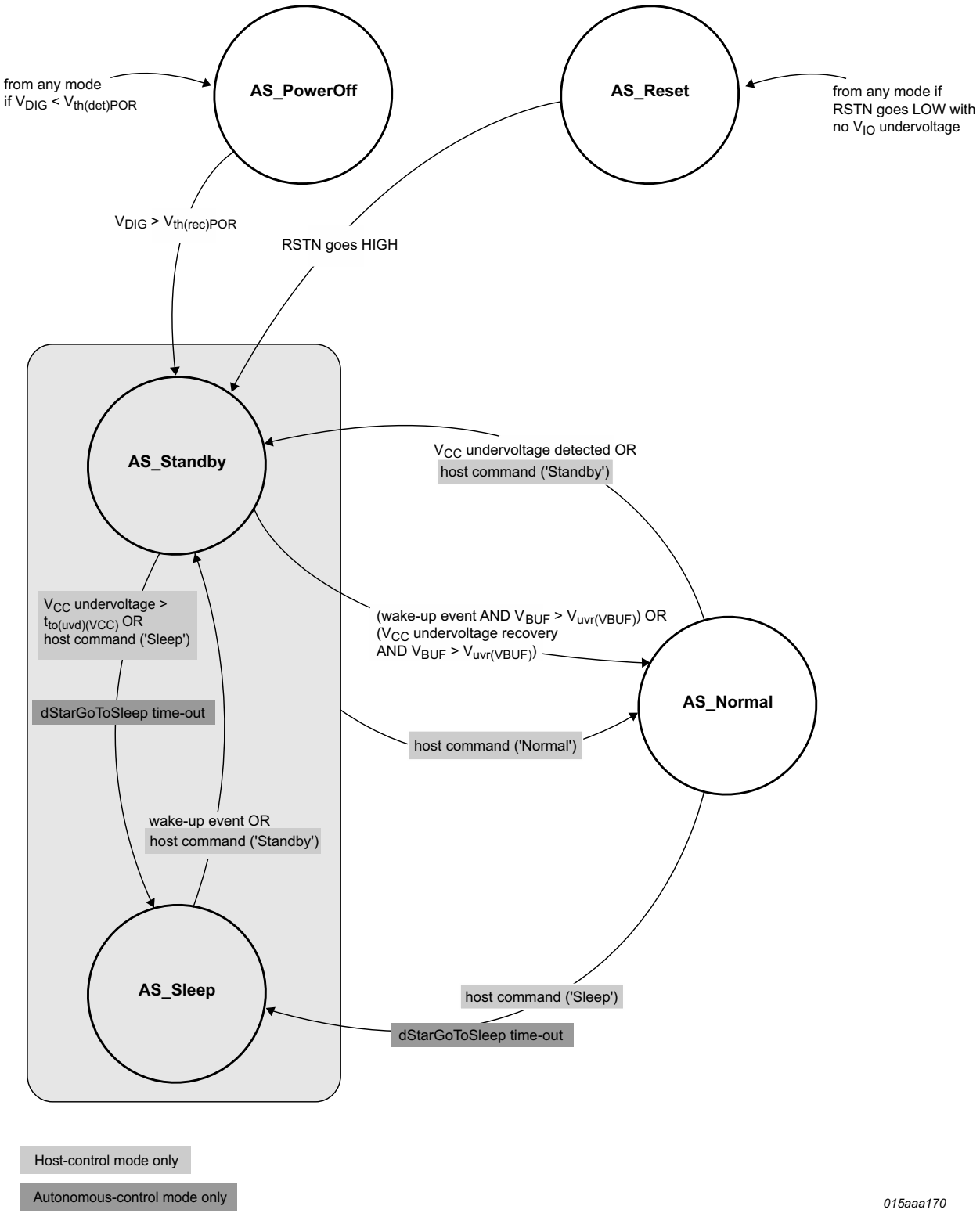


Fig 6. Mode transition diagram

7.9 Branch operating modes

Each of the two branches in the TJA1086G features six branch operating modes:

- Branch_Off
  Both branches are in Branch_Off mode when the TJA1086G is in AS_PowerOff or AS_Reset mode. The transmitter, normal receiver, low-power receiver and bus error detection are disabled. The bus pins are floating.
- Branch_LowPower
  Both branches are in Branch_LowPower mode when the TJA1086G is in AS_Standby or AS_Sleep mode. The transmitter, the normal receiver and bus error detection are disabled. The low-power receiver is active (i.e. remote wake-up is possible). The bus pins are biased to ground.
- Branch_Disabled
  The TJA1086G switches to Branch_Disabled if an overtemperature is detected. The 'Branch_Disabled' and 'Branch_Normal' commands allow the host to enable/disable a branch without affecting the other branch. The transmitter, normal receiver and bus error detection are disabled. Only the low-power receiver is active (remote wake-up is possible). The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_Normal
  When a branch is in Branch_Normal, the TJA1086G will be in AS_Normal. The transmitter, normal receiver and bus error detection are active. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_TxOnly1
  In Branch_TxOnly1 mode, the receiver is disabled, i.e. the received data is not forwarded to the signal router. The transmitter is active and bus error detection is active. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.
- Branch_TxOnly2
  This mode is host-controlled only and is operationally identical to Branch_TxOnly1. It allows the host to switch off the receiver in response to error conditions.
- Branch_FailSilent
  The transmitter, the low-power receiver and bus error detection are disabled. Only the receiver remains active to monitor the branch for idle or activity. Received data is not forwarded to the signal router. The bus pins are biased to $V_{o(idle)(BP)}$ and $V_{o(idle)(BM)}$.

7.9.1 Branch operating mode transitions

Branch-related host commands can only be issued when the TJA1086G is in AS_Normal mode.

7.9.1.1 Branch_Off

When the TJA1086G enters AS_PowerOff or AS_Reset, both branches switch to Branch-Off. When the TJA1086G subsequently switches to AS_Standby, both branches switch to Branch_LowPower.

7.9.1.2 Branch_LowPower

Both branches switch to Branch_LowPower when the TJA1086G enters AS_Standby or AS_Sleep. Both branches will remain in this mode until the TJA1086G enters AS_Normal. When this transition happens, any branch that was in Branch_Disabled before switching to Branch_LowPower will return to Branch_Disabled. Otherwise, both branches switch to

Branch_Normal.

7.9.1.3 Branch_Disabled

An overtemperature event (TEMP_HIGH flag set) triggers a transition from Branch_Normal to Branch_Disabled in both branches.

If an overtemperature event triggered the transition from Branch_Normal to Branch_Disabled, both branches return to Branch_Normal when the overtemperature problem has been resolved (TEMP_WARN flag reset).

The ‘Branch_Disabled’ and ‘Branch_Normal’ commands can be used to enable/disable individual branches. A host command is also available to trigger a transition from Branch_Disabled to Branch_TxOnly1 (‘Branch_TxOnly').

If a branch switches from Branch_Disabled to Branch_LowPower because the TJA1086G has entered AS_Standby or AS_Sleep, it will return to Branch_Disabled when the TJA1086G enters AS_Normal.

7.9.1.4 Branch_FailSilent

A branch switches to Branch_FailSilent:

- from Branch_Normal if a branch is clamped (Clamp_BRx flag set), provided clamp-detection is enabled (bit CLAMP_DET set; see Table 9)
- from Branch_Normal if a transmit error (TxE_BRx = 1) is detected, provided autonomous error confinement is enabled (bit AEC set; see Table 9)
- from Branch_TxOnly1 if a transmit error (TxE_BRx = 1) is detected.

The branch remains in Branch_FailSilent until idle is detected on both branches, when it switches to Branch_TxOnly1 (a ‘Branch_TxOnly’ command is needed in HC mode).

7.9.1.5 Branch_TxOnly1

A branch switches to Branch_TxOnly1:

- from Branch_Disabled in response to a ‘Branch_TxOnly’ command (HC mode)
- from Branch_FailSilent in response to a ‘Branch_TxOnly’ command when both branches are idle (HC mode)
- from Branch_FailSilent when both branches are idle (AP mode)

A branch switches from Branch_TxOnly1:

- to Branch_Normal when a transmission ends without error
- to Branch_FailSilent if a transmit error is detected (TxE_BRx = 1)

7.9.1.6 Branch_TxOnly2

This mode is purely host controlled. A branch switches to Branch_TxOnly2 only in response to a ‘Branch_TxOnly’ command issued in Branch_Normal mode. The branch remains in Branch_TxOnly2 mode until a ‘Branch_Normal’ command is received.

7.9.1.7 Branch_Normal

A branch switches to Branch_Normal:

- from Branch_LowPower when the TJA1086G enters AS_Normal mode (provided it was not in Branch_Disabled before the transition to Branch_LowPower mode)
- from Branch_TxOnly2 in response to a host ‘Branch_Normal’ command
- from Branch_TxOnly1 when a transmission ends without error
- from Branch_Disabled in response to a host ‘Branch_Normal’ command
- from Branch_Disabled when an overtemperature is resolved (TEMP_WARN = 0), provided the overtemperature triggered the earlier transition to Branch_Disabled.

A branch switches from Branch_Normal:

- to Branch_FailSilent if a branch is clamped, provided clamp-detection is enabled (CLAMP_DET = 1)
- to Branch_FailSilent if a transmit error is detected, provided bit AEC = 1
- to Branch_TxOnly2 if a host ‘Branch_TxOnly’ command is received
- to Branch_Disabled if an overtemperature event is detected (TEMP_HIGH = 1)

7.9.1.8 Branch operating mode transition diagram

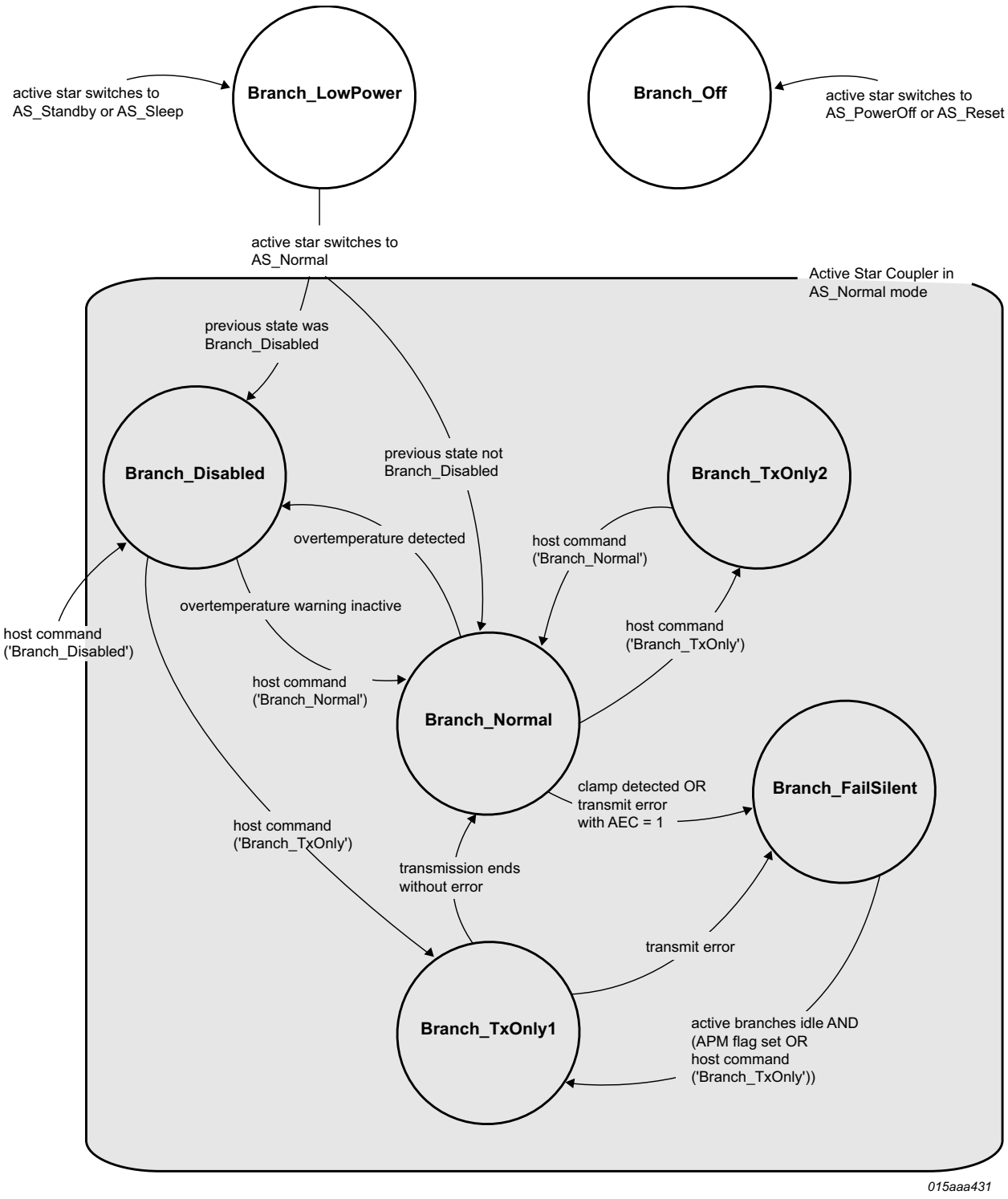


Fig 7. Branch mode transition diagram

7.10 SPI interface

The TJA1086G contains a bidirectional 16-bit Serial Peripheral Interface (SPI) for communicating with a host. The SPI allows the host to configure the TJA1086G and to access error and status information.

7.10.1 Register access

The SPI supports full duplex data transfer, so status information is read out on pin SDO while control data is being shifted in on pin SDI. Bit sampling is performed on the falling edge of the clock signal on pin SCLK and data is shifted on the rising edge (MSB first; see Figure 8).

The clock signal must be LOW when SCSN goes LOW to initiate an SPI register access cycle.

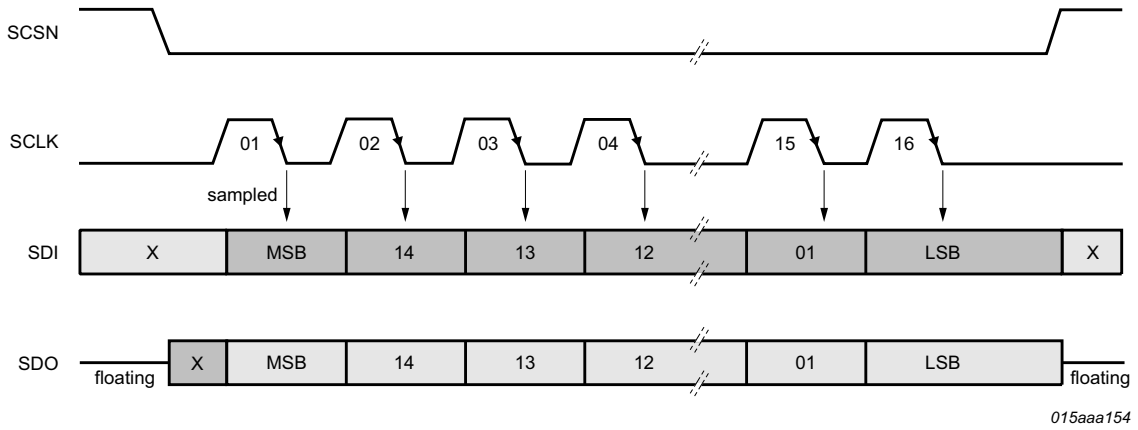


Fig 8. SPI register access

7.10.2 SPI registers

The SPI register structure in the TJA1086G is illustrated in Figure 9. The three MSBs (bits15 to 13) contain the 3-bit register address. Bit 12 defines the selected register access as read/write or read only. If bit 12 is 1, the SPI data transfer will be read only and all data on the SDI pin will be ignored. If bit 12 is 0, data bits 11 to 0 will be written to the selected register.

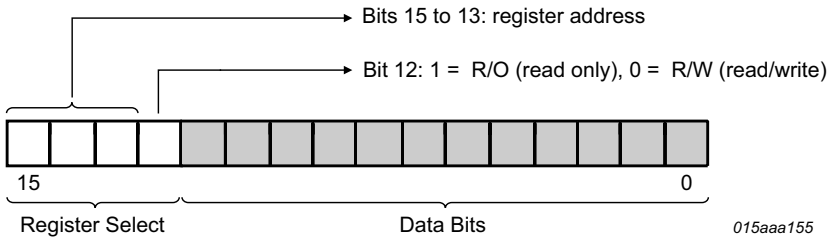


Fig 9. SPI register structure

The assignment of control and status register addresses is detailed in Table 7. Data can only be written to the Control and Configuration registers (status registers are read-only by definition). Therefore the state of bit 12 is only evaluated when these registers are being accessed.

Table 7. Register map

Address bits 15, 14 and 13	Write access bit 12[1]	Register
000	0 =R/W, 1 = R/O	Control register; see Table 8
001	1 = R/O	Interrupt status register; see Table 10
010	1 = R/O	General status register; see Table 11
011	1 = R/O	Branch 1 status register; see Table 12
100	1 = R/O	Branch 2 status register; see Table 12
111	0 =R/W, 1 = R/O	Configuration register; see Table 9

[1] Bit 12 is assumed to be 1 for status registers

The following subsections provide details of the bits in these registers and the control and status functionality assigned to each.

7.10.2.1 Control register

The read/write Control register allows the host controller to set the operating modes and to switch the TJA1086G between HC and AP modes.

Table 8. Control register bit description

Bit	Symbol	Access	Default	Description
11:10	OPM	R/W	00	operating mode:
				00: no change
				01: AS_Standby
				10: AS_Sleep
				11: AS_Normal
9:8	CTRL_BR1	R/W	00	branch 1 control:
				00: no change
				01: Branch_Normal
				10: Branch_TxOnly
				11: Branch_Disabled
7:6	CTRL_BR2	R/W	00	branch 2 control:
				00: no change
				01: Branch_Normal
				10: Branch_TxOnly
				11: Branch_Disabled
5:2	reserved			after power-up, write 1111 once to bits [5:2] in AS_Standby before entering AS_Normal to minimize the power supply current
1	APM[1]	R/W	1	Autonomous Power mode
				0: disabled
				1: enabled
0	RESET_ERROR[2]	R/W	0	reset error flags and status bits
				0: no change
				1: reset flags/bits

[1] The TJA1086G sets the APM flag at power-on, in response to a wake-up event (local, remote or TRXD), if a V_{CC} undervoltage is detected in AS_Normal or a V_{IO} undervoltage is detected for longer than $t_{to(uvd)(VIO)}$.

[2] Setting the RESET_ERROR bit resets all error status bits in the General Status (bits 8 to 1) and Branch Status registers (bits 7 to 4).

7.10.2.2 Configuration register

The read/write Configuration register allows the host controller to configure a number of TJA1086G parameters and functions.

Table 9. Configuration register bit description

Bit	Symbol	Access	Default	Description
11	AEC	R/W	0	Autonomous error confinement:
				0: disabled
				1: enabled
10	BFT	R/W	1	Bus failure timer
				0: disabled
				1: enabled
9	WUD_BR1	R/W	1	wake-up detection on branch 1:
				0: disabled
				1: enabled
8	WUD_BR2	R/W	1	wake-up detection on branch 2:
				0: disabled
				1: enabled
7:6	reserved			after power-up, write 00 once to bits [7:6] to minimize the power supply current
5	CC_EN	R/W	0	CC interface enable (TXD and TXEN inputs; RXD output):
				0: disabled
				1: enabled
4	TRXD_EN	R/W	1	TRXD interface enable:
				0: disabled
				1: enabled
3	reserved			always 0
2	CLAMP_DET	R/W	1	clamping detection:
				0: disabled
				1: enabled
1	BIT_LATCHING	R/W	0	status bit latching:
				0: disabled
				1: enabled
0	PARITY	R	-	parity bit - odd parity (including parity bit)

Autonomous Error Confinement (AEC):
Setting the AEC bit enables the autonomous error confinement feature of the TJA1086G.

When AEC is enabled, a bus error (TxE_BRx = 1) triggers a transition from Branch_Normal to Branch_FailSilent. AEC is disabled by default.

Bus Failure Timer (BFT):
Setting the BFT bit enables the bus failure timer.

When the BFT is enabled, pulses shorter than $t_{to(BFT)}$ are ignored, resulting in more robust bus error detection. The BFT is enabled by default.

Wake-up detection on branch x (WUD_BRx):
Setting the WUD_BRx bit enables wake-up detection on the specified branch.

Each branch in a TJA1086G star network contains a low-power receiver for detecting remote wake-up events. These events can be enabled and disabled individually. This feature makes it possible to minimize quiescent current consumption, especially in AS_Sleep mode. Wake-up detection is enabled by default on both branches.

Communication Controller interface Enable (CC_EN):
Setting bit CC_EN enables the communication controller interface.

A communication controller can be connected to the TJA1086G when CC_EN = 1. If CC_EN = 0, the RXD output driver is switched off to minimize current consumption in AS_Normal mode. The CC interface is disabled by default.

TRXD0/1 interface Enable (TRXD_EN):
Setting bit TRXD_EN enables the TRXD0 and TRXD1 interfaces.

When the TRXD0/1 interfaces are enabled, several TJA1086G devices can be connected together to form a single active star. If only one TJA1086G is needed at any time, the TRXD0/1 interfaces can be disabled to minimize current consumption in AS_Normal mode. The TRXD0 and TRXD1 interfaces are enabled by default.

Clamp detection (CLAMP_DET):
Setting bit CLAMP_DET enables clamp detection on TXEN, TRXD and on both branches.

When clamp detection is enabled, a CLAMP_ERROR interrupt is generated if clamping is detected on TXEN (CLAMP_TXEN = 1), TRXD (CLAMP_TRXD = 1) or on a branch (CLAMP_BRx). Clamp detection is enabled by default.

Bit latching (BIT_LATCHING):
When bit latching is enabled (BIT_LATCHING = 1), the status bits in the General and Branch X status registers reflect the latched state until the register is read. Once the register has been read, latching is released and the bits then reflect the current ‘live’ status. When bit latching is disabled, the status bits reflect the ‘live’ status at all times. Bit latching is disabled by default.