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TJA1100

100BASE-T1 PHY for Automotive Ethernet

Rev. 3 — 23 May 2017 Product data sheet

1. General description

The TJA1100 is a 100BASE-T1 compliant Ethernet PHY optimized for automotive use cases. The device provides 100 Mbit/s transmit and receive capability over a single Unshielded Twisted Pair (UTP) cable, supporting a cable length of up to at least 15 m. Optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed to minimize power consumption and system costs, while still providing the robustness required for automotive use cases.

2. Features and benefits

2.1 Optimized for automotive use cases

- Transmitter optimized for capacitive coupling to unshielded twisted-pair cable
- Enhanced integrated PAM-3 pulse shaping for low RF emissions
- Adaptive receive equalizer optimized for automotive cable length of up to at least 15 m
- Reduced power consumption through configurable transmitter pulse amplitude adapted to cable length
- Dedicated PHY enable/disable input pin to minimize power consumption
- Low-power Sleep mode with local wake-up support
- Robust remote wake-up via the bus lines
- Gap-free supply undervoltage detection with fail-silent behavior
- EMC-optimized output driver strength for Media Independent Interface (MII) and Reduced MII (RMII)
- Diagnosis of cabling errors (shorts and opens)
- Small HVQFN-36 package for PCB space-constrained applications
- MDI pins protected against ESD to ±6kV HBM and ±6kV IEC61000-4-2
- MDI pins protected against transients in automotive environment
- Automotive-grade temperature range from −40 °C to +125 °C
- Automotive product qualification in accordance with AEC-Q100

2.2 Miscellaneous

- MII as well as RMII standard compliant interface
- Reverse MII mode for back-to-back connection of two PHYs
- 3V3 single supply operation with on-chip 1.8 V LDO regulators
- On-chip termination resistors for balanced UTP cable
- Jumbo frame support up to 16 kB
- Internal, external and remote loopback mode for diagnosis

- Bus pins short-circuit proof to battery voltage and ground (including common mode choke, 100 nF coupling capacitors)
- LED control output for link diagnosis

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1100HN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 × 6 × 0.85 mm	SOT1092-2

4. Block diagram

A block diagram of the TJA1100 is shown in Figure 1. The 100BASE-T1 section contains the functional blocks specified in the 100BASE-T1 standard that make up the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) layer for both the transmit and receive signal paths. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE802.3 clause 22.

Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, LED control, local wake-up and configuration control. A number of power supply related functional blocks are defined: Very Low Power (VLP) supply in Sleep mode, Reset circuit, supply monitoring and a 1.8 V regulator for the digital core. Pin strapping allows a number of default PHY settings (e.g. Master or Slave configuration) to be hardware-configured at power-up.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

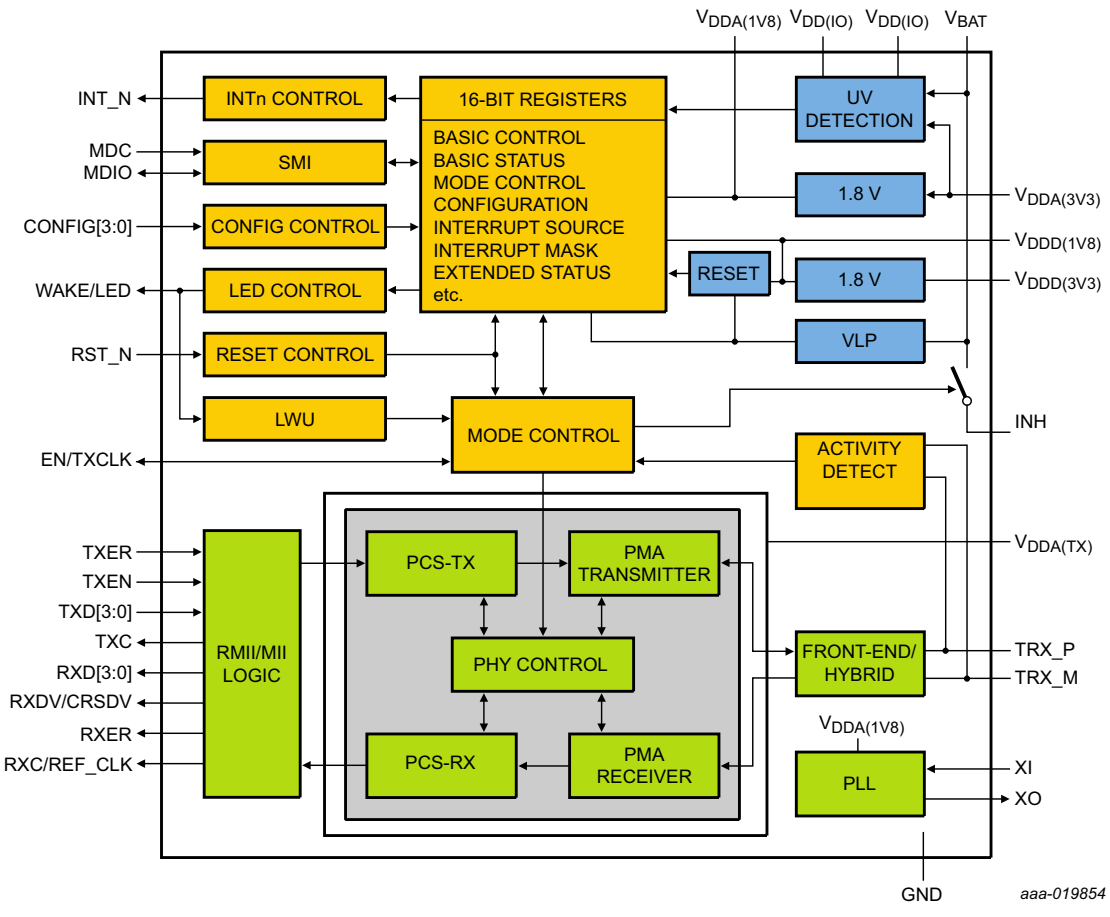


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

The pin configuration of the TJA1100 is shown in Figure 2. The following standard interfaces are provided by the TJA1100: MII/RMII (including SMI) and MDI. Since 100BASE-T1 allows for full-duplex bidirectional communication, the standard MII signals COL and CRS are not needed.

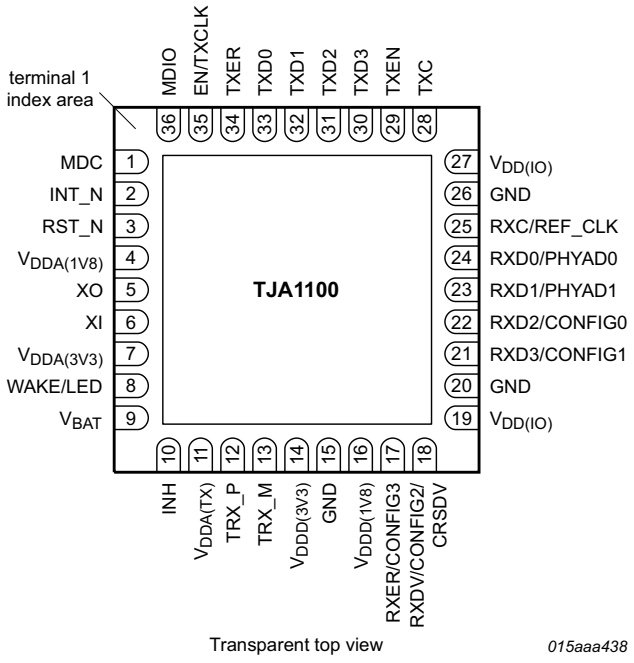


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
MDC	1	I	SMI clock input (weak pull-down)
INT_N	2	O	interrupt output (active-LOW, open-drain output)
RST_N	3	I	reset input (active-LOW)
$V_{DDA(1V8)}$	4	P	1.8 V analog supply voltage (internally generated; needs to be filtered externally)
XO	5	AO	crystal feedback - used in MII/RMII mode with 25 MHz crystal
XI	6	AI	crystal input - used in MII/RMII mode with 25 MHz crystal
$V_{DDA(3V3)}$	7	P	3.3 V analog supply voltage
LED	8	AO	LED open-drain output (when enabled: LED_ENABLE = 1)
WAKE	8	AI	local WAKE input (when LED output disabled: LED_ENABLE = 0)
V_{BAT}	9	P	battery supply voltage
INH	10	AO	inhibit output for voltage regulator control (V_{BAT}-related, active-HIGH)
$V_{DDA(TX)}$	11	P	3.3 V analog supply voltage for the transmitter
TRX_P	12	AIO	+ terminal for transmit/receive signal
TRX_M	13	AIO	− terminal for transmit/receive signal
$V_{DDD(3V3)}$	14	P	3.3 V digital supply voltage
GND[2]	15	G	ground reference
$V_{DDD(1V8)}$	16	P	1.8 V digital supply voltage (internally generated; needs to be filtered externally)
RXER	17	O	MII/RMII receive error output
CONFIG3	17	I	pin strapping configuration input 3
RXDV	18	O	MII/RMII receive data valid output
CONFIG2	18	I	pin strapping configuration input 2
CRSDV	18	O	RMII mode: carrier sense/receive data valid output
$V_{DD(IO)}$	19	P	3.3 V I/O supply voltage
GND[2]	20	G	ground reference
RXD3	21	O	MII mode: receive data output, bit 3 of RXD[3:0] nibble
CONFIG1	21	I	pin strapping configuration input 1
RXD2	22	O	MII mode: receive data output, bit 2 of RXD[3:0] nibble
CONFIG0	22	I	pin strapping configuration input 0
RXD1	23	O	MII mode: receive data output, bit 1 of RXD[3:0] nibble RMII mode: receive data output, bit 1 of RXD[1:0] nibble
PHYAD1	23	I	pin strapping configuration input for bit 1 of the PHY address used for the SMI address/Cipher scrambler
RXD0	24	O	MII mode: receive data output, bit 0 of RXD[3:0] nibble RMII mode: receive data output, bit 0 of RXD[1:0] nibble
PHYAD0	24	I	pin strapping configuration input for bit 0 of the PHY address used for the SMI address/Cipher scrambler
RXC	25	O	MII mode: 25 MHz receive clock output
		I	MII reverse mode: 25 MHz receive clock input

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
REF_CLK	25	I	RMII mode: 50 MHz oscillator clock input
		O	RMII mode: 50 MHz interface reference clock
GND[2]	26	G	ground reference
$V_{DD(IO)}$	27	P	3.3 V I/O supply voltage
TXC	28	IO	MII mode: 25 MHz transmit clock output MII reverse mode: 25 MHz transmit clock input
TXEN	29	I	MII/RMII mode: transmit enable input (active-HIGH, weak pull-down)
TXD3	30	I	MII mode: transmit data input, bit 3 of TXD[3:0] nibble
TXD2	31	I	MII mode: transmit data input, bit 2 of TXD[3:0] nibble
TXD1	32	I	MII mode: transmit data input, bit 1 of TXD[3:0] nibble RMII mode: transmit data input, bit 1 of TXD[1:0] nibble
TXD0	33	I	MII mode: transmit data input, bit 0 of TXD[3:0] nibble RMII mode: transmit data input, bit 0 of TXD[1:0] nibble
TXER	34	I	MII/RMII: transmit error input (weak pull-down)
EN	35	I	PHY enable input (active-HIGH)
TXCLK	35	O	transmit clock output in test mode and during slave jitter test
MDIO	36	IO	SMI data I/O (weak pull-up)

[1] AIO: analog input/output; AO: analog output; AI: analog input; I: digital input ($V_{DD(IO)}$ related); O: digital output ($V_{DD(IO)}$ related); IO: digital input/output ($V_{DD(IO)}$ related); P: power supply; G: ground.

[2] The HVQFN36 package die supply ground is connected to the GND pins and the exposed center pad. The GND pins must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended to connect the exposed center pad to board ground as well.

6. Functional description

6.1 System configuration

A 100BASE-T1 compliant Ethernet PHY, the TJA1100 provides 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable, supporting a cable length of up to at least 15 m with a bit error rate less than or equal to 1E−10. It is optimized for capacitive signal coupling to the twisted-pair lines. To comply with automotive EMC requirements, a common-mode choke (CMC) is typically inserted into the signal path.

The TJA1100 is designed to provide a cost-optimized system solution for automotive Ethernet links. Communication with the Media Access Control (MAC) unit can be realized via the MII or the RMII.

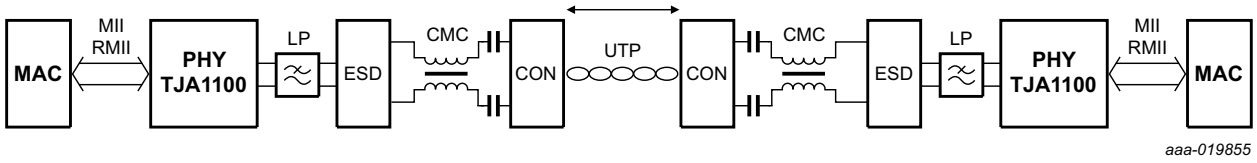


Fig 3. A system diagram showing capacitive coupling

6.2 MII and RMII

The TJA1100 contains MII and RMII interfaces to the MAC controller.

6.2.1 MII

6.2.1.1 Signaling and encoding

The connections between the PHY and the MAC are shown in more detail in Figure 4. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal frequency of 25 MHz (±100 ppm). Normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.

MII encoding is described in Table 3 and Table 4.

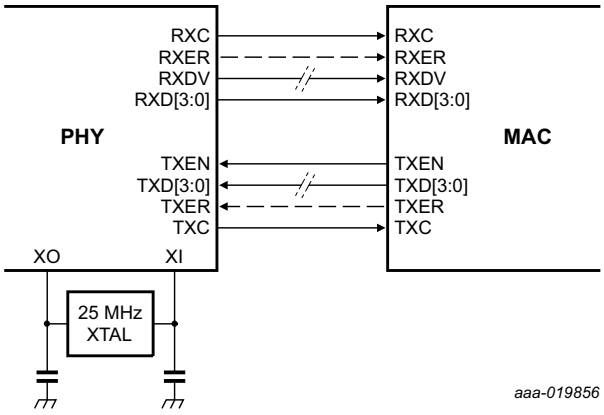


Fig 4. MII signaling

Table 3. MII encoding of TXD[3:0], TXEN and TXER

TXEN	TXER	TXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000 through 1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	transmit error propagation

Table 4. MII encoding of RXD[3:0], RXDV and RXER

RXDV	RXER	RXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000	normal interframe
0	1	0001 through 1101	reserved
0	1	1110	false carrier indication
0	1	1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	data reception with errors

Since 100BASE-T1 provides full-duplex communication, the standard signals COL and CRS are not needed.

6.2.2 RMII

6.2.2.1 Signaling and encoding

In the case of RMII, data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 5. To achieve the same data rate as MII, the interface is clocked at a nominal frequency of 50 MHz. A single clock signal, REF_CLK, is provided for both transmit and received data. This clock signal is provided by the PHY and is typically derived from an external 25 MHz (±100 ppm) crystal (see Figure 5). Alternatively, a 50 MHz clock signal (±50 ppm) generated by an external oscillator can be connected to pin REFCLK_IN (see Figure 6).

RMII encoding is described in Table 5 and Table 6.

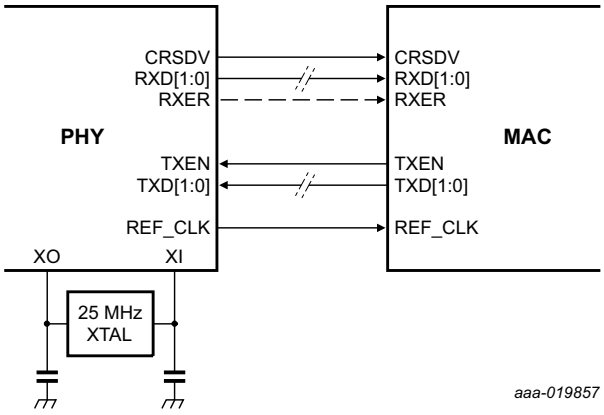


Fig 5. RMII signaling using an external crystal

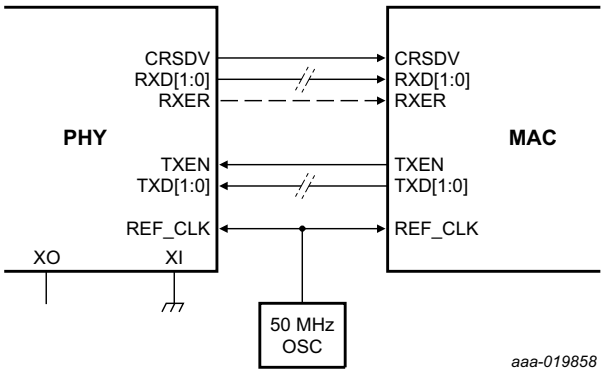


Fig 6. RMII signaling using an externally generated reference clock

Table 5. RMII encoding of TXD[1:0], TXEN

TXEN	TXD[1:0]	Indication
0	00 through 11	normal interframe
1	00 through 11	normal data transmission

Table 6. RMII encoding of RXD[1:0], CRSDV and RXER

CRSDV	RXER	RXD[1:0]	Indication
0	0	00 through 11	normal interframe
0	1	00	normal interframe
0	1	01 through 11	reserved
1	0	00 through 11	normal data transmission
1	1	00 through 11	data reception with errors

6.2.3 Reverse MII

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer (see Figure 7). The MII signals are cross-connected: RX output signals from each PHY are connected to the TX inputs on the other PHY. For the PHY connected in Reverse MII mode, the TXC and RXC clock signals become inputs.

Since the MII interface is a standardized solution, two PHYs can be used to implement two different physical layers to realize, for example, a conversion from Fast Ethernet to 100BASE-T1 and vice versa. Another use case for such a repeater could be to double the link length up to 30 m.

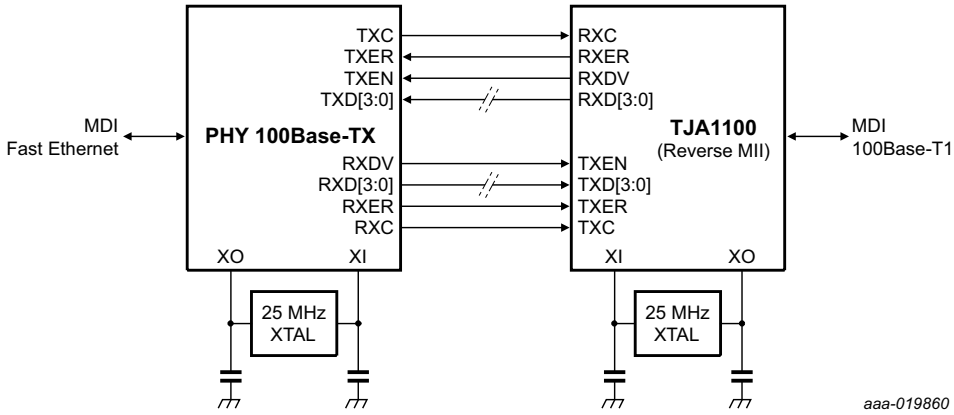


Fig 7. Fast Ethernet to 100BASE-T1 media converter with TJA1100 Reverse MII

6.3 System controller

6.3.1 Operating modes

6.3.1.1 Power-off mode

TJA1100 remains in Power-off mode as long as the voltage on pin V_{BAT} is below the power-on reset threshold. The analog blocks are disabled and the digital blocks are in a passive reset state in this mode.

6.3.1.2 Standby mode

At power-on, when the voltage on pin V_{BAT} rises above the under-voltage recovery threshold ($V_{uvr(VBAT)}$), the TJA1100 enters Standby mode, switching on the INH control output. This control signal may be used to activate the supply to the microcontroller in the ECU. Once the 3.3 V supply voltage is available, the internal 1.8 V regulators are activated and the PHY is configured according to the pin-strapping implemented on the CONFIGn and PHYADn pins. No SMI access takes place during the power-on settling time ($t_{s(pon)}$).

From an operating point of view, Standby mode corresponds to the IEEE 802.3 Power-down mode, where the transmit and receive functions (in the PHY) are disabled. Standby mode also acts as a fail-silent mode. The TJA1100 switches to Standby mode when an under-voltage condition is detected on $V_{DDA(3V3)}$, $V_{DDA(1V8)}$, $V_{DDD(1V8)}$ or $V_{DD(IO)}$.

6.3.1.3 Normal mode

To establish a communication link, the TJA1100 must be switched to Normal mode, either autonomously (AUTO_OP = 1; see Table 20) or via an SMI command (AUTO_OP = 0).

When the PHY is configured for autonomous operation, the TJA1100 will automatically enter Normal mode and activate the link on power-on.

When the PHY is host-controlled, the internal PLL starts running when the TJA1100 enters Normal mode and the transmit and receive functions (both PCS and PMA) are enabled. After a period of stabilization, $t_{init(PHY)}$, the TJA1100 is ready to set up a link. Once the LINK_CONTROL bit is set to 'ENABLE', the PHY configured as Master initiates the training sequence by transmitting idle pulses. The link is established when bit LINK_UP in the Communication Status register is set.

6.3.1.4 Disable mode

Whenever the Ethernet interface is not in use or must be disabled for fail-safe reasons, the PHY can be switched off by pulling pin EN LOW. The PHY is switched off completely in Disable mode, minimizing power consumption. The configuration register settings are maintained. To exit Disable mode, pin EN must be forced HIGH to activate the PHY.

6.3.1.5 Sleep mode

If the network management in a node decides to withdraw from the network because the functions of the node are no longer needed, it may power down the entire ECU via PHY Sleep mode. In Sleep mode, the transmit and receive functions are switched off and no signal is driven onto the twisted-pair lines. Transmit requests from the MII interface are ignored and the MII output pins are in a high-ohmic state. The SMI is also deactivated to minimize power consumption.

By releasing the INH output, the ECU is allowed to switch off its main power supply unit. Typically, the entire ECU is powered-down. The TJA1100 is kept partly alive by the permanent battery supply and can still react to activity on the Ethernet lines. Once valid Ethernet idle pulses are detected on the lines, the TJA1100 wakes up, switching on the main power unit via the INH control signal. As soon as the supply voltages are stable within their operating ranges, the TJA1100 can be switched to Normal mode via an SMI command and the communication link to the partner can be re-established. Sleep mode can be entered from Normal mode via the intermediate Sleep Request mode as well as from Standby mode, as shown in Figure 8. Note that the configuration register settings are maintained in Sleep mode.

6.3.1.6 Sleep Request mode

Sleep Request mode is an intermediate state used to introduce a transition to Sleep mode. The PHY sleep request timer starts when the TJA1100 enters Sleep Request mode. This timer determines how long the PHY remains in Sleep Request mode. When the timer expires (after $t_{to(req)sleep}$), the PHY switches to Sleep mode and INH is switched off. The PHY does not expect to receive Ethernet frames in Sleep Request mode. If any Ethernet frames are received at MDI or MII in Sleep Request mode, the PHY returns to Normal mode, the DATA_DET_WU flag in the General status register is set and a WAKEUP interrupt is generated.

Table 7 presents an overview of the status of TJA1100 functional blocks in each operating mode.

Table 7. Status of functional blocks in TJA1100 operating modes

Functional block	Normal	Standby[1]	Sleep Request	Sleep	Disable
MII	on	high-ohmic[2]	on	high-ohmic	high-ohmic
PMA/PCS-TX	on	off	on	off	off
PMA/PCS-RX	on	off	on	off	off
SMI	on	on	on	off	off
Activity detection	off	on	off	on	off
Crystal oscillator	on	off	on	off	off
LDO_1V8	on	on	on	off	off
RST_N input	on	on	on	off	on
EN input	on[3]	on	on	off	on
WAKE input	off	on/off[4]	on/off[4]	on/off[4]	off
INT_N output	on	on	on	high-ohmic	high-ohmic
LED output	on/off[4]	off	on/off[4]	off	off
INH output	on	on	on	off	on/off[5]
Temp detection	on	on	on	off	off

[1] Outputs RXD[3:0], RXER and RXDV are LOW in Standby mode; the other MII pins are configured as inputs via internal 100 kΩ pull-down resistors.

[2] Pins configured as outputs will be LOW in Standby mode.

[3] In Normal mode, this pin is used as the TXCLK output for the test modes and the slave jitter test (the PHY enable input is held HIGH internally during this time).

[4] The WAKE input is active in Standby, Sleep Request and Sleep modes if LED_ENABLE = 0; the LED output is active in Normal and Sleep Request modes if LED_ENABLE = 1.

[5] The behavior of the INH output in Disable mode is configurable.

6.3.1.7 Reset mode

The TJA1100 switches to Reset mode from any mode except Power-off when pin RST_N is held LOW for at least the maximum reset detection time ($t_{det(rst)(max)}$), provided the voltage on $V_{DD(IO)}$ is above the undervoltage threshold.

When RST_N goes HIGH again, or an undervoltage is detected on $V_{DD(IO)}$, the TJA1100, switches to Standby mode. All register bits are reset to their default values in Reset mode.

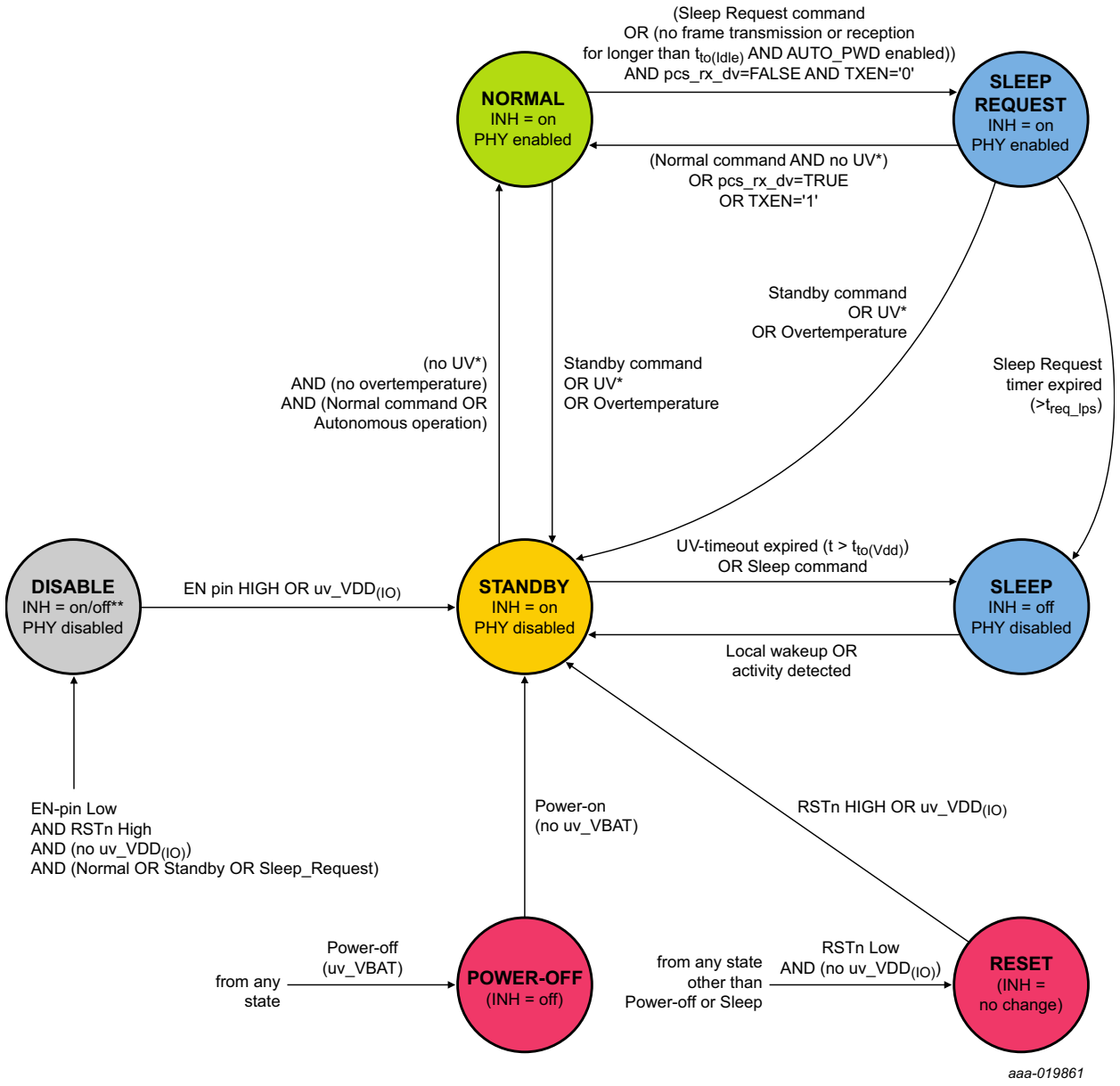
6.3.2 Transitions between operating modes

One of the key features of the TJA1100 is the possibility to put a link and its associated nodes into Sleep mode, while ensuring that the node can be woken up by activity on the Ethernet wires. A node can be switched to Sleep mode when link operation is not needed, minimizing power consumption.

Figure 8 shows the TJA1100 mode transition diagram. For a detailed description of the Sleep transition process, see the TJA1100 application hints [Ref. 1].

The following events, listed in order of priority, trigger mode transitions:

- Power on/off
- Undervoltage on $V_{DD(IO)}$ or $V_{DDD(1V8)}$
- RST_N input
- EN input
- Overtemperature or Undervoltage on $V_{DDA(3V3)}$, $V_{DDA(1V8)}$ or $V_{DDD(1V8)}$
- SMI command and wake-up (local or remote)



* UV means undervoltage on one of the power supply pins $V_{DD(IO)}$, $V_{DDA(3V3)}$, $V_{DDD(1V8)}$, $V_{DDA(1V8)}$
** INH can be configured to be on or off

Fig 8. Operating mode transitions

6.4 Wake-up request

A link that is in Sleep mode must be woken up before the link can be re-established. The node requesting the link can issue a wake request by sending idle symbols onto the link. The link partner detects the idle activity and wakes up.

For the Master PHY, it is only necessary to enable link control (LINK_CONTROL = 1). The training sequence is then detected as a wake-up request. For the Slave PHY, a link wake-up request is issued by setting bit WAKE_REQUEST in the Extended Control

register to 1 while the TJA1100 is in Normal mode with link control disabled (LINK_CONTROL = 0). The wake request phase lasts at least 5 ms to ensure a reliable wake-up. The TJA1100 aborts this wake request and stops sending idle symbols if bit WAKE_REQUEST is reset or link control is enabled.

6.5 Wake-up

When the TJA1100 detects a wake-up event, a WAKEUP interrupt is generated and the wake-up source is indicated in the General status register (status bits LOCAL_WU, REMOTE_WU and DATA_DET_WU; see Table 26). The wake-up source status bits are reset when the TJA1100 enters Sleep Request or Sleep mode. The TJA1100 distinguishes three wake-up sources:

6.5.1 Remote wake-up

In Standby and Sleep modes, any Ethernet activity on the MDI (idle pulses or Ethernet frames) triggers a remote wake-up.

6.5.2 Local wake-up

In Standby, Sleep Request and Sleep modes, a falling edge on pin WAKE (provided configuration bit LED_ENABLE = 0) triggers a local wake-up.

6.5.3 Wake-up by data detection

In Sleep Request mode, any Ethernet frame detected at the MDI or MII triggers wake-up by data detection.

6.6 Autonomous operation

If the PHY is configured for autonomous operation (either via pin strapping, see Section 6.11, or via bit AUTO_OP in Configuration register 1, see Table 20), the TJA1100 can operate and establish a link without further interaction with a host controller. On power-on or wake-up from Sleep mode, the TJA1100 goes directly to Normal mode once all supply voltages are available and the link-up process starts automatically. AUTO_OP must be reset when link or mode control are configured by the Host.

6.7 Autonomous power-down

If autonomous power-down is enabled via Configuration register 1 (AUTO_PWD = 1), the TJA1100 goes to Sleep Request mode automatically if no Ethernet frames have been received at the MDI and MII for the time-out time, $t_{to(pd)autn}$.

6.8 Transmitter amplitude

Power can be saved by adapting the amplitude of the transmitter output to the specific needs of a link. For example, a short link of up to 2 m does not need to operate on the same transmitter amplitude as a link of 15 m to achieve the same signal-to-noise ratio. The nominal transmitter output amplitude can be selected via bit TX_AMPLITUDE (see Table 20). The default value of 1000 mV can support a link of up to 15 m, while the lower values of 500 mV and 750 mV may be sufficient for shorter links of up to 2 m. The compliance, interoperability and EMC tests are performed at the default amplitude.

6.9 Test modes

Five test modes are supported. Only test modes 1, 2, 4 and 5 are included in 100BASE-T1 [Ref. 2]. The test modes can be individually selected via an SMI command in Normal mode while link control is disabled. The EN pin is used as a clock output in test modes that need a reference clock. The normal EN function is disabled in test modes.

6.9.1 Test mode 1

Test mode 1 is for testing the transmitter droop. In Test mode 1, the PHY transmits '+1' symbols for 600 ns followed by '−1' symbols for a further 600 ns. This sequence is repeated continuously.

6.9.2 Test mode 2

Test mode 2 is for testing the transmitter timing jitter in Master configuration. In test mode 2, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the local external oscillator.

6.9.3 Test mode 3

Test mode 3 is for testing the transmitter timing jitter in Slave configuration. In test mode 3, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the recovered receiver clock.

6.9.4 Test mode 4

Test mode 4 is for testing the transmitter distortion. In test mode 4, the PHY transmits the sequence of symbols generated by the scrambler polynomial gs1 = 1 + x9 + x11.

The bit sequence x0n, x1n is derived from the scrambler according to the following equations:

$$x0n = Scrn[0]$$
$$x1n = Scrn[1] \text{ XOR } Scrn[4]$$

This stream of 3-bit nibbles is mapped to a stream of ternary symbols according to Table 8.

Table 8. Symbol mapping in test mode 4

x1n	x0n	PAM-3 transmit symbol
0	0	0
0	1	+1
1	0	0
1	1	−1

6.9.5 Test mode 5

Test mode 5 is for testing the transmit PSD mask. In test mode 5, the PHY transmits a random sequence of PAM-3 symbols.

6.9.6 Slave jitter test

Selecting the 100BASE-T1 Slave jitter test (SLAVE_JITTER_TEST = 1; see Table 19) in Normal mode with LINK_CONTROL = 1 feeds the transmitter reference clock to pin EN. The normal EN function is disabled in this mode.

6.10 Error diagnosis

6.10.1 Undervoltage detection

Like state-of-the-art CAN and FlexRay transceivers, the TJA1100 monitors the status of the supply voltages continuously. Once a supply voltage drops below the specified minimum operating voltage, the TJA1100 enters the fail-silent Standby mode and communication is halted. A UV_ERR interrupt is generated and the source of the undervoltage ($V_{DDA(1V8)}$, $V_{DDD(1V8)}$ or $V_{DDA(3V3)}$) is indicated in the External status register (Table 27). The under-voltage detection/recovery range is positioned immediately next to the operating range, without a gap. Since parameters are specified down to the min. value of the under-voltage detection threshold, it is guaranteed that the behavior of the TJA1100 is fully specified and defined for all possible voltage condition on the supply pins.

6.10.2 Cabling errors

The TJA1100 can detect open and short circuits between the twisted-pair bus lines when neither of the link partners is transmitting (link control disabled). It may make sense to run the diagnostic before establishing the Ethernet link. When bit CABLE_TEST in the Extended Control register (Table 19) is set to 1, test pulses are transmitted onto the transmission medium with a repetition rate of 666.6 kHz. The TJA1100 evaluates the reflected signals and uses impedance mismatch data along the channel to determine the quality of the link. The results of the cable test are available in the External status register (Table 27) within $t_{to(cbl\_tst)}$. The tests performed and associated results are summarized in Table 9.

Table 9. Cable tests and results

The cable bus lines are designated BI_DA+ and BI_DA−, in alignment with 100BASE-T1 [Ref. 2].

BI_DA+	BI_DA-	Result
open	open	open detected
+ shorted to -	- shorted to +	short detected
shorted to V_{DD}	open	open detected
open	shorted to V_{DD}	open detected
shorted to V_{DD}	shorted to V_{DD}	short detected
shorted to GND	open	open detected
open	shorted to GND	open detected
shorted to GND	shorted to GND	short detected
connected to active link partner (master)	connected to active link partner (master)	short and open detected

6.10.3 Link stability

The signal-to-noise ratio is the parameter used to estimate link stability. The PMA Receive function monitors the signal-to-noise ratio continuously. Once the signal-to-noise ratio falls below a configurable threshold (SQI_FAILLIMIT), the link status is set to FAIL and communication is interrupted. The TJA1100 allows for adjusting the sensitivity of the PMA Receive function by configuring this threshold. The microcontroller can always check the current value of the signal-to-noise ratio via the SMI, allowing it to track a possible degradation in link stability.

6.10.4 Link-fail counter

High losses and/or a noisy channel may cause the link to shut down when reception is no longer reliable. In such cases, a LINK_STATUS_FAIL interrupt is generated by the PHY. Retraining of the link begins automatically provided link control is enabled (LINK_CONTROL = 1).

LOC_RCVR_COUNTER and REM_RCVR_COUNTER in the Link-fail counter register (Table 28) are incremented after every link fail event. Both counters are reset when this register is read.

6.10.5 Jabber detection

The Jabber detection function prevents the PHY being locked in the DATA state of the PCS Receive state diagram when the End-of-Stream Delimiters, ESD1 and ESD2, are not detected. The maximum time the PHY can reside in the DATA state is limited to $t_{to(PCS\text{-}RX)}$ (rcv_max_timer in 100BASE-T1; [Ref. 2]). After this time, the PCS-RX state machine is reset and a transition to PHY Idle state is triggered.

6.10.6 Polarity detection

When the TJA1100 is in Slave configuration, it can detect when the ternary symbols sent from the Master PHY are received with the wrong polarity. A polarity error would occur if the two signal wires of the UTP cable were mixed up at the Slave node connection. If the TJA1100 detects a polarity error in the Slave, it will correct it internally while setting the POLARITY_DETECT bit in the External status register (Table 27).

6.10.7 Interleave detection

A 100BASE-T1 PHY can send two different interleave sequences of ternary symbols, (TAn, TBn) or (TBn, TAn). The receiver in the TJA1100 is able to de-interleave both sequences. The order of the ternary symbols detected by the receiver is indicated by the INTERLEAVE_DETECT bit in the External status register (Table 27).

6.10.8 Loopback modes

The TJA1100 supports three loopback modes:

- Internal loopback (PCS loopback in accordance with 100BASE-T1)
- External loopback
- Remote loopback

6.10.8.1 Internal loopback

In Internal loopback mode, the PCS Receive function gets the ternary symbols A_n and B_n directly from the PCS Transmit function as shown in Figure 9. This action allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS function.

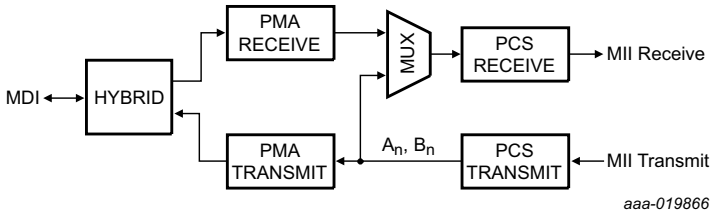


Fig 9. Internal loopback

6.10.8.2 External loopback

In external loopback mode, the PMA Receive function receives signals directly from the PMA Transmit function as shown in Figure 10. This external loopback test allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS and PMA functions.

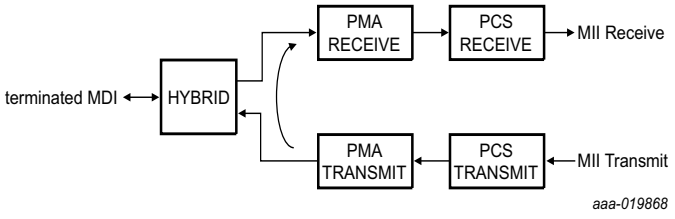


Fig 10. External loopback

6.10.8.3 Remote loopback

In Remote loopback mode, the packet received by the link partner at the MDI is passed through the PMA Receive and PCS Receive functions and forwarded to the PCS Transmit functions, which in turn sends it back to the link partner from where it came. The PCS receive data is made available at the MII. Remote loopback allows the MAC to compare the packets sent to the MDI with the packets received back from the MDI and thus to validate the functionality of the physical channel, including both 100BASE-T1 PHYs. To run the PHY in a loopback mode, the LOOPBACK control bit in the Basic control register should be set before enabling link control.

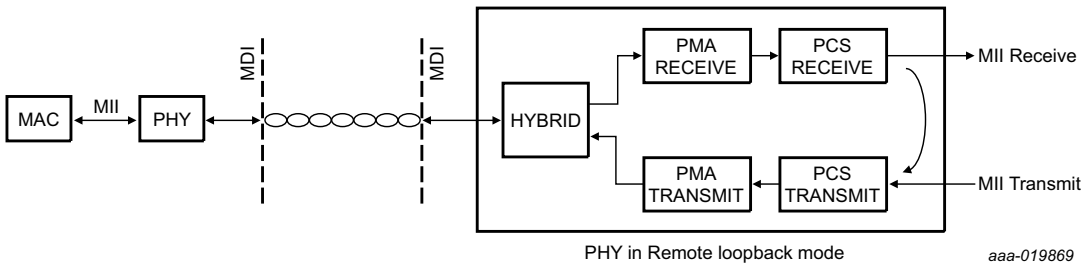


Fig 11. Remote loopback

6.11 Auto-configuration of the PHY during power-up via pin strapping

The logic levels on inputs PHYAD0, PHYAD1 and CONFIG0 to CONFIG3 determine the default configuration of the PHY at power-up or after a hardware reset. Pin strapping occurs during the power-on settling time ($t_{s(pon)}$), once all voltages (including 1V8) are available.

Pin strapping at pins 23 (PHYAD1) and 24 (PHYAD0) determine bits 1 and 0, respectively, of the PHY address used for the SMI address/Cipher scrambler. The PHY address cannot be changed once the PHY has been configured. Besides the address configured via pin strapping, the TJA1100 can always be accessed via address 0.

Table 10. Hardware configuration via CONFIG0 to CONFIG3 pin strapping during power-up

Pin	Value	Description
CONFIG0 (pin 22)	HIGH	PHY configured as Master
	LOW	PHY configured as Slave
CONFIG1 (pin 21)	HIGH	Autonomous operation
	LOW	Managed operation
CONFIG3/CONFIG2 (pin 17/pin 18)	LOW LOW	Normal MII mode
	LOW HIGH	RMII mode (external 50 MHz oscillator)
	HIGH LOW	RMII mode (25 MHz crystal)
	HIGH HIGH	Reverse MII mode

6.12 SMI registers

6.12.1 SMI register mapping

Table 11. SMI register mapping

Register index (dec)	Register name	Group
0	Basic control register	Basic
1	Basic status register	Basic
2	PHY identification register 1	Extended
3	PHY identification register 2	Extended
15	Extended status register	Extended
16	PHY identification register 3	NXP specific
17	Extended control register	NXP specific
18	Configuration register 1	NXP specific
19	Configuration register 2	NXP specific
20	Symbol error counter register	NXP specific
21	Interrupt source register	NXP specific
22	Interrupt enable register	NXP specific
23	Communication status register	NXP specific
24	General status register	NXP specific
25	External status register	NXP specific
26	Link-fail counter register	NXP specific

Table 12. Register notation

Notation	Description
R/W	Read/write
R	Read only
LH	Latched HIGH
LL	Latched LOW
SC	Self-clearing
CR	Cleared on reset

Table 13. Basic control register (Register 0)

Bit	Symbol	Access	Value	Description
15	RESET	R/W SC		software reset control:
			0[1]	normal operation
			1	PHY reset
14	LOOPBACK	R/W		loopback control:
			0[1]	normal operation
			1	loopback mode
13	SPEED_SELECT (LSB)	R/W	[2]	speed select (LSB):
			0	10 Mbit/s if SPEED_SELECT (MSB) = 0 1000 Mbit/s if SPEED_SELECT (MSB) = 1
			1[1]	100 Mbit/s if SPEED_SELECT (MSB) = 0 reserved if SPEED_SELECT (MSB) = 1
12	AUTONEG_EN	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
11	POWER_DOWN	R/W		Standby power down enable:
			0[1]	normal operation (clearing this bit automatically triggers a transition to Normal mode; control bits POWER_MODE must be set to 0011 to select Normal mode, see Table 19)
			1	power down and switch to Standby mode (provided ISOLATE = 0; ignored if ISOLATE = 1 and CONTROL_ERR interrupt generated)
10	ISOLATE	R/W		PHY isolation:
			0[1]	normal operation
			1	isolate PHY from MII/RMII (provided POWER_DOWN = 0; ignored if POWER_DOWN = 1 and CONTROL_ERR interrupt generated)
9	RE_AUTONEG	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
8	DUPLEX_MODE	R/W	1[1]	only full duplex supported; always 1; a write access is ignored.
7	COLLISION_TEST	R/W	0[1]	COL signal test not supported; always 0; a write access is ignored.
6	SPEED_SELECT (MSB)	R/W	[2]	speed select (MSB):
			0[1]	10 Mbit/s if SPEED_SELECT (LSB) = 0 100 Mbit/s if SPEED_SELECT (LSB) = 1
			1	1000 Mbit/s if SPEED_SELECT (LSB) = 0 reserved if SPEED_SELECT (LSB) = 1

Table 13. Basic control register (Register 0) *…continued*

Bit	Symbol	Access	Value	Description
5	UNIDIRECT_EN	R/W		unidirectional enable when bit 12 = 0 and bit 8 = 1:
			0[1]	enable transmit from MII only when the PHY has determined that a valid link has been established
			1	enable transmit from MII regardless of whether the PHY has determined that a valid link has been established
4:0	reserved	R/W	00000[1]	always write 00000; ignore on read

[1] Default value.

[2] Speed Select: 00: 10 Mbit/s; 01: 100 Mbit/s; 10: 1000 Mbit/s; 11: reserved; a write access value other than 01 is ignored.

Table 14. Basic status register (Register 1)

Bit	Symbol	Access	Value	Description
15	100BASE-T4	R	0[1]	PHY not able to perform 100BASE-T4
			1	PHY able to perform 100BASE-T4
14	100BASE-X_FD	R	0[1]	PHY not able to perform 100BASE-X full duplex
			1	PHY able to perform 100BASE-X full duplex
13	100BASE-X_HD	R	0[1]	PHY not able to perform 100BASE-X half duplex
			1	PHY able to perform 100BASE-X half duplex
12	10Mbps_FD	R	0[1]	PHY not able to perform 10 Mbit/s full duplex
			1	PHY able to perform 10 Mbit/s full duplex
11	10Mbps_HD	R	0[1]	PHY not able to perform 10 Mbit/s half duplex
			1	PHY able to perform 10 Mbit/s half duplex
10	100BASE-T2_FD	R	0[1]	PHY not able to perform 100BASE-T2 full duplex
			1	PHY able to perform 100BASE-T2 full duplex
9	100BASE-T2_HD	R	0[1]	PHY not able to perform 100BASE-T2 half duplex
			1	PHY able to perform 100BASE-T2 half duplex
8	EXTENDED_STATUS	R	0	no extended status information in register 15h
			1[1]	extended status information in register 15h
7	UNIDIRECT_ ABILITY	R	0	PHY able to transmit from MII only when the PHY has determined that a valid link has been established
			1[1]	PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	MF_PREAMBLE_SUPPRESSION	R	0	PHY will not accept management frames with preamble suppressed
			1[1]	PHY will accept management frames with preamble suppressed
5	AUTONEG_COMPLETE	R	0	Autonegotiation process not completed
			1[1]	Autonegotiation process completed
4	REMOTE_FAULT	R LH	0[1][2]	no remote fault condition detected
			1	remote fault condition detected
3	AUTONEG_ABILITY	R	0[1]	PHY not able to perform Autonegotiation
			1	PHY able to perform Autonegotiation
2	LINK_STATUS	R LL	0[1][2]	link is down
			1	link is up
1	JABBER_DETECT	R LH	0[1][2]	no jabber condition detected
			1	jabber condition detected
0	EXTENDED_CAPABILITY	R	0	basic register set capabilities only
			1[1]	extended register capabilities

[1] Default value.

[2] Reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 15. PHY identification register 1 (Register 2)

Bit	Symbol	Access	Value	Description
15:0	PHY_ID	R	0180h[1]	bits 3 to 18 of the Organizationally Unique IDentifier (OUI)[2]

[1] Default value.

[2] OUI = 00.60.37h (note that bits 1 and 2 of OUI are always 0).

Table 16. PHY identification register 2 (Register 3)

Bit	Symbol	Access	Value	Description
15:10	PHY_ID	R	110111[1]	bits 19 to 24 of the OUI[2]
9:4	TYPE_NO	R	000100[1]	six-bit manufacturer's type number
3:0	REVISION_NO	R	0001[1]	four-bit manufacturer's revision number

[1] Default value.

[2] OUI = 00.60.37h (note that bits 1 and 2 of OUI are always 0).

Table 17. Extended status register (Register 15)

Bit	Symbol	Access	Value	Description
15	1000BASE-X_FD	R	0[1]	PHY not able to perform 1000BASE-X full duplex
			1	PHY able to perform 1000BASE-X full duplex
14	1000BASE-X_HD	R	0[1]	PHY not able to perform 1000BASE-X half duplex
			1	PHY able to perform 1000BASE-X half duplex
13	1000BASE-T_FD	R	0[1]	PHY not able to perform 1000BASE-T full duplex
			1	PHY able to perform 1000BASE-T full duplex
12	1000BASE-T_HD	R	0[1]	PHY not able to perform 1000BASE-T half duplex
			1	PHY able to perform 1000BASE-T half duplex
11:8	reserved	R	-	
7	100BASE-T1	R	0	PHY not able to 1-pair 100BASE-T1 100 Mbit/s
			1[1]	PHY able to 1-pair 100BASE-T1 100 Mbit/s
6	1000BASE-T1	R	0[1]	PHY not able to perform 1000BASE-T1
			1	PHY able to perform 1000BASE-T1
5:0	reserved	R	-	

[1] Default value.

Table 18. PHY identification register 3 (Register 16)

Bit	Symbol	Access	Value	Description
15:8	reserved	R	-	
7:0	VERSION_NO	R	xxh	8-bit manufacturer's firmware revision number

Table 19. Extended control register (Register 17)

Bit	Symbol	Access	Value	Description
15	LINK_CONTROL	R/W	[1]	link control enable:
			0	link control disabled
			1	link control enabled
14:11	POWER_MODE	R/W	[2]	operating mode select:
			0000[3]	no change
			0011	Normal mode
			1100	Standby mode
			1011	Sleep Request mode
10	SLAVE_JITTER_TEST	R/W		enable/disable Slave jitter test
			0[3]	disable Slave jitter test
			1	enable Slave jitter test
9	TRAINING_RESTART	R/W SC		Autonegotiation process restart:
			0[3]	halts the training phase
			1	forces a restart of the training phase
8:6	TEST_MODE	R/W		test mode selection:
			000[3]	no test mode
			001	100BASE-T1 test mode 1
			010	100BASE-T1 test mode 2
			011	test mode 3
			100	100BASE-T1 test mode 4
			101	100BASE-T1 test mode 5
			110	scrambler and descrambler bypassed
			111	reserved
5	CABLE_TEST	R/W SC		TDR-based cable test:
			0[3]	stops TDR-based cable test
			1	forces TDR-based cable test
4:3	LOOPBACK_MODE	R/W		loopback mode select:
			00[3]	internal loopback
			01	external loopback
			10	external loopback
			11	remote loopback
2	CONFIG_EN	R/W		configuration register access:
			0[3]	configuration register access disabled
			1	configuration register access enabled
1	CONFIG_INH	R/W		INH configuration:
			0	INH switched off in Disable mode
			1[3]	INH switched on in Disable mode
0	WAKE_REQUEST[4]	R/W		wake-up request configuration:
			0[3]	no wake-up signal to be transmitted
			1	transmit idle symbols as bus wake-up request