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TJA1145

High-speed CAN transceiver for partial networking

Rev. 4 — 09 May 2018 Product data sheet

1. General description

The TJA1145 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1145 features very low power consumption in Standby and Sleep modes and supports ISO 11898-2:2016 compliant CAN Partial Networking by means of a selective wake-up function.

A dedicated implementation of the partial networking function has been embedded into the TJA1145/FD variants TJA1145T/FD and TJA1145TK/FD (see Section 7.3.2 for further details on CAN FD). This function is called ‘FD-passive’ and is the ability to ignore CAN FD frames while waiting for a valid wake-up frame in Sleep/Standby mode. This additional feature of partial networking is the perfect fit for networks that support both CAN FD and standard CAN 2.0 communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

Advanced power management regulates the supply throughout the node and supports local and remote wake-up functionality. I/O levels are automatically adjusted to the I/O levels of the controller, allowing the TJA1145 to interface directly with 3.3 V to 5 V microcontrollers. An SPI interface is provided for transceiver control and for retrieving status information. Bus connections are truly floating when power is off.

The TJA1145 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-4. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 2 Mbit/s.

These features make the TJA1145 the ideal choice for high-speed CAN networks containing nodes that are always connected to the battery supply line but, in order to minimize current consumption, are only active when required by the application.

2. Features and benefits

2.1 General

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-4 compliant
- Timing guaranteed for data rates up to 2 Mbit/s
- Autonomous bus biasing according to ISO 11898-2:2016
- Optimized for in-vehicle high-speed CAN communication
- No ‘false’ wake-ups due to CAN FD in TJA1145/FD variants

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC 61000-4-2 on pins BAT and WAKE and on the CAN bus pins
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins protected against transients according to ISO 7637-3, test pulses 1, 2a, 3a and 3b.
- Suitable for use in 12 V and 24 V systems
- Available in SO14 and leadless HVSON14 package (3 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- AEC-Q100 qualified
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Advanced ECU power management system

- Very low-current Standby and Sleep modes, with full wake-up capability
- Entire node can be powered down via the inhibit output
- Remote wake-up capability via standard CAN wake-up pattern or via ISO 11898-2:2016 compliant selective wake-up frame detection
- Local wake-up via the WAKE pin
- Wake-up source recognition
- Bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s supported during selective wake-up'
- Local and/or remote wake-up can be disabled to reduce current consumption
- Transceiver disengages from the bus when the battery supply is removed
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers

2.4 Protection and diagnosis

- 16-, 24- or 32-bit SPI for configuration, control and diagnosis
- Transmit Data (TXD) dominant time-out function with diagnosis
- Overtemperature warning and shut-down
- Undervoltage detection and recovery on pins VCC, VIO and BAT
- Cold start diagnosis (via bits PO and NMS)
- Advanced system and transceiver interrupt handling

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3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage		4.5	-	28	V
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.85	-	5.5	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4.5	-	4.75	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	V_{BAT} > 4.5 V	2.7	-	2.85	V
I_{BAT}	battery supply current	Normal mode	-	1	1.5	mA
		Sleep mode; CAN Offline mode; −40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	40	59	µA
		Standby mode; CAN Offline mode; −40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	44	68	µA
I_{CC}	supply current	CAN Active mode; CAN recessive; V_{TXD} = V_{IO}	-	3	6	mA
		CAN Active mode; CAN dominant; V_{TXD} = 0 V	-	45	65	mA
		Standby/Normal mode; CAN inactive; −40 °C < T_{vj} < 85 °C	-	4.7	8.5	µA
		Sleep mode; CAN inactive; −40 °C < T_{vj} < 85 °C	-	3.8	7	µA
I_{IO}	supply current on pin V_{IO}	Standby/Normal mode; −40 °C < T_{vj} < 85 °C	-	7.1	11	µA
		Sleep mode; −40 °C < T_{vj} < 85 °C	-	5	8	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH, CANL	−6	-	+6	kV
V_{CANH}	voltage on pin CANH		−58	-	+58	V
V_{CANL}	voltage on pin CANL		−58	-	+58	V
T_{vj}	virtual junction temperature		−40	-	+150	°C

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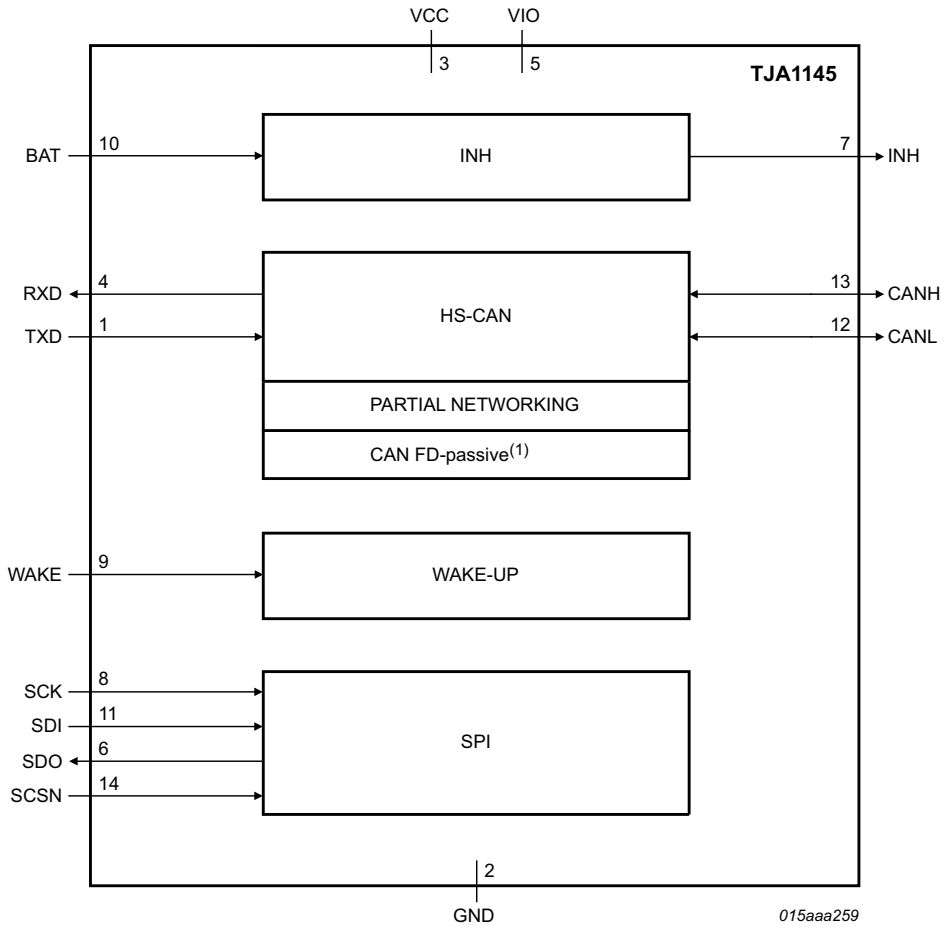
4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1145T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145T/FD	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145TK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
TJA1145TK/FD	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

5. Block diagram



(1) TJA1145T/FD and TJA1145TK/FD only.

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

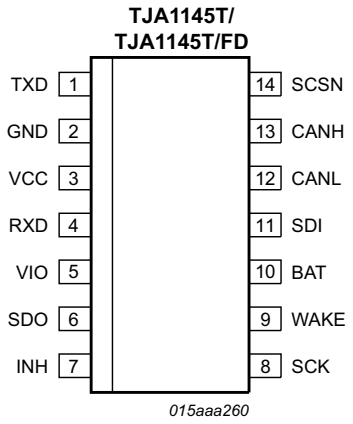

Fig 2. Pin configuration diagram: SO14

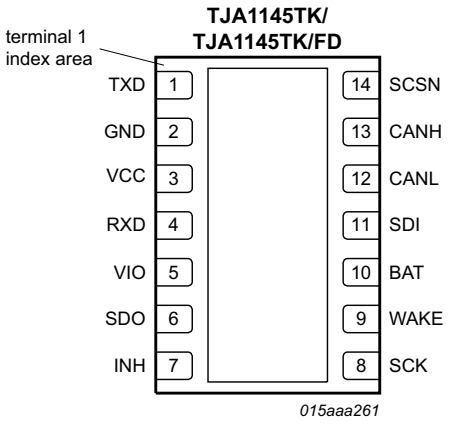

Fig 3. Pin configuration diagram: HVSON14 Transparent top view

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
VCC	3	5 V CAN transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
VIO	5	supply voltage for I/O level adaptor
SDO	6	SPI data output
INH	7	inhibit output for switching external voltage regulators
SCK	8	SPI clock input
WAKE	9	local wake-up input
BAT	10	battery supply voltage
SDI	11	SPI data input
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
SCSN	14	SPI chip select input

[1] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground

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7. Functional description

The TJA1145 is a stand-alone high-speed CAN transceiver containing a variety of fail-safe and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver combines the functionality of the TJA1043 with ISO 11898-2:2016 compliant CAN partial networking and autonomous bus biasing.

7.1 System controller

The system controller manages register configuration and controls the internal functions of the TJA1145. Detailed device status information is collected and made available to the microcontroller.

7.1.1 Operating modes

The system controller contains a state machine that supports five operating modes: Normal, Standby, Sleep, Overtemp and Off. The state transitions are illustrated in Figure 4.

7.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, the TJA1145 is fully operational. All device hardware is available and can be activated (see Table 4).

Normal mode can be selected from Standby or Sleep mode via an SPI command (MC = 111).

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the TJA1145, featuring low current consumption. The transceiver is unable to transmit or receive data in Standby mode, but the INH pin remains active so voltage regulators controlled by this pin will be active.

If remote CAN wake-up is enabled (CWE = 1; see Table 22), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1; otherwise standard wake-up is enabled).

Pin RXD is forced LOW when any enabled wake-up or interrupt event is detected (see Section 7.6).

The TJA1145 switches to Standby mode:

- from Off mode if the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$.
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$.
- from Sleep mode on the occurrence of a wake-up or interrupt event (see Section 7.6)
- from Normal or Sleep mode via an SPI command (MC = 100)
- from Normal mode if Sleep mode is selected via an SPI command (MC = 001) while a wake-up event is pending or all wake-up sources are disabled

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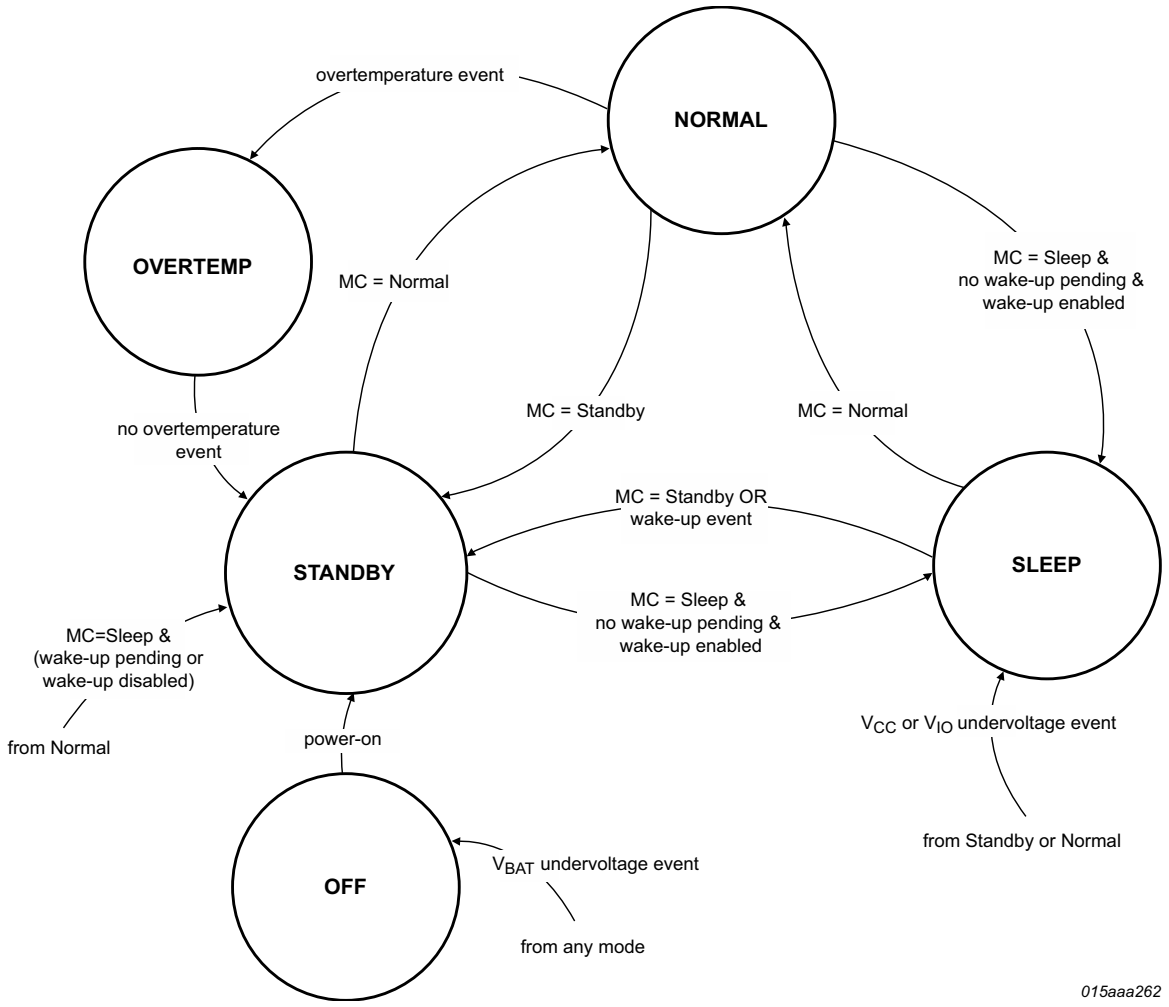

Fig 4. TJA1145 system controller state diagram

7.1.1.3 Sleep mode

Sleep mode is the second-level power saving mode of the TJA1145. In Sleep mode, the transceiver behaves as in Standby Mode with the exception that pin INH is set to a high-ohmic state. Voltage regulators controlled by this pin will be switched off, and the current into pin BAT will be reduced to a minimum.

Any enabled wake-up or interrupt event (except SPIF), or an SPI command (provided a valid V_{IO} voltage is connected), will wake up the transceiver from Sleep mode.

Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001). The TJA1145 will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source (CAN bus or WAKE pin; see Section 7.6) is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the TJA1145 to switch to Standby mode.

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The TJA1145 will also be forced to switch to Sleep mode if a V_{CC} of V_{IO} undervoltage event is detected ($V_{CC}/V_{IO} < V_{UVD(VCC)}/V_{UVD(VIO)}$ for longer than $t_{det(uv)(VCC)}/t_{det(uv)(VIO)}$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock (see Section 7.11) and selective wake-up is disabled (CPNC = 0).

Status bit FSMS in the Main status register (Table 6) indicates whether a transition to Sleep mode was selected via an SPI command (FSMS = 0) or was forced by an undervoltage event on VCC or VIO (FSMS = 1). This bit can be read after the TJA1145 wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

7.1.1.4 Off mode

The TJA1145 will be in Off mode when the battery voltage is too low to supply the IC. This is the default mode when the battery is first connected. The TJA1145 will switch to Off mode from any mode if the battery voltage drops below the power-off threshold ($V_{th(det)poff}$). In Off mode, the CAN pins and pin INH are in a high-ohmic state.

When the battery supply voltage rises above the power-on threshold ($V_{th(det)pon}$), the TJA1145 starts to boot up, triggering an initialization procedure. The TJA1145 will switch to Standby mode after $t_{startup}$.

7.1.1.5 Overtemp mode

Overtemp mode is provided to prevent TJA1145 being damaged by excessive temperatures. The TJA1145 switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the TJA1145 issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, status bit OTWS is set and an overtemperature interrupt is generated (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. No wake-up event will be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD.

The TJA1145 exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

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7.1.1.6 Hardware characterization for the TJA1145 operating modes

Table 4. Hardware characterization by functional block

Block	Operating mode				
	Off	**Standby**	**Normal**	**Sleep**	**Overtemp**
SPI	disabled	active	active	active if V_{IO} supplied[1]	disabled
INH	high-ohmic	V_{BAT} level	V_{BAT} level	high-ohmic	V_{BAT} level
CAN	off	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 7)	Offline	off
RXD	V_{IO} level	V_{IO} level/LOW if wake-up event detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V_{IO} level/LOW if wake-up event detected	V_{IO} level/LOW if wake-up pending

[1] SPI speed is limited in Sleep mode (see Table 35).

7.1.2 System control registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 7.12).

Table 5. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the TJA1145 has entered Normal mode after initial power-up. Bit FSMS indicates whether the most recent transition to Sleep mode was triggered by an undervoltage event or by an SPI command.

Table 6. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	FSMS	R		Sleep mode transition status:
			0	transition to Sleep mode triggered by an SPI command
			1	an undervoltage on VCC and/or VIO forced a transition to Sleep mode
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	TJA1145 has entered Normal mode (after power-up)
			1	TJA1145 has powered up but has not yet switched to Normal mode
4:0	reserved	R	-	

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7.2 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2016 compliant (defining high-speed CAN with selective wake-up functionality and autonomous bus biasing). The CAN transmitter is supplied via pin VCC while the CAN receiver is supplied via pin BAT. The TJA1145 includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 2 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11).

Autonomous biasing is active in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller or when CAN partial networking is enabled. The TJA1145 ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

7.2.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 5). The CAN transceiver operating mode depends on the TJA1145 operating mode and on the setting of bits CMC in the CAN control register (Table 7).

When the TJA1145 is in Normal mode, the CAN transceiver operating mode (Offline, Active or Listen-only) can be selected via bits CMC in the CAN control register (Table 7). When the TJA1145 is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

7.2.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, V_{CC} undervoltage detection is enabled and the transceiver switches to CAN Offline or CAN Offline Bias mode when the voltage on V_{CC} drops below the 90 % threshold. When CMC = 10, V_{CC} undervoltage detection is disabled. The transmitter will remain active until the TJA1145 is forced into Sleep mode by the V_{CC} undervoltage event; the transceiver will then switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

- the TJA1145 is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10 (see Table 7) and:

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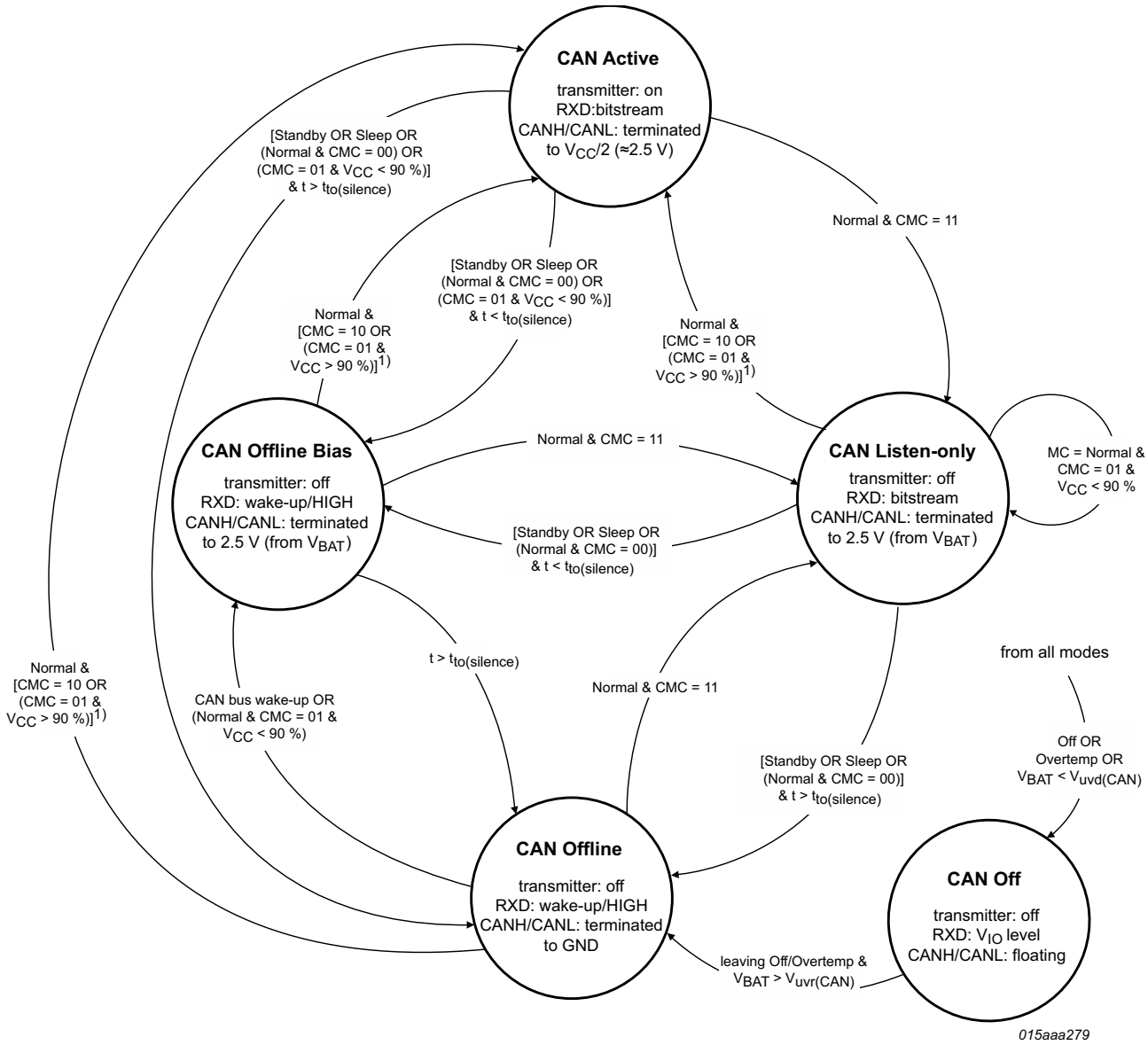
– if CMC = 01, the voltage on pin VCC is above the V_{CC} undervoltage detection threshold ($V_{uvd(VCC)}$)

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from V_{CC}.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 5. CAN transceiver state machine

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The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (Table 8).

7.2.1.2 CAN Listen-only mode

CAN Listen-only mode allows the TJA1145 to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the TJA1145 is in Normal mode and CMC = 11

The CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 while the voltage on V1 is below the 90 % undervoltage threshold.

7.2.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode or CAN Listen-only mode if:

- the TJA1145 switches to Standby or Sleep mode OR
- the TJA1145 is in Normal mode and CMC = 00

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode if CMC = 01 and the voltage on VCC drops below the 90 % undervoltage threshold or if CMC = 10 and the TJA1145 switches to Sleep mode in response to a V_{CC} undervoltage event.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR

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- when the TJA1145 switches from Off or Overtemp mode to Standby mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern (according to ISO 11898-2:2016) is detected on the CAN bus OR
- the CAN transceiver is in Normal mode, CMC = 01 and V_{CC} < 90 %

7.2.1.4 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the TJA1145 switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the CAN transceiver is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the CAN transceiver is lost.

7.2.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the TJA1145 will monitor the bus for a standard wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The TJA1145 wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2:2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 19) and pin RXD is driven LOW. If the TJA1145 was in Sleep mode when the wake-up pattern was detected, it will switch pin INH to V_{BAT} to activate external voltage regulators (e.g. for supplying V_{CC} and V_{IO}) and enter Standby mode.

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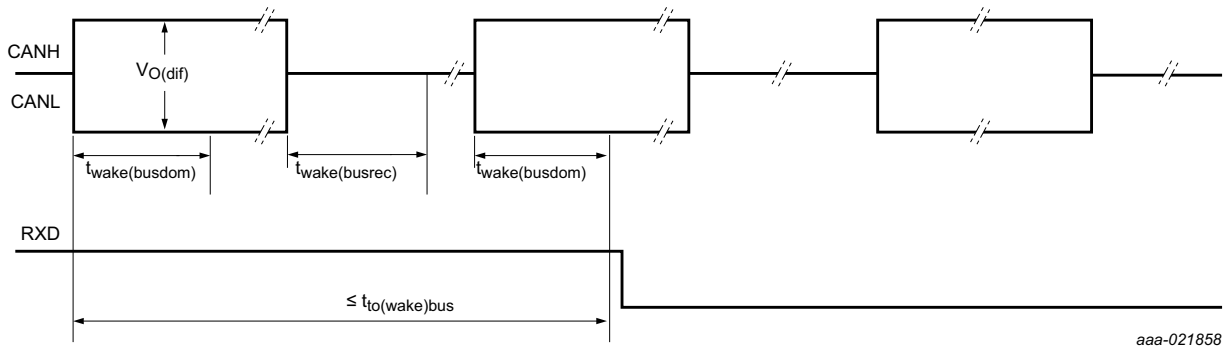

Fig 6. CAN wake-up timing

7.2.3 CAN control and Transceiver status registers

Table 7. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	CFDC	R/W		CAN FD tolerance (TJA1145T/FD and TJA1145TK/FD only; otherwise ignored)
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection:
			00	Offline mode
			01	Active mode (when the TJA1145 is in Normal mode); V_{CC} 90 % undervoltage detection active
			10	Active mode (when the TJA1145 is in Normal mode); V_{CC} undervoltage detection inactive; TJA1145 switches from Normal to Off mode when $V_{BAT} < V_{uvd(CAN)}$
			11	Listen-only mode

Table 8. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode

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Table 8. Transceiver status register (address 22h) *…continued*

Bit	Symbol	Access	Value	Description
6	CPNERR	R		CAN partial networking error status:
			0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0); wake-up via standard wake-up pattern only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration OK (PNCOK = 1)
4	COSCS	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$
2	reserved	R	-	
1	VCS[1]	R		V_{CC} supply voltage status:
			0	V_{CC} is above the undervoltage detection threshold ($V_{uvd(VCC)}$)
			1	V_{CC} is below the undervoltage detection threshold ($V_{uvd(VCC)}$)
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

[1] Only active when CMC = 01.

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7.3 CAN partial networking

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

7.3.1 Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO 11898-1:2015, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 12).

A valid WUF identifier is defined and stored in the ID registers (Table 10). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the mask registers (Table 11), where a 1 means ‘don’t care’.

In the example illustrated in Figure 7, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D) are set to 1, which means that the corresponding identifier bits are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).

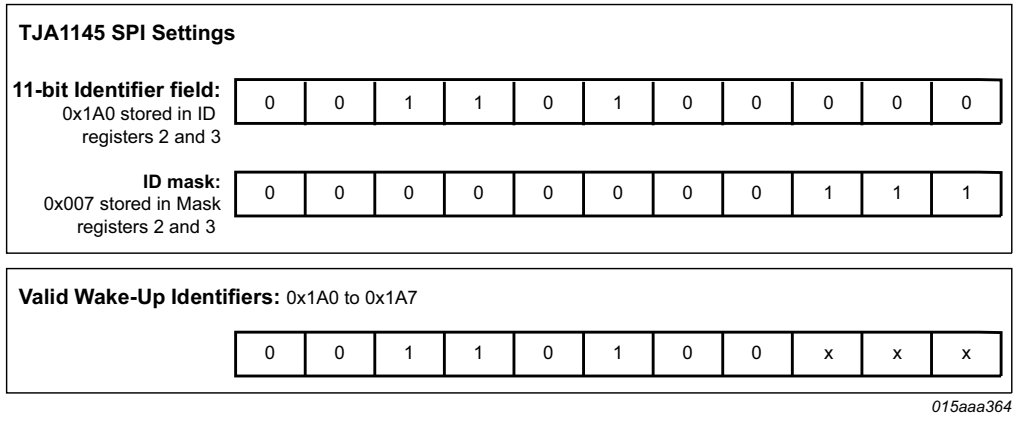

Fig 7. Evaluating the ID field in a selective wake-up frame

The data field indicates which nodes are to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

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The data length code (bits DLC in the Frame control register; Table 12) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 13) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 byes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see Table 31). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

In the example illustrated in Figure 8, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 13 and Figure 9). Data mask 7 is defined as 10101000 in the example. This means that up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1.

The received message shown in Figure 8 could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

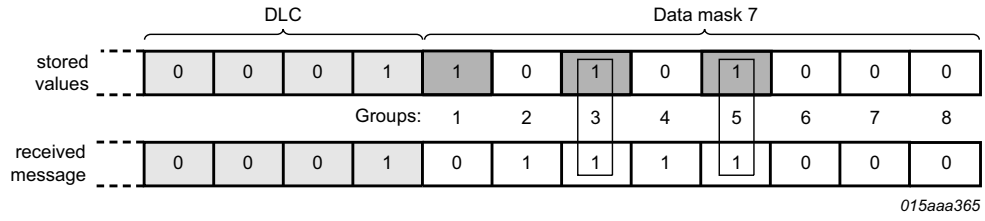

Fig 8. Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included in the wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND

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- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

If the TJA1145 receives a CAN message containing errors (e.g. a 'stuffing' error) transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The TJA1145 clears PNCOK after a write access to any of the CAN partial networking configuration registers (see Section 7.3.3).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern (according to ISO 11898-2:2016) will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC $\neq$ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see Table 9).

7.3.2 CAN FD frames

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as specified in ISO 11898-1:2015.

CAN FD is being gradually introduced into the automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes). The TJA1145x/FD variants support FD-passive features by means of a dedicated implementation of the partial networking protocol.

These variants can be configured to recognize CAN FD frames as valid frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The TJA1145x/FD remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the TJA1145x/FD ignores further bus signals until idle is again detected.

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CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2016 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module in the TJA1145, and in the TJA1145xFD variants when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

7.3.3 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 9. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 10. ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 11. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format

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Table 11. ID mask registers 0 to 3 (addresses 2Bh to 2Eh) *…continued*

Addr.	Bit	Symbol	Access	Value	Description
2Dh	7:2	M23:M18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 12. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected; DM0 ignored

Table 13. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

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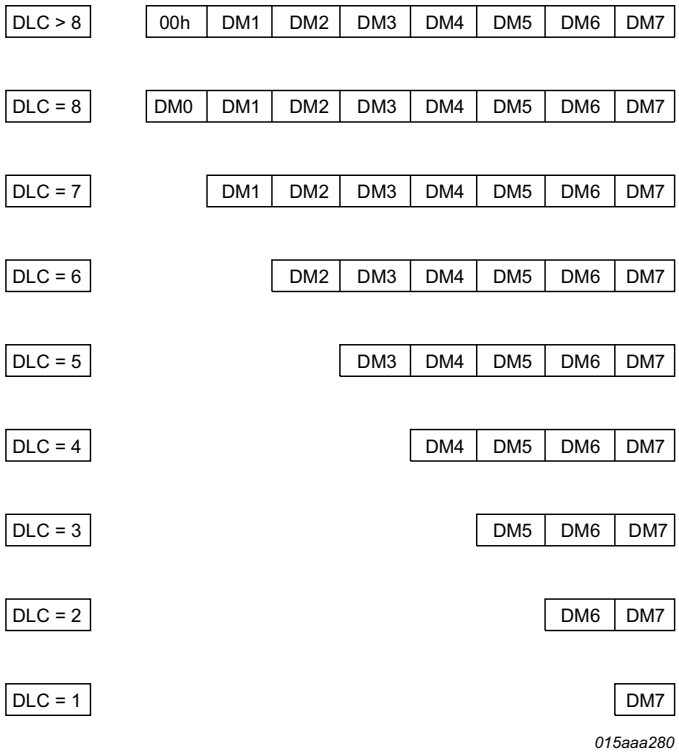

Fig 9. Data mask register usage for different values of DLC

7.4 Fail-safe features

7.4.1 TXD dominant time-out

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (CF = 1; see Table 19), if enabled (CFE = 1; see Table 22). In addition, the status of the TXD dominant time-out can be read via the CFS bit in the Transceiver status register (Table 8) and bit CTS is set to 0.

7.4.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V_{IO} to ensure a safe defined recessive driver state in case the pin is left floating.

7.4.3 V_{CC} undervoltage event

An enabled CAN failure interrupt is generated (CF = 1) when the CAN transceiver supply voltage on VCC falls below the undervoltage detection threshold ($V_{UVD(VCC)}$), provided CMC = 01. In addition, status bit VCS is set to 1.

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7.4.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

7.5 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 23). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 14. WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the TJA1145 is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

7.6 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the TJA1145 is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (Table 18 to Table 20) and is signaled on pin RXD pin, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the TJA1145 to switch to Sleep mode; see Section 7.1.1.3).

Table 15. Regular wake-up events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

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Table 16. Interrupt events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	the TJA1145 has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (only detected in Normal mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal MC code or attempted write access to locked register (an SPI failure event will not wake-up the TJA1145 from Sleep mode)
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected (not is Sleep mode): - CAN transceiver deactivated due to a dominant clamped TXD - CAN transceiver deactivated due to a V_{CC} undervoltage event (if CMC = 01)

PO and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 21 to Table 23).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the TJA1145 is in Sleep mode when an event (other than a SPIF interrupt) occurs, pin INH is forced HIGH and the TJA1145 switches to Standby mode. If the TJA1145 is in Standby mode when the event occurs, pin RXD is forced LOW to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby mode. The detection of any enabled wake-up or interrupt event other than a SPIF interrupt will trigger a wake-up in Sleep mode.

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 17), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant table (Table 18, Table 19 or Table 20 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

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7.6.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The TJA1145 incorporates an interrupt/wake-up delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d(event)}$, pin RXD remains HIGH (since there are no pending events). The event capture registers can be read at any time.

7.6.2 Sleep mode protection

It is very important that event detection is configured correctly when the TJA1145 switches to Sleep mode to ensure it will respond to a wake-up event. For this reason, and to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the TJA1145 switches to Sleep mode. Otherwise the TJA1145 will switch to Standby mode in response to a go-to-sleep command (MC = 001).

7.6.3 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 17. Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	reserved	R	-	
0	SYSE	R		system event:
			0	no pending system event
			1	system event pending at address 0x61

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Table 18. System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	PO[1]	R/W		power-on:
			0	no recent battery power-on
			1	the TJA1145 has left Off mode after battery power-on
3	reserved	R	-	
2	OTW	R/W		overtemperature warning:
			0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W		SPI failure:
			0	no SPI failure detected
			1	SPI failure detected
0	reserved	R	-	

[1] PO is cleared when the TJA1145 is forced to Sleep mode due to an undervoltage event. The information stored in PO could be lost if the transition to Sleep mode was forced by an undervoltage event. Bit NMS, which is set to 0 when the TJA1145 switches to Normal mode after power-on, compensates for this.

Table 19. Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W		CAN-bus status:
			0	CAN-bus active
			1	no activity on CAN-bus for $t_{to(silence)}$
3:2	reserved	R	-	
1	CF[1]	R/W		CAN failure:
			0	no CAN failure detected
			1	CAN failure event detected
0	CW	R/W		CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected

[1] CF is only enabled in Normal mode while the transceiver is in CAN Active mode and is triggered if TXD is clamped dominant OR a V_{CC} undervoltage is detected (when CMC = 01).

Table 20. WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	

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