Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

## Features

- **Contactless Read/Write Data Transmission**
- **992-bit EEPROM User Programmable in 31 Blocks × 32 Bits**
- **Inductively Coupled Power Supply at 125 kHz**
- **Basic Component: R/W IDIC® Transponder IC**
- **Built-in Coil and Capacitor for Circuit Antenna**
- **Starts with Cyclical Data Read Out**
- **Typical < 50 ms to Write and Verify a Block**
- **Modulation Defeat (for EAS)**
- **Direct Access to Each Block**
- **Configurable POR Delay**
- **Write Protection by Lock Bits**
- **Malprogramming Protection**
- **Configurable Options:**
  - **Bit Rate [Bit/s]: RF/16 and RF/32**
  - **Modulation: Manchester**
  - **POR Delay: 1 ms/65 ms**
  - **Maximum Block: 0, 1, 1 to 2, 1 to 3, 1 to 4, .... 1 to 31**

## Applications

- **Industrial Asset Management**
- **Process Control and Automation**
- **Installation and Medical Equipment**

## Description

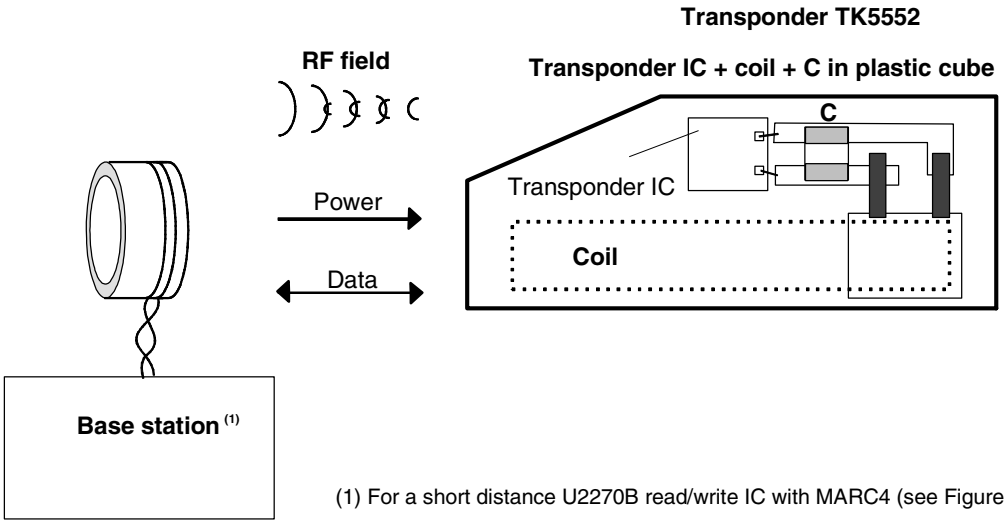
The TK5552 is a complete programmable R/W transponder that implements all important functions for identification systems. It allows the contactless reading (uplink) and writing (downlink) of data which are transmitted bi-directionally between a read/write base station and the transponder. It is a plastic cube device which accomodates the IDIC transponder IC and the antenna is realized as an LC circuit. No additional external power supply is necessary for the transponder because it receives power from the RF field generated by the base station. Data is transmitted by modulating the amplitude of the RF field (uplink mode). The TK5552 can be used to adjust and modify the ID code or any other stored data, e.g., rolling code systems. The on-chip 1056-bit EEPROM (32 blocks, 33 bits per block) can be read (uplink) and written (downlink) blockwise from the base station. The blocks can be protected against overwriting. One block is reserved for setting the operation modes of the IC.

# Read/Write Transponder

# TK5552

Rev. 4698A–RFID–04/03

**Figure 1.** Transponder and Base Station




(1) For a short distance U2270B read/write IC with MARC4 (see Figure 12)

## General

The transponder is the mobile part of a closed coupled identification system (see Figure 1), where the read/write base station incorporates a reader IC such as the U2270B, and the read/write transponder is based on the transponder IDIC.

The transponder is a plastic cube device consisting of the following parts:

- The transponder antenna, realized as a tuned LC circuit
- The read/write IDIC (transponder IC) with EEPROM

## Transponder Antenna

The antenna consists of a coil and a capacitor for tuning the circuit to the nominal carrier frequency of 125 kHz. The coil has a ferrite core to improve the distance of read (uplink) and write (downlink) operations.

## Read/Write IDIC

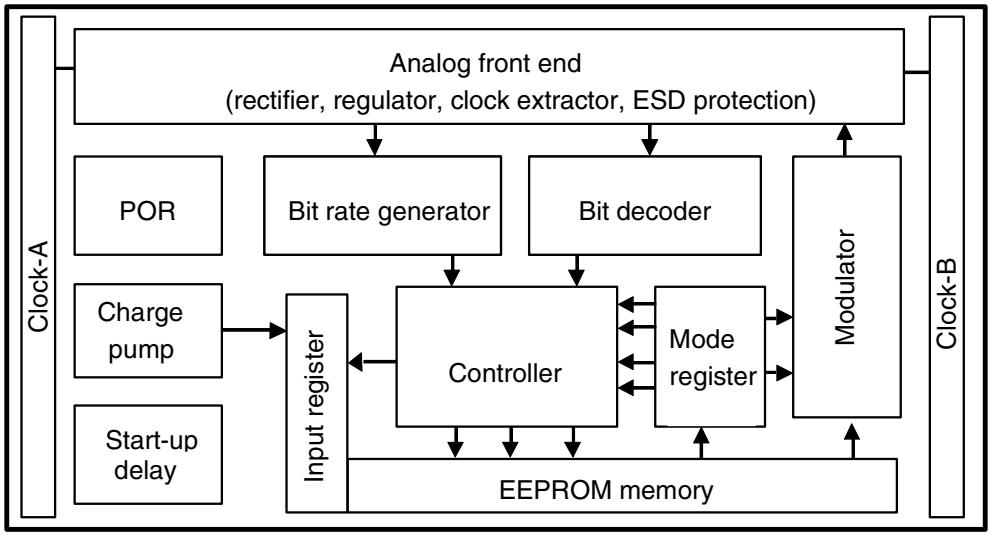
The read/write Transponder IDIC is part of the transponder TK5552. The data is transmitted bi-directionally between the base station and the transponder. The transponder receives power via a single coil from the RF signal generated by the base station. The single coil is connected to the chip and also serves as the IC's bi-directional communication interface.

Data transmission is done by modulating the amplitude of the RF signal. Reading (uplink) occurs by damping the coil by an internal load. Writing (downlink) occurs by interrupting the RF field in a specific way. The TK5552 transponder operates at a nominal frequency of 125 kHz. Different bit rates and encoding schemes are available.

The on-chip 1056-bit EEPROM (32 block, 33 bits each) can be read (uplink) and written (downlink) blockwise from the base station. The blocks can be protected against overwriting by using lock bits. One block is reserved for setting the operation modes of the IC.

See section “Transponder IC Read/Write Identification IC with 1k-bit Memory”.

**Figure 2.** Block Diagram Transponder IC




## Absolute Maximum Ratings

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Operating temperature range | $T_{amb}$ | -25 to +75 | °C |
| Storage temperature range | $T_{stg}$ | -40 to +125 | °C |
| Maximum assembly temperature, t < 5 min. | $T_{ass}$ | 170 | °C |
| Magnetic field strength at 125 kHz | $H_{pp}$ | 1000 | A/m |

## Operating Characteristics Transponder

$T_{amb}$ = 25°C, f = 125 kHz, RF/32 and Manchester if not otherwise noted

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Inductance | | L | | 4 | | mH |
| Resonance frequency | LC circuit, $H_{PP}$ = 12 A/m | $f_r$ | 119 | 125 | 131 | kHz |
| **Magnetic Field Strength (H)** | | | | | | |
| Maximum field strength where tag does not modulate | No influence on other tags in the field | $H_{pp\ not}$ | | 4 | | A/m |
| **Minimum Field Strength** | | | | | | |
| Uplink/downlink mode | | $H_{pp\ 25}$ | | 12 | | A/m |
| Programming mode | | $H_{pp\ 25}$ | | 18 | | A/m |
| Data retention EEPROM | | $t_{retention}$ | 10 | | | Years |
| Programming cycles EEPROM | | | 100,000 | | | |
| Maximum field strength | | $H_{pp\ max}$ | | | 600 | A/m |

**Figure 3.** Typical TK Range of Resonance Frequency

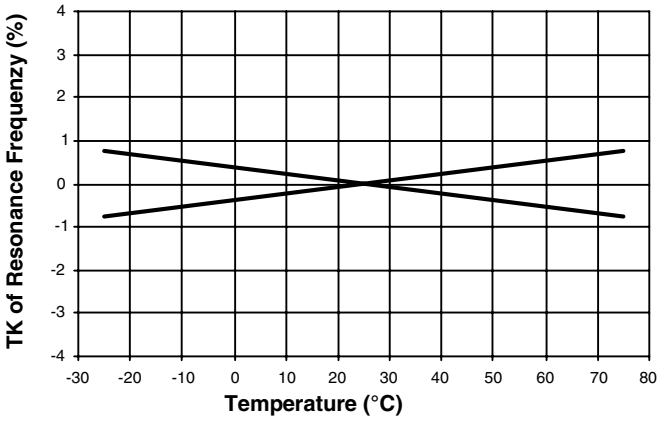



**Figure 4.** Degree of Modulation Measurement

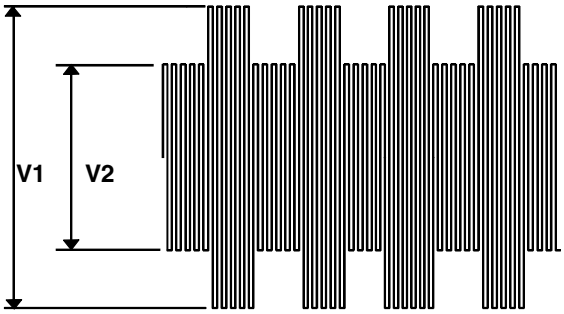
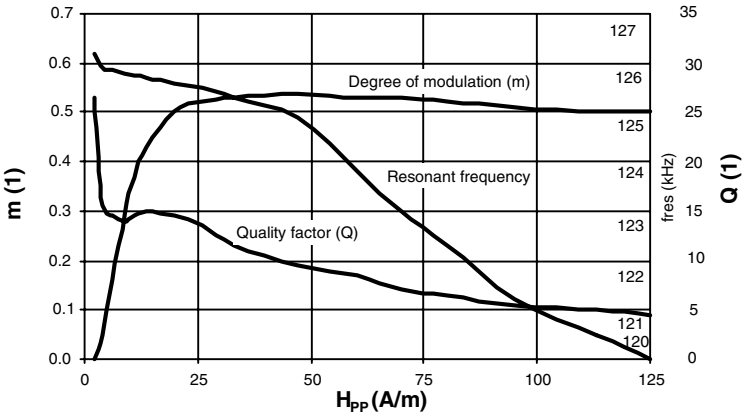



**Figure 5.** Typical Behaviour of Resonant Frequency, Degree of Modulation and Quality Factor versus Field Strength (by RF/32, Manchester)



## Measurement Assembly

All parameters are measured in a Helmholtz arrangement, which generates a homogenous magnetic field (see Figure 6 and Figure 7). A function generator drives the field generating coils, so the magnetic field can be varied in terms of frequency and field strength.

**Figure 6.** Testing Application

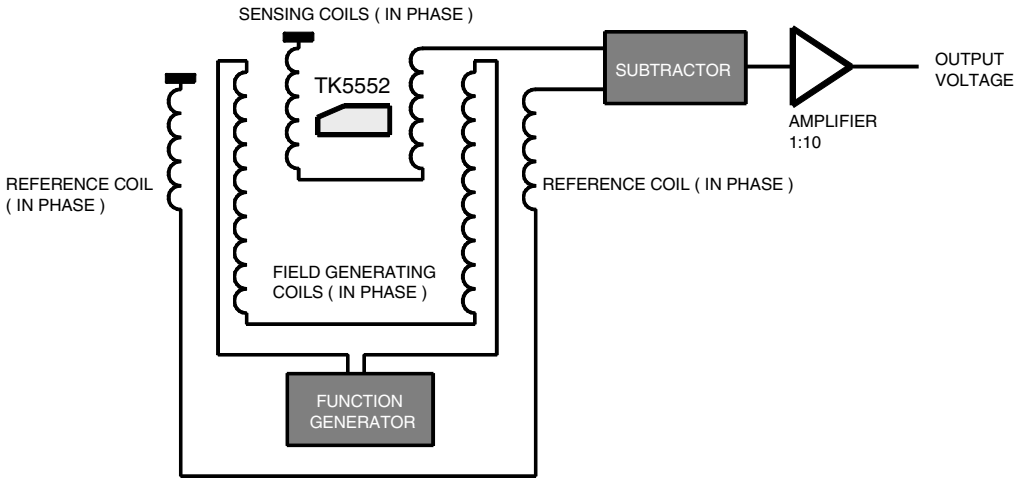
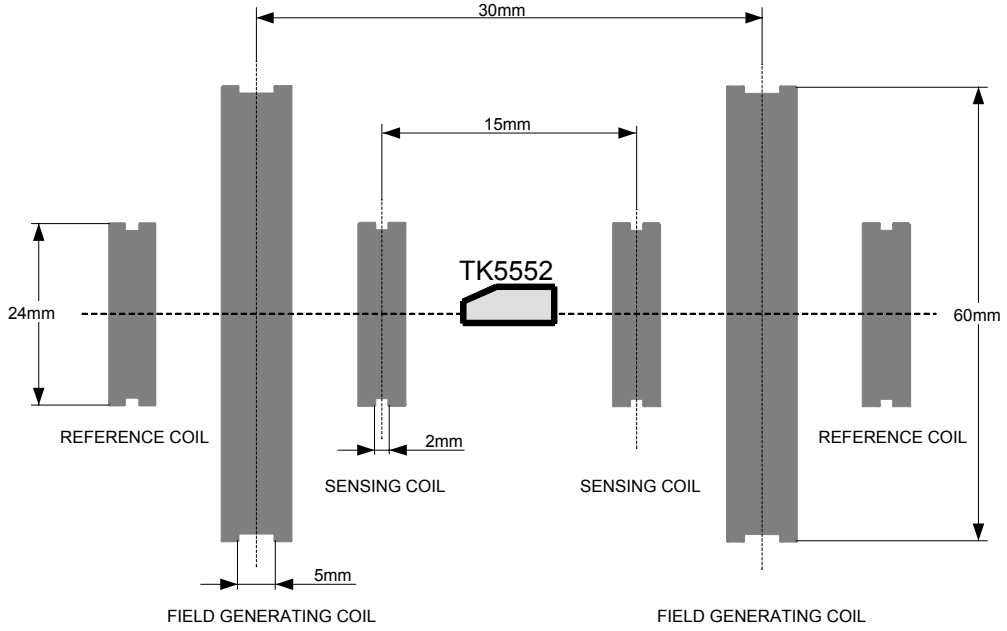



**Figure 7.** Testing Geometry




## Downlink Operation

The write sequence (downlink mode) of the TK5552 is shown in Figure 10. Writing data into the transponder occurs by interrupting the RF field with short gaps. After the start gap the standard op code (11) is followed by the lock bit. The next 32 bits contain the actual data. The last 5 bits denote the destination block address. If the correct number of bits has been received, the actual data is programmed into the specified memory block.

**Figure 8.** Downlink Protocol

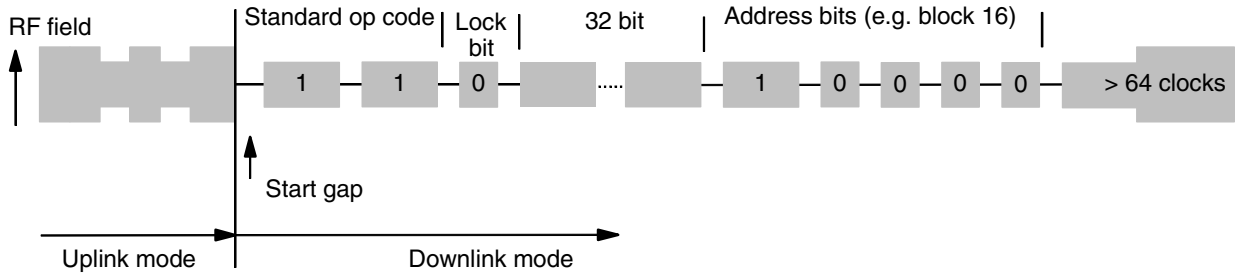
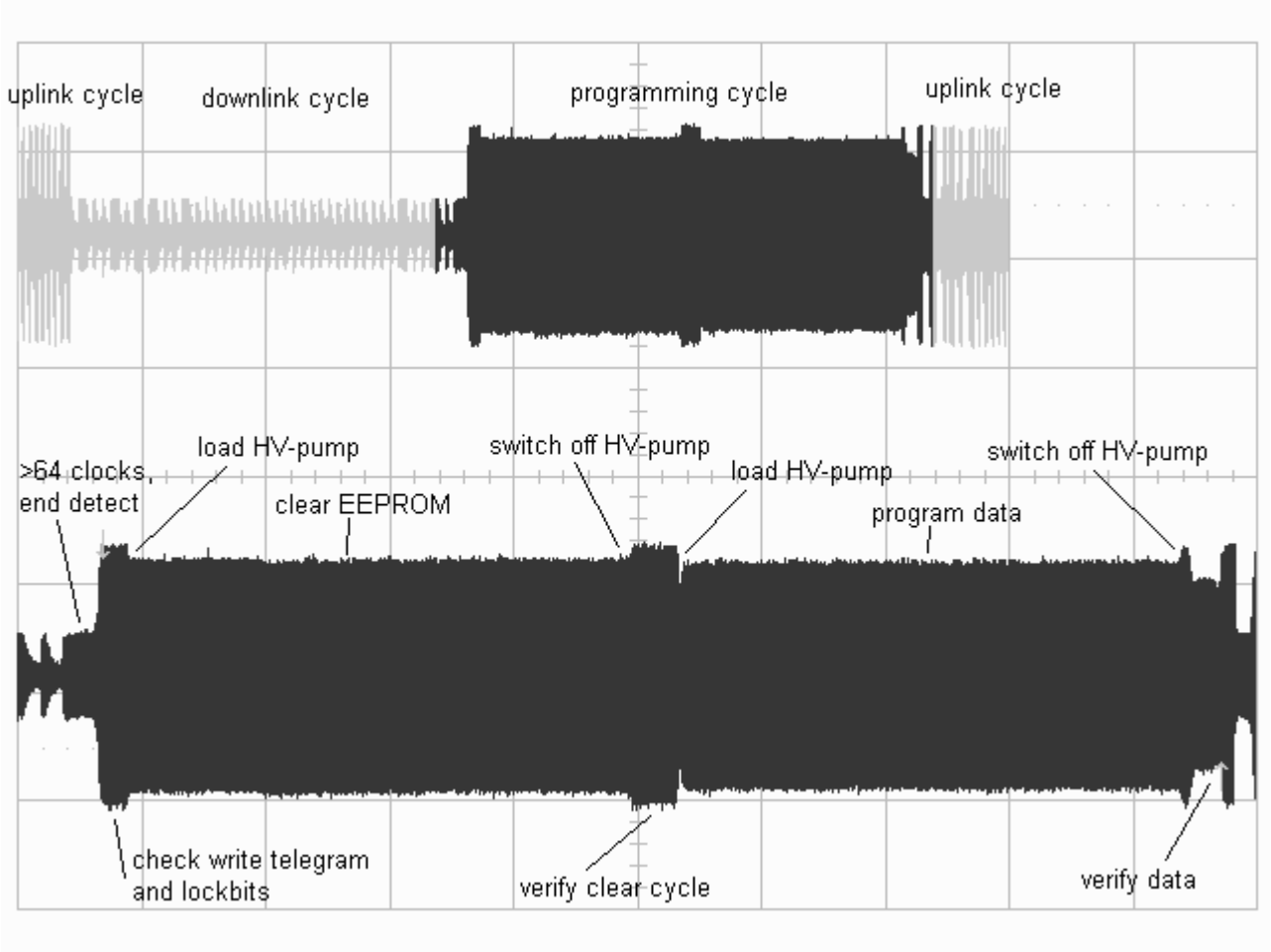


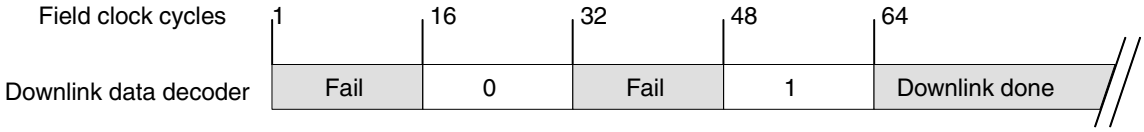

**Figure 9.** Explanation of the Programming Cycle



## Downlink Data Decoding

The time between two detected gaps is used to encode the information. As soon as a gap is detected, a counter starts counting the number of field clock cycles until the next gap is detected. Depending on how many field clocks elapse, the data is regarded as 0 or 1. The required number of field clocks is shown in Figure 10. A valid 0 is assumed if the number of counted clock periods is between 16 and 32, for a valid 1 it is 48 or 64, respectively. If the data transmission was correct, programming is started and the written block is cycling its data back to the base station until POR.

**Figure 10.** Downlink Data Decoding Scheme




## Behavior of the Real Device

The TK5552 detects a gap if the voltage across the coils decreases below the threshold value of an internal MOS transistor. Until then, the clock pulses are counted. The number given for a valid '0' or '1' (see Figure 10) refers to the actual clock pulses counted by the device. There are, however, always more clock pulses being counted than applied by the base station. The reason for this is that an RF field cannot be switched off immediately. The coil voltage decreases exponentially. Even if the RF field coming from the base station is switched off, it takes some time until the voltage across the coils reaches the threshold value of an internal MOS transistor and the device detects the gap.

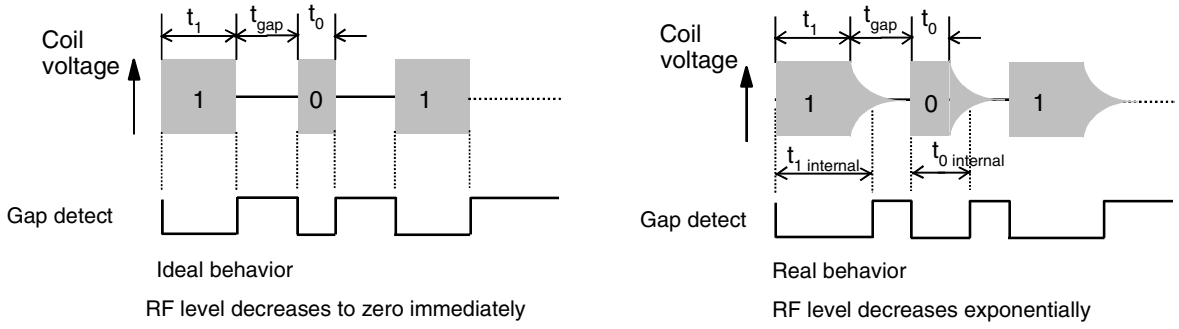
Referring to Figure 11, the device uses $t_{0\ internal}$ and $t_{1\ internal}$. The exact values for $t_0$ and $t_1$ are depend on the application (e.g., field strength, etc.)

Typical time frames are:

$t_0$ = 70 µs to 150 µs
$t_1$ = 300 µs to 400 µs
$t_{gap}$ = 180 µs to 400 µs

Antennas with a high Q-factor require longer times for $t_{gap}$ and shorter time values for $t_0$ and $t_1$.

**Figure 11.** Ideal and Real Behavior of Signals



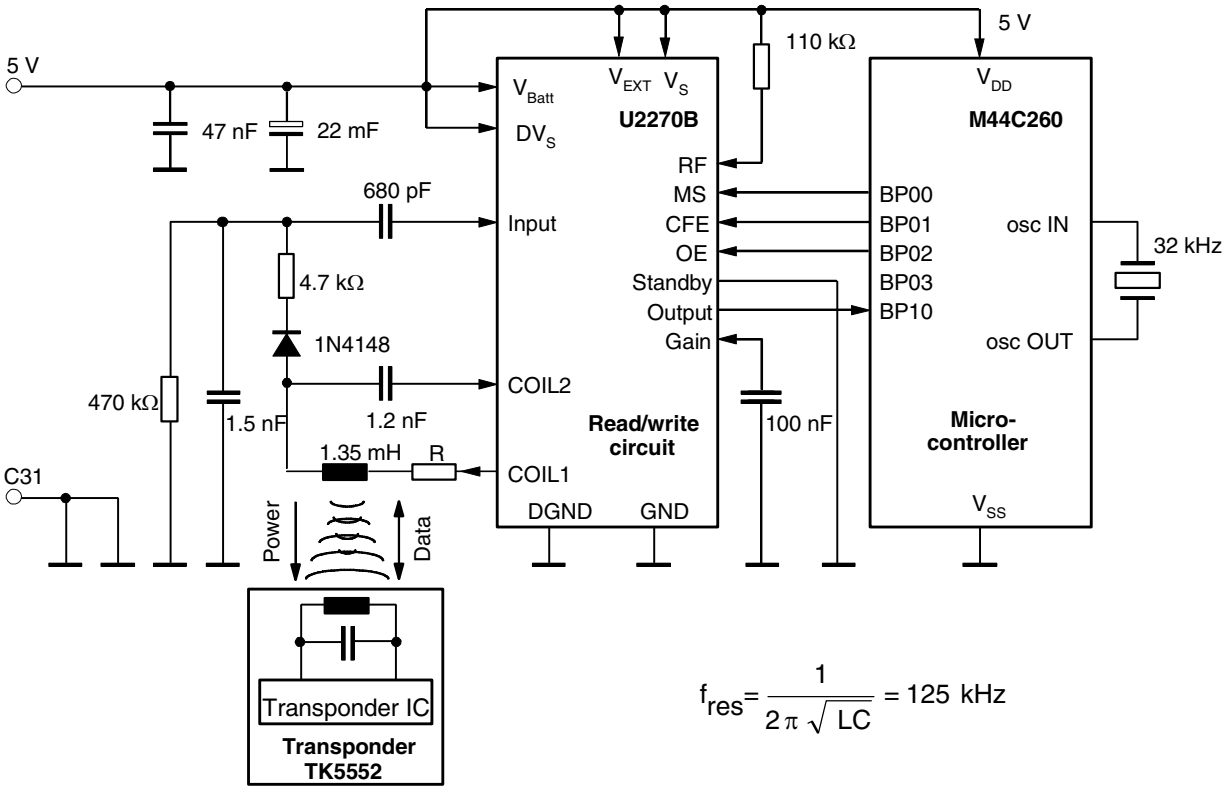
## Operating Distance

The maximum distance between the base station and the TK5552 depends mainly on the base station, the coil geometries and the modulation options chosen (see “U2270B Antenna Design Hints” application note and the “U2270B” datasheet). When using Atmel’s U2270B demo board, typical distances in the range of 0 to 5 cm can be achieved. Maximum distance values which are generally valid can not be given in this datasheet. The exact measurement of the maximum distance should be carried out with the TK5552 being integrated into the specific application.

For longer distances used in industrial applications, please use specific solutions like two or more reader coils.

# Application

**Figure 12.** Complete Transponder System with the Read/Write Base Station IC U2270B (Only Manchester Code, Short Distance)

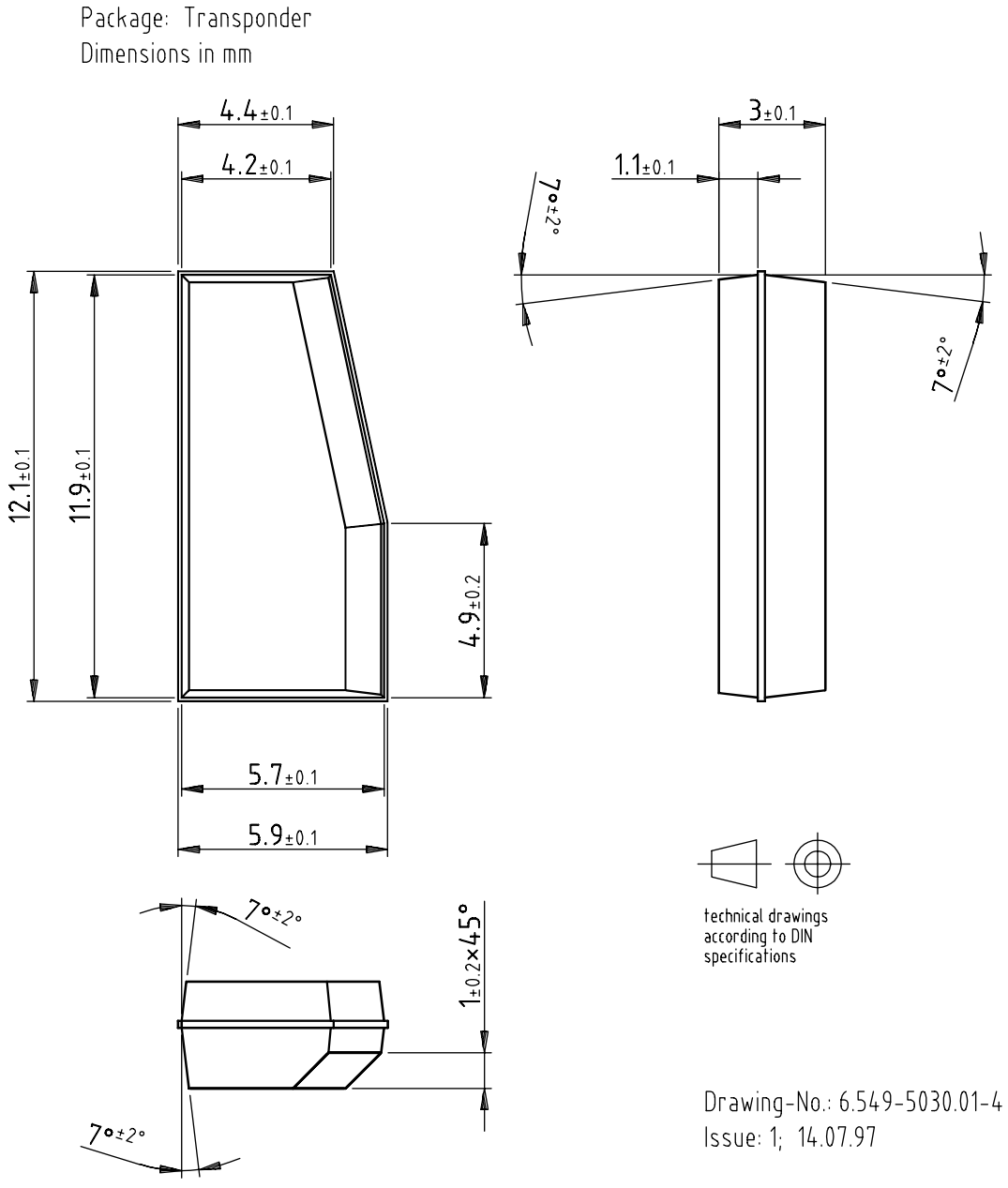


## Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| TK5552A-PP | Plastic cube | Various kinds of modulation; RF/16 and RF/32[1]<br>Programmed by default: Manchester modulation, RF/16, MAXBLK = 1 to 31 |

Note: 1. See section “Transponder IC Read/Write Identification IC with 1k-bit Memory”

## Package Information



# Transponder IC Read/Write Identification IC with 1k-bit Memory

## Features

- **Low Power, Low Voltage Operation**
- **ESD Protection: > 8 kV (HBM)**
- **Optimized for Flip Chip Die Attach Processes**
- **Contactless Power Supply**
- **Contactless Read/Write Data Transmission**
- **Radio Frequency (RF): 100 kHz to 150 kHz**
- **1056 Bits of EEPROM Memory**
- **992 Bits (31 × 32 Bits) of User Memory**
- **Defined Start of Data Transmission**
- **Auto-verify after EEPROM Programming**
- **Block Write Protection for Each Block**
- **Configurable Options Include:**
  - **Modulation Type: PSK/Manchester**
  - **Bit Rate [Bit/s]: RF/16 / RF/32**
  - **Number of Readable Blocks**
  - **Modulation Defeat**
  - **POR Start-up Delay: ≈ 1 ms / ≈ 65 ms**

## Functional Description

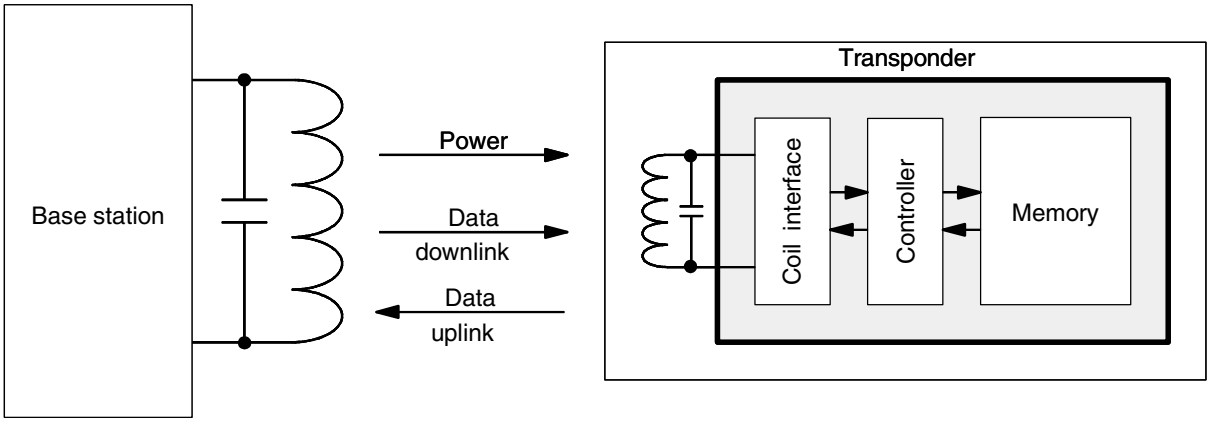
The transponder IC is a two-terminal, contactless R/W-IDentification IC (IDIC) for tag applications in the 125 kHz (±25 kHz) range. The IC uses the external RF signal to generate its own power supply and internal clock reference.

The IC contains a total of 1056 bits of EEPROM memory grouped into 32 individually addressable data blocks. Each block is made up of 32 bits of data plus an associated lock bit for block write protection. Blocks 1 to 31 are provided for user related data and block 0 for system configuration.

Data is transmitted from the IC (uplink) using reflective load (back scatter) modulation. This is achieved by damping the external RF field by switching a resistive load between the two terminals Clock-A/Clock-B. The IC receives and decodes amplitude modulated-data from the base station.

As soon as the tag including the transponder IC is exposed to an RF field (providing that the field is strong enough to derive enough energy to operate), the tag will respond by continuously transmitting stored data (uplink mode). The base station can, at any time, switch the tag to downlink mode to write new user or configuration data. Generally, the tag will automatically return to the default uplink mode when the downlink transfer is completed, interrupted or an error condition occurs.

**Figure 13.** Transponder System Example Using Transponder IC



## Functional Modules

**Analog Front End (AFE)**

The Analog Front End (AFE) includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bi-directional data communication with the base station. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- ESD protection
- Clock extractor
- Switchable load between Clock-A/Clock-B for data transmission from the IC to the reader electronics (uplink mode)
- Field gap detector for data transmission from the base station to the IC (downlink mode)

**Controller**

The control logic is responsible for the following:

- Initializing and refreshing configuration register from EEPROM block 0
- Controlling read and write memory access
- Handling data transmission and opcode decoding
- Error detection and error handling

**Clock Extraction**

The clock extraction circuit generates the internal clock source out of the external RF signal.

**Data Rate Generator**

The data rate in uplink mode can be selected to operate at either RF/16 (nominally 7.81 kHz, default) or RF/32 (nominally 3.91 kHz).

**Bit Decoder**

This functional block decodes the field gaps and verifies the validity of the incoming data stream.

**Charge Pump**

This circuit generates the high voltage required for programming the EEPROM.

**Power-On Reset (POR)**

This circuit delays the IC's functionality until an acceptable voltage threshold has been reached.

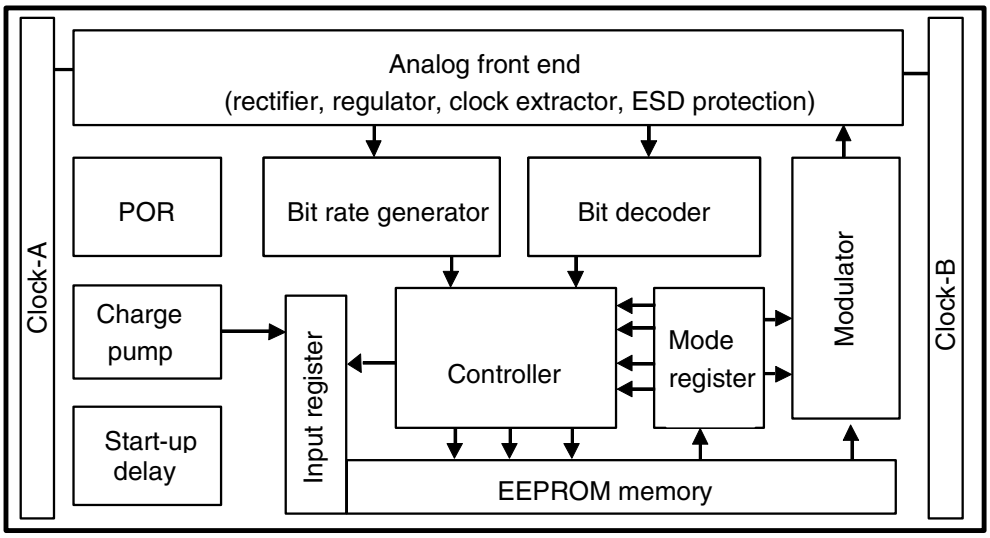
**Mode Register**

This register holds the configuration data bits stored in EEPROM block 0. It is refreshed at the start of every block read operation.

**Modulator**

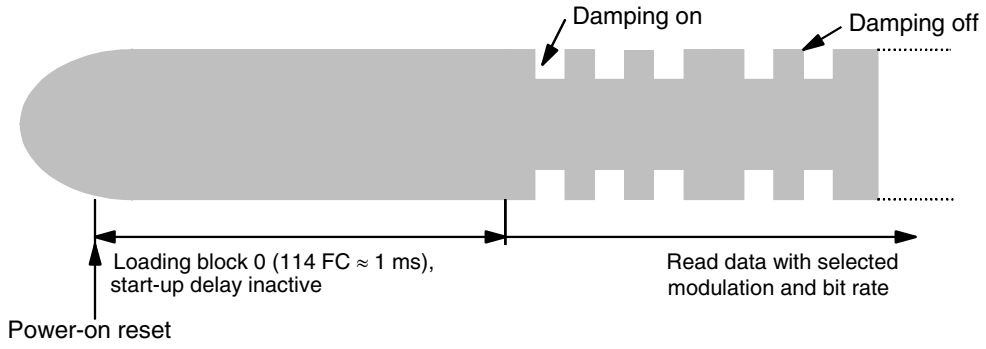
The modulator encodes the serial data stream shifted out of the selected EEPROM data block and controls the damping circuit in the AFE. The transponder IC front end supports PSK and Manchester encoding.

**Figure 14.** Functional Block Diagram




## Operating the Transponder IC

**Figure 15.** Voltage at Clock-A/Clock-B After Power-on




### General

The basic functions of the transponder IC are to supply the IC from the RF field, read data out of the EEPROM and shift them to the modulator, receive data and program these data bits into the EEPROM. An error detecting circuit prevents the EEPROM from being overwritten with wrong data.

### Power Supply

The IC is supplied via a tuned LC-circuit which is connected to the Clock-A/Clock-B pads. The incoming RF induces a current into the coil. The on-chip rectifier generates the DC supply voltage. Overvoltage protection prevents the IC from damage due to high field strengths. Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V.

### Initialization

The occurrence of an RF field triggers a power-on reset pulse, ensuring a defined start-up. The Power-On-Reset (POR) circuit remains active until an adequate voltage threshold has been reached. This in turn triggers the default start-up delay sequence. During this period of 114 Field Clock cycles (FC), the transponder IC is initialized with the configuration data stored in EEPROM block 0. This is followed by an additional delay time which is defined by the 'Start-up Delay' bit.

If the 'Start-up Delay' bit is set, the transponder IC remains inactive until 8192 RF clock cycles have occured. If this option is deactivated, no delay will occur after the configuration period of 114 RF clock cycles (≈ 1 ms).

Any field gap occuring during initialization will restart the complete sequence.

$T_{INIT}$ = (114 + 8,192 × delay bit)/125 kHz ≈ 65 ms

After this initialization time, the transponder IC enters uplink mode and modulation starts automatically using the parameters defined in the configuration block.

## Uplink Operation

All transmissions from the IC to the base station utilize amplitude modulation (ASK) of the RF carrier. This takes place by switching a resistive load between the coil pads (Clock-A and Clock-B) which in turn modulate the RF field generated by the base station (reflective back scatter modulation).

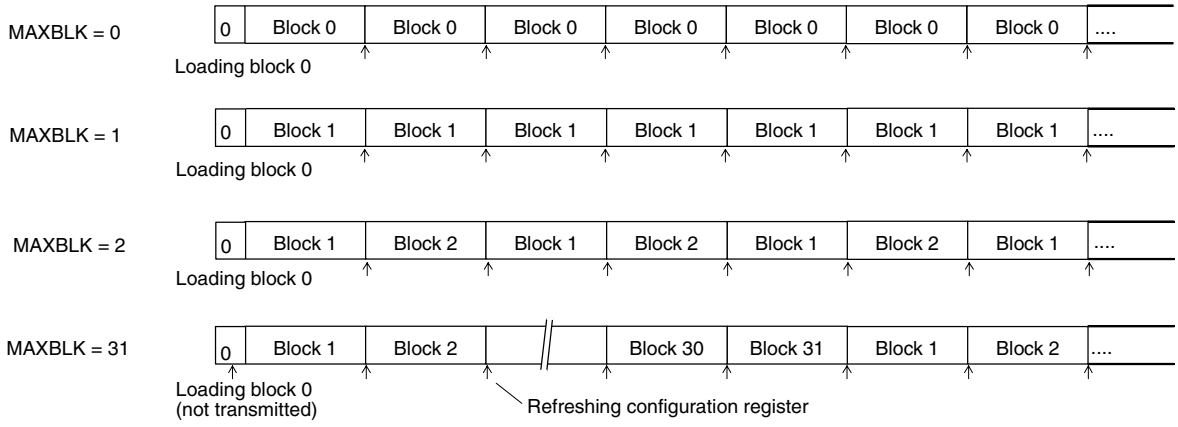
## MaxBlock

Data from the memory is serially transmitted, starting with block 1, bit 1, up to the last block (MAXBLK), bit 32. The last block to will be transmitted is defined by the mode parameter field MAXBLK which is stored in EEPROM block 0. When the MAXBLK address has been reached, data transmission restarts with block 1.

The user defines the cyclic data stream by setting the MAXBLK to a value between 0 and 31 (representing each of the 32 data blocks). If set to 1, only block 1 is transmitted. If set to 31, blocks 1 to 31 will be sequentially transmitted. If set to 0, only the contents of the configuration block (normally not accessible) will be transmitted (see Figure 16).

It is also possible to access a single data block selectively, independent of the MAXBLK value, by using the direct access command (Opcode 11). Thus the addressed data block is transmitted continously.

**Figure 16.** Data Stream Pattern Depending on MAXBLK




## Data Encoding

When entering the uplink mode, the data stream is always preceeded by a single start bit (always 0). Then the data stream continues with block 1, bit 1, etc., up to MAXBLK, bit 32. This data stream pattern cycles continuously.

The modulator is configurable for Manchester mode.

Manchester-encoded data represent a logical 1 with a rising edge and a logical 0 with a falling edge.

It is also suitable to PSK using the sub-carrier frequency RF/2. The PSK modulator changes its phase with each change of data. The first phase shift represents a data change from 0 to 1.

**Figure 17.** Example of Manchester Encoding with Data Rate RF/16

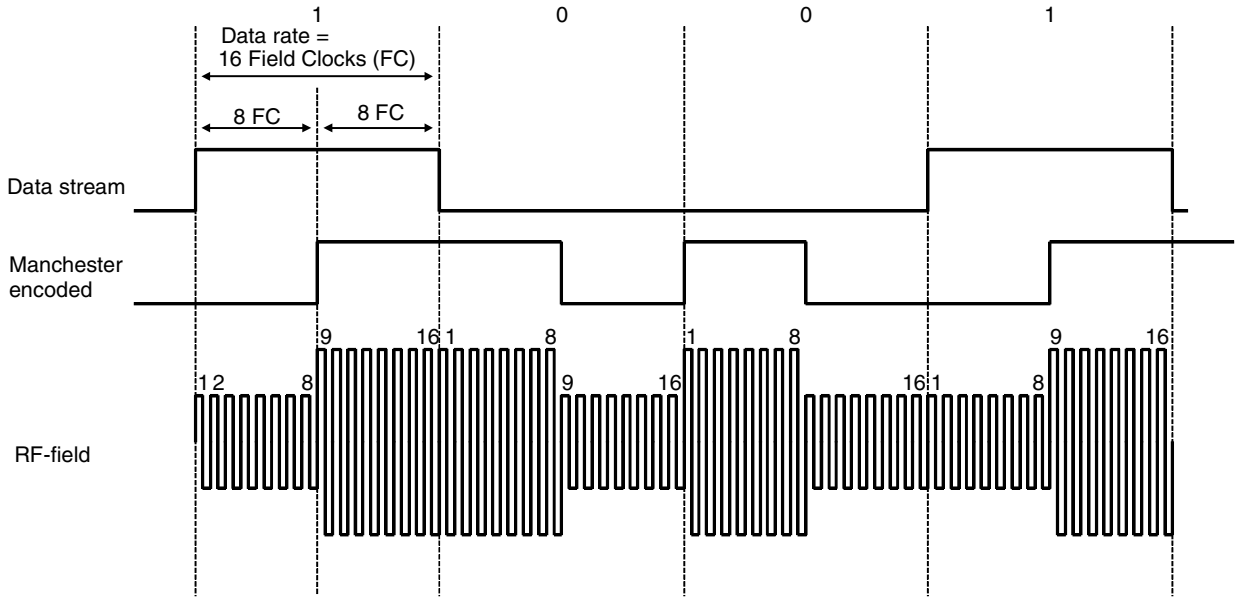
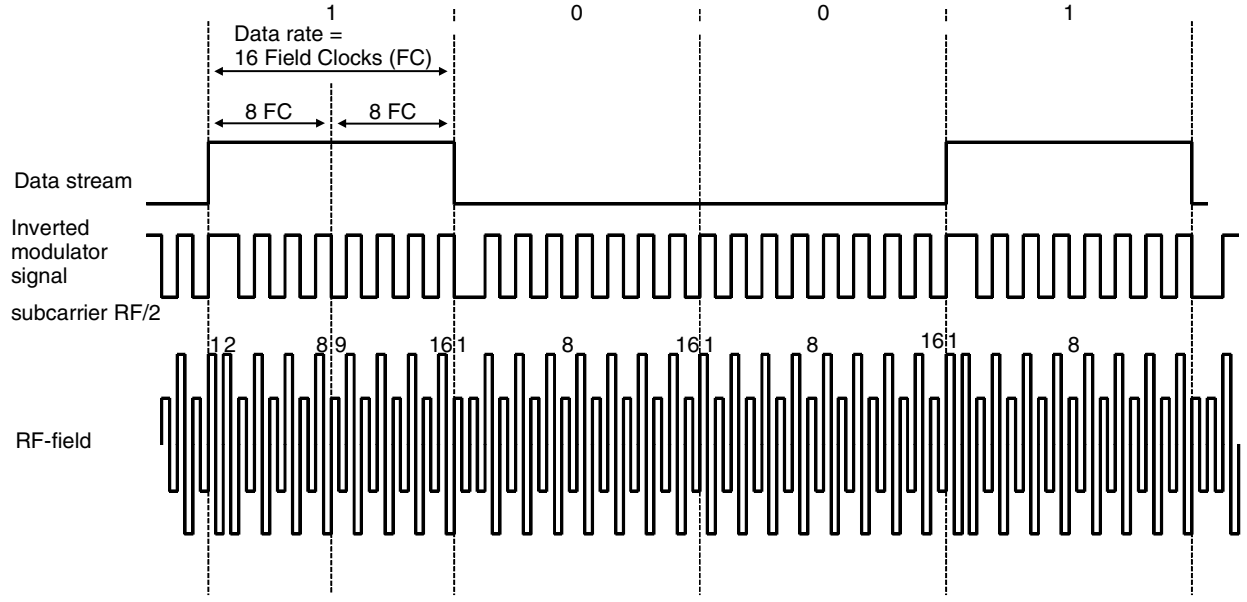



**Figure 18.** Example of PSK Encoding with Data Rate RF/16

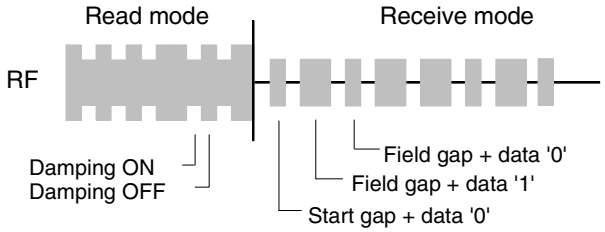


## Downlink Operation

Data is transmitted from the base station by amplitude modulation of the field (m = 1), using a series of so called gaps. With the exception of the initial synchronization gap (start gap), all field gaps have the same duration, the logical data being encoded in the length of the unmodulated phases (see Figure 19)

A valid data stream is always preceeded by a start gap which is approximately twice as long as a normal field gap. Detection of this first gap causes the transponder IC to switch immediately to downlink mode where it can receive and decode the following data stream. This stream consists of two opcode bits, followed by (0 or 33) data bits (including the lock bit) and finally (0, 3 or 5) address bits. In downlink mode the transponder damping is permanently enabled. This loads the resonant transponder coil circuit so that it comes quickly to rest when field gaps occur – thus allowing fast gap detection.

**Figure 19.** Entering Downlink Mode




A start gap will be accepted at any time after start-up initialization has been finished (RF field ON plus ≈ 1 ms, start-up delay inactive) if the IC is not in downlink mode.

### Downlink Data Coding

The duration of a field gap is typically between 80 µs and 250 µs. After the start gap the data bits are transmitted by the base station whereby each bit is separated by a field gap. The bit decoder interprets 16 to 32 internal field clocks as a logical 0 and 48 to 64 internal field clocks as a logical 1 (see Figure 20). Therefore, the time between two gaps is typically 24 field clocks for a 0 and 56 field clocks for a 1.

Whenever the bit decoder detects more than 64 field clocks, the transponder IC will abort the downlink mode. The incoming data stream is checked continuously. If any error occurs, the corresponding error handling will be initiated.

The control logic initiates an EEPROM programming cycle if the correct number of bits had been received (see Figure 21).

**Figure 20.** Operation of Bit Decoder – Data Stream Decoder

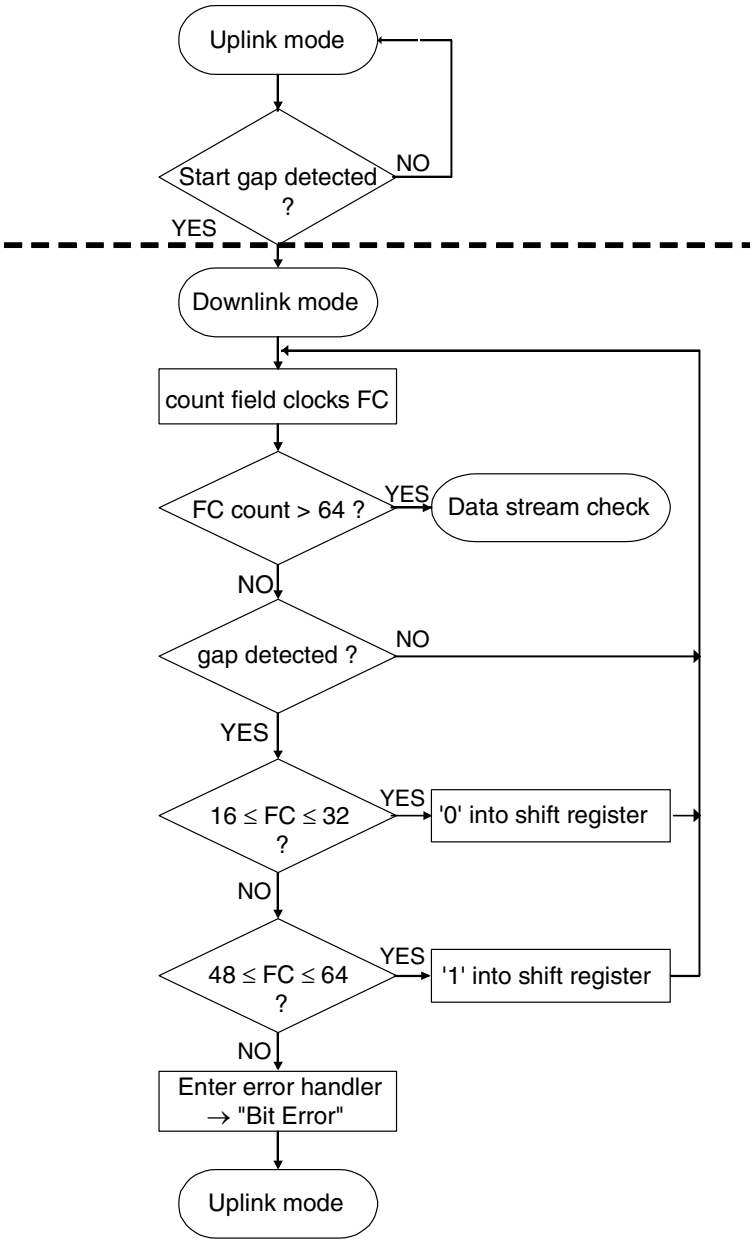
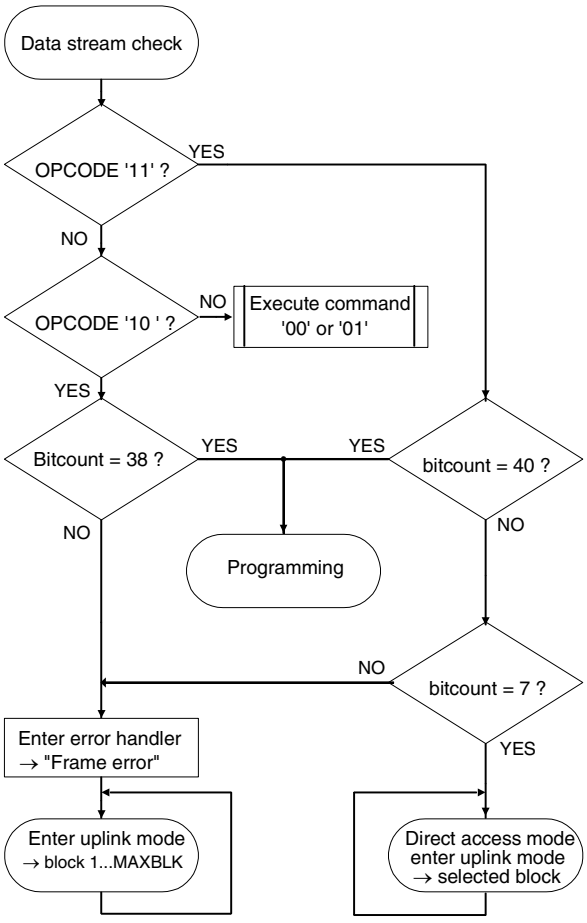


**Figure 21.** Data Stream Checking




**Opcode Definitions**

The first two bits of the data stream are decoded by the controller as the opcode bits (see Figure 22):

11: Opcode for a 5-bit address data stream

- To initiate a standard block write cycle the 2 opcode bits are followed by the lock bit, the 32 data bits and the 5-bit block address (40 bits in total)
- The direct access command consists of the opcode 11 followed by the 5-bit block address and is a read-only command (7 bits in total)

10: Opcode for a 3-bit address data stream

- Receive mode compatible to e5550
  To initiate a block write cycle, the opcode 10 is followed by the lock bit, the 32 data bits and the 3-bit block address (38 bits in total)

01: Reserved for production test commands

00: Opcode for an internal reset command

**Figure 22.** Transponder IC Opcode Format Definition

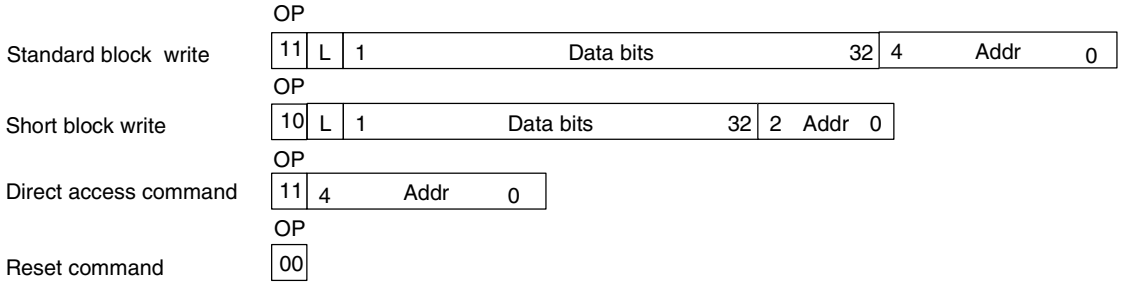
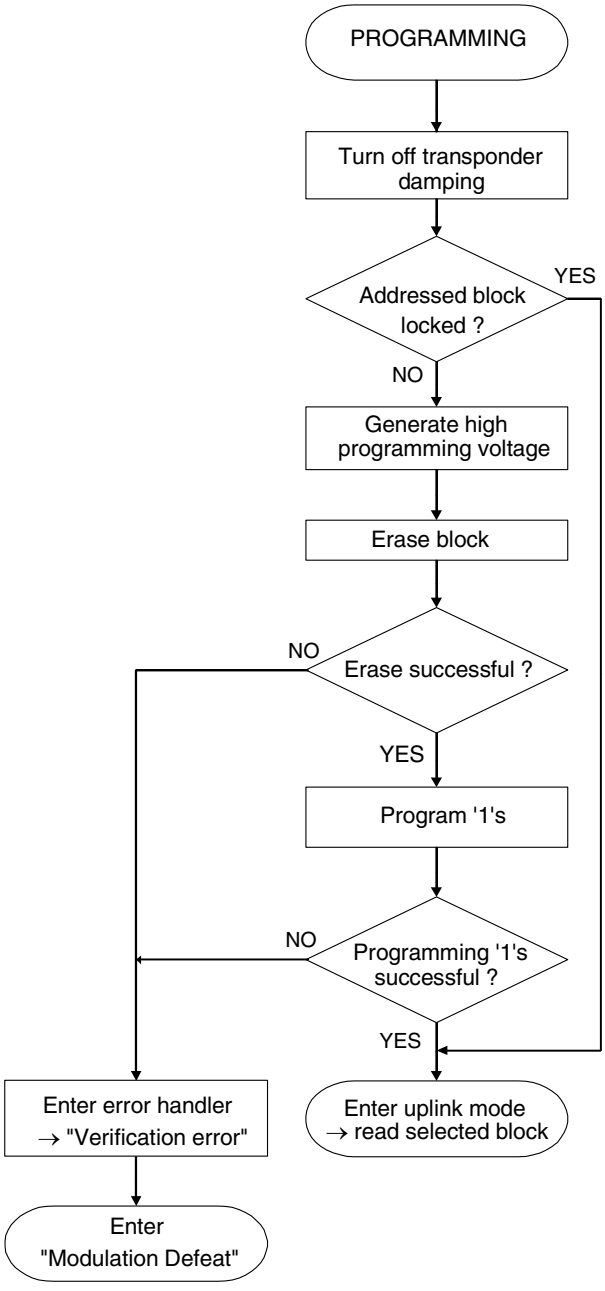



**Figure 23.** Programming Cycle Flow Chart



### Programming

When the bit decoder and controller detect a valid data stream, the transponder IC will start an erase and programming cycle if a data write command was decoded (see Figure 23).

During the erase and programming cycle, downlink damping is turned off. The programming cycle includes a data verification read to check the integrity of the data. When EEPROM programming and verification have been finished successfully, the Transponder IC enters uplink mode, transmitting the block just programmed.

The typical programming time is ≈ 18 ms.

## Error Handling

Several error conditions are detected by the transponder IC to ensure that only valid information is programmed into the EEPROM.

### Errors During EEPROM Programming

There are two types of errors which will lead to dedicated actions.

- Verification error

  If one of the data verification cycles fails, the transponder IC will inhibit modulation and will not return to the uplink mode. This modulation defeat state is terminated by re-entering the downlink mode with a start gap.
- Block write protection

  If the lock bit of the addressed block is set, programming is disabled. In this case, the programming cycle is not initiated and the transponder IC reverts to uplink mode, transmitting the currently addressed (and unmodified) block continuously.

### Errors During Data Transmission

The following errors are detected by the decoder:

- Bit error

  Wrong number of field clocks between two gaps (i.e., not a valid 0 or 1 pulse stream).
- Frame error

  The number of data bits received is incorrect:
  - Valid bit count for 3-bit address write is 38 bits
  - Valid bit count for 5-bit address write is 40 bits
  - 7 bits for a direct access command

If any of these conditions is detected, the transponder IC enters uplink mode starting with block 1.

## EEPROM Memory Organization

The memory array of the transponder IC consists of 1,056-bits of EEPROM, arranged in 32 individually addressable blocks of 33 bits each, consisting of one lock bit and 32 data bits. All 33 bits, including the lock bit, are programmed simultaneously.

The programming voltage is generated on-chip.

### Lock Bit

Each block has an associated write lock bit that protects the entire block. By default all lock bits L are reset (0).

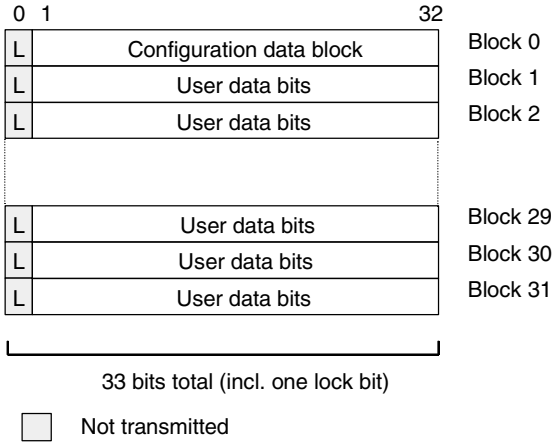
Note: Once set, the lock bit and the content of the associated block cannot be altered.

### Memory Map

The configuration data of the transponder IC is stored in block 0 of the EEPROM.

The remaining 31 data blocks (1 to 31) each consist of 1 lock bit and 32 user data bits.

**Figure 24.** Memory Map




**Configuration Data Block**

This data block contains 9 configuration bits. The remaining bits of block 0 are reserved for future enhancements and should be set to 0.

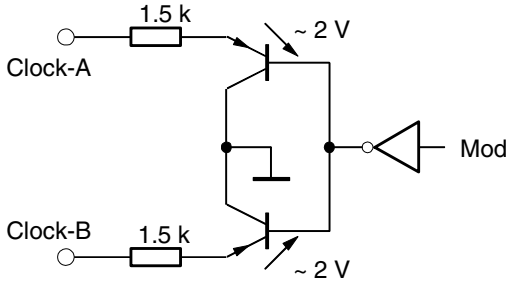
- Start-up Delay bit (SD, default: NO delay).
  When set, an additional delay time of 64 ms is added after any internal reset.
- Data Rate bit (DR, default: RF/16).
  Selects the data rate of RF/16 or RF/32.
- Modulation Select bit (MS, default is PSK)
  Selects the type of data encoding which is either Manchester or PSK.
- Modulation Defeat bit (MD, default is OFF)
  When set (to 1) the modulation output is deactivated, hence no data will be transmitted. The modulation defeat state does not impact the transponder damping function.
- MAXBLK address bits (MAXBLK, default is 31)
  This 5-bit block address is used to define the upper limit of cyclic block reads.

Note: The configuration is changed by re-programming block 0 as long as the corresponding lock bit is not set. The default settings can be lost due to the die cut.

**Table 1.** Transponder IC Configuration Block 0 Bit Mapping

| L | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | 0 |
| Lockbit | Reserved, set to '0' | | | | | | | | | | | | | | | | | | | | | | Start-up delay SD | Data rate DR | Modul. select MS | MD | MAXBLOCK<br>00000 = Block 0<br>00001 = Block 1<br>00010 = Block 1...2<br>00011 = Block 1..3 | | | | | | | Reserved |
| | | | | | | | | | | | | | | | | | | | | | | | | | | Modulation Defeat | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 0 = Normal function | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | 1 = Modulation off | | | | | | |
| 0 = Unlocked | | | | | | | | | | | | | | | | | | | | | | | | | | 0 = PSK | | | | | | |
| 1 = Locked | | | | | | | | | | | | | | | | | | | | | | | | | | 1 = MANCHESTER | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | No delay = 0 | | | 0 = RF/16 | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | Delay of 8,192 field clocks | | | | | | | | | |

**Figure 25.** Simplified Damping Circuit




## Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Maximum DC current into Clock-A/Clock-B | $I_{coil}$ | 10 | mA |
| Maximum AC current into Clock-A/Clock-B, f = 125 kHz | $I_{coil\ PP}$ | 20 | mA |
| Power dissipation (dice)(1) | $P_{tot}$ | 100 | mW |
| Electrostatic discharge voltage according to MIL-Standard 883D method 3015 (HBM) | $V_{max}$ | 8000 | V |
| Operation ambient temperature range | $T_{amb}$ | -25 to +75 | °C |
| Storage temperature range(2) | $T_{stg}$ | -40 to +125 | °C |
| Maximum assembly temperature for less than 5 min(3) | $T_{sld}$ | +150 | °C |

Notes: 1. Free-air condition, time of application: 1s
2. Data retention reduced
3. Assembly temperature of 150°C for less than 5 minutes does not affect the data retention

## Operating Characteristics

$T_{amb}$ = 25°C, $f_{RF}$ = 125 kHz, reference terminal is $V_{SS}$

| Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RF frequency range | | $f_{RF}$ | 100 | 125 | 150 | kHz |
| Supply current | Uplink and downlink mode – full temperature range | $I_{DD}$ | | 5 | 7.5 | µA |
| | Programming – full temperature range | $I_{DD}$ | | 14 | 28 | µA |
| Clamp voltage | 10 mA current into Clock-A/B | $V_{clamp}$ | 7 | | 11 | V |
| Programming time | Per block | $t_P$ | | 18 | | ms |
| Start-up time | (2) | $t_{startup}$ | 1 | | 65 | ms |
| Data retention | (1) | $t_{retention}$ | 10 | | | Years |
| Programming cycles | (1) | ncycles | 100,000 | | | |
| Clock-A/B voltage | Uplink and downlink mode | $V_{clockPP}$ | 6 | | | V |
| Clock-A/B voltage | Programming, RF field w/o damping | $V_{clockPP}$ | 12 | | | V |
| Damping resistor | Each at Clock-A and Clock-B | RD | | 1.5 | | kΩ |

Notes: 1. Since the EEPROM performance is influenced by assembly and packaging, Atmel confirms the parameters for DOW (= tested Dice On Wafer) and ICs assembled in a standard package.
2. Depends on the start-up delay bit in the configuration register.

## Atmel Headquarters


*Corporate Headquarters*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

*Europe*
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

*Asia*
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

*Japan*
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581


## Atmel Operations


*Memory*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

*Microcontrollers*
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

*ASIC/ASSP/Smart Cards*
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

*RF/Automotive*
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

*Biometrics/Imaging/Hi-Rel MPU/*
*High Speed Converters/RF Datacom*
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80


---


*e-mail*
literature@atmel.com

*Web Site*
http://www.atmel.com





4698A–RFID–04/03 xM