MAX44206

180MHz, Low-Noise, Low-Distortion, Fully Differential Op Amp/ADC Driver

General Description

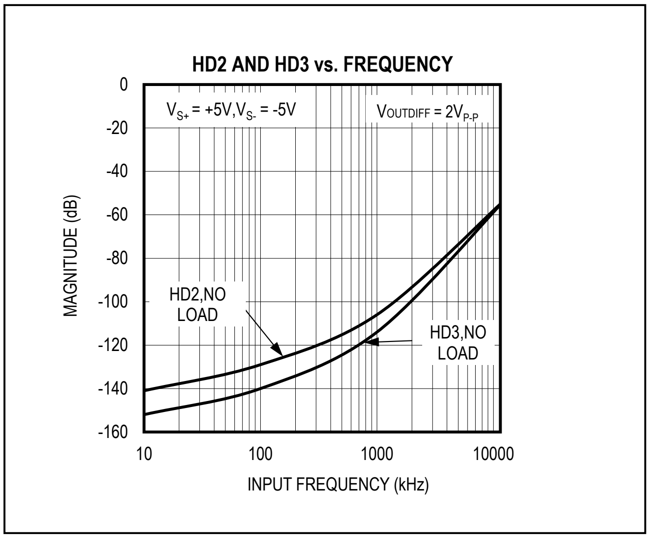
The MAX44206 is a low-noise, low-distortion fully differential operational amplifier suitable for driving high-speed, high-resolution, 20-/18-/16-bit SAR ADCs, including the MAX11905 ADC family. Featuring a combination of wide 2.7V to 13.2V supply voltage range and wide 400MHz bandwidth, the MAX44206 is suitable for low-power, high-performance data acquisition systems.

The MAX44206 offers a VOCM input to adjust the output common-mode voltage, eliminating the need for a coupling transformer or AC-coupling capacitors. This adjustable output common-mode voltage allows the MAX44206 to match the input common-mode voltage range of the ADC following it. Shutdown mode consumes only 6.8µA and extends battery life in battery-powered applications or reduces average power in systems cycling between shutdown and periodic data readings.

The MAX44206 is available in an 8-pin µMAX® package and is specified for operation over the -40°C to +125°C temperature range.

Applications

- Single-Ended to Differential Conversion
- High-Speed Process Control
- Medical Imaging
- Fully-Differential Signal Conditioning
- Active Filters



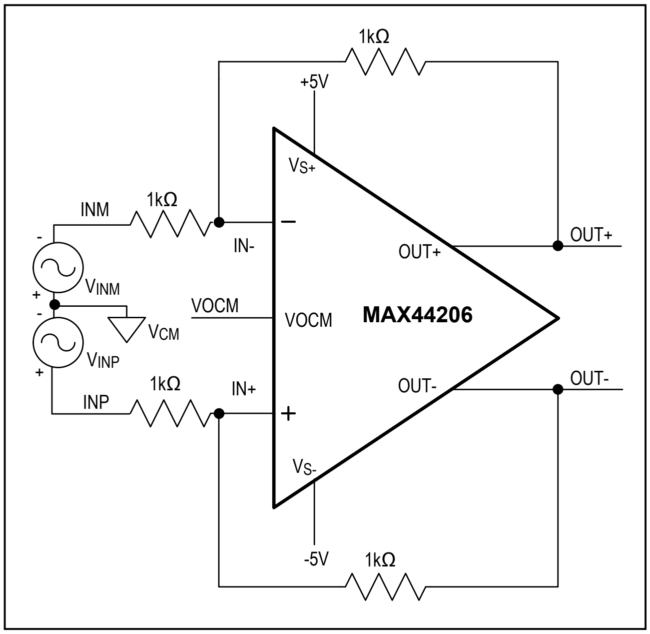
µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features and Benefits

- Low Input Noise Drives Precision SAR ADCs
  - 3.1nV/√Hz at 1kHz
  - 200nV$_{P-P}$ from 0.1Hz to 10Hz
- High Speed for DC and AC Applications
  - Gain-Bandwidth Product 400MHz
  - -3dB Gain-Bandwidth Product 180MHz
  - Slew Rate 180V/µs
- Ultra-Low Distortion Drives AC Inputs to 20-Bit SAR ADCs
  - HD2 = -141dB, HD3 = -152dB at f_{IN} = 10kHz, $V_{OUT,DIFF}$ = $2V_{P-P}$
  - HD2 = -106dB, HD3 = -115dB at f_{IN} = 1MHz, $V_{OUT,DIFF}$ = $2V_{P-P}$
- Wide Supply Range (2.7V to 13.2V) Drives Unipolar or Bipolar (±6.6V) Signals
- 3.7mA Quiescent Supply Current with Only 6.8µA Shutdown Current
- 8-Pin µMAX Package Saves Board Space

***Ordering Information** appears at end of data sheet.*

Typical Application Circuit



Absolute Maximum Ratings

V_S+ to V_S- .... -0.3V to +15V
All Other Pins .... (V_S-) - 0.3V to (V_S+) + 0.3V
IN+ to IN- .... -0.3V to +0.3V
Continuous Input Current into Any Pin (Note 1) .... ±20mA
Output Short-Circuit Duration (Note 1) 10s
Continuous Power Dissipation (T_A = +70°C)
  µMAX (derate 10.3mW/°C above +70°C) 824.7mW

Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Package Thermal Characteristics (Note 1)

µMAX
  Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 77.6°C/W
  Junction-to-Case Thermal Resistance (θ_{JC}) .... 5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (±5V Supply)

(V_{S+} = +5V, V_S- = -5V, V_{OCM} = 0V, $\overline{\text{SHDN}}$ = V_{S+}, EP = 0V (Note 2), R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_S	V_S+ to V_S-, guaranteed by PSRR (EP = V_S-)	2.7		13.2	V
Quiescent Current	I_S	No load, R_L = ∞		3.7	6.8	mA
		$\overline{\text{SHDN}}$ = 0V		6.8	20	µA
Power-Supply Rejection Ratio	PSRR	V_S+ to V_S- = 2.7V to 13.2V (EP = V_{S-})	90	123		dB
DIFFERENTIAL PERFORMANCE—DC SPECIFICATIONS						
Input Common-Mode Range	V_{ICM}	Guaranteed by CMRR	(V_S-) + 1.1		(V_S+) - 1.1	V
Input Common-Mode Rejection Ratio	CMRR	V_{ICM} = (V_S-) + 1.1V to (V_S+) - 1.1V	94	130		dB
Input Offset Voltage	V_{OS}			±0.2	±1.5	mV
Input Offset Voltage Drift	TCV_{OS}			0.2		µV/°C
Input Bias Current	I_B			30	750	nA
Input Offset Current	I_{OS}			±15	±350	nA
Open-Loop Gain	A_{VOL}	$V_{OUT,DIFF}$ = 6.6V_{P-P} , T_A = +25°C	96	130		dB
Output Short-Circuit Current	I_{SC}			60		mA
Output Voltage Swing	V_S+ - V_{OUT}	Applies to V_{OUT+}, V_{OUT}		0.98	1.15	V
	V_{OUT} - V_S-	Applies to V_{OUT+}, V_{OUT-}		0.92	1.10	

Electrical Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V (Note 2), R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL PERFORMANCE—AC SPECIFICATIONS						
Input Voltage-Noise Density	e_N	f = 1kHz		3.1		nV/√Hz
Input Voltage Noise		0.1Hz < f < 10Hz		200		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz		1.5		pA/√Hz
1/f Noise Due to Input Current		0.1Hz < f < 10Hz		220		pA_{P-P}
-3dB Small-Signal Bandwidth		$V_{OUT,DIFF} = 0.1V_{P-P}$		180		MHz
0.1dB Gain Flatness Bandwidth		$V_{OUT,DIFF} = 0.1V_{P-P}$		25		MHz
-3dB Large-Signal Bandwidth		$V_{OUT,DIFF} = 2V_{P-P}$		38		MHz
0.1dB Gain Flatness Bandwidth		$V_{OUT,DIFF} = 2V_{P-P}$		19		MHz
Slew Rate (Differential)	SR	$V_{OUT,DIFF} = 2V_{P-P}$		180		V/µs
Capacitive Loading	C_L	No sustained oscillations		5		pF
HD2/HD3 Specifications		$V_{OUT,DIFF} = 2V_{P-P}$, f = 10kHz		-129/-146		dBc
		$V_{OUT,DIFF} = 2V_{P-P}$, f = 1MHz		-90/-98		
		$V_{OUT,DIFF} = 6.6V_{P-P}$, f = 10kHz		-124/-142		
		$V_{OUT,DIFF} = 6.6V_{P-P}$, f = 1MHz		-86/-90		
Settling Time	t_S	Settling to 0.1%, $V_{OUT,DIFF} = 4V_{P-P}$		58		ns
		Settling to 0.1%, $V_{OUT,DIFF} = 6.6V_{P-P}$		107		
Output Impedance	$R_{OUT,DIFF}$	f_C = 1MHz		0.1		Ω
Output Balance Error		$V_{OUT,DIFF} = 1V_{P-P}$, f = 1MHz		-54		dB
$\overline{SHDN}$ INPUT						
Input Voltage	V_{IH}		1.25			V
	V_{IL}				0.65	
Input Current	I_{IH}	$V_{\overline{SHDN}}$ = 2V		0.2	1.5	µA
	I_{IL}	$V_{\overline{SHDN}}$ = 0V	-1.5	-0.2		
Turn-On Time	t_{ON}	Output condition		1.2		µs
Turn-Off Time	t_{OFF}	Output condition		0.8		µs
V_{OCM} INPUT to $V_{OUT,CM}$ PERFORMANCE						
Input Voltage Range		Guaranteed by gain parameter	(V_S-) + 1.2		(V_S+) - 1.2	V
Output Common-Mode Gain	G_{OCM}	$\Delta(V_{OUT,CM})/\Delta(V_{OCM})$, V_{OCM} = (V_S-) + 1.2 to (V_S+) - 1.2	0.99	1	1.01	V/V
Input Offset Voltage				±13	±38	mV
Input Bias Current			-2	-0.30		µA
Output Common-Mode Rejection Ratio (Note 4)	OCMRR	2 x $\Delta(V_{OS})/\Delta(V_{OCM})$, V_{OCM} = (V_S-) + 1.2 to (V_S+) - 1.2	100	130		dB
-3dB Small-Signal Bandwidth		$V_{OUT,CM} = 100mV_{P-P}$		16		MHz
Slew Rate		$V_{OUT,CM} = 1V_{P-P}$		6		V/µs

Electrical Characteristics (+5V Supply)

(V_{S+} = +5V, V_{S-} = 0V, VOCM = 2.5V, $\overline{\text{SHDN}}$ = V_{S+}, EP = 0V (Note 2), R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_S	V_S+ to V_S-, guaranteed by PSRR ($EP = V_S$-)	2.7		13.2	V
Quiescent Current	I_S	No load, R_L = ∞		3.7	6.8	mA
		$V_{\overline{SHDN}}$ = 0V		5.9	20	µA
DIFFERENTIAL PERFORMANCE—DC SPECIFICATIONS						
Input Common-Mode Range	V_{ICM}	Guaranteed by CMRR	(V_S-) + 1.1		(V_S+) - 1.1	V
Input Common-Mode Rejection Ratio	CMRR	V_{ICM} = (V_S-) + 1.1V to (V_S+) - 1.1V	94	130		dB
Input Offset Voltage	V_{OS}			±0.2	±1.5	mV
Input Offset Voltage Drift	TC V_{OS}			0.2		µV/°C
Input Bias Current	I_B			30	750	nA
Input Offset Current	I_{OS}			±15	±350	nA
Open-Loop Gain	A_{VOL}	$V_{OUT,DIFF}$ = 2.8V_{P-P}, T_A = +25°C	95	120		dB
Output Short-Circuit Current	I_{SC}			60		mA
Output Voltage Swing	V_S+ - V_{OUT}	Applies to V_{OUT+}, V_{OUT}		0.95	1.1	V
	V_{OUT} - V_S-	Applies to V_{OUT+}, V_{OUT}		0.85	1.1	
DIFFERENTIAL PERFORMANCE—AC SPECIFICATIONS						
Input Voltage-Noise Density	e_N	f = 1kHz		3.1		nV/√Hz
Input Voltage Noise		0.1Hz < f < 10Hz		200		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz		1.5		pA/√Hz
1/f Noise Due to Input Current		0.1Hz < f < 10Hz		220		pA_{P-P}
-3dB Small-Signal Bandwidth		$V_{OUT,DIFF}$ = 0.1V_{P-P}		180		MHz
0.1dB Gain Flatness Bandwidth		$V_{OUT,DIFF}$ = 0.1V_{P-P}		25		MHz
-3dB Large-Signal Bandwidth		$V_{OUT,DIFF}$ = 2V_{P-P}		38		MHz
0.1dB Gain Flatness Bandwidth		$V_{OUT,DIFF}$ = 2V_{P-P}		19		MHz
Slew Rate (Differential)	SR	$V_{OUT,DIFF}$ = 2V_{P-P}		120		V/µs
Capacitive Loading	C_L	No sustained oscillations		5		pF
HD2/HD3 Specifications		V_{OUT} = 4V_{P-P}, f = 10kHz		-123/-143		dBc
		V_{OUT} = 4V_{P-P}, f = 1MHz		-88.5/-95.5		
Settling Time	t_S	Settling to 0.1%, $V_{OUT,DIFF}$ = 4V_{P-P}		58		ns
		Settling to 0.1%, $V_{OUT,DIFF}$ = 6.6V_{P-P}		100		
Output Impedance	$R_{OUT,DIFF}$	f_C = 1MHz ($V_{OUT,DIFF}$)		0.1		Ω
Output Balance Error		$V_{OUT,DIFF}$ = 1V_{P-P}, f = 1MHz		-52		dB

Electrical Characteristics (continued)

(V_{S+} = +5V, V_{S-} = 0V, VOCM = 2.5V, $\overline{\text{SHDN}}$ = V_{S+}, EP = 0V (Note 2), R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{SHDN}}$ INPUT						
Input Voltage	V_{IH}		1.25			V
	V_{IL}				0.65	
Input Current	I_{IH}	$V_{\overline{SHDN}}$ = 2V		0.2	1.5	µA
	I_{IL}	$V_{\overline{SHDN}}$ = 0V	-1.5	-0.2		
Turn-On Time	t_{ON}	Output condition		1.2		µs
Turn-Off Time	t_{OFF}	Output condition		0.8		µs
VOCM INPUT to $V_{OUT,CM}$ PERFORMANCE						
Input Voltage Range		Guaranteed by gain parameter	(V_S-) +1.2		(V_S+)-1.2	V
Output Common-Mode Gain	G_{OCM}	$\Delta(V_{OUT,CM})/\Delta(V_{OCM})$, V_{OCM} = (V_S-) + 1.2 to (V_S+) - 1.2	0.99	1	1.01	V/V
Input Offset Voltage				±13	±38	mV
Input Bias Current			-2	-0.3		µA
Output Common-Mode Rejection Ratio (Note 4)	OCMRR	2 x $\Delta(V_{OS})/\Delta(V_{OCM})$, V_{OCM} = (V_S-) + 1.2 to (V_S+) - 1.2	90	130		dB
-3dB Small-Signal Bandwidth		$V_{OUT,CM}$ = 100mV_{P-P}		16		MHz
Slew Rate		$V_{OUT,CM}$ = 1V_{P-P}		6		V/µs

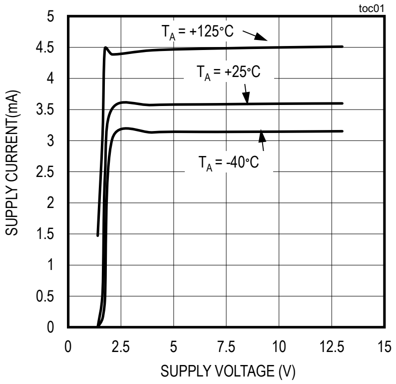
Note 2: EP is the logic ground reference to the $\overline{\text{SHDN}}$ pin.

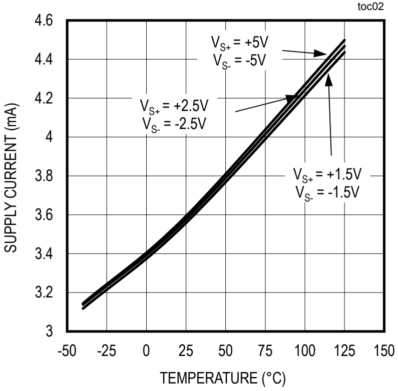
Note 3: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.

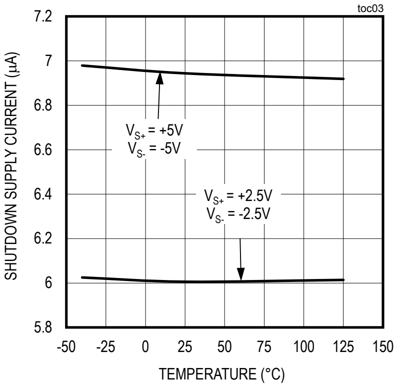
Note 4: OCMRR is mainly determined by external gain resistors matching. The formula used for OCMRR calculation assumes that gain resistors are perfectly matched. Therefore, OCMRR = (1 + R_F/R_G) x $\Delta V_{OS}/\Delta V(VOCM)$.

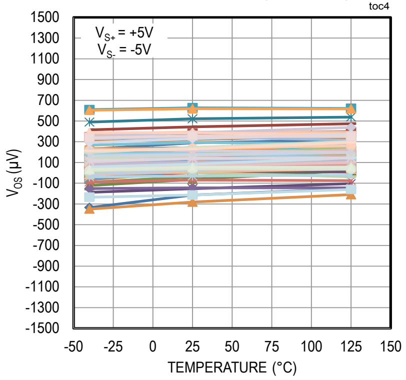
Typical Operating Characteristics

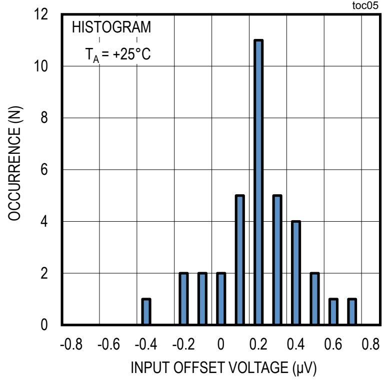
(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

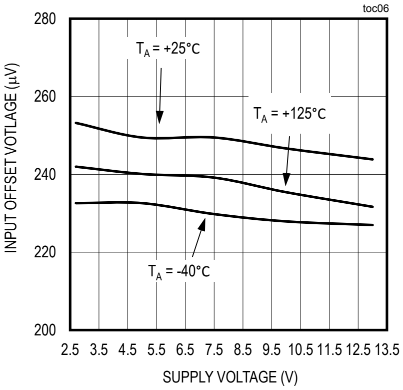

SUPPLY CURRENT vs. SUPPLY VOLTAGE

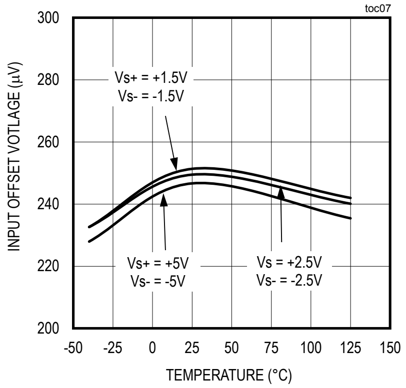

SUPPLY CURRENT vs. TEMPERATURE

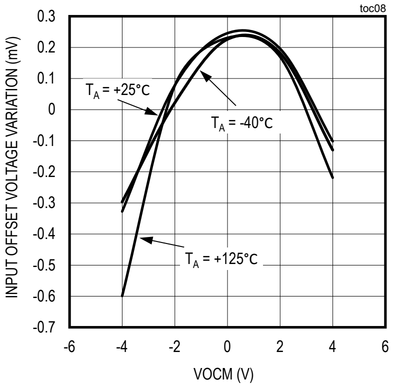

SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE

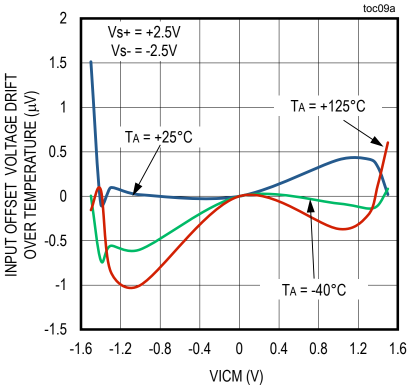

INPUT OFFSET VOLTAGE (IN+, IN-) vs. TEMPERATURE (100 UNITS)


INPUT OFFSET VOLTAGE (IN+, IN-) HISTOGRAM


IN+, IN- INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE


INPUT OFFSET VOLTAGE (IN+, IN-) vs. TEMPERATURE

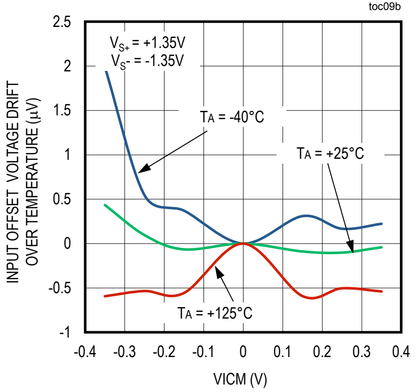

INPUT OFFSET VOLTAGE VARIATION vs. VOCM


INPUT OFFSET VOLTAGE CHANGE OVER TEMPERATURE vs. VICM

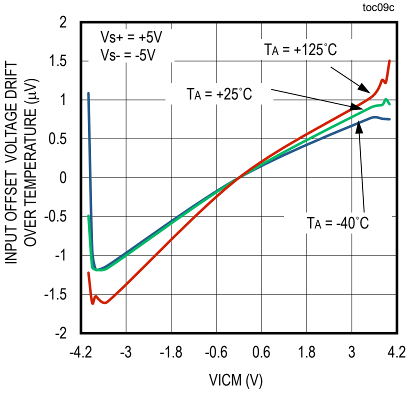
Typical Operating Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

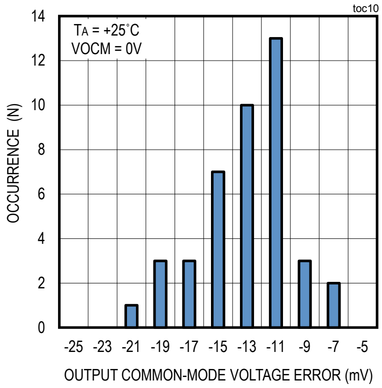
INPUT OFFSET VOLTAGE CHANGE OVER TEMPERATURE vs. VICM



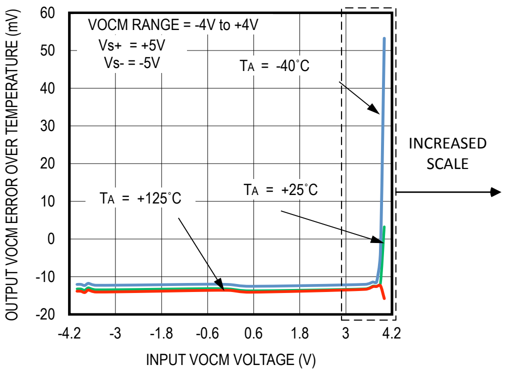
INPUT OFFSET VOLTAGE CHANGE OVER TEMPERATURE vs. VICM



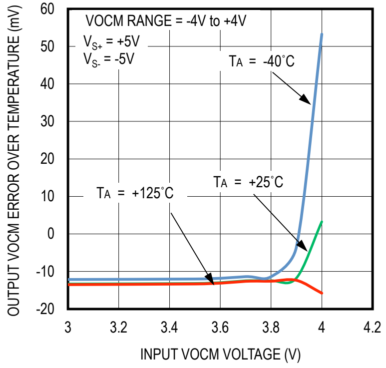
OUTPUT COMMON-MODE VOLTAGE ERROR HISTOGRAM



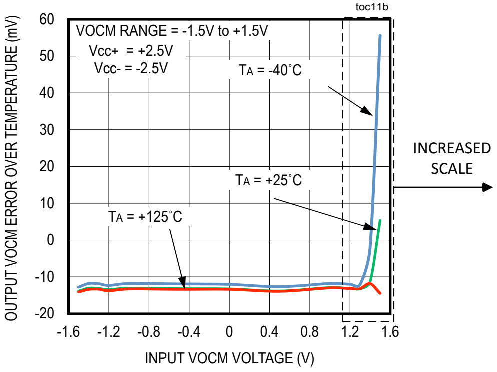
VOCM ERROR OVER TEMPERATURE vs. VOCM INPUT



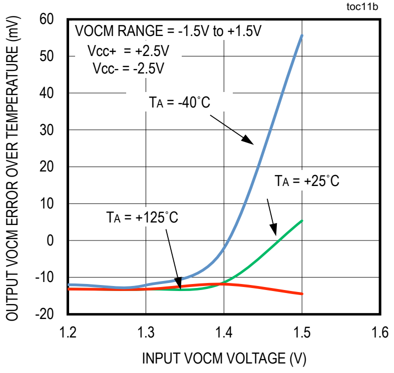
VOCM ERROR OVER TEMPERATURE vs. VOCM INPUT



VOCM ERROR OVER TEMPERATURE vs. VOCM INPUT

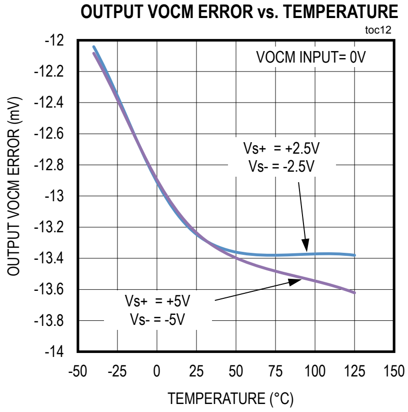


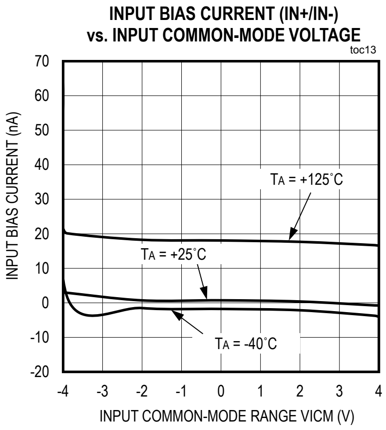
VOCM ERROR OVER TEMPERATURE vs. VOCM INPUT

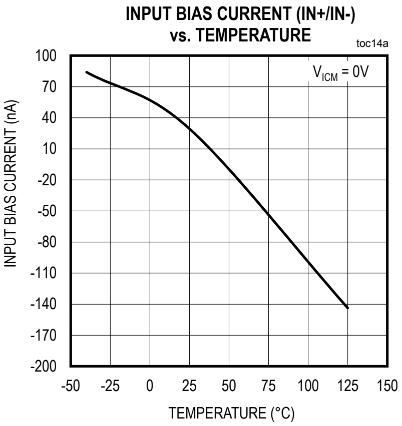


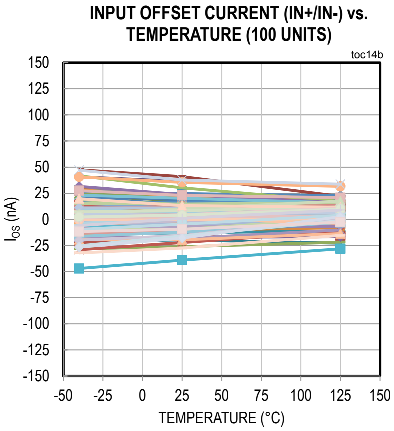
Typical Operating Characteristics (continued)

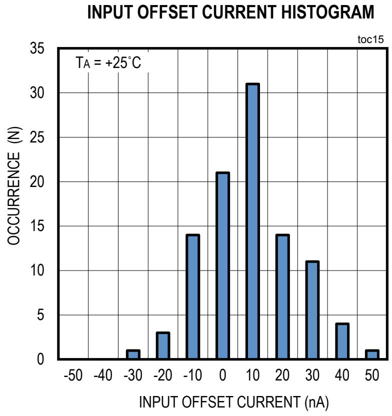
(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

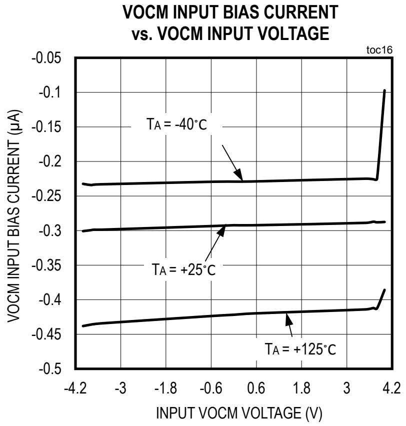

OUTPUT VOCM ERROR vs. TEMPERATURE

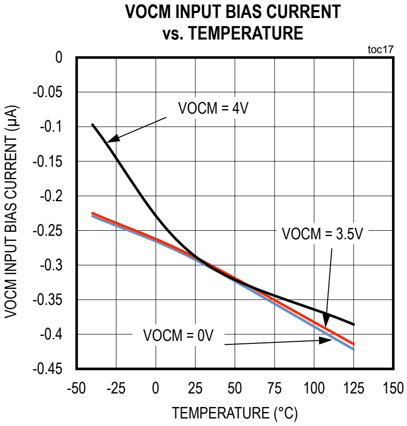

INPUT BIAS CURRENT (IN+/IN-) vs. INPUT COMMON-MODE VOLTAGE


INPUT BIAS CURRENT (IN+/IN-) vs. TEMPERATURE


INPUT OFFSET CURRENT (IN+/IN-) vs. TEMPERATURE (100 UNITS)


INPUT OFFSET CURRENT HISTOGRAM

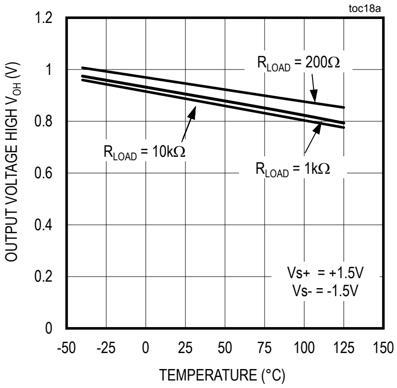

VOCM INPUT BIAS CURRENT vs. VOCM INPUT VOLTAGE


VOCM INPUT BIAS CURRENT vs. TEMPERATURE

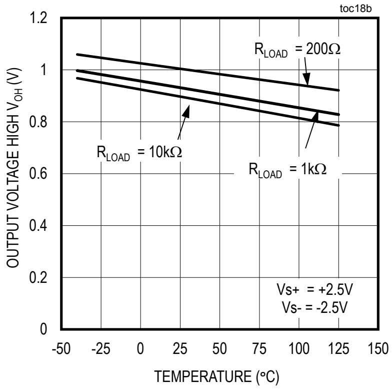
Typical Operating Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

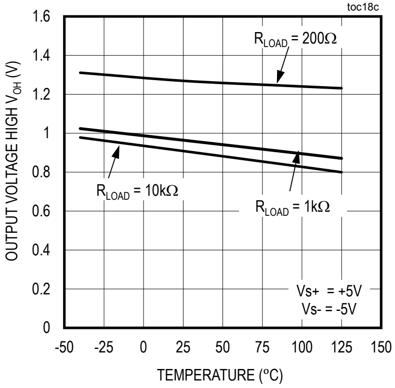
V_{OH} vs. TEMPERATURE vs. LOAD RESISTOR



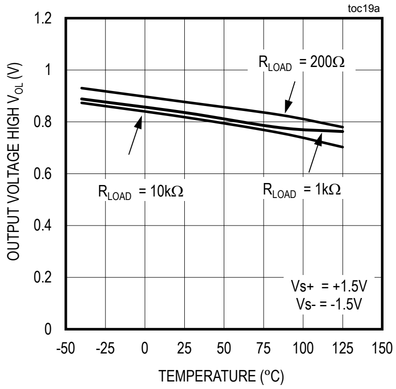
V_{OH} vs. TEMPERATURE vs. LOAD RESISTOR



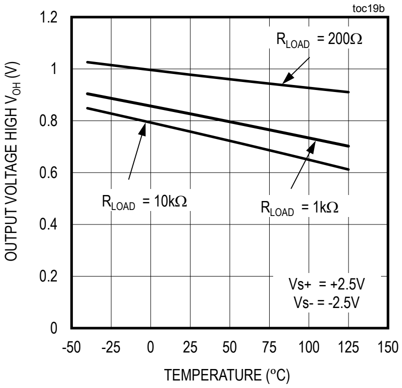
V_{OH} vs. TEMPERATURE vs. LOAD RESISTOR



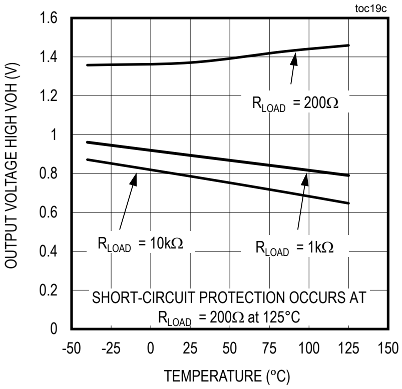
V_{OL} vs. TEMPERATURE vs. LOAD RESISTOR



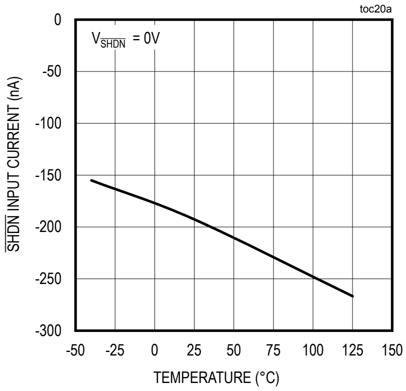
V_{OL} vs. TEMPERATURE vs. LOAD RESISTOR



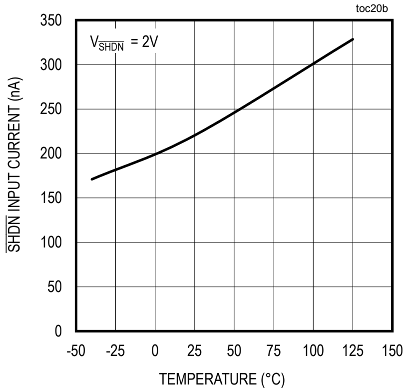
V_{OL} vs. TEMPERATURE vs. LOAD RESISTOR



$\overline{SHDN}$ INPUT CURRENT vs. $\overline{SHDN}$ VOLTAGE vs. TEMPERATURE

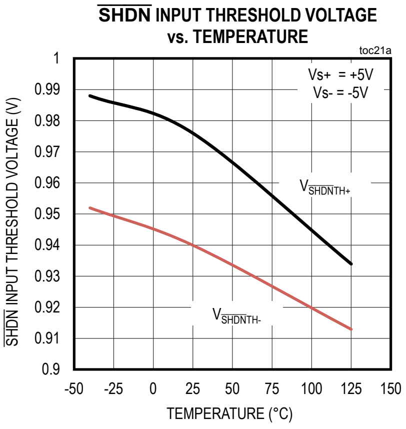


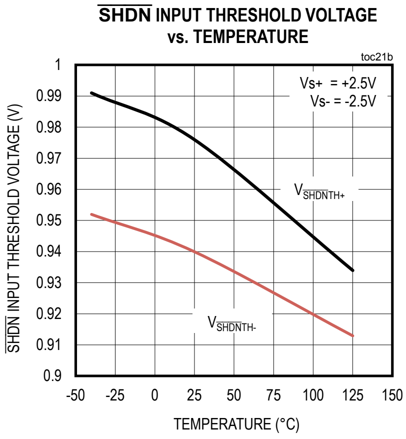
$\overline{SHDN}$ INPUT CURRENT vs. $\overline{SHDN}$ INPUT VOLTAGE

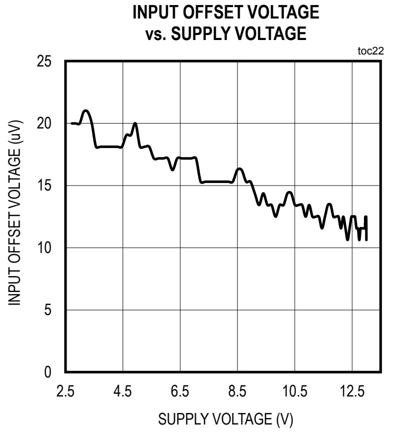


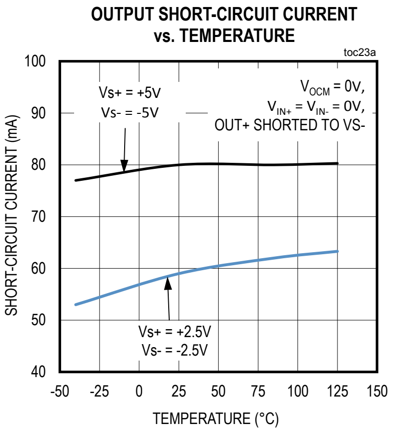
Typical Operating Characteristics (continued)

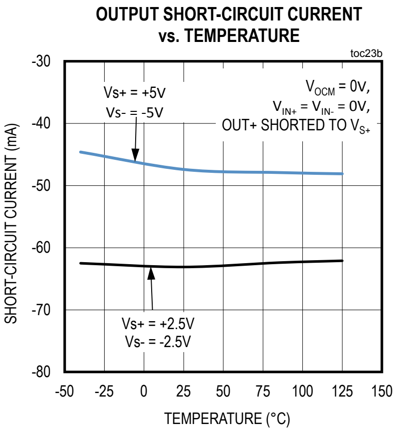
(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)


$\overline{SHDN}$ INPUT THRESHOLD VOLTAGE vs. TEMPERATURE


$\overline{SHDN}$ INPUT THRESHOLD VOLTAGE vs. TEMPERATURE


INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE

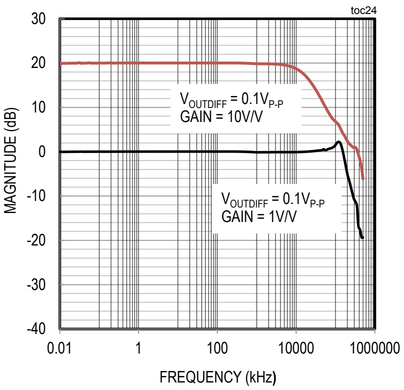

OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE


OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE

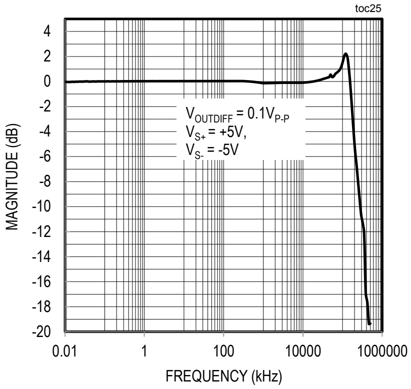
Typical Operating Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

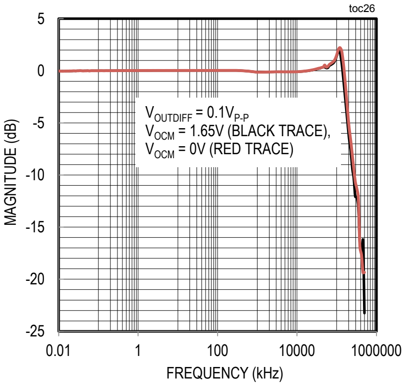
SMALL-SIGNAL GAIN vs. FREQUENCY



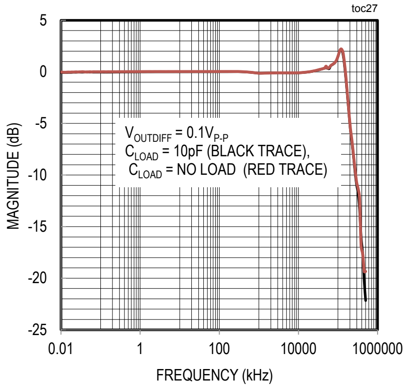
SMALL-SIGNAL GAIN vs. FREQUENCY



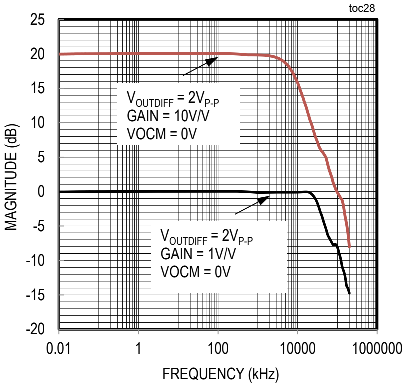
SMALL-SIGNAL GAIN vs. FREQUENCY



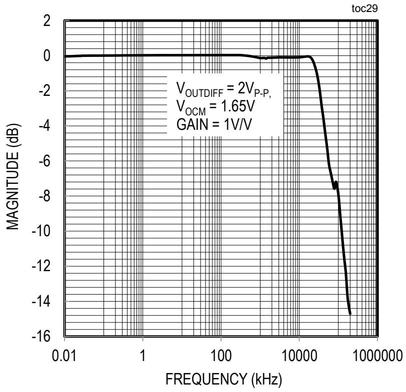
SMALL-SIGNAL GAIN vs. FREQUENCY



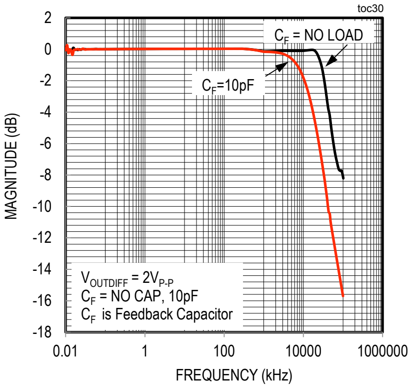
LARGE-SIGNAL GAIN vs. FREQUENCY



LARGE-SIGNAL GAIN vs. FREQUENCY



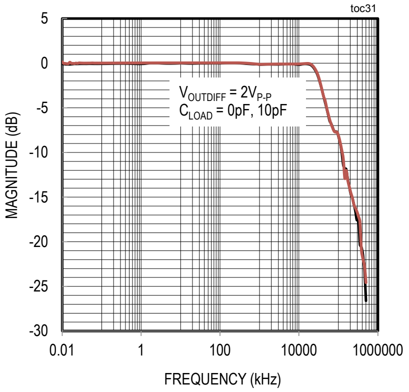
LARGE-SIGNAL GAIN vs. FREQUENCY



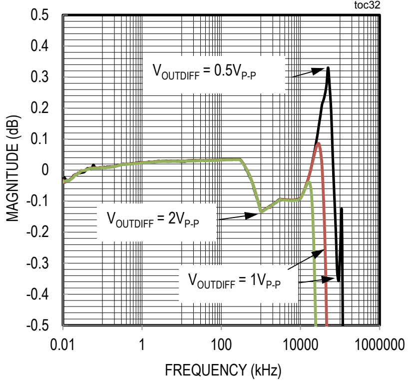
Typical Operating Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

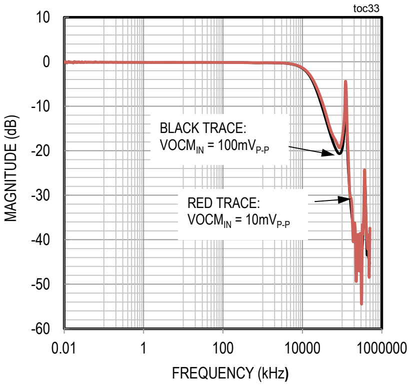
LARGE-SIGNAL GAIN vs. FREQUENCY



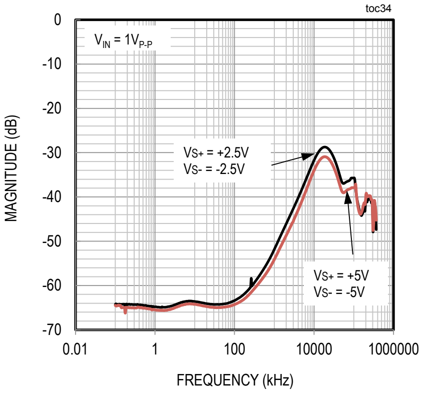
LARGE-SIGNAL GAIN FLATNESS vs. FREQUENCY



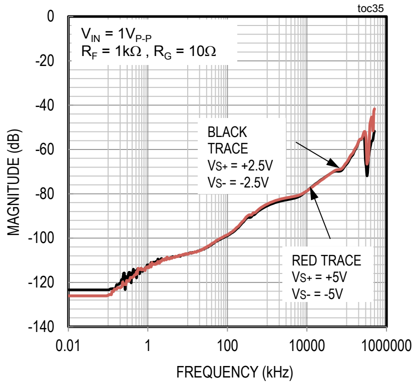
VOCM RESPONSE vs. FREQUENCY



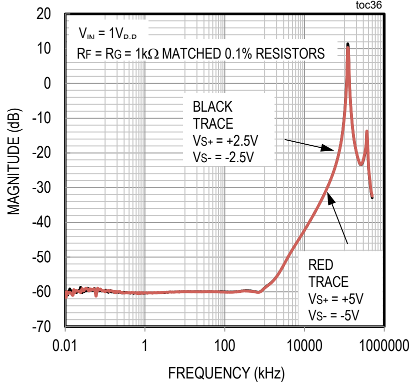
OUTPUT BALANCE ERROR vs. FREQUENCY



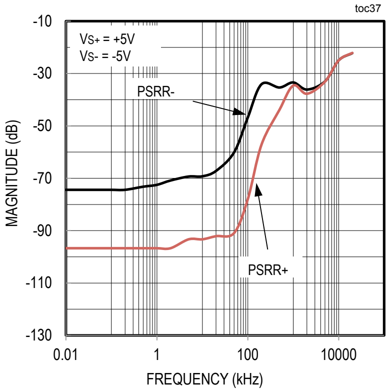
INPUT AC CMRR vs. FREQUENCY



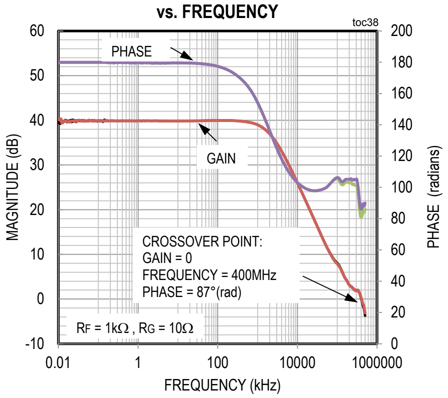
VOCM OUTPUT AC CMRR vs. FREQUENCY



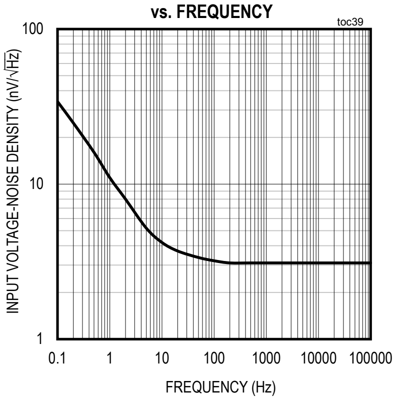
PSRR+ vs. FREQUENCY



UNITY-GAIN BANDWIDTH AND PHASE vs. FREQUENCY

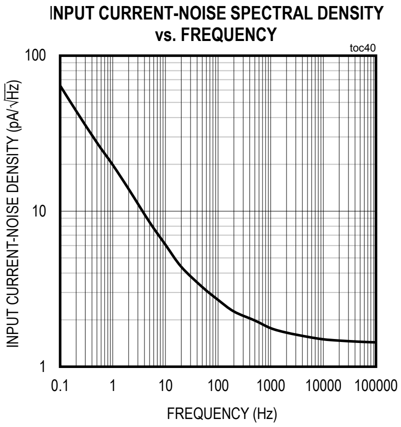


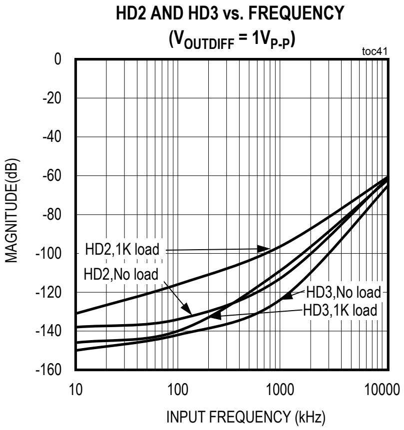
INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY

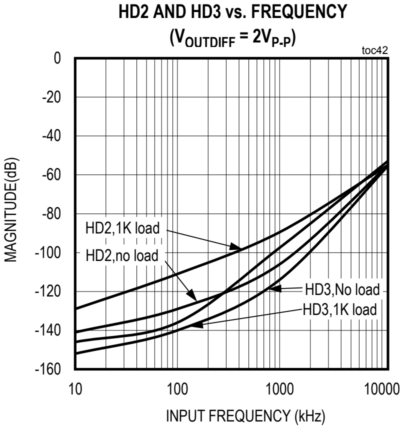


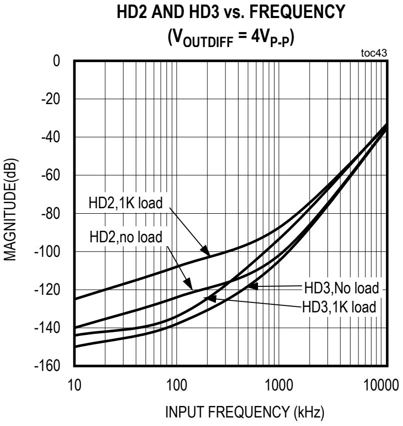
Typical Operating Characteristics (continued)

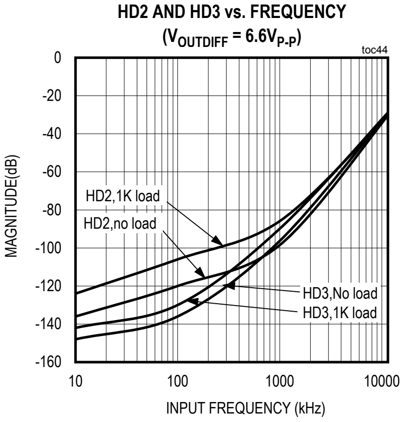
(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

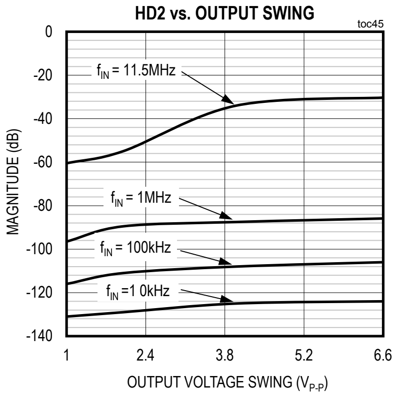

INPUT CURRENT-NOISE SPECTRAL DENSITY vs. FREQUENCY

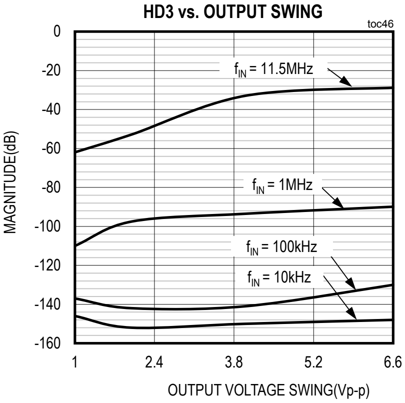

HD2 AND HD3 vs. FREQUENCY ($V_{OUTDIFF}$ = $1V_{P-P}$)

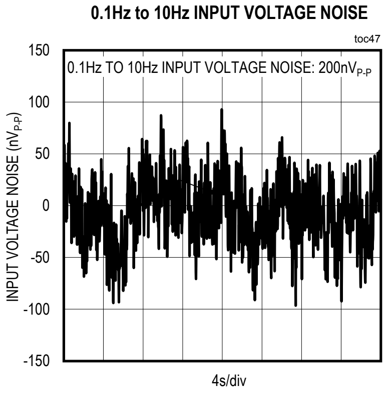

HD2 AND HD3 vs. FREQUENCY ($V_{OUTDIFF}$ = $2V_{P-P}$)

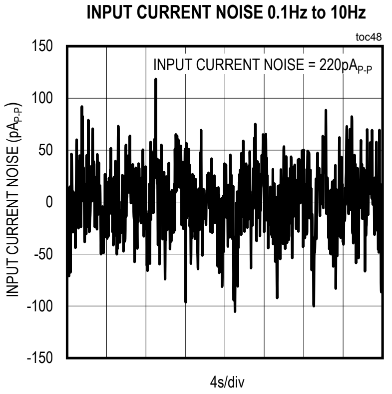

HD2 AND HD3 vs. FREQUENCY ($V_{OUTDIFF}$ = $4V_{P-P}$)


HD2 AND HD3 vs. FREQUENCY ($V_{OUTDIFF}$ = $6.6V_{P-P}$)


HD2 vs. OUTPUT SWING


HD3 vs. OUTPUT SWING

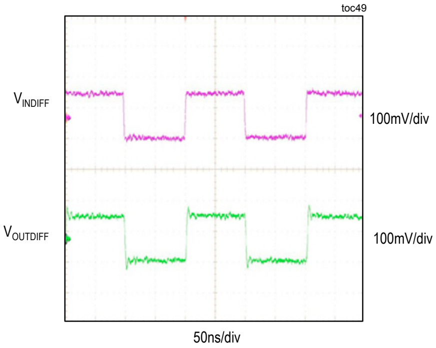

0.1Hz to 10Hz INPUT VOLTAGE NOISE


INPUT CURRENT NOISE 0.1Hz to 10Hz

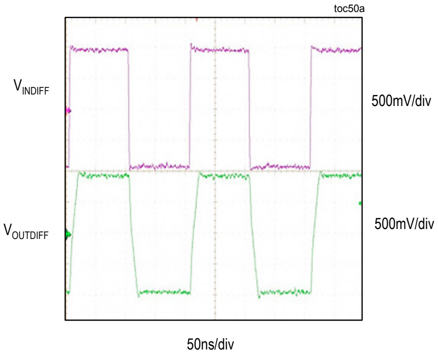
Typical Operating Characteristics (continued)

(V_{S+} = +5V, V_{S-} = -5V, V_{OCM} = 0V, $\overline{SHDN}$ = V_{S+}, EP = 0V, R_F = R_G = 1kΩ, R_L = 1kΩ (between OUT+ and OUT-), T_A = -40°C to +125°C, unless otherwise noted.)

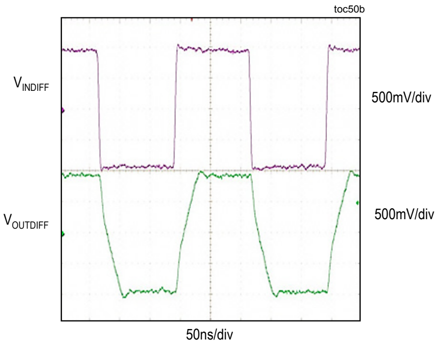
SMALL-SIGNAL RESPONSE



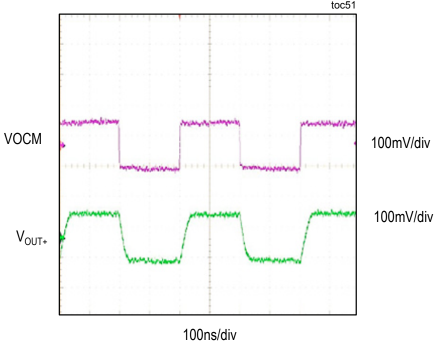
LARGE-SIGNAL TRANSIENT RESPONSE



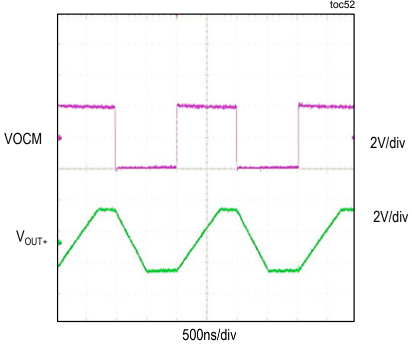
LARGE-SIGNAL TRANSIENT RESPONSE



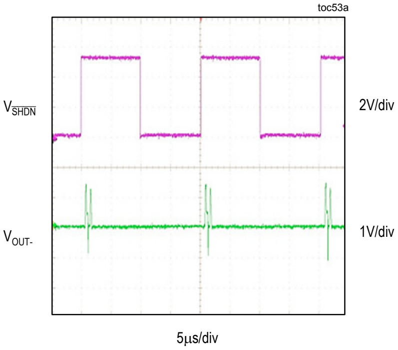
VOCM SMALL-SIGNAL TRANSIENT RESPONSE



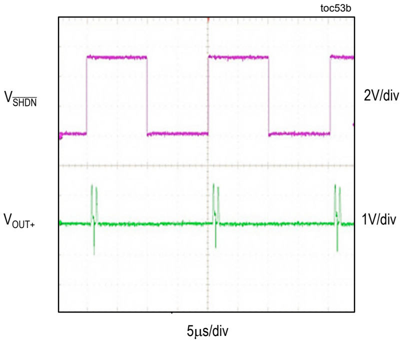
VOCM LARGE-SIGNAL TRANSIENT RESPONSE



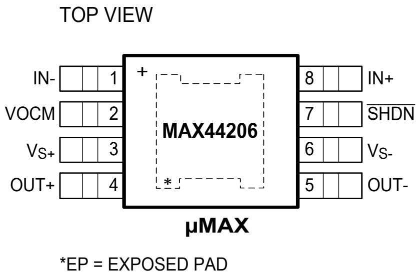
OUTPUT-TRANSIENT RESPONSE vs. SHUTDOWN PULSE



OUTPUT+ TRANSIENT RESPONSE vs. SHUTDOWN PULSE



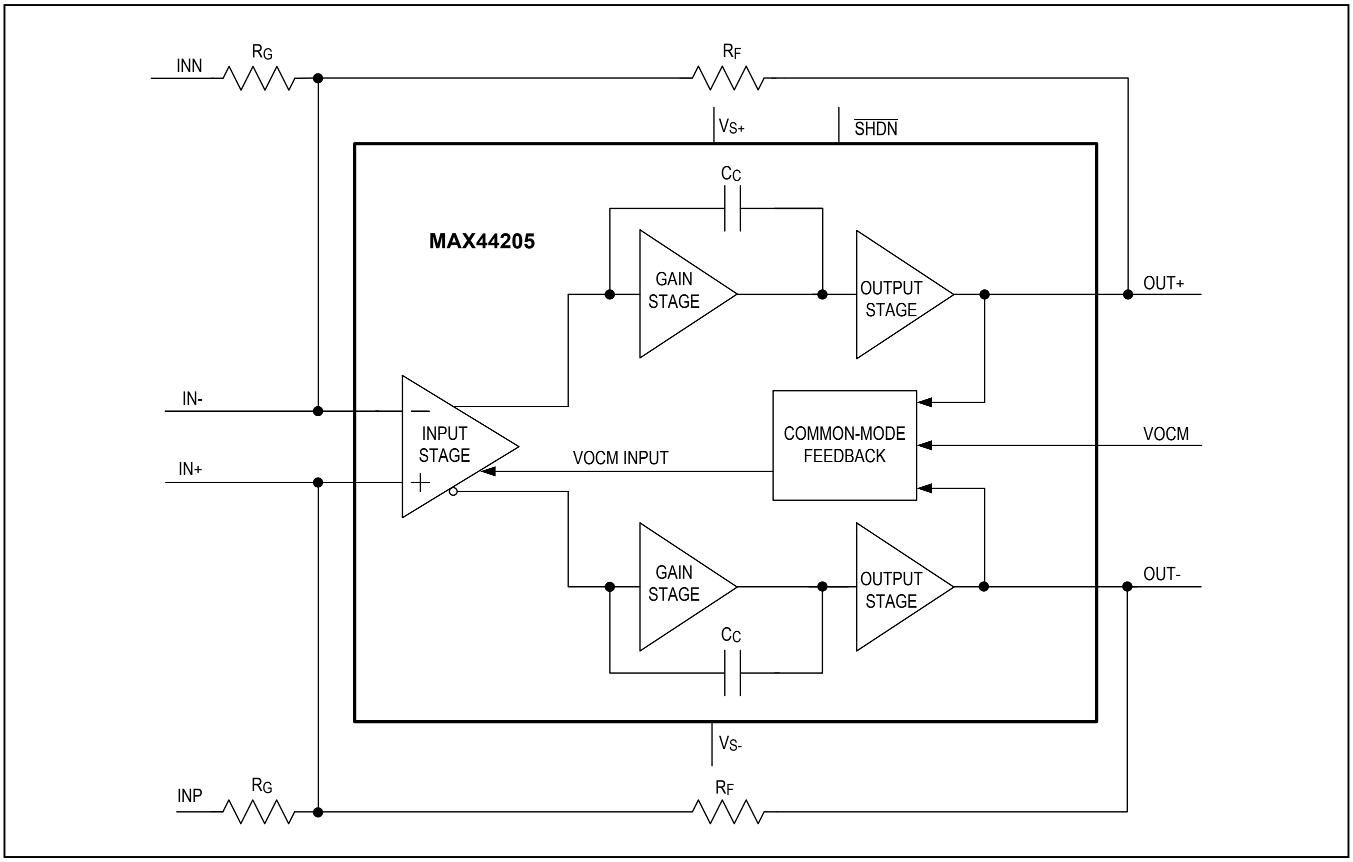
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	IN-	Inverting Input
2	VOCM	Output Common-Mode Voltage Input
3	V_{S+}	Positive Supply Voltage Input
4	OUT+	Noninverting Differential Output
5	OUT-	Inverting Differential Output
6	V_{S-}	Negative Supply Voltage Input
7	$\overline{\text{SHDN}}$	Shutdown Mode Input (Active-Low). $\overline{\text{SHDN}}$ is referred to the exposed pad.
8	IN+	Noninverting Input
—	EP	Exposed Pad. EP is the logic ground reference to the $\overline{\text{SHDN}}$ pin.

Functional Diagram



Detailed Description

The MAX44206 is a low-noise, low-power, very low-distortion fully differential (input and output) op amp capable of driving high-resolution 16-/18-/20-bit SAR ADCs with input signal frequencies from DC to 1MHz. These high-resolution signal chain ICs are used in test and measurement applications, as well as medical instrumentation and industrial control systems.

This fully differential op amp accepts either single-ended or fully differential input signals at its inputs and converts the input signal into fully differential outputs that are exactly equal in amplitude and 180° apart in phase. Ideally, the noise and distortion performance of the amplifier should match or exceed the linearity of the ADC to preserve the overall system accuracy.

Four precisely matched resistors (two for feedback and two for gain setting) set the differential closed-loop gain as shown in the *Functional Diagram*.

The MAX44206 has an output voltage common-mode (VOCM) input to set the DC common-mode voltage level of the differential outputs without affecting the balance of the AC differential output signal on each output. The MAX44206 also features a low-power shutdown mode that consumes only 6.8µA of supply current from the V_S+ pin. Note that while the outputs are high impedance during shutdown, the feedback networks may provide paths for current to flow from the input source(s).

Terminology and Definitions

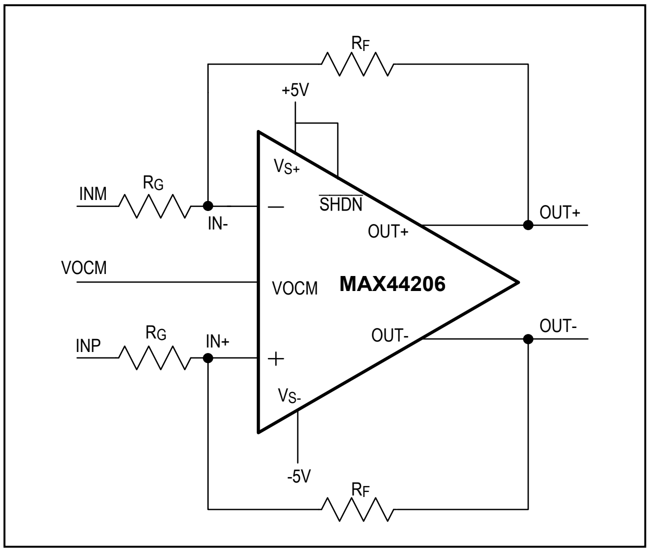


Figure 1. Differential Input, Differential Output Configuration (Decoupling Capacitors Not Shown for Simplicity)

Differential Voltage

The differential voltage at the input is the voltage applied across INP to INM and the differential voltage at the output is the voltage across OUT+ to OUT-. Equations for input and output differential voltages are listed below:

$$V_{IN,dm} = (V_{INP} - V_{INM})$$

$$V_{OUT,dm} = (V_{OUT+} - V_{OUT-})$$

V_{OUT+} and V_{OUT-} are voltages at the OUT+ and OUT- terminals with respect to output common-mode voltage set by the VOCM input voltage.

Common-Mode Voltage

The common-mode voltage at the input is the average of the input pins (IN+ and IN-) and at the output, it is the average of two outputs. Equations for input and output common-mode voltages are listed below:

$$V_{IN,cm} = (V_{IN+} + V_{IN-})/2$$

$$V_{OUT,cm} = V_{OCM} = (V_{OUT+} + V_{OUT-})/2$$

Though it was mentioned that the input common-mode voltage is the average of the voltage seen on both input pins, the range is slightly different depending on if the input signal is fully differential or single ended.

For fully differential input applications, where $V_{INP} = -V_{INM}$, the common-mode input voltage is:

$$V_{IN,cm} = (V_{IN+} + V_{IN-})/2 \cong \text{VOCM} \times R_G/(R_F + R_G) + V_{CM} \times R_F/(R_F + R_G)$$

With single-ended input applications, there will be an input signal component to the input common-mode voltage, as there is no out-of-phase signal not applied on the other input. Applying V_{INP} (connecting V_{INM} to zero), the common-mode input voltage is:

$$V_{IN,cm} = (V_{IN+} + V_{IN-})/2 \cong \text{VOCM} \times R_G/(R_F + R_G) + V_{CM} \times R_F/(R_F + R_G) + V_{INP}/2 \times R_F/(R_F + R_G)$$

Common-Mode Offset Voltage

The common-mode offset voltage is defined as the difference between the voltage applied to the VOCM terminal and the output common-mode voltage.

$$V_{OS,cm} = (V_{OUT,cm} - V_{OCM})$$

Input Offset Voltage, CMRR, and VOCM CMRR

Input offset voltage is the differential voltage error ($V_{OS,dm}$) between the input pins (IN+ and IN-). CMRR performance is affected by both the input offset voltage error at the input due to change in input common-mode voltage ($V_{IN\_,cm}$) and the change in input offset voltage $V_{OS,dm}$) due to VOCM change. So, there are two CMRR terms:

$$CMRR_{VIN,cm} = \Delta(V_{IN\_,cm})/\Delta(V_{OS,dm})$$

$$CMRR_{VOCM} = \Delta(V_{OCM})/\Delta(V_{OS,dm})$$

The output common-mode rejection ratio is strongly affected by the matching of gain-setting feedback network.

Output Balance Error

An ideal differential output implies the two outputs of the amplifier should be exactly equal in amplitude but 180° apart in phase. Output balance is the measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal. It is generally expressed as dB in log scale.

$$\text{Output Balance Error} = 20 \times \log|(V_{OUT,cm})/(V_{OUT,dm})|$$

Operation and Equations

The *Functional Diagram* details the internal architecture of the differential op amp. The negative feedback loop across the outputs to respective inputs force voltages on IN+ and IN- pins equal to each other. That implies:

$$\frac{V_{INP}}{R_F} = \frac{-V_{OUT-}}{R_G}$$

$$\frac{V_{INN}}{R_F} = \frac{-V_{OUT+}}{R_G}$$

From above equations see the relationship between differential output voltage and inputs.

$$(V_{OUT+} - V_{OUT-}) = (V_{INP} - V_{INN}) \times \frac{R_F}{R_G}$$

The VOCM input voltage with the help of the common-mode feedback circuit drives the output common-mode voltage level to VOCM. This results in the following output relations:

$$(V_{OUT+}) = (VOCM) + \frac{V_{OUT,DM}}{2}$$

$$(V_{OUT-}) = (VOCM) - \frac{V_{OUT,DM}}{2}$$

Input and ESD Protection

As shown in Figure 2, ESD diodes are present on all the pins with respect to the V_{S+} and V_{S-} pins so that these ESD diodes turn on and protect the part when voltages on these pins go out of range from either supplies by more than one diode drop. There are two series input resistors and back-to-back diode protection between the inputs for protection against excessive differential voltages across the amplifier's inputs.

$\overline{\text{SHDN}}$ and Exposed Pad Shutdown Operation

The MAX44206 offers a shutdown mode for low-power operation. Drive $\overline{\text{SHDN}}$ below 0.65V with respect to the µMAX exposed pad (EP) to shut down the part and only 6.8µA (typ) will be drawn from V_{S+}. To keep the part active, $\overline{\text{SHDN}}$ needs to be at least 1.25V above EP.

Exposed Pad

EP is the logic ground reference to the $\overline{\text{SHDN}}$ pin. EP should be connected to the PCB ground plane for optimum thermal dissipation.

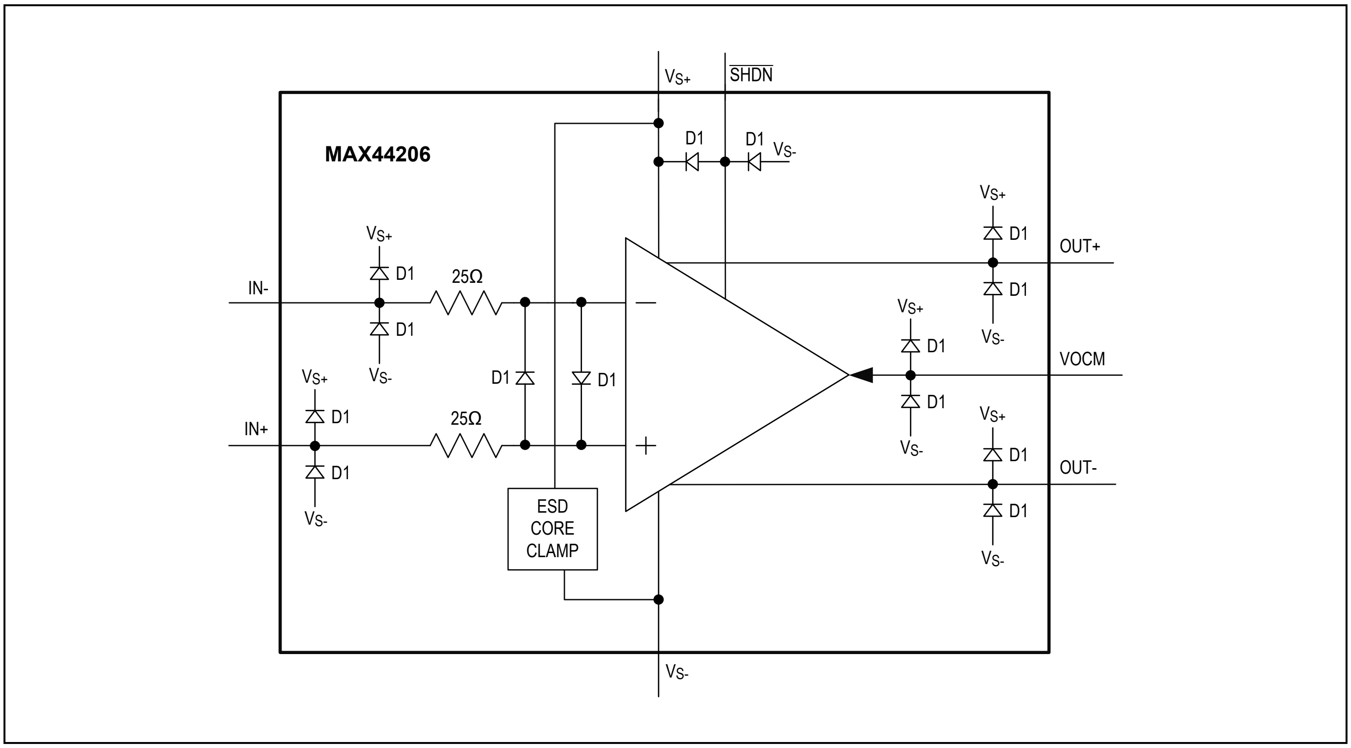


Figure 2. Showing ESD Protection Scheme in MAX44206

Shutdown Operation with External Components and Stimuli

In shutdown mode, quiescent supply current is low. However, there will be currents flowing into the IC pins depending on the external components and applied signals. Figure 3 shows the block diagram with these current paths and Figure 2 shows internal protection devices. In active operation mode (shutdown disabled), input signals are applied to INP and INN. The voltage applied to the VOCM pin sets the output common-mode voltage.

In shutdown mode, the voltages applied to INP, INN, and VOCM will interact with the IC internal components resulting in current flowing into the IC pins. It must be noted that the op amp's outputs, OUT+ and OUT-, exhibit high-impedance state in shutdown mode.

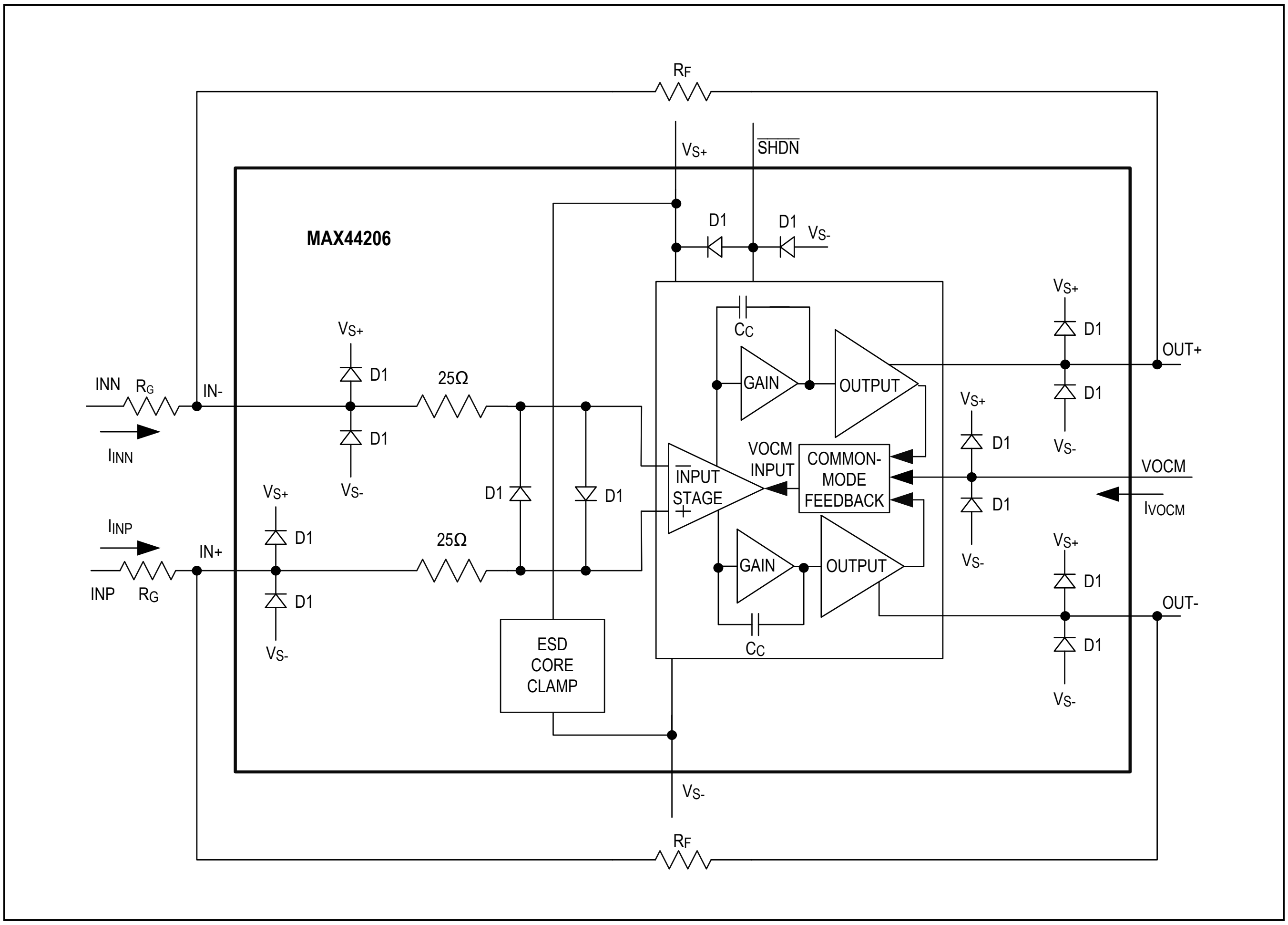


Figure 3. Currents Flowing when MAX44206 is in Shutdown

Applications Information

The fully differential op amp is shown in Figure 4 for reference. Fully differential op amps provide a lot of advantages, including rejecting common-mode noise coupled to the input, the output, and from the power supply. The effective output swing is increased by a factor of two as the outputs are equal in amplitude and 180° apart in phase.

For example, by applying a fully differential input signal of $1V_{P-P}$ across INP and INN on Figure 1 there is a $1V_{P-P}$ differential output voltage swing. Another advantage of having fully differential outputs is that even order harmonics will be suppressed at the output.

Input Impedance Mismatch Due to Source Impedance

The impedance looking into the IN+ and IN- nodes of Figure 5 depends on how the inputs are driven. For a fully differential input signal, i.e., $V_{INP} = V_{INM} + 180°$. The input impedance looking into inputs is shown in Figure 5.

$$R_{INP} = R_{INM} = R_G$$

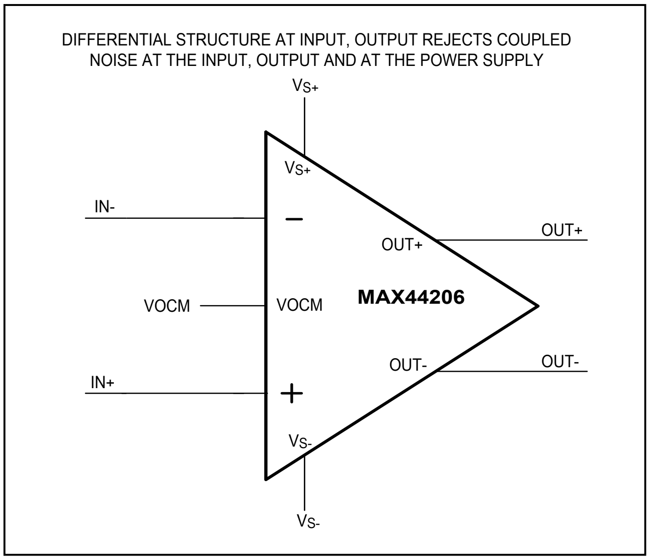


Figure 4. Fully Differential Op Amp

For a single-ended input signal, since the inputs are not balanced, the input impedance actually increases relative to the fully differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_G}{[1-\left(\frac{1}{2}\right)\times\frac{R_F}{(R_G+R_F)}]}$$

Apart from the single-ended input and differential input signal cases, an input signal source from a nonzero source impedance may cause imbalance between feedback resistor networks for single-ended input driving case as shown in the Figure 6. A terminating resistor RT as shown in Figure 6 is used to impedance match to the source such that:

$$R_T = R_{INM} \times \frac{R_S}{R_{INM} - R_S}$$

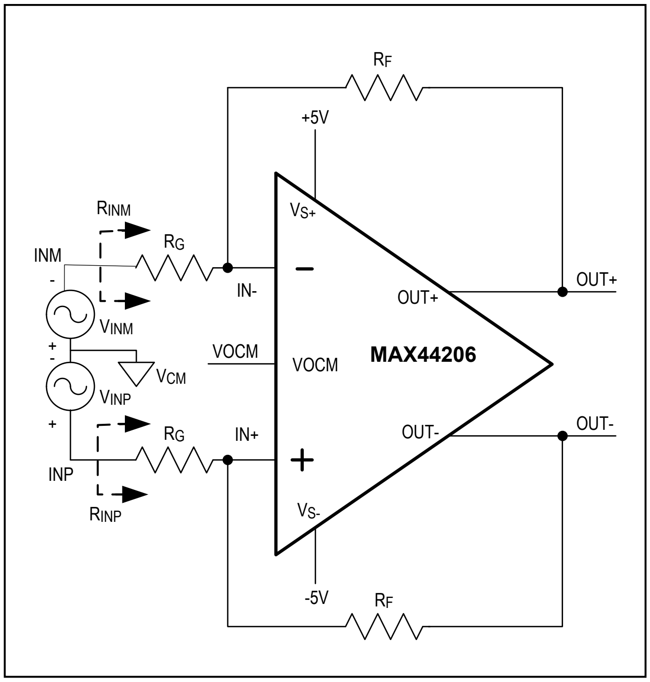


Figure 5. Showing Fully Differential Architecture

A terminating resistor is inserted to correct for impedance mismatch between the source and input. The gain resistor mismatch across feedback networks is created due to the parallel combination of R_T and R_S. So, to balance out the gain resistor mismatch on the other input, insert R_B such that:

$$R_B = R_T \times \frac{R_S}{R_T - R_S}$$

Effects of Input Resistor Mismatch

If there is a mismatch between the feedback resistor (R_F) pair and gain resistor (R_G) pair, there will be a small delta in the feedback factor across the input pins. This delta in the feedback factor is a source of common-mode error. To apply an AC CMRR test without a differential input signal, the common-mode rejection is proportional to the resistor mismatch. Using 0.1% or better resistors will mitigate most of the problems and will yield good CMRR performance.

Noise Calculations

The MAX44206 offers input voltage and current noise densities of 3.1nV/√Hz and 1.5pA/√Hz, respectively. From Figure 7, the total output noise is a combination of noise generated by the amplifier and the feedback and gain resistors. The total output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{nt} = \sqrt{\begin{aligned}&[e_n \times (1+\frac{R_F}{R_G})]^2 + 2\times(i_n \times R_F)^2 \\ &+2\times(e_{nRG}\times\frac{R_F}{R_G})^2 + 2\times(e_{nRF})^2\end{aligned}}$$

e_{nt} is total output noise of the circuit shown in Figure 7

e_n is the input voltage-noise density

i_n is the input current-noise density

e_{nRG} is the noise voltage density contributed by the gain resistor RG

e_{nRF} is the noise voltage density contributed by the feedback resistor RF

Resistor Noise = $\sqrt{4 \times k \times T \times R \times \Delta f}$ in nV/√Hz

T is absolute temperature in Kelvin

k is Boltzmann constant: k = 1.38 x 10^{-23} in joules/Kelvin

R is resistance in ohms and Δf is frequency range in Hertz

The MAX44206 input-referred voltage noise contributes the equivalent noise of a 600Ω resistor. For low noise, keep the source and feedback resistance at or below this value, i.e. $R_S + R_G//R_F \le 600\Omega$. At combinations of below 600Ω, amplifier noise is dominant, but in the region 600Ω to 10kΩ, the noise is dominated by resistor thermal noise. Any larger resistances beyond that, the noise current multiplied by the total resistance dominated the noise.

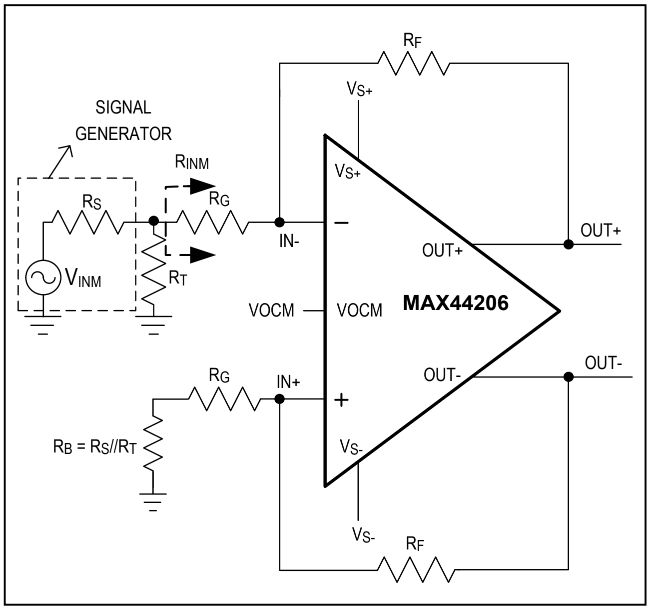


Figure 6. Compensation for Source Impedance

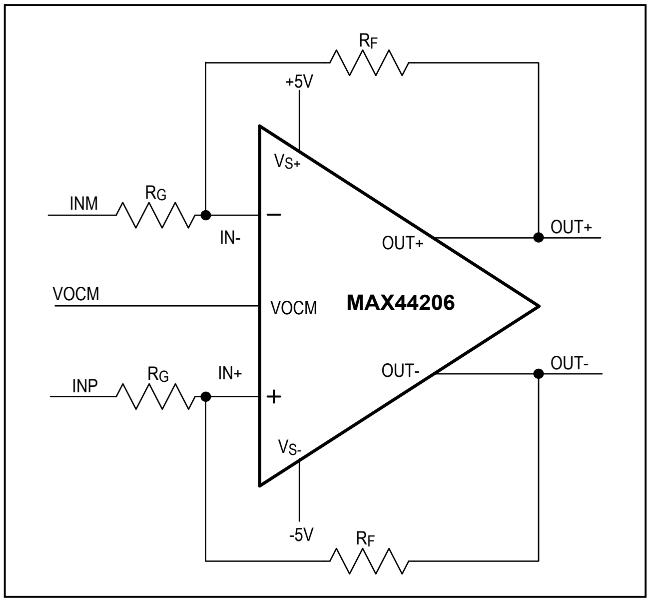


Figure 7. Fully Differential Amplifier

Lower resistor values are ideal for low-noise performance at the cost of increased distortion due to increased loading of the feedback network on the output stage. Higher resistor values will yield better distortion performance due to less loading on the output stage but at the cost of increase in higher output noise.

Improving Stability Using Feedback Capacitors

When the MAX44206 is configured such that a combination of parasitic capacitances at the inverting input form a pole whose frequency lies within the closed-loop bandwidth of the amplifier, a feedback capacitor across the feedback resistor is needed to form a zero at a frequency close to the frequency of the parasitic pole to recover the lost phase margin.

Adding larger value feedback capacitors will reduce the peaking of the amplifier but decreases the closed-loop -3dB bandwidth.

Layout and Bypass Capacitors

For single-supply applications, it is recommended to place a 0.1µF NPO or C0G ceramic capacitor within 1/8th of an inch from the V_{S+} pin to ground and to also connect a 10µF ceramic capacitor within 1 inch of the V_{S+} pin to GND.

In dual-supply applications, it is recommended to install 0.1µF NPO or C0G ceramic capacitor within 1/8th of an inch from the V_{S+} and V_{S-} pins to GND and place 10µF ceramic capacitors within 1 inch of the V_{S+} and V_{S-} pins to GND. Low ESR\ESL NPO capacitors are recommended for 0.1µF or smaller decoupling capacitors. A 0.1µF or 0.22µF capacitor is a good choice close to VOCM input pin to ground.

Signal routing into and out of the part should be direct and as short as possible into and out of the op amp inputs and outputs. The feedback path should be carefully routed with the shortest path possible without any parasitic capacitance forming between feedback trace and board power planes. Ground and power planes should be removed from directly under the amplifier input and output pins. Also, care should be taken such that there will be no parasitic capacitance formed around the summing nodes at the inputs that could affect the phase margin of the part.

Any load capacitance beyond a few picofarads needs to be isolated using series output resistors placed as close as possible to the output pins to avoid excessive peaking or instability.

Driving a Fully Differential ADC

The MAX44206 was designed to drive fully differential SAR ADCs such as the MAX11905. The MAX11905 is part of a family of 20-/18-/16-bit, 1.6Msps/1Msps ADCs that offer excellent AC and DC performance. Figure 8 details a fully differential input to the MAX44206, which then drives the fully differential MAX11905 ADC inputs through the ADC input filter shown in the dashed box.

The MAX6126 provides a 3V reference output voltage, which is fed to the ADC's reference. The MAX44206's common mode (VOCM) is created by dividing down the reference voltage by a factor of two. A pair of 1kΩ 0.1% resistors are used for this purpose. The VOCM input is bypassed to GND with a combination of 2.2µF (X7R) and 0.1µF (NPO) capacitors.

The MAX44206 is connected in a unity-gain configuration. The input resistors and feedback resistors are all 1kΩ 0.1% resistors. The feedback resistors are bypassed by a pair of 4.7nF (C0G, 100V) capacitors. These feedback components roll the amplifier off to about 60MHz corner frequency.

The ADC input filter uses a pair of 10Ω 0.1% resistors and a 2.2nF (C0G) capacitor. This input filter assists the MAX44206's settling response with the MAX11905's fast acquisition window.

Figure 8 was used to test the AC performance in Figures 9 and 10. Data were taken with the input frequencies at 10kHz on the MAX11905 Evaluation Kit. Figures 9 to 13 detail the results of the MAX11905 Evaluation Kit (MAX11905DIFEVKIT#) GUI.

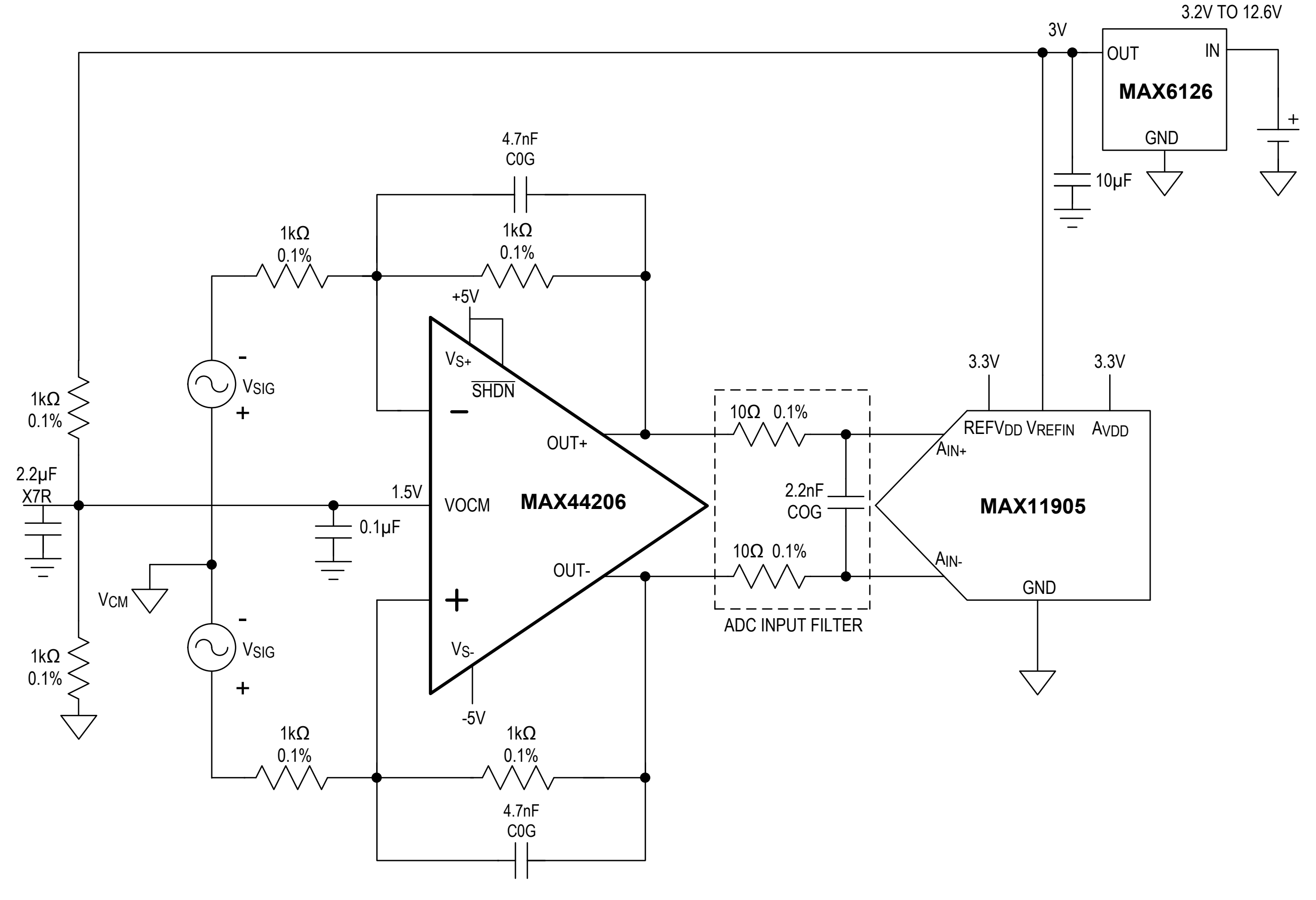


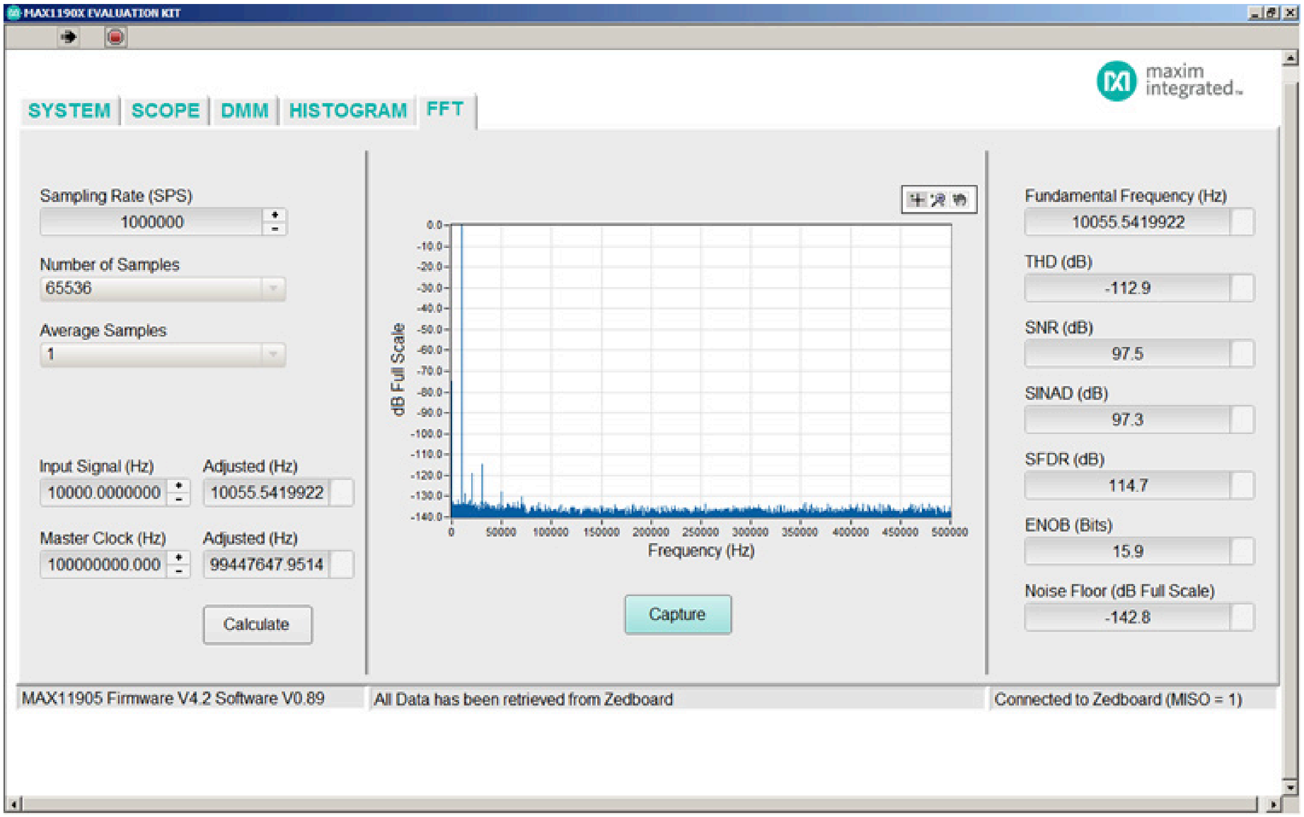
Figure 8. MAX44206 Driving a 20-Bit MAX11905 SAR ADC

The sample rate for Figure 9 is 1Msps and the sample rate for Figure 10 is 1.6Msps, the MAX11905's maximum sample rate. As measured at the MAX11905 output, the signal-to-noise ratio is > 97dB for both sample rates, with total harmonic distortion > 112.9dB.

Figures 11 to 13 detail the DC performance of the MAX44206 and MAX11905. These three figures detail the results of shorting the inputs together to GND at the V_{SIG} sources and measuring the noise histogram at the output of the ADC. All data was measured at 1Msps, with 65,536 samples taken. Figure 11 shows the results at a 20-bit code level with no averaging. Effective number of bits (ENOB) is 17.9 bits.

One technique to improve a system's ENOB is to average multiple samples. The tradeoff is a reduced effective sample rate. The theoretical expected results of averaging are a 0.5 improvement in ENOB for every average factor of 2. Therefore, averaging by 16x should improve ENOB by 2 bits. Figure 12 details this example, and the ENOB is improved nearly 2 bits, from 17.9 bits to 19.8 bits. This shows that the noise from the ADC and the op amp are not limiting the ENOB.

Figure 13 shows the results of averaging by 64x, which will limit the effective sample rate to 15.6ksps (1Msps/64). ENOB is 20.8 bits in this mode, making the MAX11905 a lower power alternative to high-speed 24-bit delta-sigma ADCs.



Sampling Rate (SPS): 1000000

Number of Samples: 65536

Average Samples: 1

Input Signal (Hz): 10000.0000000

Adjusted (Hz): 10055.5419922

Master Clock (Hz): 100000000.000

Adjusted (Hz): 99447647.9514

Fundamental Frequency (Hz): 10055.5419922

THD (dB): -112.9

SNR (dB): 97.5

SINAD (dB): 97.3

SFDR (dB): 114.7

ENOB (Bits): 15.9

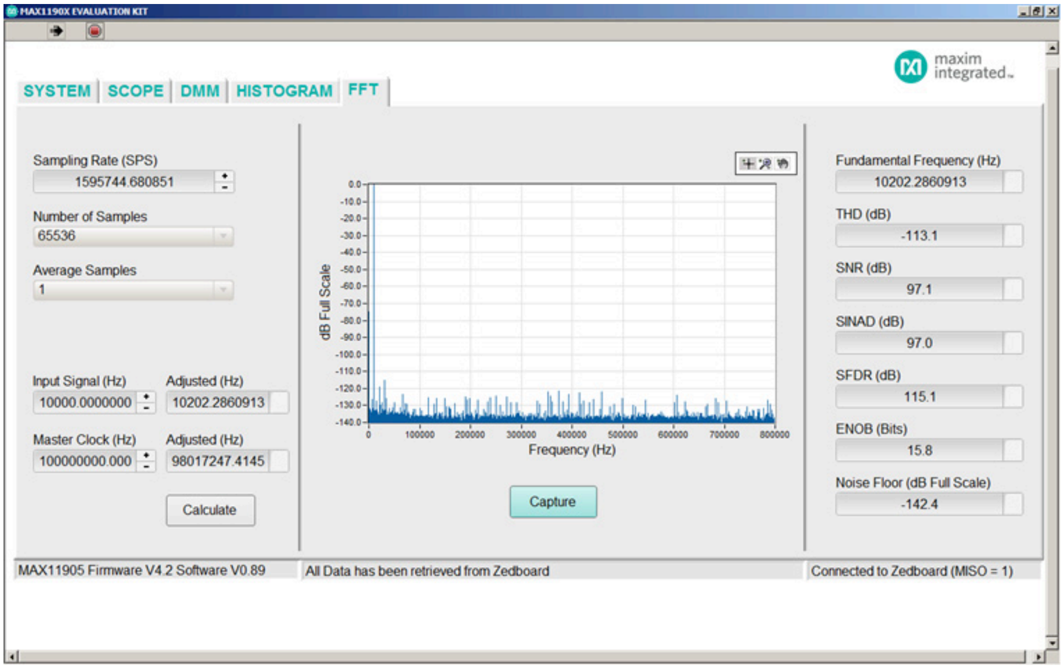
Noise Floor (dB Full Scale): -142.8

MAX11905 Firmware V4.2 Software V0.89

All Data has been retrieved from Zedboard

Connected to Zedboard (MISO = 1)

Figure 9. MAX11905 FFT (f_{SAMPLE} = 1Msps, f_{IN} = 10kHz)



Sampling Rate (SPS)
1595744.680851

Number of Samples
65536

Average Samples
1

Input Signal (Hz)
10000.0000000

Adjusted (Hz)
10202.2860913

Master Clock (Hz)
100000000.000

Adjusted (Hz)
98017247.4145

Fundamental Frequency (Hz)
10202.2860913

THD (dB)
-113.1

SNR (dB)
97.1

SINAD (dB)
97.0

SFDR (dB)
115.1

ENOB (Bits)
15.8

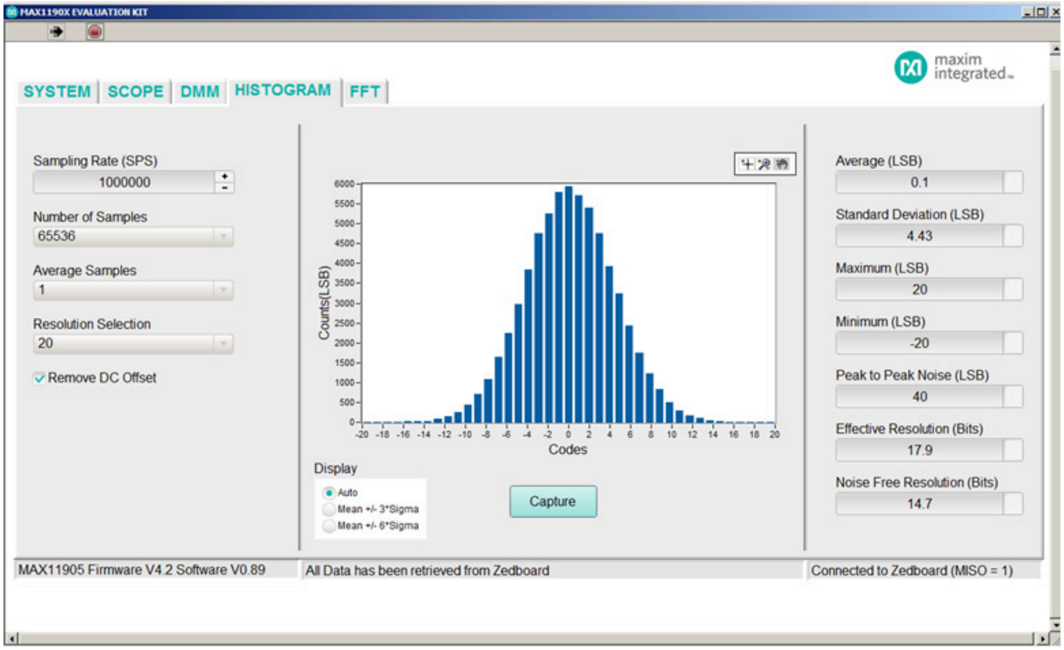
Noise Floor (dB Full Scale)
-142.4

MAX11905 Firmware V4.2 Software V0.89

All Data has been retrieved from Zedboard

Connected to Zedboard (MISO = 1)

Figure 10. MAX11905 FFT (f_{SAMPLE} = 1.6Msps, f_{IN} = 10kHz)



Sampling Rate (SPS)
1000000

Number of Samples
65536

Average Samples
1

Resolution Selection
20

☑ Remove DC Offset

Display
● Auto
○ Mean +/- 3*Sigma
○ Mean +/- 6*Sigma

Average (LSB)
0.1

Standard Deviation (LSB)
4.43

Maximum (LSB)
20

Minimum (LSB)
-20

Peak to Peak Noise (LSB)
40

Effective Resolution (Bits)
17.9

Noise Free Resolution (Bits)
14.7

MAX11905 Firmware V4.2 Software V0.89

All Data has been retrieved from Zedboard

Connected to Zedboard (MISO = 1)

Figure 11. MAX11905 Output Data Histogram (Inputs Shorted, Averaging = 1, f_{SAMPLE} = 1Msps)