Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Infineon® LITIX™ Basic

TLD1315EL

3 Channel High Side Current Source

Data Sheet

Rev. 1.1, 2015-03-24

Automotive

3 Channel High Side Current Source
LITIX[TM] Basic

TLD1315EL

1 Overview

Features

- 3 Channel device with integrated output stages (current sources), optimized to drive LEDs
- Output current up to 120mA per channel
- Low current consumption in sleep mode
- PWM-operation supported via VS- and EN-pin
- Integrated PWM dimming engine to provide two LED brightness levels without external logic (e.g. µC)
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection
- Overload protection
- Undervoltage detection
- Infineon® N-1 detection functionality
- Wide temperature range: -40 °C < T_j < 150 °C
- PG-SSOP14 package with exposed heatslug
- Green Product (RoHS compliant)
- AEC Qualified

PG-SSOP14

Description

The LITIX[TM] Basic TLD1315EL is a three channel high side driver IC with integrated output stages. It is designed to control LEDs with a current up to 120 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs per chain (total 9 LEDs) with a current up to 60mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

Table 1 Product Summary

Operating voltage	$V_{S(nom)}$	5.5 V… 40 V
Maximum voltage	$V_{S(max)}$ $V_{OUTx(max)}$	40 V
Nominal output (load) current	$I_{OUTx(nom)}$	60 mA when using a supply voltage range of 8V - 18V (e.g. Automotive car battery). Currents up to $I_{OUT(max)}$ possible in applications with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUTx(max)}$	120 mA; depending on thermal resistance R_{thJA}

Type	Package	Marking
TLD1315EL	PG-SSOP14	TLD1315EL

Table 1 Product Summary

Output current accuracy at R_{SET} = 12 kΩ	k_{LT}	750 ± 7%
Current consumption in sleep mode	$I_{S(sleep,typ)}$	0.1 µA

Protective functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

Diagnostic functions

- N-1 detection, latched function
- SC to Vs (indicated by N-1 diagnosis)

Applications

Designed for exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...

The device is also well suited for interior LED lighting applications such as ambient lighting, interior illumination and dash board lighting.

2 Block Diagram

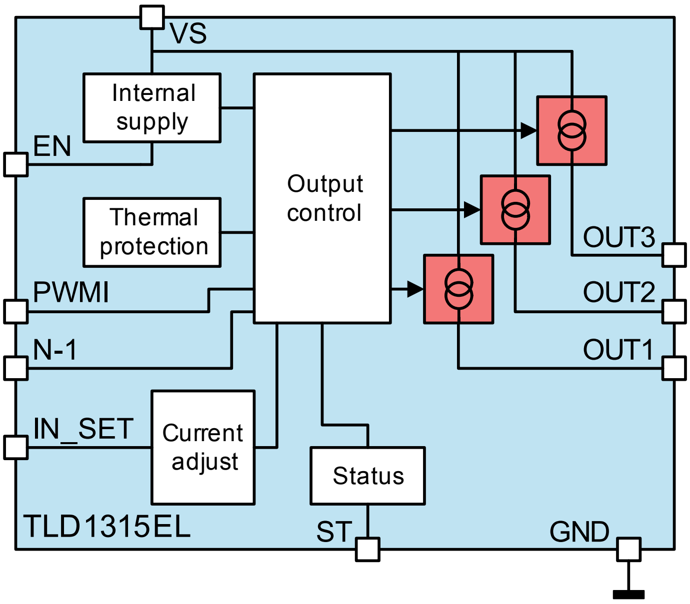

Figure 1 Basic Block Diagram

3 Pin Configuration

3.1 Pin Assignment

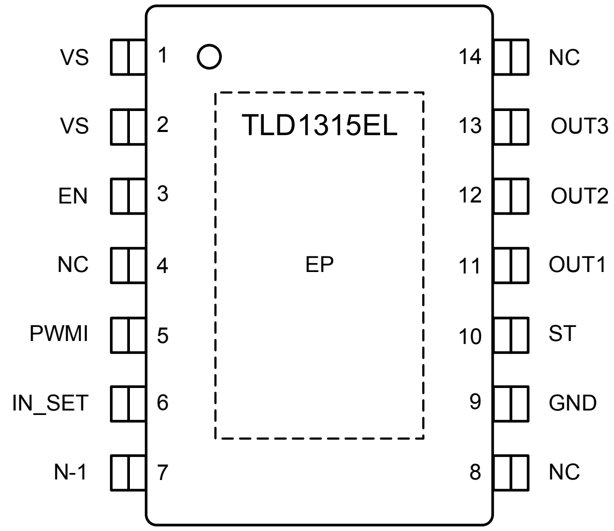

Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	**Supply Voltage;** battery supply, connect a decoupling capacitor (100 nF - 1 µF) to GND
3	EN	I	**Enable pin**
4	NC	–	**Pin not connected**
5	PWMI	I/O	**PWM Input**
6	IN_SET	I/O	**Input / SET pin;** Connect a low power resistor to adjust the output current
7	N-1	I/O	**N-1 pin**
8	NC	–	**Pin not connected**
9	GND	–	[1] **Ground**
10	ST	I/O	**Status pin**
11	OUT1	O	**Output 1**
12	OUT2	O	**Output 2**
13	OUT3	O	**Output 3**
14	NC	–	**Pin not connected**
Exposed Pad	GND	–	[1] **Exposed Pad;** connect to GND in application

1) Connect all GND-pins together.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-16	40	V	–
4.1.2	Input voltage EN	V_{EN}	-16	40	V	–
4.1.3	Input voltage EN related to V_S	$V_{EN(VS)}$	V_S - 40	V_S + 16	V	–
4.1.4	Input voltage EN related to V_{OUTx} V_{EN} - V_{OUTx}	V_{EN} - V_{OUTx}	-16	40	V	–
4.1.5	Output voltage	V_{OUTx}	-1	40	V	–
4.1.6	Power stage voltage V_{PS} = V_S - V_{OUTx}	V_{PS}	-16	40	V	–
4.1.7	Input voltage PWMI	V_{PWMI}	-0.3	6	V	–
4.1.8	IN_SET voltage	V_{IN_SET}	-0.3	6	V	–
4.1.9	N-1 voltage	V_{N-1}	-0.3	6	V	–
4.1.10	Status voltage	V_{ST}	-0.3	6	V	–
Currents						
4.1.11	IN_SET current	I_{IN_SET}	– –	2 8	mA	– Diagnosis output
4.1.12	N-1 current	I_{N-1}	-0.5	0.5	mA	–
4.1.13	Output current	I_{OUTx}	–	130	mA	–
Temperatures						
4.1.14	Junction temperature	T_j	-40	150	°C	–
4.1.15	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.16	ESD resistivity to GND	V_{ESD}	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]
4.1.17	ESD resistivity all pins to GND	V_{ESD}	-500	500	V	CDM[3)]
4.1.18	ESD resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM[3)]

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001-2011
3) ESD susceptibility, Charged Device Model “CDM” according to JESD22-C101E

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.19	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.20	Power on reset threshold	$V_{S(POR)}$	–	5	V	$V_{EN} = V_S$ R_{SET} = 12 kΩ I_{OUTx} = 80% $I_{OUTx(nom)}$ V_{OUTx} = 2.5 V
4.2.21	Junction temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	8	10	K/W	1) 2)
4.3.2	Junction to Ambient 1s0p board	R_{thJA1}	 – –	 61 56	 – –	K/W	1) 3) T_a = 85 °C T_a = 135 °C
4.3.3	Junction to Ambient 2s2p board	R_{thJA2}	 – –	 45 43	 – –	K/W	1) 4) T_a = 85 °C T_a = 135 °C

1) Not subject to production test, specified by design. Based on simulation results.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature). T_a = 85°C, Total power dissipation 1.5 W.

3) The R_{thJA} values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 70µm Cu, 300 mm^2 cooling area. Total power dissipation 1.5 W distributed statically and homogenously over all power stages.

4) The R_{thJA} values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5 mm^3 board with 2 inner copper layers (outside 2 x 70 µm Cu, inner 2 x 35µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over all power stages.

5 EN Pin

The EN pin is a dual function pin:

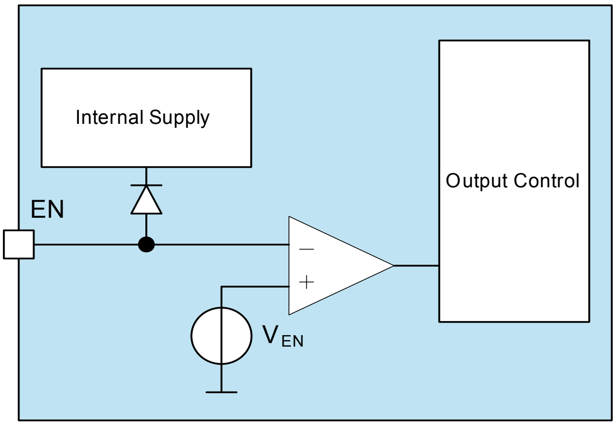

Figure 3 Block Diagram EN pin

Note: The current consumption at the EN-pin I_{EN} needs to be added to the total device current consumption. The total current consumption is the sum of the currents at the VS-pin I_S and the EN-pin I_{EN}.

5.1 EN Function

If the voltage at the pin EN is below a threshold of $V_{EN(off)}$ the LITIX™ Basic IC will enter Sleep mode. In this state all internal functions are switched off, the current consumption is reduced to $I_{S(sleep)}$. A voltage above $V_{EN(on)}$ at this pin enables the device after the Power on reset time t_{POR}.

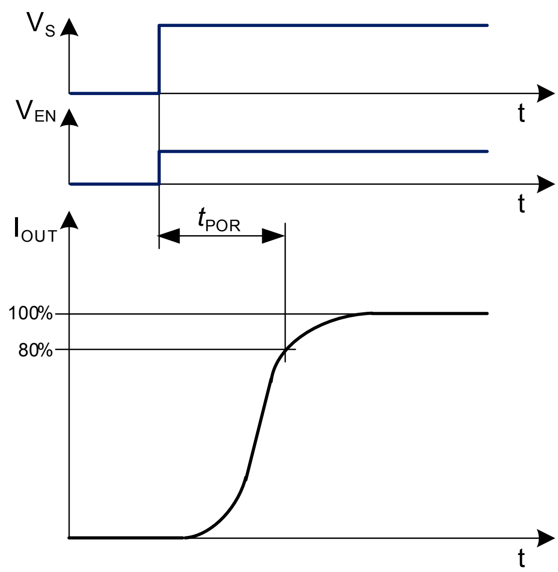

Figure 4 Power on reset

5.2 Internal Supply Pin

The EN pin can be used to supply the internal logic. There are two typical application conditions, where this feature can be used:

1) In "DC/DC control Buck" configurations, where the voltage V_s can be below 5.5V.

2) In configurations, where a PWM signal is applied at the Vbatt pin of a light module. The buffer capacitor C_{BUF} is used to supply the LITIX™ Basic IC during Vbatt low (V_s low) periods. This feature can be used to minimize the turn-on time to the values specified in **Pos. 10.2.15**. Otherwise, the power-on reset delay time t_{POR} (**Pos. 6.3.8**) has to be considered.

The capacitor can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(LS)}}{V_S - V_{D1} - V_{S(POR)}} \tag{1}$$

See also a typical application drawing in **Chapter 11**.

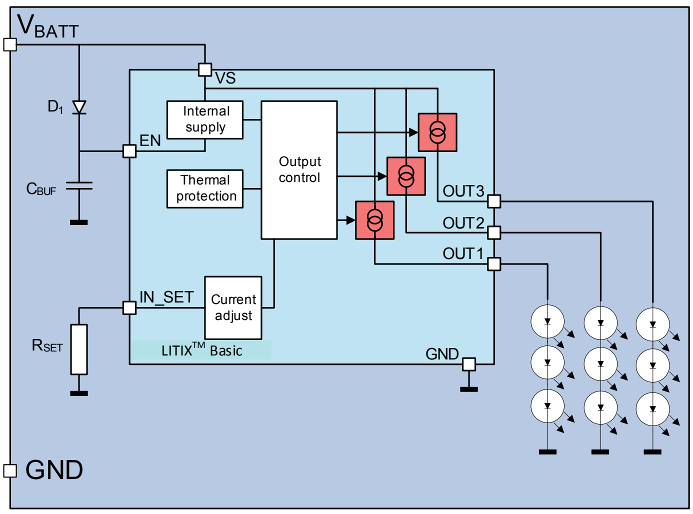

Figure 5 External circuit when applying a fast PWM signal on V_{BATT}

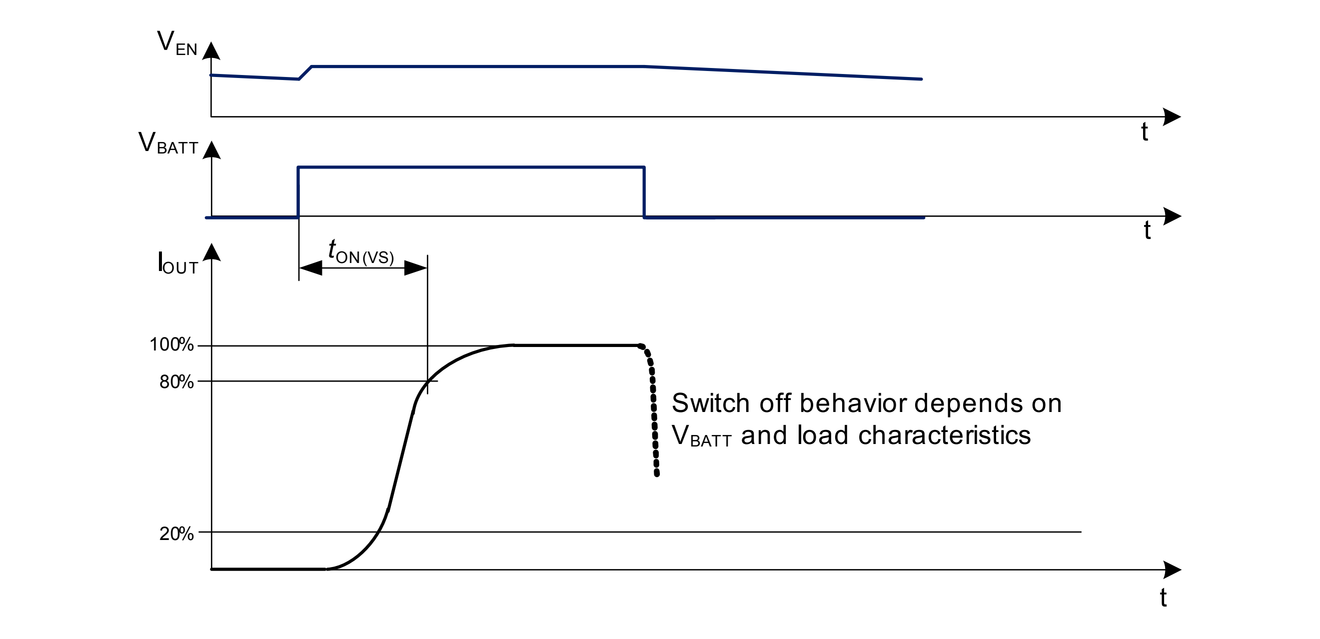

Figure 6 Typical waveforms when applying a fast PWM signal on V_{BATT}

The parameter $t_{ON(VS)}$ is defined at **Pos. 10.2.15**. The parameter $t_{OFF(VS)}$ depends on the load and supply voltage V_{BATT} characteristics.

5.3 EN Unused

In case of an unused EN pin, there are two different ways to connect it:

5.3.1 EN - Pull Up to VS

The EN pin can be connected with a pull up resistor (e.g. 10 kΩ) to V_s potential. In this configuration the LITIX™ Basic IC is always enabled.

5.3.2 EN - Direct Connection to VS

The EN pin can be connected directly to the VS pin (IC always enabled). This configuration has the advantage (compared to the configuration described in **Chapter 5.3.1**) that no additional external component is required.

6 PWMI Pin

The PWMI pin is designed as a dual function pin.

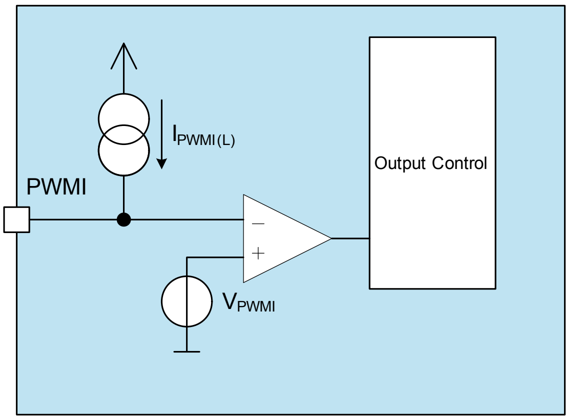

Figure 7 Block Diagram PWMI pin

The pin can be used for PWM-dimming via a push-pull stage of a micro controller, which is connecting the PWMI-pin to a low or high potential.

*Note: The micro controller's push-pull stage has to able to sink currents according to **Pos. 6.3.18** to activate the device.*

Furthermore, the device offers also an internal PWM unit by connecting an external-RC network according to **Figure 10**.

6.1 PWM Dimming

A PWM signal can be applied at the PWMI pin for LED brightness regulation of all 3 output stages. The dimming frequency can be adjusted in a very wide range (e.g. 400 Hz). The PWMI pin is low active. Turn on/off thresholds $V_{PWMI(L)}$ and $V_{PWMI(H)}$ are specified in parameters **Pos. 6.3.15** and **Pos. 6.3.16**.

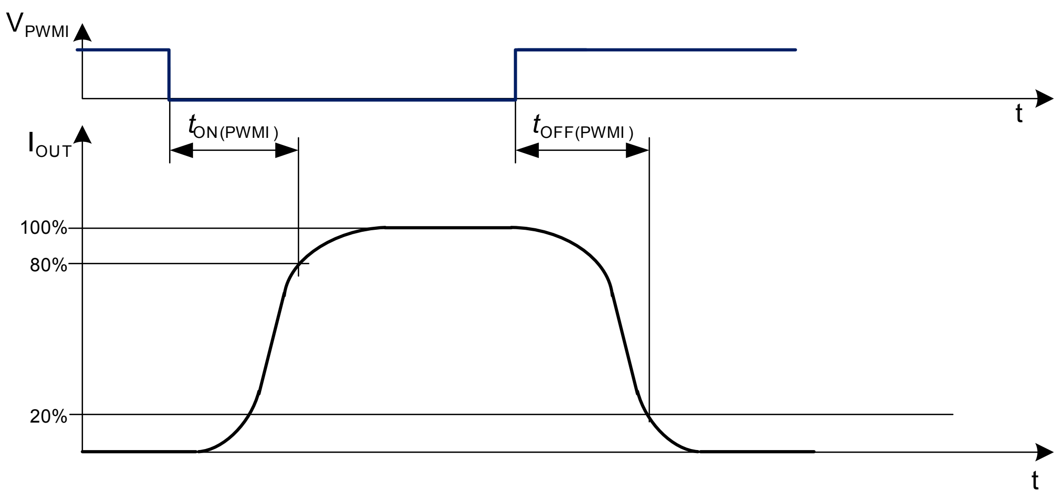

Figure 8 Turn on and Turn off time for PWMI pin usage

6.2 Internal PWM Unit

Connecting a resistor and a capacitor in parallel on the PWMI pin enables the internal pulse width modulation unit. The following figure shows the charging and discharging defined by the RC-network according to **Figure 10** and the internal PWM unit.

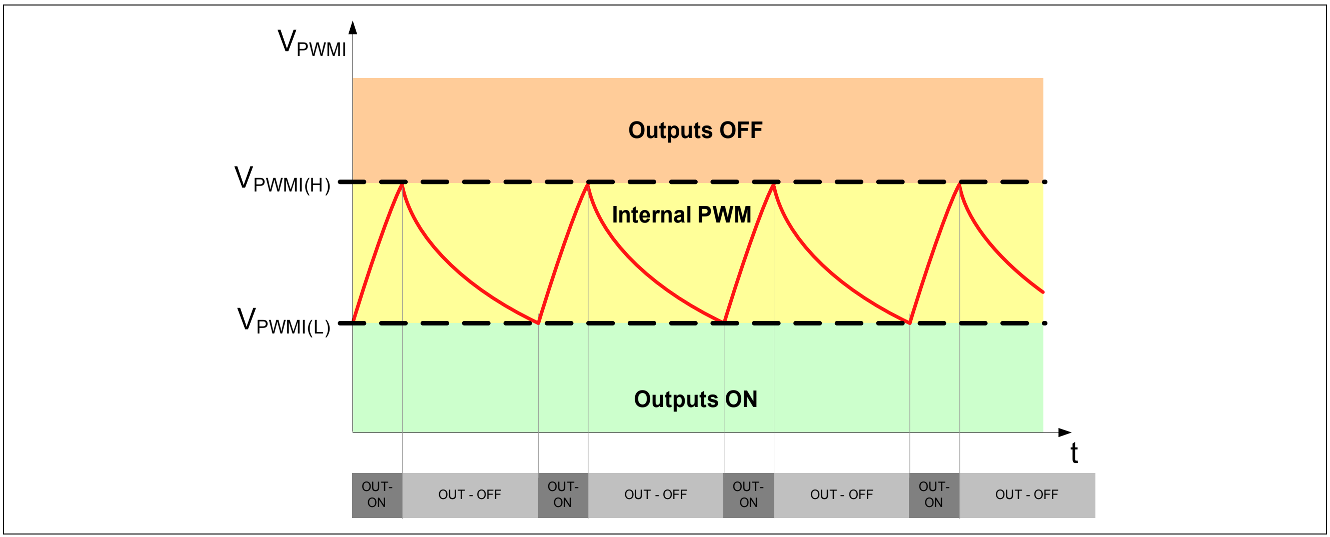

Figure 9 PWMI operating voltages

The PWM Duty cycle (DC) and the PWM frequency can be adjusted using the formulas below. Please use only typical values of $V_{PWMI(L)}$, $V_{PWMI(H)}$ and $I_{PWMI(on)}$ for the calculation of $t_{PWMI(on)}$ and $t_{PWMI(off)}$ (as described in **Pos. 6.3.15** to **Pos. 6.3.18**).

$$t_{PWMI(on)} = -R_{PWMI} \cdot C_{PWMI} \cdot LN\left(\frac{V_{PWMI(H)} - I_{PWMI(on)} \cdot R_{PWMI}}{V_{PWMI(L)} - I_{PWMI(on)} \cdot R_{PWMI}}\right) \quad (2)$$

$$t_{PWMI(off)} = R_{PWMI} \cdot C_{PWMI} \cdot LN\left(\frac{V_{PWMI(H)}}{V_{PWMI(L)}}\right) \quad (3)$$

$$f_{PWMI} = \frac{1}{t_{PWMI(on)} + t_{PWMI(off)}} \quad (4)$$

$$DC = t_{PWMI(on)} \cdot f_{PWMI} \quad (5)$$

Out of this equations the required C_{PWMI} and R_{PWMI} can be calculated:

$$C_{PWMI} = \frac{-I_{PWMI(on)} \cdot t_{PWMI(off)} \cdot \left[\left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}}\right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - 1\right]}{LN\left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}}\right) \cdot \left[V_{PWMI(L)} \cdot \left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}}\right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - V_{PWMI(H)}\right]} \quad (6)$$

$$R_{PWMI} = \frac{t_{PWMI(off)}}{C_{PWMI} \cdot LN\left(\frac{V_{PWMI(H)}}{V_{PWMI(L)}}\right)} \quad (7)$$

See **Figure 10** for a typical external circuitry.

*Note: In case of junction temperatures above $T_{j(CRT)}$ (**Pos. 10.2.16**) the device provides a temperature dependent current reduction feature as described in **Chapter 10.1.1**. In case of output current reduction I_{IN_SET} is reduced as well, which leads to increased turn on-times $t_{PWMI(on)}$, because the C_{PWMI} is charged slower. The turn off-time $t_{PWMI(off)}$ remains the same.*

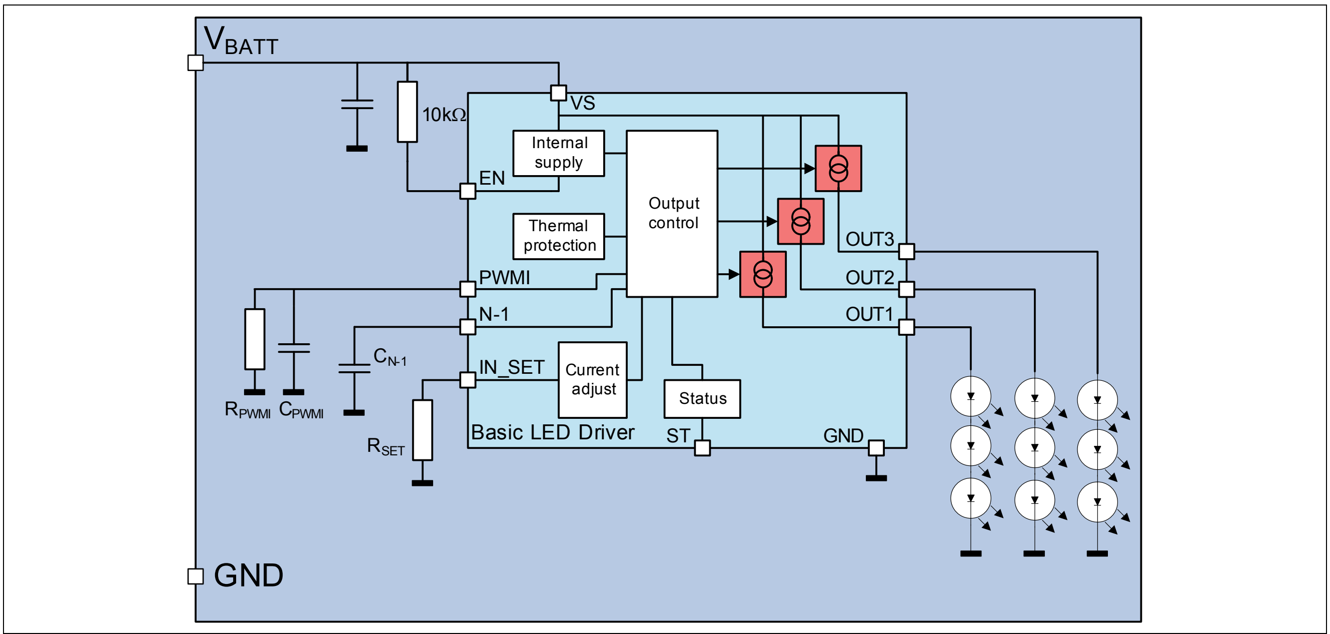

Figure 10 Typical circuit using internal PWM unit

6.3 Electrical Characteristics Internal Supply / EN / PWMI Pin

Electrical Characteristics Internal Supply / EN / PWMI pin

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40 °C to +150 °C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.1	Current consumption, sleep mode	$I_{S(sleep)}$	–	0.1	2	µA	1) V_{EN} = 0.5 V T_j < 85 °C V_S = 18 V V_{OUTx} = 3.6 V
6.3.2	Current consumption, active mode	$I_{S(on)}$	 – – –	 – – –	 1.4 0.75 1.5	mA	2) V_{PWMI} = 0.5 V I_{IN_SET} = 0 µA T_j < 105 °C V_S = 18 V V_{OUTx} = 3.6V V_{EN} = 5.5 V V_{EN} = 18 V 1) R_{EN} = 10 kΩ between VS and EN-pin

Electrical Characteristics Internal Supply / EN / PWMI pin (cont'd)

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40 °C to +150 °C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.3	Current consumption, device disabled via ST	$I_{S(dis,ST)}$	– – –	– – –	1.4 0.65 1.4	mA	[2] V_S = 18 V T_j < 105 °C V_{ST} = 5 V V_{EN} = 5.5 V V_{EN} = 18 V [1] R_{EN} = 10 kΩ between VS and EN-pin
6.3.4	Current consumption, device disabled via IN_SET	$I_{S(dis,IN\_SET)}$	– – –	– – –	1.4 0.7 1.4	mA	[2] V_S = 18 V T_j < 105 °C V_{IN_SET} = 5 V V_{EN} = 5.5 V V_{EN} = 18 V [1] R_{EN} = 10 kΩ between VS and EN-pin
6.3.5	Current consumption, device disabled via PWMI	$I_{S(dis,PWMI)}$	– – –	– – –	1.6 0.75 1.6	mA	[2] V_S = 18 V T_j < 105 °C V_{PWMI} = 3.4 V V_{EN} = 5.5 V V_{EN} = 18 V [1] R_{EN} = 10 kΩ between VS and EN-pin
6.3.6	Current consumption, active mode in single fault detection condition with ST-pin unconnected	$I_{S(fault,STu)}$	– – –	– – –	1.7 1.1 1.8	mA	[2] V_S = 18 V T_j < 105 °C R_{SET} = 12 kΩ V_{PWMI} = 0.5 V V_{OUTx} = 18 V V_{EN} = 5.5 V V_{EN} = 18 V [1] R_{EN} = 10 kΩ between VS and EN-pin
6.3.7	Current consumption, active mode in single fault detection condition with ST-pin connected to GND	$I_{S(fault,STG)}$	– – –	– – –	6.0 4.9 5.9	mA	[2] V_S = 18 V T_j < 105 °C R_{SET} = 12 kΩ V_{PWMI} = 0.5 V V_{OUTx} = 18 V V_{ST} = 0 V V_{EN} = 5.5 V V_{EN} = 18 V [1] R_{EN} = 10 kΩ between VS and EN-pin
6.3.8	Power-on reset delay time [3]	t_{POR}	–	–	25	µs	[1] V_S = V_{EN} = 0 → 13.5 V $V_{OUTx(nom)}$ = 3.6 ± 0.3V I_{OUTx} = 80% $I_{OUTx(nom)}$

Electrical Characteristics Internal Supply / EN / PWMI pin (cont'd)

Unless otherwise specified: V_S = 5.5 V to 40 V, T_j = -40 °C to +150 °C, R_{SET} = 12 kΩ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.9	Required supply voltage for output activation	$V_{S(on)}$	–	–	4	V	V_{EN} = 5.5 V V_{OUTx} = 3 V I_{OUTx} = 50% $I_{OUTx(nom)}$
6.3.10	Required supply voltage for current control	$V_{S(CC)}$	–	–	5.2	V	V_{EN} = 5.5 V V_{OUTx} = 3.6 V $I_{OUTx} \geq$ 90% $I_{OUTx(nom)}$
6.3.11	EN turn on threshold	$V_{EN(on)}$	–	–	2.5	V	–
6.3.12	EN turn off threshold	$V_{EN(off)}$	0.8	–	–	V	–
6.3.13	EN input current during low supply voltage	$I_{EN(LS)}$	–	–	1.8	mA	[1] V_S = 4.5 V T_j < 105 °C V_{EN} = 5.5 V
6.3.14	EN high input current	$I_{EN(H)}$	 – – – –	 – – – –	 0.1 0.1 1.65 0.45	mA	T_j < 105 °C V_S = 13.5 V, V_{EN} = 5.5 V V_S = 18 V, V_{EN} = 5.5 V V_S = V_{EN} = 18 V [1] V_S = 18 V, R_{EN} = 10 kΩ between VS and EN-pin
6.3.15	PWMI (active low) Switching low threshold (outputs on)	$V_{PWMI(L)}$	1.5	1.85	2.3	V	[1][4] V_S = 8...18 V
6.3.16	PWMI(active low) Switching high threshold (outputs off)	$V_{PWMI(H)}$	2.45	2.85	3.2	V	[1][4][5] V_S = 8...18 V
6.3.17	PWMI Switching threshold difference $V_{PWMI(H)}$ - $V_{PWMI(L)}$	ΔV_{PWMI}	0.75	1	1.10	V	[1][4][5] V_S = 8...18 V
6.3.18	PWMI (active low) Low input current with active channels (voltage < $V_{PWMI(L)}$)	$I_{PWMI(on)}$	I_{IN_SET} *3.1	I_{IN_SET} *4	I_{IN_SET} *4.9	µA	[1] T_j = 25...115 °C I_{IN_SET} = 100 µA V_{PWMI} = 1.7 V V_{EN} = 5.5 V V_S = 8...18 V
6.3.19	PWMI(active low) High input current	$I_{PWMI(off)}$	-5	–	5	µA	V_{PWMI} = 5 V V_{EN} = 5.5 V V_S = 8...18 V

1) Not subject to production test, specified by design
2) The total device current consumption is the sum of the currents I_S and $I_{EN(H)}$, please refer to **Pos. 6.3.14**
3) See also **Figure 4**
4) Parameter valid if an external PWM signal is applied
5) If TTL level compatibility is required, use µC open drain output with pull up resistor

7 IN_SET Pin

The IN_SET pin is a multiple function pin for output current definition, input and diagnostics:

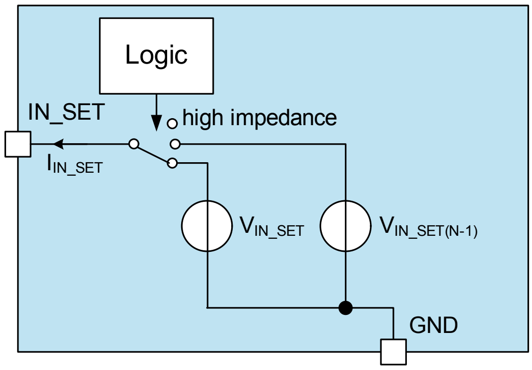

Figure 11 Block Diagram IN_SET pin

7.1 Output Current Adjustment via RSET

The output current for all three channels can only be adjusted simultaneously. The current adjustment can be done by placing a low power resistor (R_{SET}) at the IN_SET pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \tag{8}$$

The gain factor k (R_{SET} * output current) is specified in **Pos. 10.2.4** and **Pos. 10.2.5**. The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN\_SET(ref)}$, which is applied to the IN_SET during supplied device.

7.2 Smart Input Pin

The IN_SET pin can be connected via R_{SET} to the open-drain output of a µC or to an external NMOS transistor as described in **Figure 12**. This signal can be used to turn off the output stages of the IC. A minimum IN_SET current of $I_{IN\_SET(act)}$ is required to turn on the output stages. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN_SET pin, see **Figure 15** for details. In addition, the IN_SET pin offers the diagnostic feedback information, if the status pin is connected to GND. Another diagnostic possibility is shown in **Figure 13**, where the diagnosis information is provided via the ST pin (refer to **Chapter 8** and **Chapter 9**) to a micro controller. In case of a fault event with the ST pin connected to GND the IN_SET voltage is increased to $V_{IN\_SET(N-1)}$ **Pos. 9.3.2**. Therefore, the device has two voltage domains at the IN_SET-pin, which is shown in **Figure 16**.

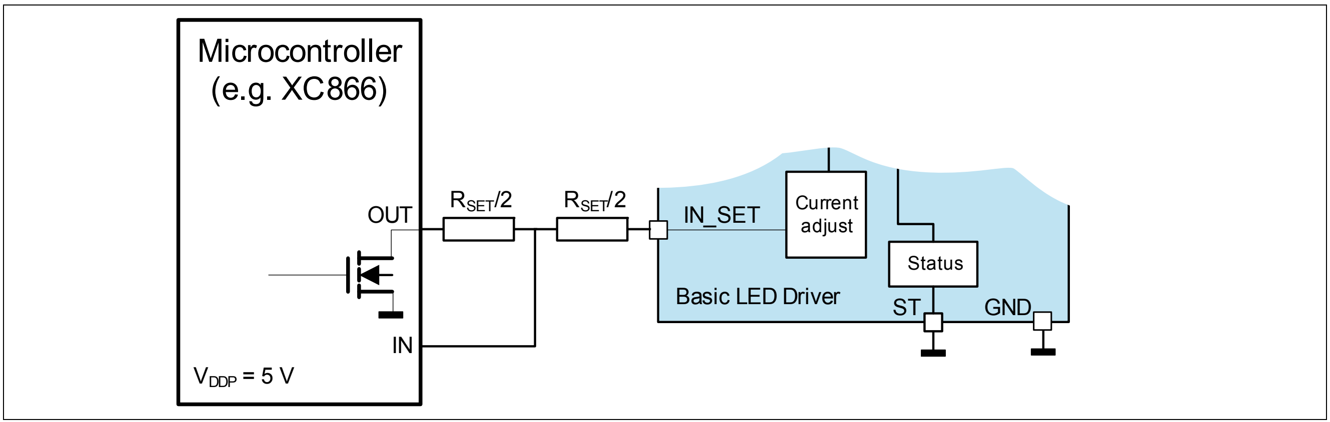

Figure 12 Schematics IN_SET interface to µC, diagnosis via IN_SET pin

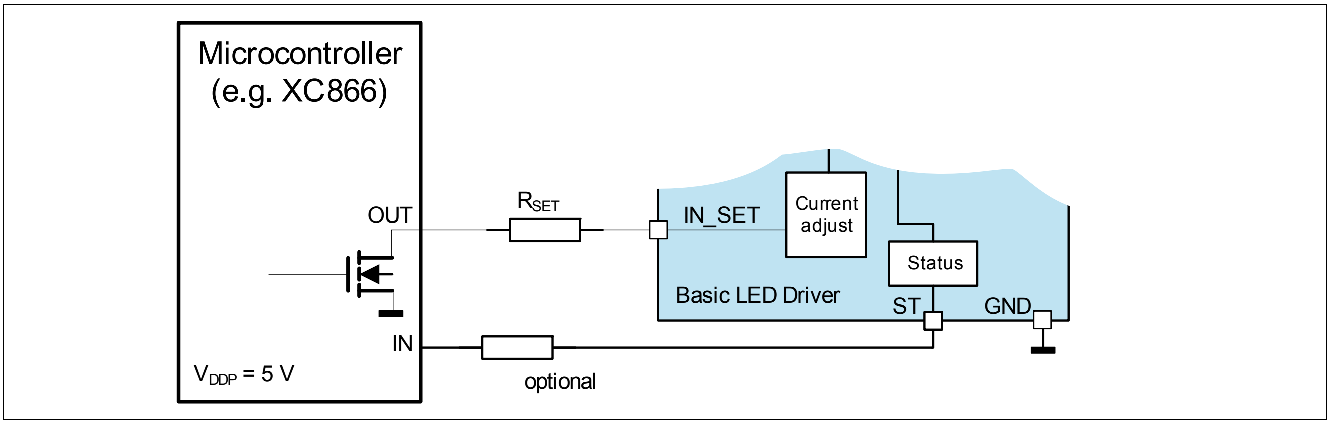

Figure 13 Schematics IN_SET interface to µC, diagnosis via ST pin

The resulting switching times are shown in **Figure 14**:

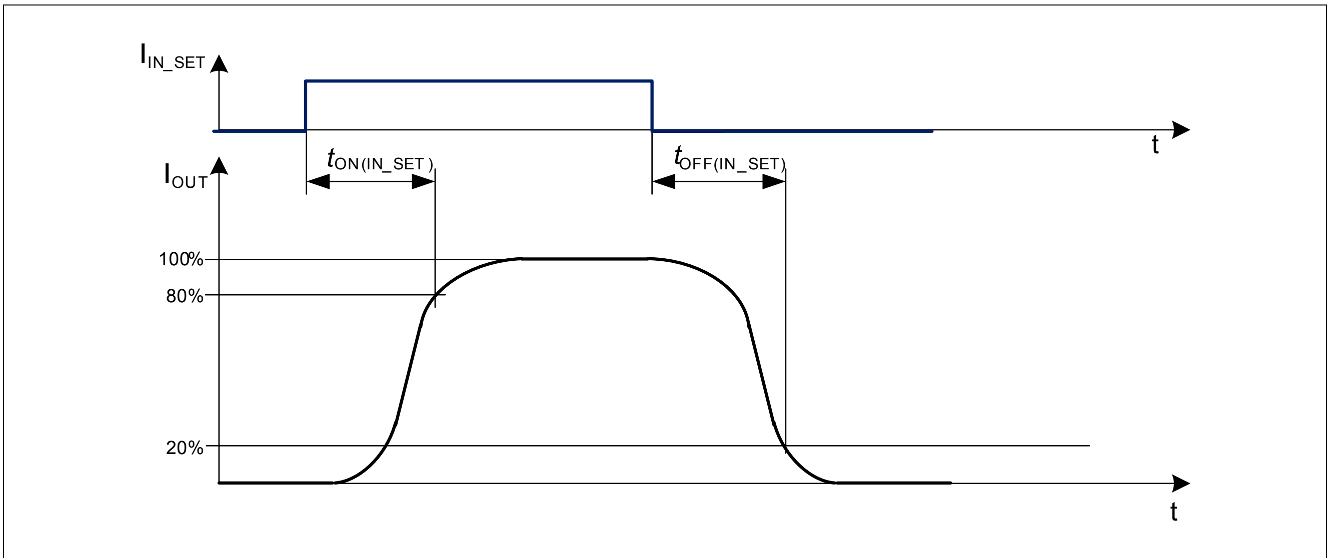

Figure 14 Switching times via IN_SET

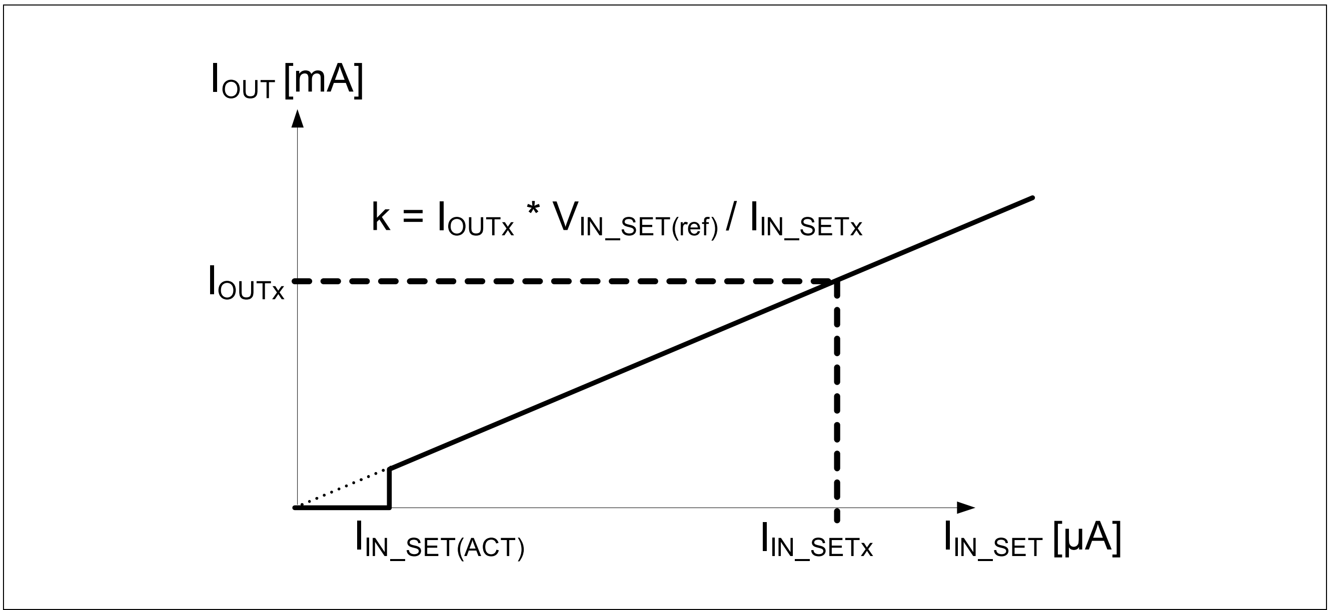

Figure 15 I_{OUT} **versus** I_{INSET}

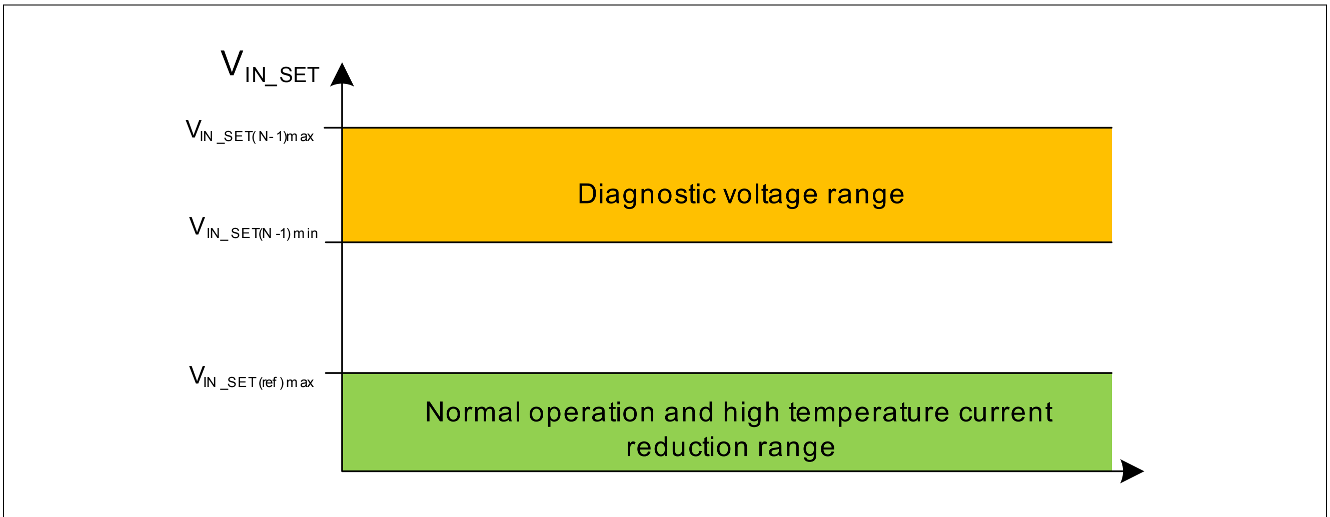

Figure 16 **Voltage domains for IN_SET pin, if ST pin is connected to GND**

8 ST Pin

The ST pin is a multiple function pin.

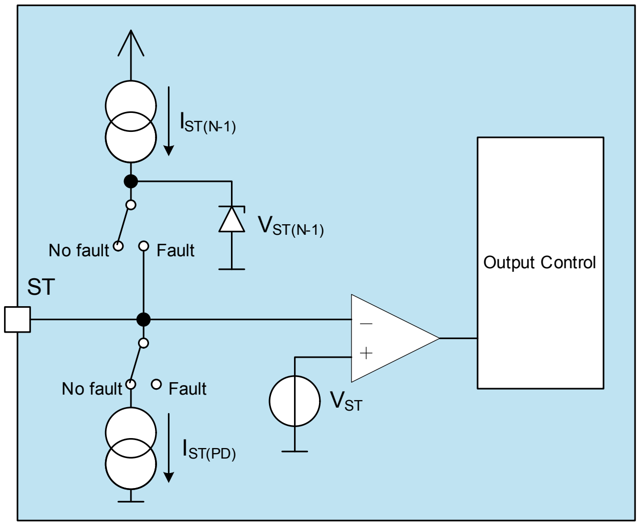

Figure 17 Block Diagram ST pin

8.1 Diagnosis Selector

If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), the ST pin acts as diagnosis output pin. In normal operation (device is activated) the ST pin is pulled to GND via the internal pull down current $I_{ST(PD)}$. In case of an open load condition the ST pin is switched to $V_{ST(N-1)}$ after the N-1 detection filter time.

If the device is operated in PWM operation via the VS and/or EN pins the ST pin should be connected to GND via a high ohmic resistor (e.g. 470kΩ) to ensure proper device behavior during fast rising VS and/or EN slopes.

If the ST pin is shorted to GND the diagnostic feedback is performed via the IN_SET-pin, which is shown in **Chapter 7.2** and **Chapter 9**.

8.2 Diagnosis Output

If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), it acts as a diagnostic output. In case of a fault condition the ST pin rises its voltage to $V_{ST(N-1)}$ (**Pos. 9.3.7**). Details are shown in **Chapter 9**.

8.3 Disable Input

If an external voltage higher than $V_{ST(H)}$ (**Pos. 9.3.5**) is applied to the ST pin, the device is switched off. This function is used for applications, where multiple drivers should be used for one light function. It is possible to combine the drivers' fault diagnosis via the ST pins. If a single LED chain fails, the entire light function is switched off. In this scenario e.g. the diagnostic circuit on the body control module can easily distinguish between the two cases (normal load or load fault), because nearly no current is flowing into the LED module during the fault scenario - the drivers consume a current of $I_{S(fault,STu)}$ (**Pos. 6.3.6**) or $I_{S(dis,ST)}$ (**Pos. 6.3.3**).

As soon as one LED chain fails, the ST-pin of this device is switched to $V_{ST(N-1)}$. The other devices used for the same light function can be connected together via the ST pins. This leads to a switch off of all devices connected together. Application examples are shown in **Chapter 11**.

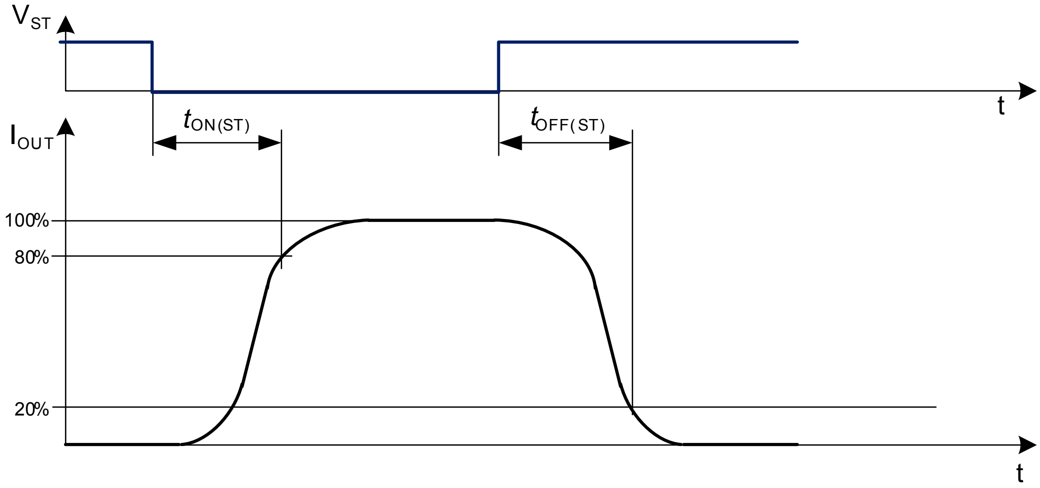

Figure 18 Switching times via ST Pin

9 Load Diagnosis

9.1 N-1 Detection

The N-1 diagnosis is specially designed to detect error conditions in LED arrays with multiple LED chains used for one light function. If one LED within one chain fails in open condition the respective LED chain is off. Different automotive applications require a complete deactivation of a light function, if the desired brightness of the function (LED array) can not be achieved due to an internal error condition. Such a deactivation feature is integrated in the LITIX^{TM} Basic IC.

The functionality of the N-1 pin is shown in the following block diagram:

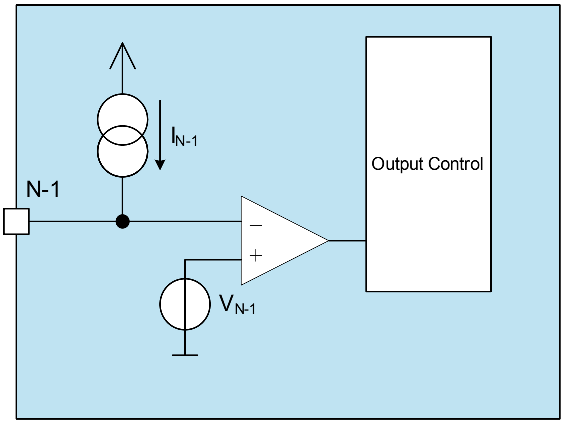

Figure 19 Block Diagram N-1 pin

In applications, where more than one LITIX^{TM} Basic IC is used, the devices can be connected via the ST pins as shown in **Figure 23**. This circuit can be used to disable all output stages (of all LITIX^{TM} Basic ICs) during an open load event on one channel. The outputs are deactivated after a N-1 filter time t_{N-1}, which is defined by the charging current I_{N-1} (**Pos. 9.3.10**). The time is adjustable with a capacitor connected to the N-1 pin according the following equation:

$$t_{typ} = \frac{C_{N-1} \cdot V_{N-1(th)}}{I_{N-1}} \qquad (9)$$

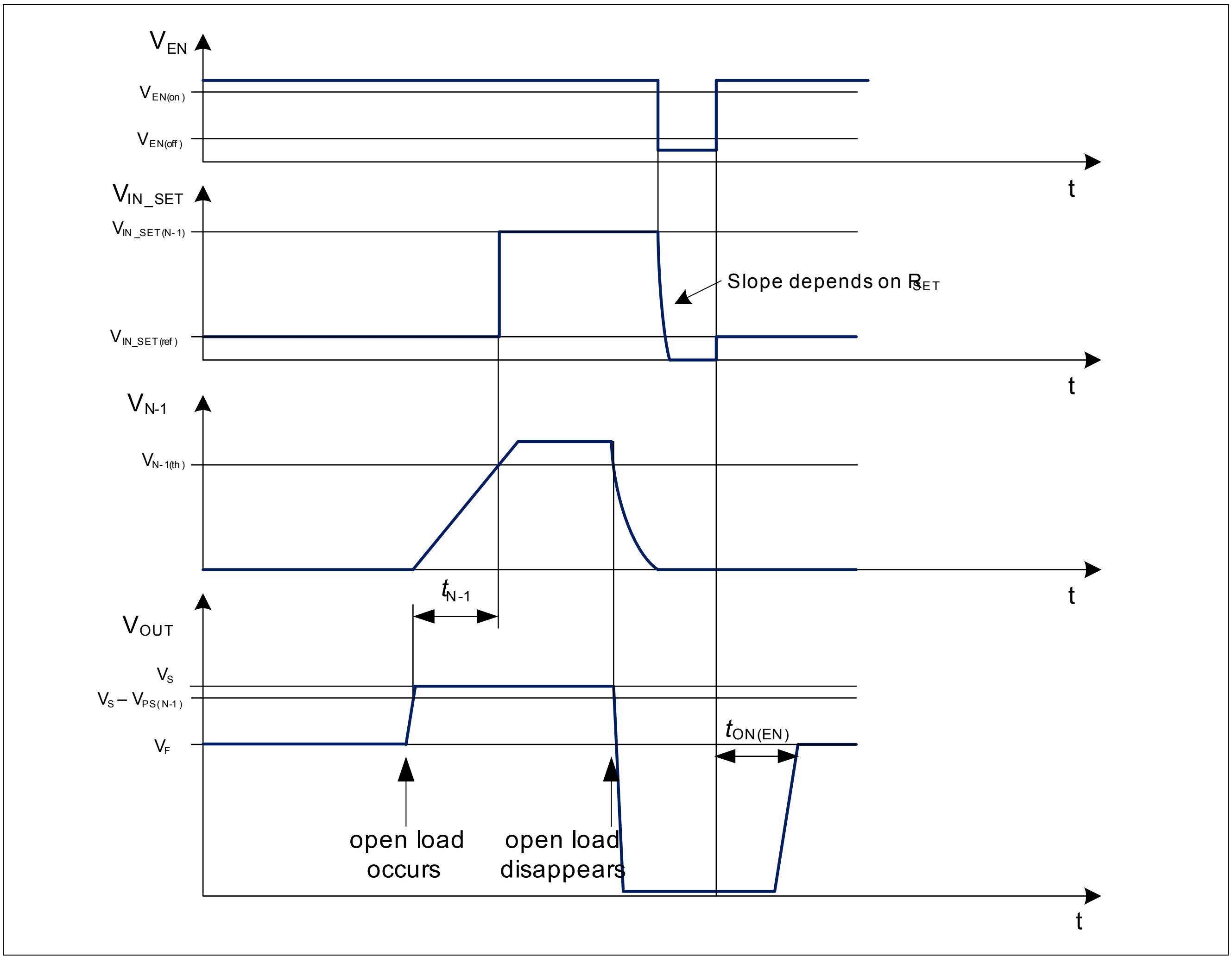

Figure 20 IN_SET behavior during open load condition with ST pin connected to GND

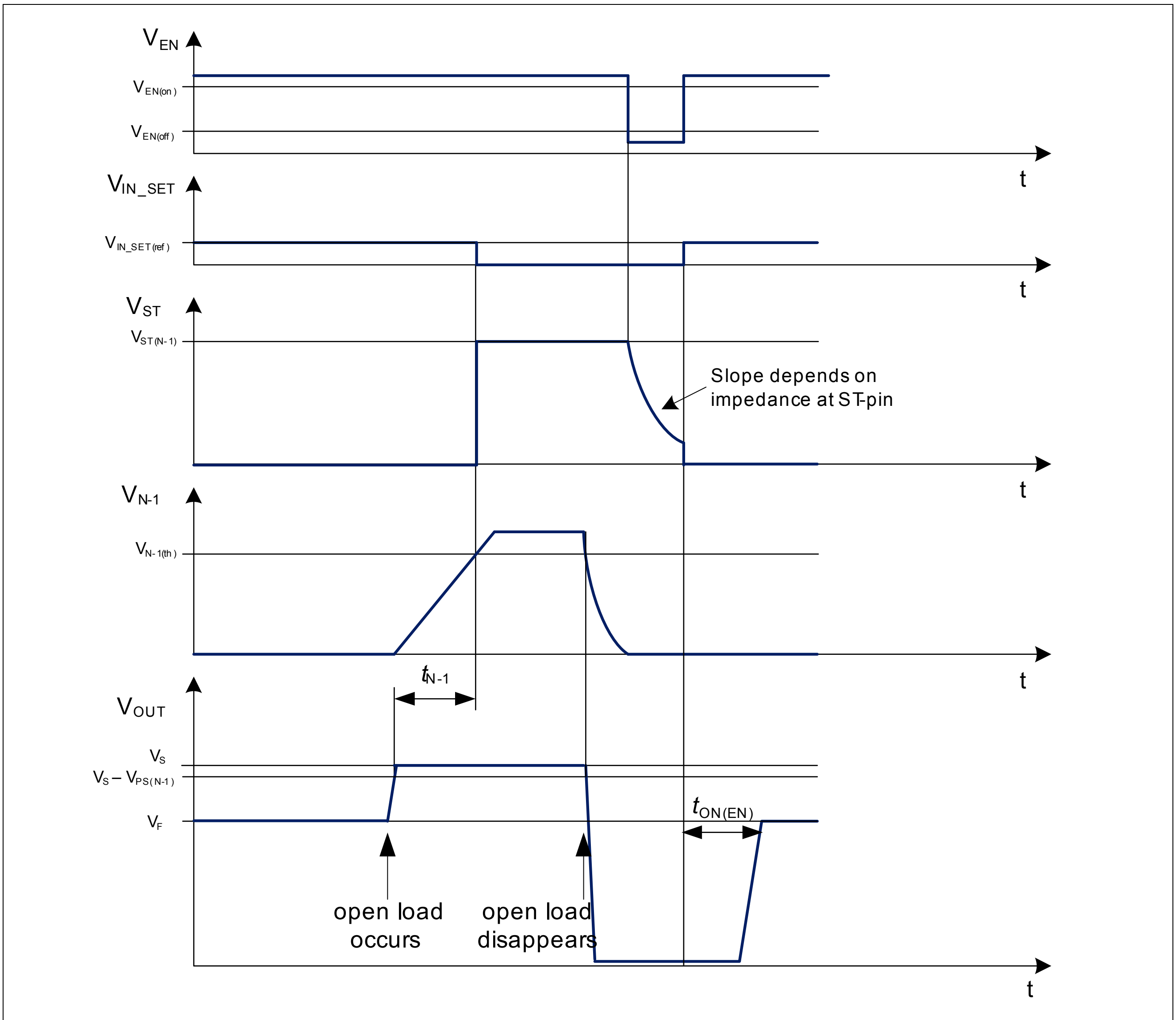

Figure 21 IN_SET and ST behavior during open load condition (ST unconnected)

The N-1 status is latched. The output stages can be re-enabled by a Low to High transition at the EN pin or by a Power on reset. To provide a Limp Home functionality (lower number of LEDs instead of complete deactivation) in the case of a partially damaged LED array, the N-1 filter time t_{N-1} can be used. If a PWM signal with an ON-time of less than t_{N-1} is applied to the VS and EN pins, the N-1 detection feature will not be activated.

If there is more than one device used for N-1 detection the maximum number of devices, which can be connected as shown in **Figure 23**, is limited to n_{N-1}. The maximum number of devices in N-1 configuration is calculated