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Infineon® LITIX™ Power

Multitopology LITIX™ Power DC/DC Controller IC

TLD5095EL

Infineon® LITIX™ Power

Multitopology LITIX™ Power DC/DC Controller IC

Data Sheet

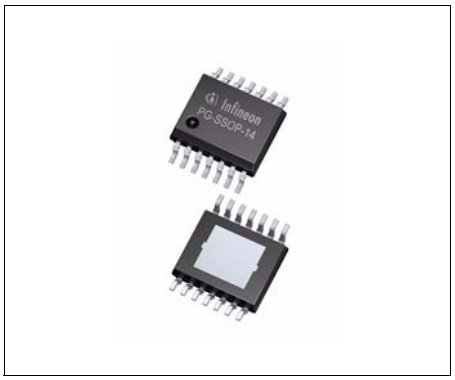
Revision 1.4

2015-03-11

Automotive Power

Table of Contents

1 Overview



PG-SSOP-14

- Wide Input Voltage Range from 4.75 V to 45 V
- Constant Current or Constant Voltage Regulation
- Drives LEDs in Boost, Buck, Buck-Boost, SEPIC and Flyback
- Topology
- Very Low Shutdown Current: IQ< 10 µA
- Flexible Switching Frequency Range, 100 kHz to 500 kHz
- Synchronization with external clock source
- Output Open Circuit Diagnostic Output
- PWM Dimming
- Internal Soft Start
- 300mV High Side Current Sense to ensure highest flexibility and LED current accuracy
- Internal 5 V Low Drop Out Voltage Regulator
- Wide LED current range via simple adaptation of external components
- Available in a small thermally enhanced PG-SSOP-14 package
- Output Overvoltage Protection
- Over Temperature Shutdown
- Automotive AEC Qualified
- Green Product (RoHS) Compliant

Description

The TLD5095EL is a smart multitopology LED controller with built in protection and diagnostic features. The main function of this device is to regulate a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and longer lifetime. The controller concept of the TLD5095EL allows a multi-purpose usage such as Boost, Buck, Buck-Boost, SEPIC and Flyback configuration with various load current levels by simply adjusting the external components. The TLD5095EL has a PWM output for dimming a LED load. The diagnostics are communicated on a status output (pin ST) to indicate a fault condition such as an LED open circuit. The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The TLD5095EL features an enable function reducing the shut-down current consumption to <10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft-start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides protection functions such as output overvoltage protection and overtemperature shutdown.

Application

- Automotive Exterior and Interior Lighting

Type	Package	Marking
TLD5095EL	PG-SSOP-14	TLD5095

2 Block Diagram

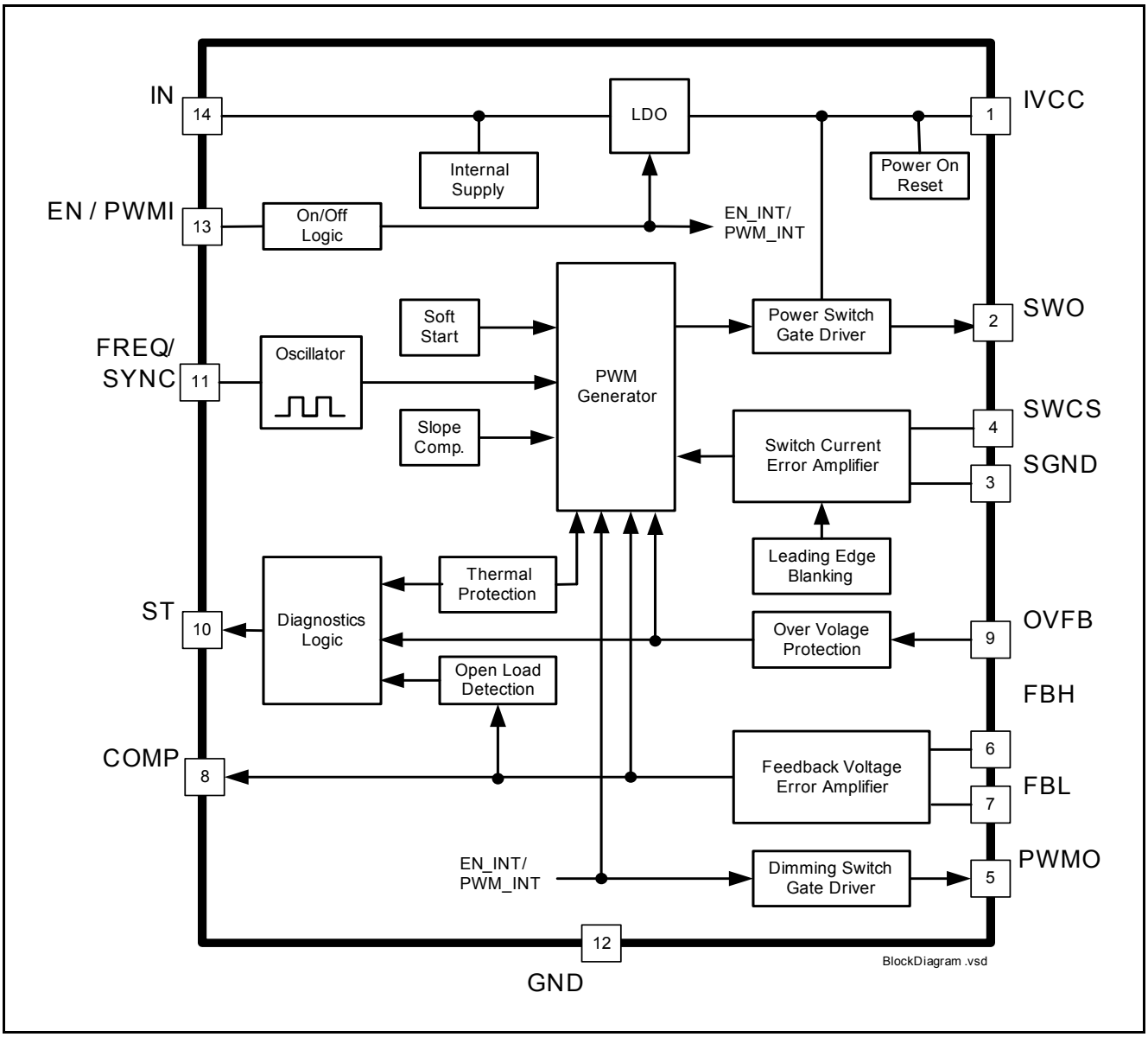


Figure 2-1 Block Diagram TLD5095EL

3 Pin Configuration

3.1 Pin Assignment

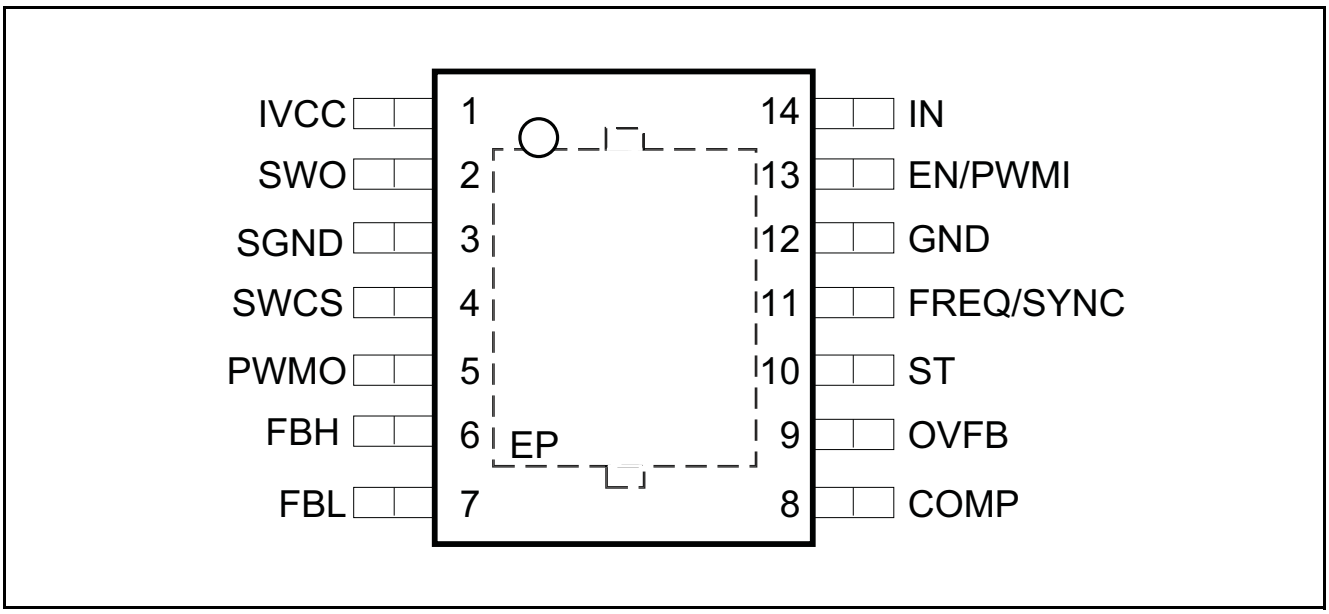


Figure 3-1 Pin Configuration TLD5095EL

3.2 Pin Definitions and Functions

Table 3-1 Pin Definition and Function

#	Symbol	Direction	Type	Function
1	IVCC			**Internal LDO Output;** Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not left open.
2	SWO			**Switch Output;** Connect to gate of external switching MOSFET
3	SGND			**Current Sense Ground;** Ground return for current sense switch
4	SWCS			**Current Sense Input;** Detects the peak current through switch
5	PWMO			**PWM Dimming Output;** Connect to gate of external MOSFET
6	FBH			**Voltage Feedback Positive;** Non inverting Input (+)
7	FBL			**Voltage Feedback Negative;** Inverting Input (-)

Table 3-1 Pin Definition and Function

#	Symbol	Direction	Type	Function
8	COMP			**Compensation Input;** Connect R and C network to pin for stability
9	OVFB			**Output Overvoltage Protection Feedback;** Connect to resistive voltage divider to set overvoltage threshold.
10	ST			**Status Output;** Open drain diagnostic output to indicate fault condition. Connect pull up resistor to pin.
11	FREQ / SYNC			**Frequency Select or Synchronization Input;** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range.
12	GND			**Ground;** Connect to system ground.
13	EN / PWMI			**Enable or PWM Input;** Apply logic high signal to enable device or PWM signal for dimming LED.
14	IN			**Supply Input;** Supply for internal biasing.
15	EP			**Exposed Pad;** Connect to external heat spreading Cu area with electrically GND (e.g. inner GND layer of multilayer PCB with thermal vias)

4 General Product Characteristics

4.1 Absolute Maximum Ratings

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Table 4-1 Absolute Maximum Ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
IN Supply Input	V_{IN}	-0.3		45	V		P_4.1.1
EN / PWMI Enable or PWM Input	V_{EN}	-40		45	V		P_4.1.2
FBH-FBL; Feedback Error Amplifier Differential	V_{FBH}-V_{FBL}	-5.5		5.5	V		P_4.1.3
FBH; Feedback Error Amplifier Positive Input	V_{FBH}	-0.3		45	V		P_4.1.4
FBL Feedback Error Amplifier Negative Input	V_{FBL}	-0.3		45	V		P_4.1.5
OVFB Over Voltage Feedback Input	V_{OVP}	-0.3		5.5	V		P_4.1.6
OVFB Over Voltage Feedback Input	V_{OVP}	-0.3		45	V	t < 10s	P_4.1.7
SWCS Switch Current Sense Input	V_{SWCS}	-0.3		5.5	V		P_4.1.8
SWCS Switch Current Sense Input	V_{SWCS}	-0.3		6.2	V	t < 10s	P_4.1.9
SWO Switch Gate Drive Output	V_{SWO}	-0.3		5.5	V		P_4.1.10
SWO Switch Gate Drive Output	V_{SWO}	-0.3		6.2	V	t < 10s	P_4.1.11
SGND Current Sense Switch GND	V_{SGND}	-0.3		0.3	V		P_4.1.12
COMP Compensation Input	V_{COMP}	-0.3		5.5	V		P_4.1.13
COMP Compensation Input	V_{COMP}	-0.3		6.2	V	t < 10s	P_4.1.14

Table 4-1 Absolute Maximum Ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
FREQ / SYNC; Frequency and Synchronization Input	$V_{FREQ / SYNC}$	-0.3		5.5	V		P_4.1.15
FREQ / SYNC; Frequency and Synchronization Input	$V_{FREQ / SYNC}$	-0.3		6.2	V	t < 10s	P_4.1.16
PWMO PWM Dimming Output	V_{PWMO}	-0.3		5.5	V		P_4.1.17
PWMO PWM Dimming Output	V_{PWMO}	-0.3		6.2	V	t < 10s	P_4.1.18
ST	V_{ST}	-0.3		45	V		P_4.1.19
Diagnostic Status Output	I_{ST}	-5		5	mA		P_4.1.20
IVCC Internal Linear Voltage Regulator Output	V_{IVCC}	-0.3		5.5	V		P_4.1.21
IVCC Internal Linear Voltage Regulator Output	V_{IVCC}	-0.3		6.2	V	t < 10s	P_4.1.22
Temperatures							
Junction Temperature	T_j	-40		150	°C		P_4.1.23
Storage Temperature	T_{stg}	-55		150	°C		P_4.1.24
ESD Susceptibility							
ESD Resistivity to GND	$V_{ESD,HBM}$	-2		2	kV	HBM[2)]	P_4.1.25
ESD Resistivity to GND	$V_{ESD,CDM}$	-500		500	V	CDM[3)]	P_4.1.26
ESD Resistivity Pin 1,7,8,14 (corner pins) to GND	$V_{ESD,CDM,C}$	-750		750	V	CDM[3)]	P_4.1.27

1) Not subject to production test, specified by design.
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5kW, 100pF)
3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 4-2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	V_{IN}	4.75		45	V	$V_{IVCC} > V_{IVCC,RTH,d}$	P_4.2.1
Feedback Voltage Input	$V_{FBH;} V_{FBL}$	4.5		45	V		P_4.2.2
Junction Temperature	T_j	-40		150	°C		P_4.2.3

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4-3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[1)2)]	R_{thJC}		10		K/W		P_4.3.1
Junction to Ambient[3)]	R_{thJA}		42		K/W	2s2p	P_4.3.2
Junction to Ambient	R_{thJA}		42		K/W	1s0p + 600mm^2	P_4.3.3
Junction to Ambient	R_{thJA}		42		K/W	1s0p + 300mm^2	P_4.3.4

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta=25°C is dissipating 1W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5mm board. The 2s2p board has 2 outer copper layers (2 x 70µm Cu) and 2 inner copper layers (2 x 35µm Cu), A thermal via (diameter = 0.3mm and 25µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta=25°C, IC is dissipating 1W

5 Regulator

5.1 Description

The TLD5095 regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller it provides a PWM signal to an internal gate driver which then outputs the same PWM signal to external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over 1 ms (typical) to minimize potential overvoltage at the output.

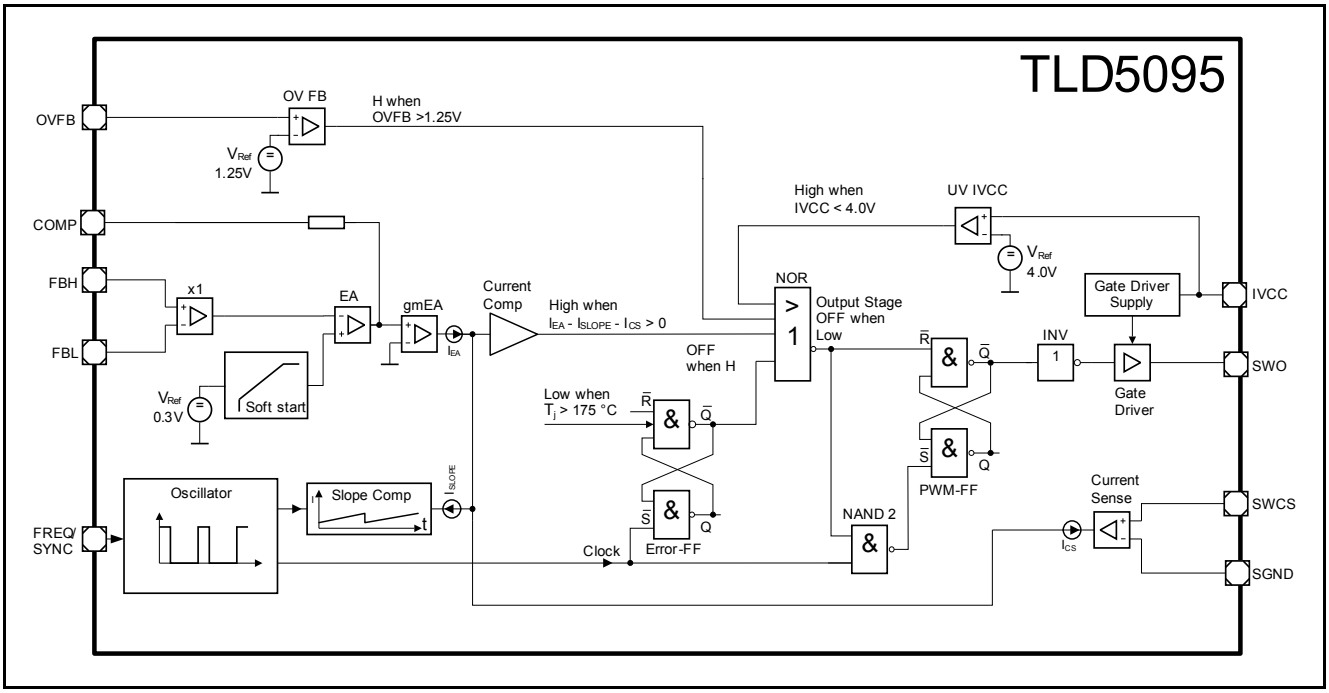


Figure 5-1 Block Diagram Buck Regulator

5.2 Electrical Characteristics

V_{IN} = 6 V to 40 V; 4.5V≤ VFBH ≤ 40V, 4.5V ≤ VFBL ≤ 40V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 5-1 Electrical Characteristics: Buck Regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator							
Feedback Reference Voltage	V_{REF}	0.28	0.30	0.32	V	V_{IN} = 19 V; V_{REF}= V_{FBH} -V_{FBL}	P_5.2.1
Voltage Line Regulation	ΔV_{REF} /ΔV_{IN}	–	–	0.15	%/V	V_{IN} = 6 to 19 V; V_{BO}= 30 V; I_{BO} = 500 mA **Figure 10-11**	P_5.2.2
Voltage Load Regulation	(ΔV_{REF}/ V_{REF}) /ΔI_{BO}	–	–	5	%/A	V_{IN} = 6 V; V_{BO} = 30V; I_{BO} = 100 to 500 mA **Figure 10-11**	P_5.2.3
Switch Peak Over Current Threshold	V_{SWCS}	130	150	170	mV	V_{IN} = 6 V V_{FBH} = V_{FBL} = 5 V V_{COMP} = 3.5V	P_5.2.4
Maximum Duty Cycle	$D_{MAX,fixed}$	90	93	95	%	Fixed frequency mode	P_5.2.5
Maximum Duty Cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode	P_5.2.6
Soft Start Ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.	P_5.2.7
Feedback Input Current	I_{FBx}	-10	-50	-100	µA	V_{FBH} - V_{FBL} = 0.3 V	P_5.2.8
Switch Current Sense Input Current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150 mV	P_5.2.9
Input Undervoltage Shutdown	$V_{IN,off}$	3.75	–	–	V	V_{IN} decreasing	P_5.2.10
Input Voltage Startup	$V_{IN,on}$	–	–	4.75	V	V_{IN} increasing	P_5.2.11
Gate Driver for External Switch							
Gate Driver Peak Sourcing Current[1)]	$I_{SWO,SRC}$	–	380	–	mA	V_{SWO} = 3.5V	P_5.2.12
Gate Driver Peak Sinking Current	$I_{SWO,SNK}$	–	550	–	mA	V_{SWO} = 1.5V	P_5.2.13
Gate Driver Output Rise Time	$t_{R,SWO}$	–	30	60	ns	$C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V	P_5.2.14

Table 5-1 Electrical Characteristics: Buck Regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Gate Driver Output Fall Time	$t_{F,SWO}$	–	20	40	ns	$C_{L,SWO}$ = 3.3nF; V_{SWO} = 1V to 4V	P_5.2.15
Gate Driver Output Voltage	V_{SWO}	4.5	–	5.5	V	$C_{L,SWO}$ = 3.3nF	P_5.2.16

1) Not subject to production test, specified by design

6 Oscillator and Synchronisation

Description

R_OSC vs. switching frequency

The internal oscillator is used to determine the switching frequency of the multitopology regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

(6.1)

$$R_{FREQ} = \frac{1}{(141 \cdot 10^{-12}\left[\frac{s}{\Omega}\right]) \cdot \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - (3.5 \cdot 10^{3}\,[\Omega])\,[\Omega]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the multitopology regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

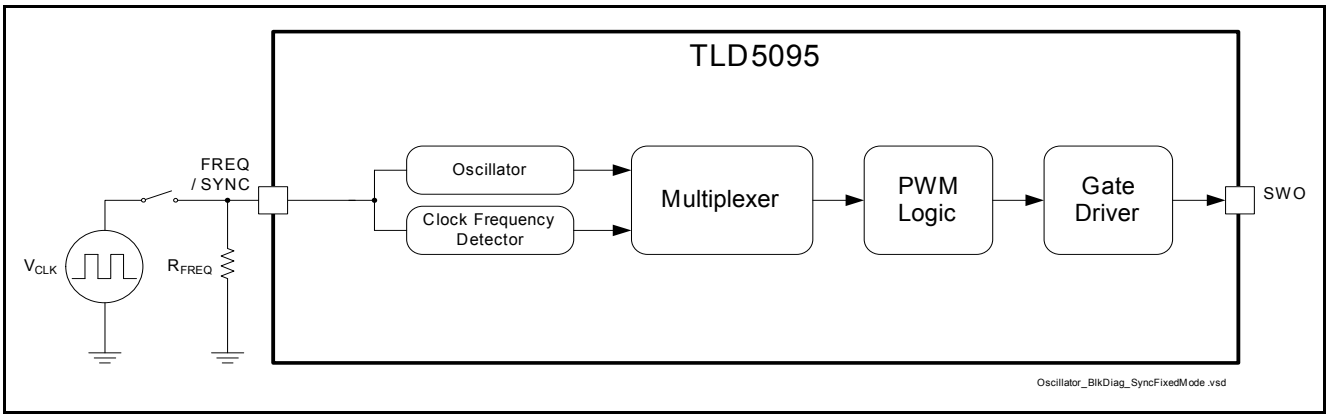


Figure 6-1 Oscillator and Synchronization Block Diagram and Simplified Application Circuit

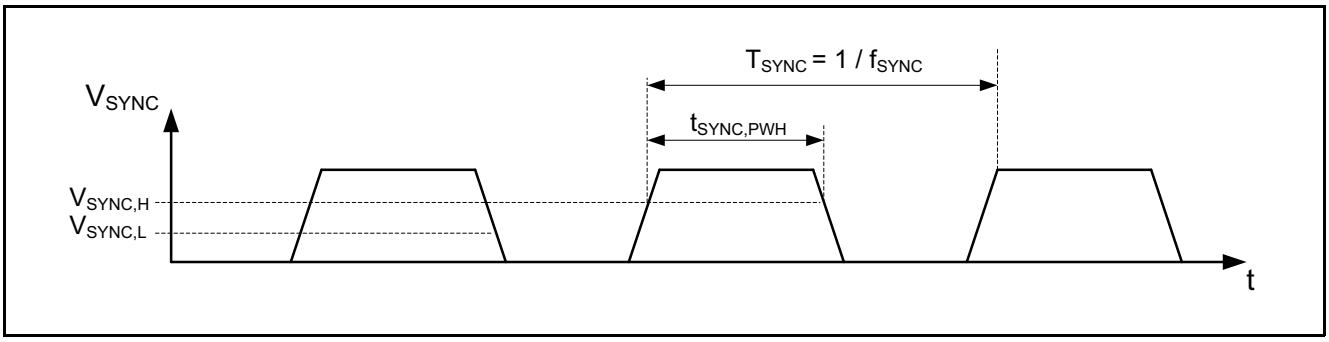


Figure 6-2 Synchronization Timing Diagram

6.1 Electrical Characteristics Oscillator

V_{IN} = 6 V to 40 V; 4.5V ≤ VFBH ≤ 40V, 4.5V ≤ VFBL ≤ 40V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 6-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Oscillator							
Oscillator Frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20kΩ	P_6.1.1
Oscillator Frequency Adjustment Range	f_{FREQ}	100	–	500	kHz	17% internal tolerance + external resistor tolerance	P_6.1.2
FREQ / SYNC Supply Current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0 V	P_6.1.3
Frequency Voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100 kHz	P_6.1.4
Synchronisation							
Synchronization Frequency Capture Range	f_{SYNC}	250	–	500	kHz		P_6.1.5
Synchronization Signal High Logic Level Valid	$V_{SYNC,H}$	3.0	–	–	V	1)	P_6.1.6
Synchronization Signal Low Logic Level Valid	$V_{SYNC,L}$	–	–	0.8	V	1)	P_6.1.7
Synchronization Signal Logic High Pulse Width	$t_{SYNC,PWH}$	200	–	–	ns	1)	P_6.1.8

1) Synchronization of external PWM ON signal to falling edge

6.2 Typical Performance Characteristics of Oscillator

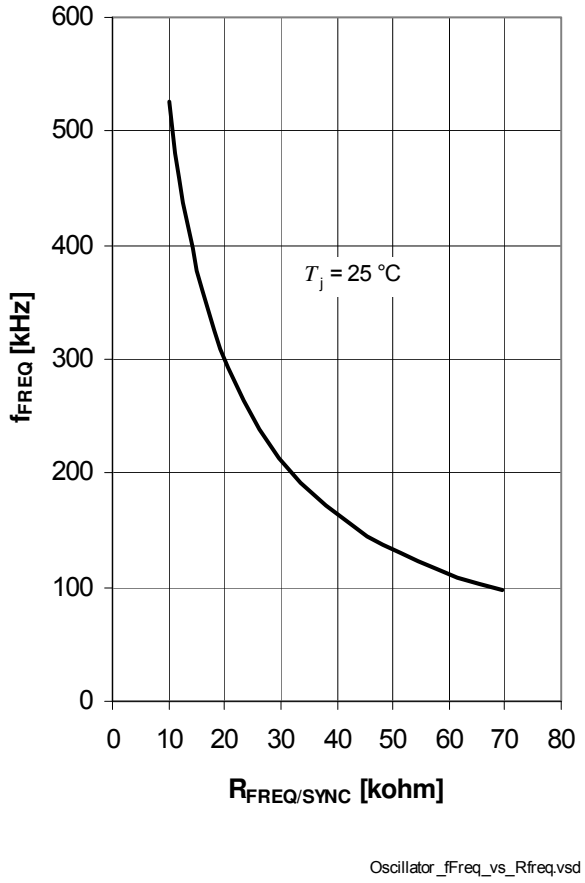


Figure 6-3 Switching Frequency f_{SW} versus Frequency Select Resistor to GND $R_{FREQ/SYNC}$

7 Enable and Dimming Function

Description

The enable function powers on or off the device. A valid logic low signal on enable pin EN/PWMI powers off the device and current consumption is less than 10 µA. A valid logic high enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is off in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to an internal gate driver. The internal gate driver outputs the same PWM signal on the PWMO pin to an external n-channel enhancement mode MOSFET for PWM dimming an LED load. PWM dimming an LED is a commonly practiced dimming method to prevent color shift in an LED light source. Moreover the PWM output function may also be used for to drive other types of loads besides LED.

The enable and PWM input function share the same pin. Therefore a valid logic low signal at the EN/PWMI pin needs to differentiate between an enable power off signal or an PWM low signal. The device differentiates between an enable off command and PWM dimming signal by requiring the signal at the EN/PWMI pin to stay low for a minimum of 8 ms.

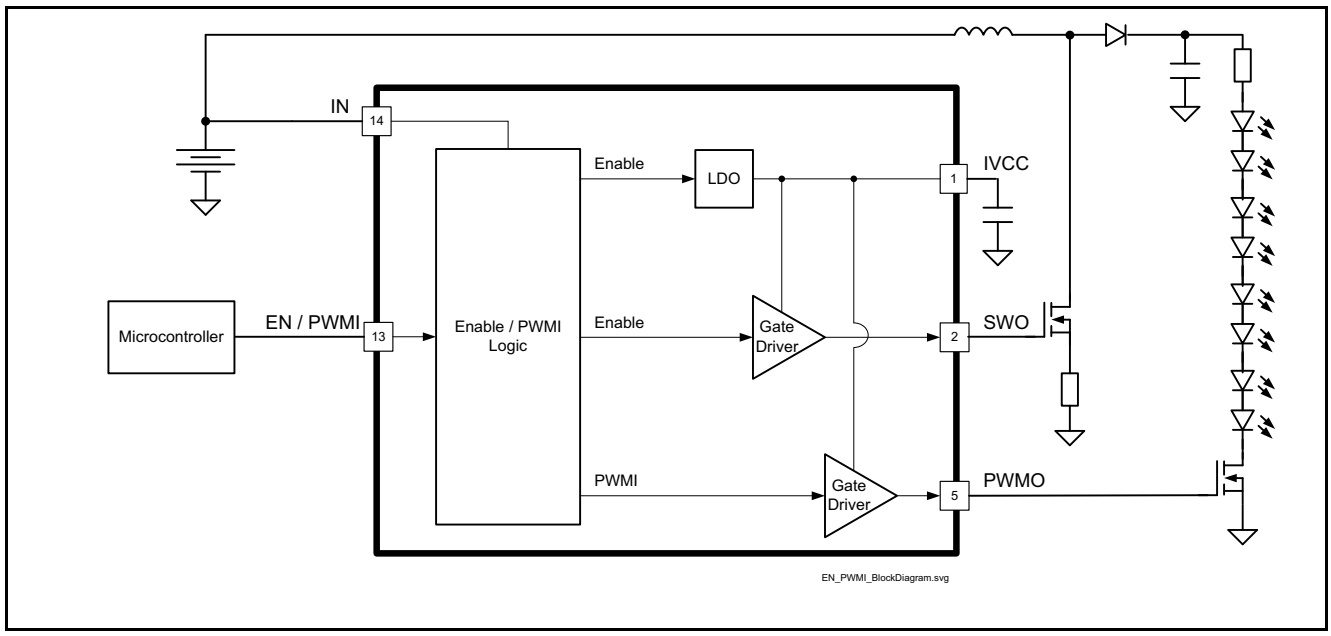


Figure 7-1 Block Diagram and Simplified Application Circuit Enable and LED Dimming

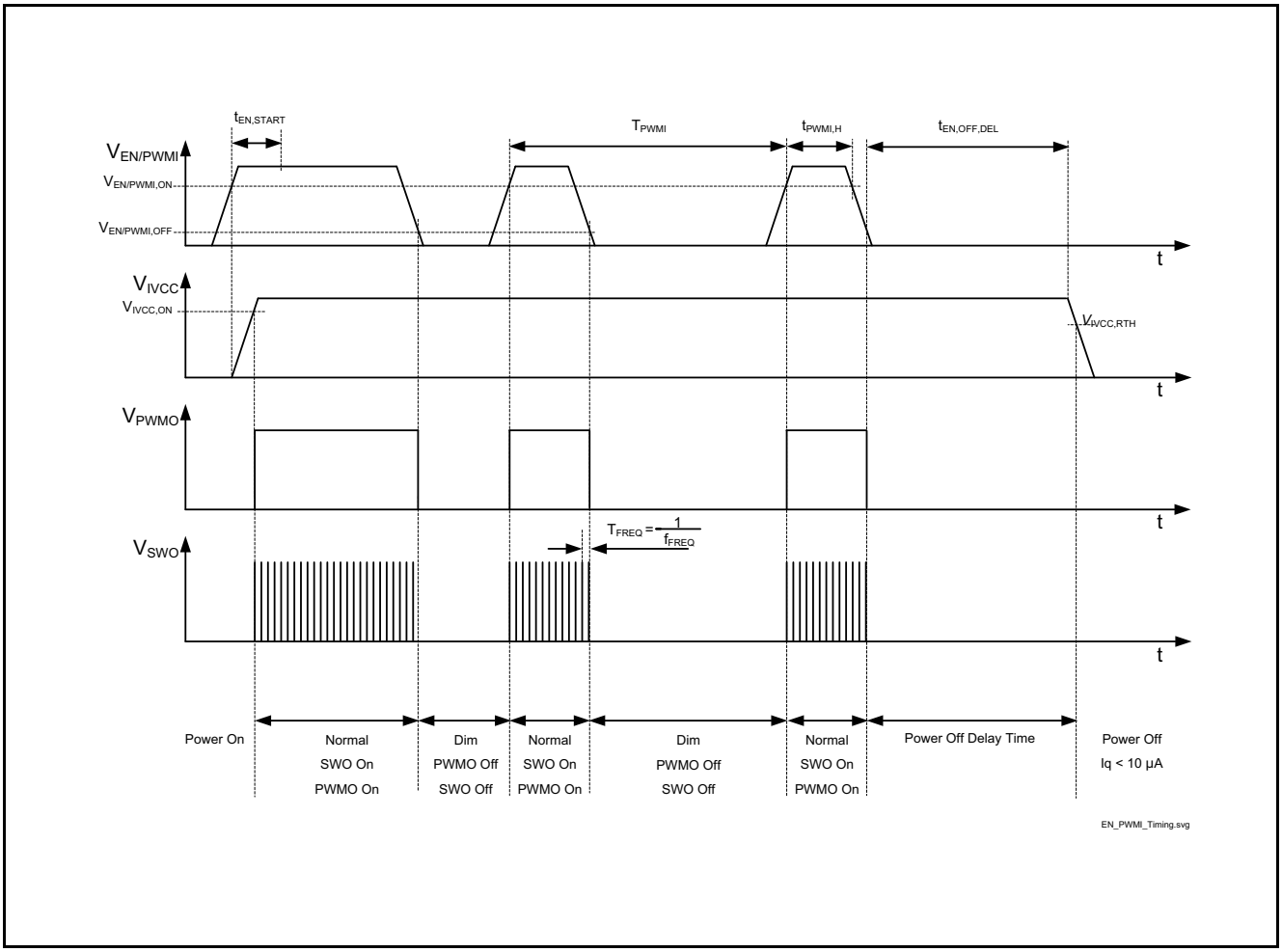


Figure 7-2 Timing Diagram Enable and LED Dimming

7.1 Electrical Characteristics

V_{IN} = 6 V to 40 V, T_j = -40°C to +150°C, all voltages with respect to ground (unless otherwise specified)

Table 7-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable / PWM Input							
Enable/PWMI Turn On Threshold	$V_{EN/PWMI,ON}$	3.0	–		V		P_7.1.1
Enable/PWMI Turn Off Threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V		P_7.1.2
Enable/PWMI Hysteresis	$V_{EN/PWMI,HYS}$	50	200	400	mV		P_7.1.3
Enable/PWMI High Input Current	$I_{EN/PWMI,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0 V	P_7.1.4

Enable and Dimming Function

Table 7-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable/PWMI Low Input Current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5 V	P_7.1.5
Enable Turn Off Delay Time	$t_{EN,OFF,DEL}$	8	10	12	ms		P_7.1.6
PWMI Min Duty Time	$t_{PWMI,H}$	4	–	–	µs		P_7.1.7
Enable Startup Time	$t_{EN,START}$	100	–	–	µs		P_7.1.8
Gate Driver for Dimming Switch							
PWMO Gate Driver Peak Sourcing Current[1)]	IPWMO,SRC	–	230	–	mA	V_{PWMO} = 3.5V	P_7.1.9
PWMO Gate Driver Peak Sinking Current	IPWMO,SNK	–	370	–	mA	V_{PWMO} = 1.5V	P_7.1.10
PWMO Gate Driver Output Rise Time	tR,PWMO	–	50	100	ns	$C_{L,PWMO}$ = 3.3nF; V_{PWMO} = 1V to 4V	P_7.1.11
PWMO Gate Driver Output Fall Time	tF,PWMO	–	30	60	ns	$C_{L,PWMO}$ = 3.3nF; V_{PWMO} = 1V to 4V	P_7.1.12
PWMO Gate Driver Output Voltage	VPWMO	4.5	–	5.5	V	$C_{L,PWMO}$ = 3.3nF	P_7.1.13
Current Consumption							
Current Consumption, Shutdown Mode	I_{q_off}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; $T_j \leq$ 105C; V_{IN} = 16V	P_7.1.14
Current Consumption, Active Mode[2)]	I_{q_on}	–	–	7	mA	$V_{EN/PWMI} \geq$ 4.75 V; I_{BO} = 0 mA; V_{IN} = 16V V_{SWO} = 0% Duty	P_7.1.15

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of external switches.

8 Linear Regulator

Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to ILIM,min (parameter 8.2.2). An external output capacitor with ESR lower than RIVCC,ESR (parameter 8.2.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated Undervoltage Protection for the External Switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC undervoltage reset switch OFF threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

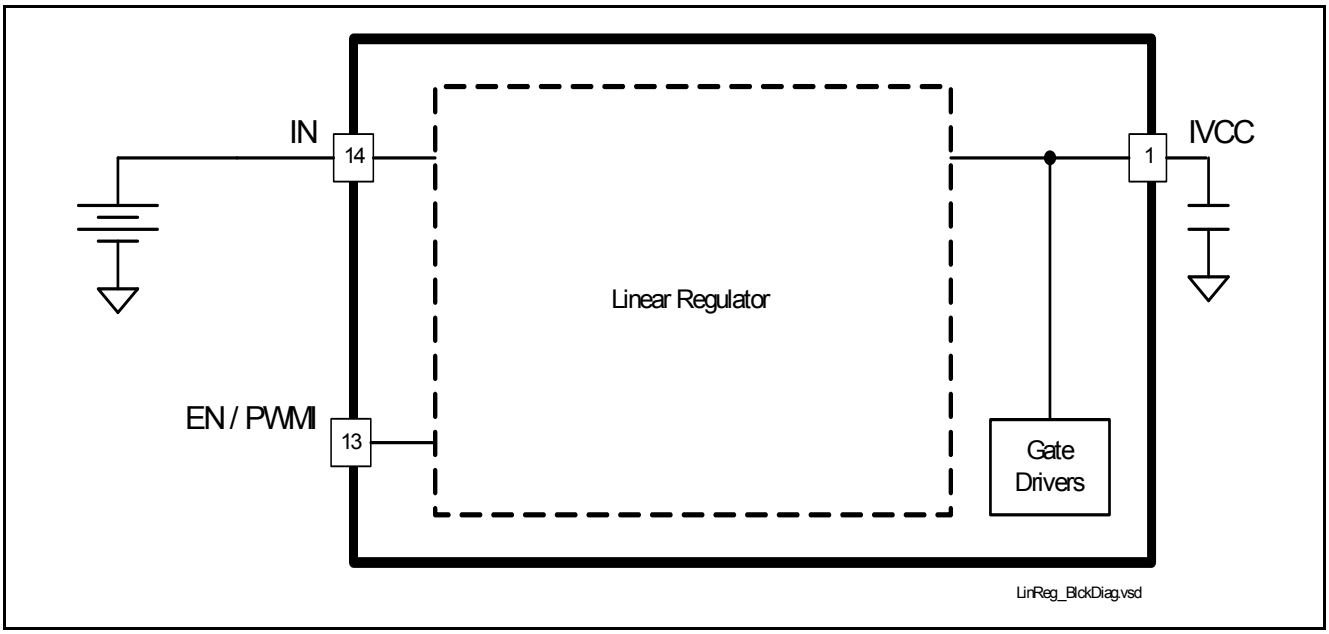


Figure 8-1 Voltage Regulator Block Diagram and Simplified Application Circuit

8.1 Electrical Characteristics

V_{IN} = 6 V to 40 V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 8-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage	V_{IVCC}	4.6	5	5.4	V	6 V ≤ V_{IN} ≤ 45 V 0.1 mA ≤ I_{IVCC} ≤ 35 mA	P_8.1.1
Output Current Limitation	I_{LIM}	51		90	mA	V_{IN} = 13.5 V V_{IVCC} = 4.5V	P_8.1.2
Drop out Voltage	V_{DR}			1.4	V	I_{IVCC} = 50mA [1]	P_8.1.3
Output Capacitor	C_{IVCC}	0.47		–	µF	[2]	P_8.1.4
Output Capacitor ESR	$R_{IVCC,ESR}$			0.5	W	f = 10kHz	P_8.1.5
Undervoltage Reset Headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$	P_8.1.6
Undervoltage Reset Threshold	$V_{IVCC,RTH,d}$	4.0	–	–	V	V_{IVCC} decreasing	P_8.1.7
Undervoltage Reset Threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing	P_8.1.8

1) Measured when the output voltage V_{CC} has dropped 100 mV from its nominal value.

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

9 Protection and Diagnostic Functions

9.1 Description

The TLD5095EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case any of the four fault conditions occur the Status output ST will output an active logic low signal to communicate that a fault has occurred. During an overvoltage or open load condition the gate driver outputs SWO and PWMO will turn off. **Figure 9-3** illustrates the various open load and open feedback conditions. In the event of an overtemperature condition (**Figure 9-6**) the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C. After cooling down the IC will automatically restart operation. Thermal shutdown is an integrated protection function designed to prevent immediate IC destruction and is not intended for continuous use in normal operation.

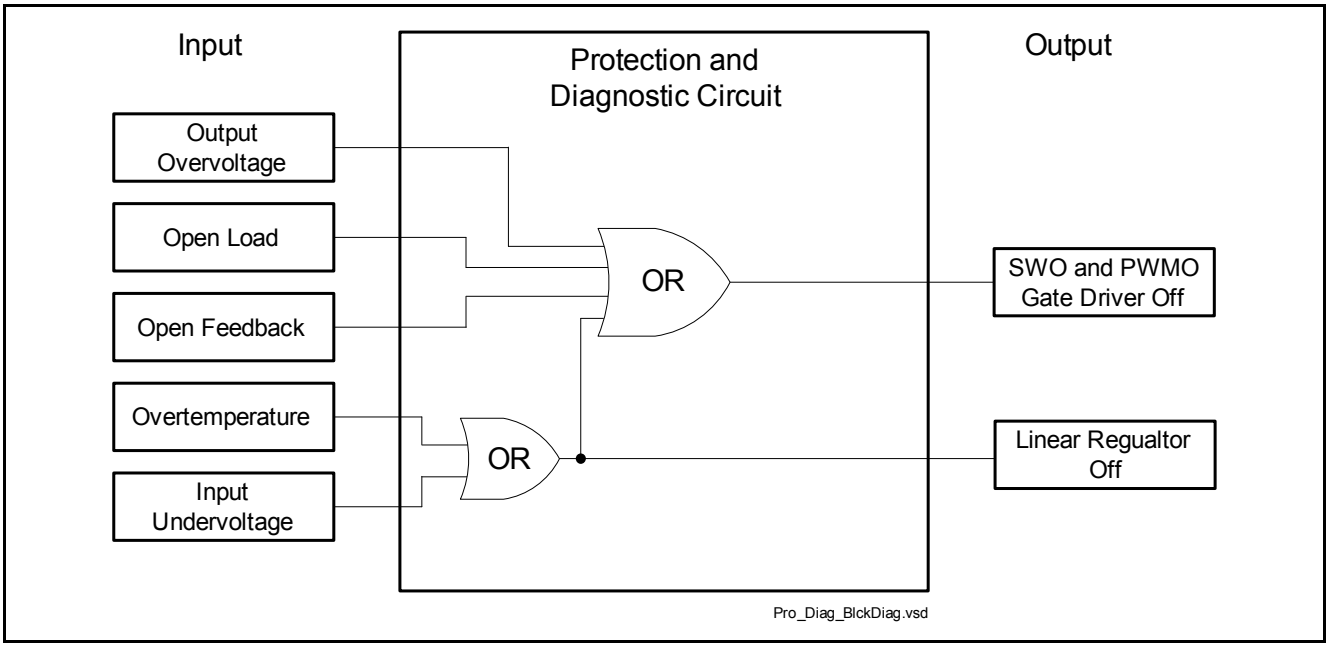


Figure 9-1 Protection and Diagnostic Function Block Diagram

Input		Output			
Condition	Level*	ST	SWO	PWMO	IVCC
Overvoltage	False	H	Sw*	H or Sw*	Active
	True	L	L	L	Active
Open Load	False	H	Sw*	H or Sw*	Active
	True	L	L	L	Active
Open Feedback	False	H	Sw*	H or Sw*	Active
	True	L	L	L	Active
Overtemperature	False	H	Sw*	H or Sw*	Active
	True	L	L	L	Shutdown

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*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist

Figure 9-2 Status Output Truth Table

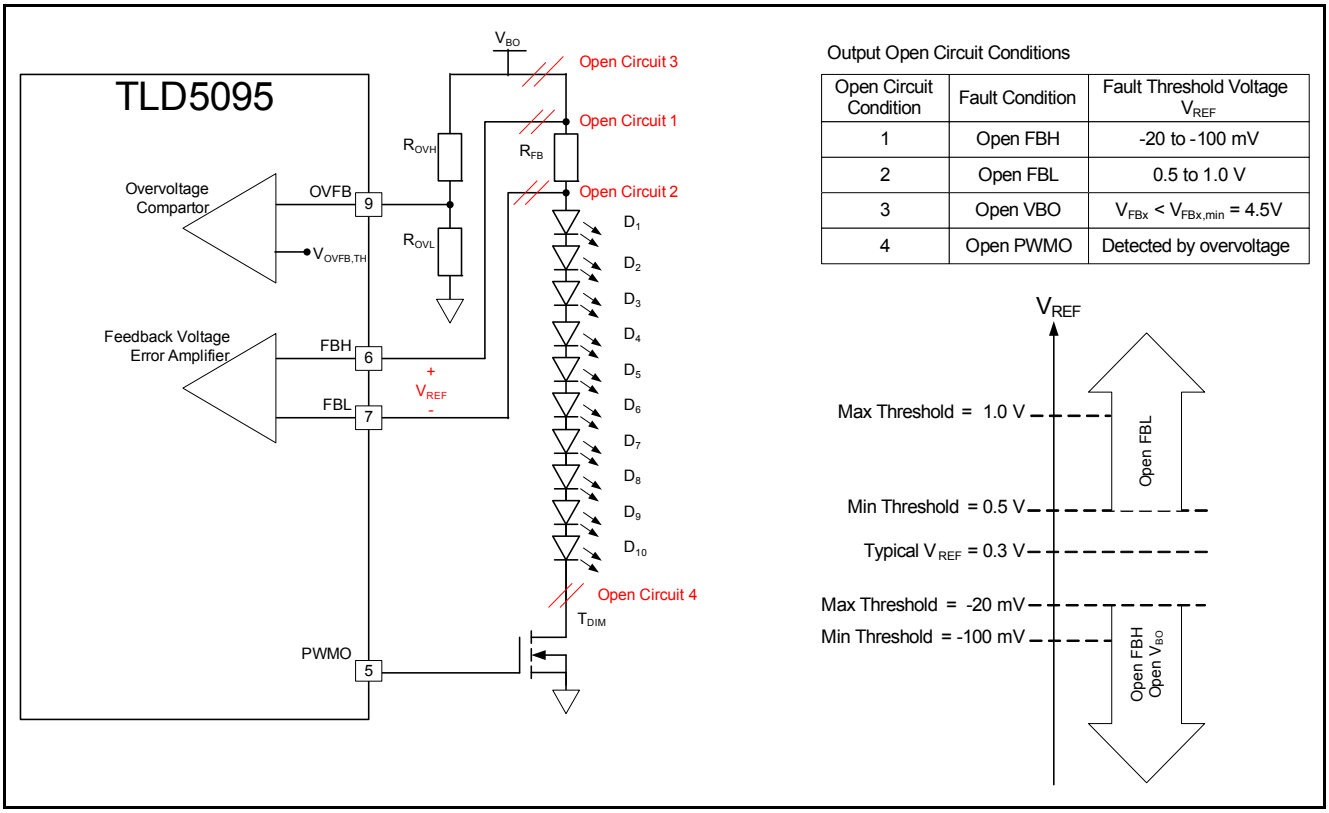

Figure 9-3 Open Load and Open Feedback Conditions

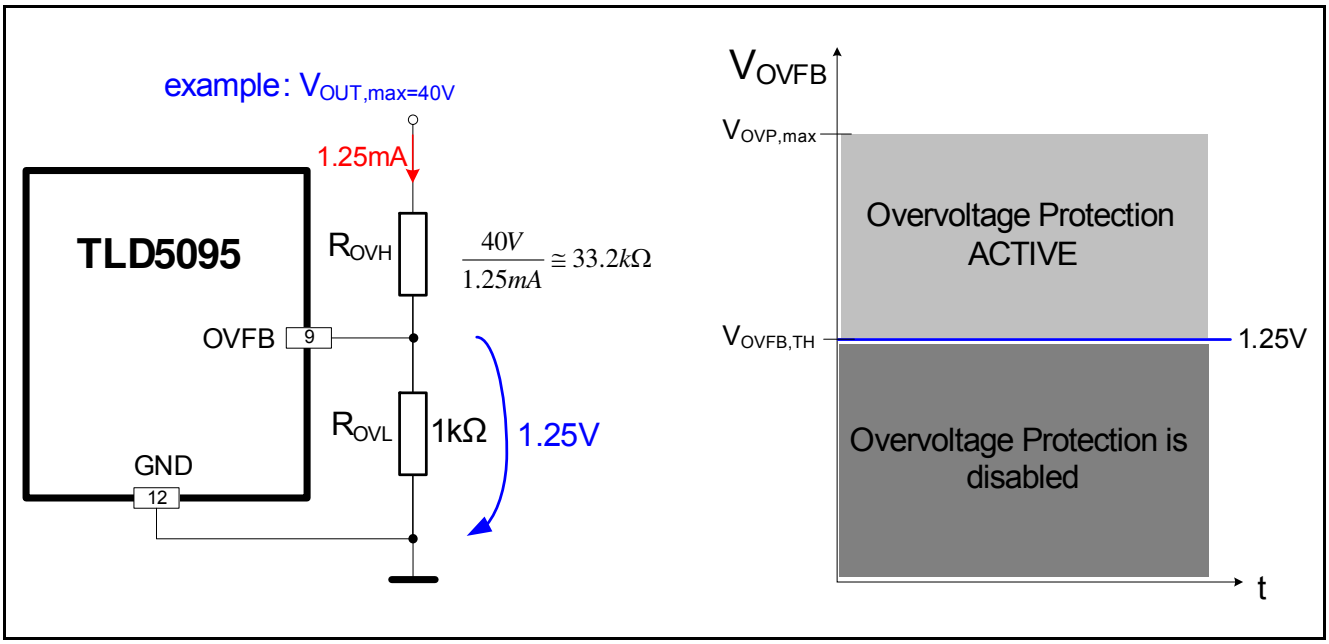

Figure 9-4 Overvoltage Protection Description

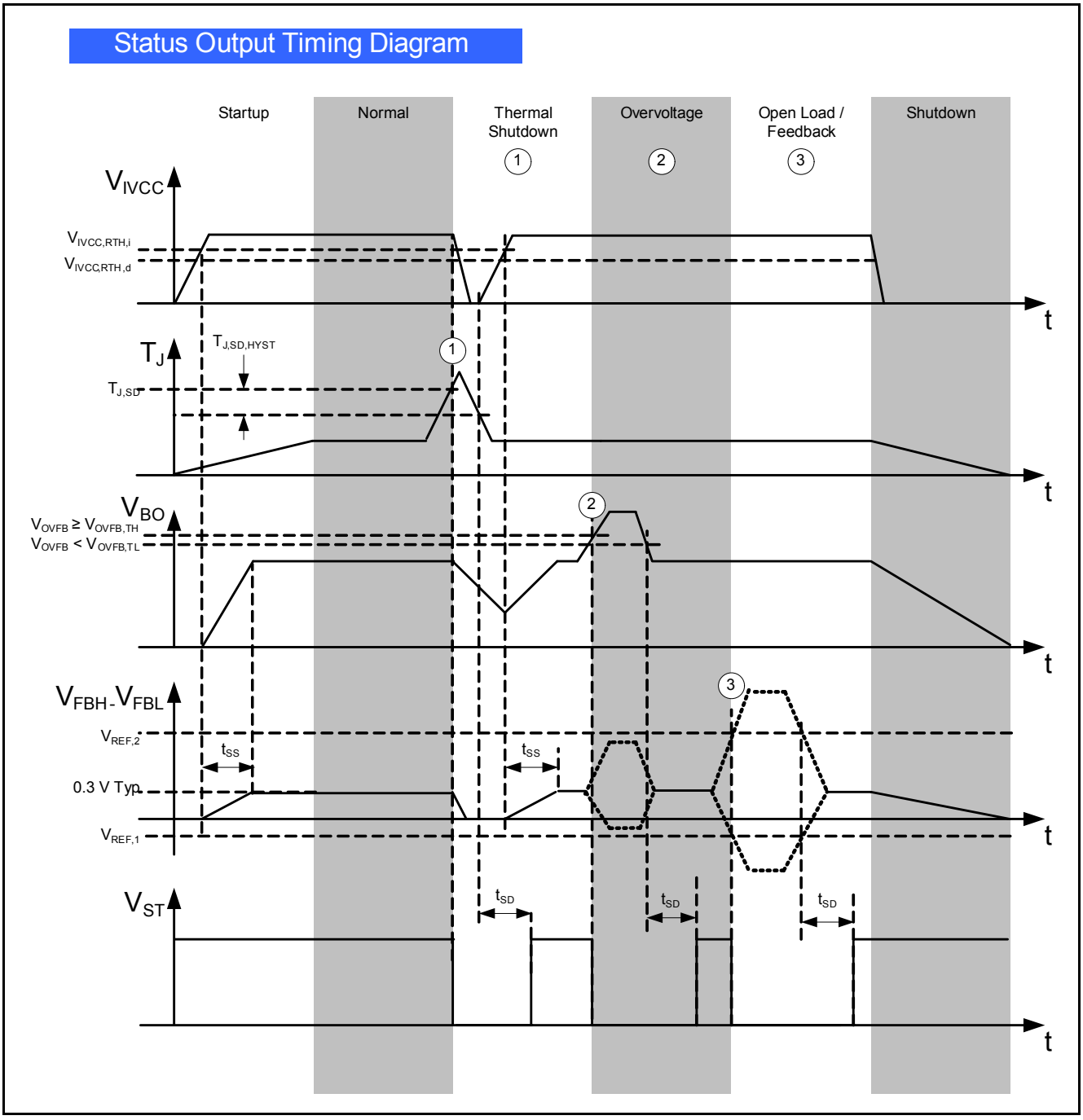

Figure 9-5 Status Output Timing Diagram

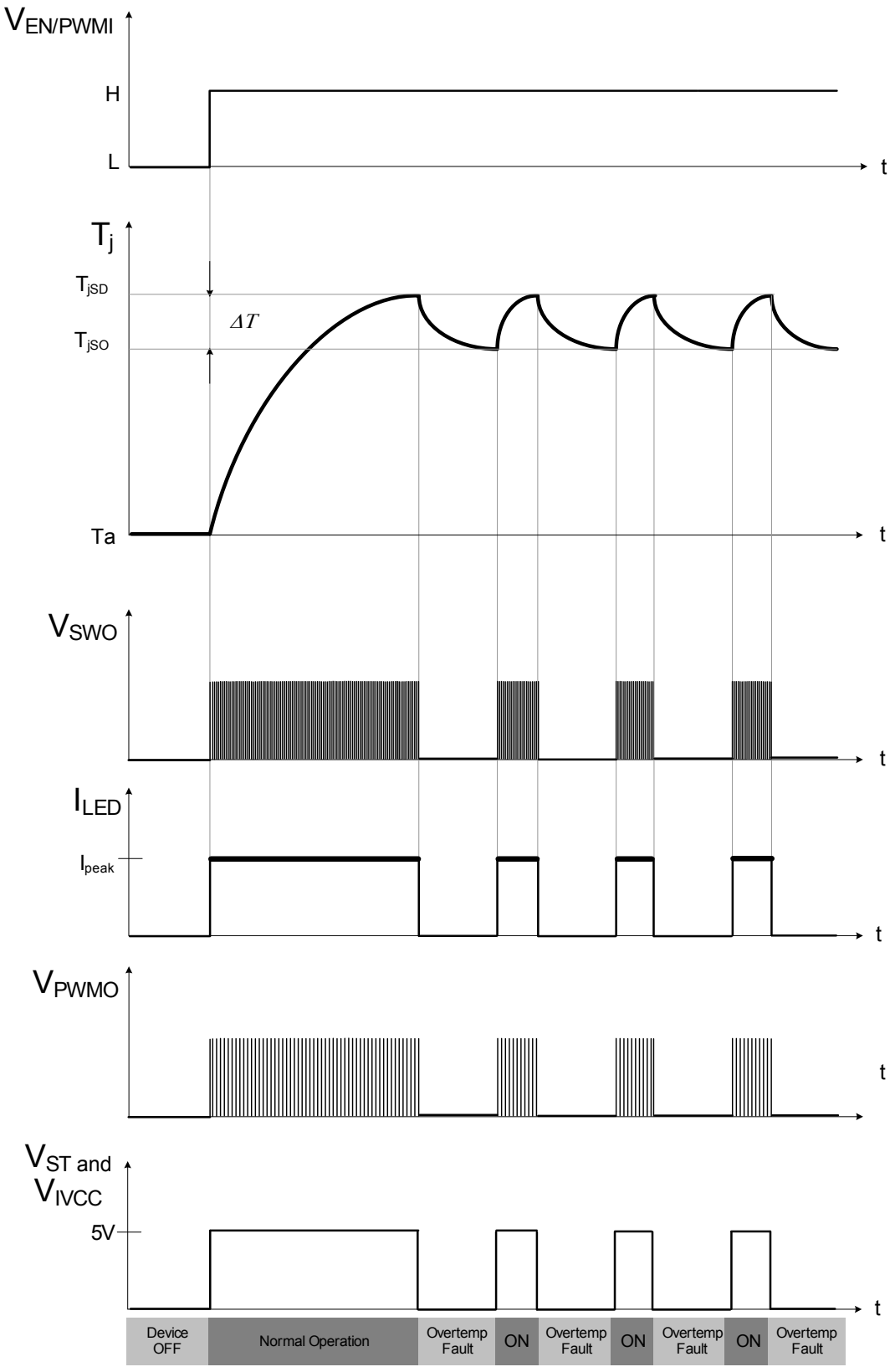

Figure 9-6 Device Overtemperature Protection Behavior

9.2 Electrical Characteristics

V_{IN} = 6 V to 40 V; 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 9-1 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Status Output							
Status Output Voltage Low	$V_{ST,LOW}$	–	–	0.4	V	I_{ST} = 1mA	P_9.2.1
Status Sink Current Limit	$I_{ST,MAX}$	2	–	–	mA	V_{ST} = 1V	P_9.2.2
Status Output Current	$I_{ST,HIGH}$	–	–	1	µA	V_{ST} = 5V	P_9.2.3
Status Delay Time	t_{SD}	8	10	12	ms		P_9.2.4
Temperature Protection							
Overtemperature Shutdown	$T_{j,SD}$	160	175	190	°C		P_9.2.5
Overtemperature Shutdown Hystereses	$T_{j,SD,HYST}$	–	15	–	°C		P_9.2.6
Overvoltage Protection							
Output Over Voltage Feedback Threshold Increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V		P_9.2.7
Output Over Voltage Feedback Hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	Output Voltage decreasing	P_9.2.8
Over Voltage Reaction Time	t_{OVPRR}	2	–	10	µs	Output Voltage decreasing	P_9.2.9
Over Voltage Feedback Input Current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25 V	P_9.2.10
Open Load and Open Feedback Diagnostics							
Open Load/Feedback Threshold	$V_{REF,1,3}$	-100	–	-20	mV	V_{REF} = V_{FBH} - V_{FBL} Open Circuit 1 or 3	P_9.2.11
Open Feedback Threshold	$V_{REF,2}$	0.5	–	1	V	V_{REF} = V_{FBH} - V_{FBL} Open Circuit 2	P_9.2.12

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.