Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# Infineon® LITIX™ Power

## Multitopology LITIX™ Power DC/DC Controller IC

TLD5097EL


# Infineon® LITIX™ Power

Multitopology LITIX™ Power DC/DC Controller IC


## Data Sheet

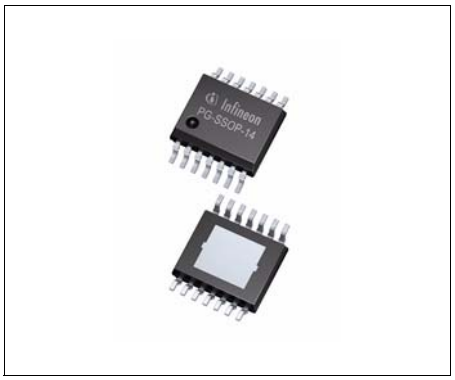
Revision 1.0

2015-03-12

Automotive Power

# Table of Contents

# 1 Overview



PG-SSOP-14

- Wide Input Voltage Range from 4.5 V to 45 V
- Constant Current or Constant Voltage Regulation
- Drives LEDs in Boost, Buck, Buck-Boost, SEPIC and Flyback Topology
- Very Low Shutdown Current: Iq_OFF < 10 µA
- Flexible Switching Frequency Range, 100 kHz to 500 kHz
- Synchronization with external clock source
- PWM Dimming
- Analog Dimming feature to adjust average LED current
- Internal 5 V Low Drop Out Voltage Regulator
- Open Circuit Detection
- Output Overvoltage Protection
- Internal Soft Start
- Over Temperature Shutdown
- Wide LED current range via simple adaptation of external components
- 300mV High Side Current Sense to ensure highest flexibility and LED current accuracy
- Available in a small thermally enhanced PG-SSOP-14 package
- Automotive AEC Qualified
- Green Product (RoHS) Compliant

### Description

The TLD5097EL is a LED boost controller with built in protection features. The main function of this device is to regulate a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and longer lifetime. The controller concept of the TLD5097EL allows multiple configurations such as Boost, Buck, Buck-Boost, SEPIC and Flyback by simply adjusting the external components. The TLD5097EL offers the most flexible dimming options. Dimming can be achieved with analog or PWM input.The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The TLD5097EL features an enable function reducing the shut-down current consumption to $I_{q\_OFF}$ < 10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides output overvoltage protection and device overtemperature shutdown.

### Application

- Automotive Exterior and Interior Lighting

| Type | Package | Marking |
|---|---|---|
| TLD5097EL | PG-SSOP-14 | TLD5097 |

# 2 Block Diagram

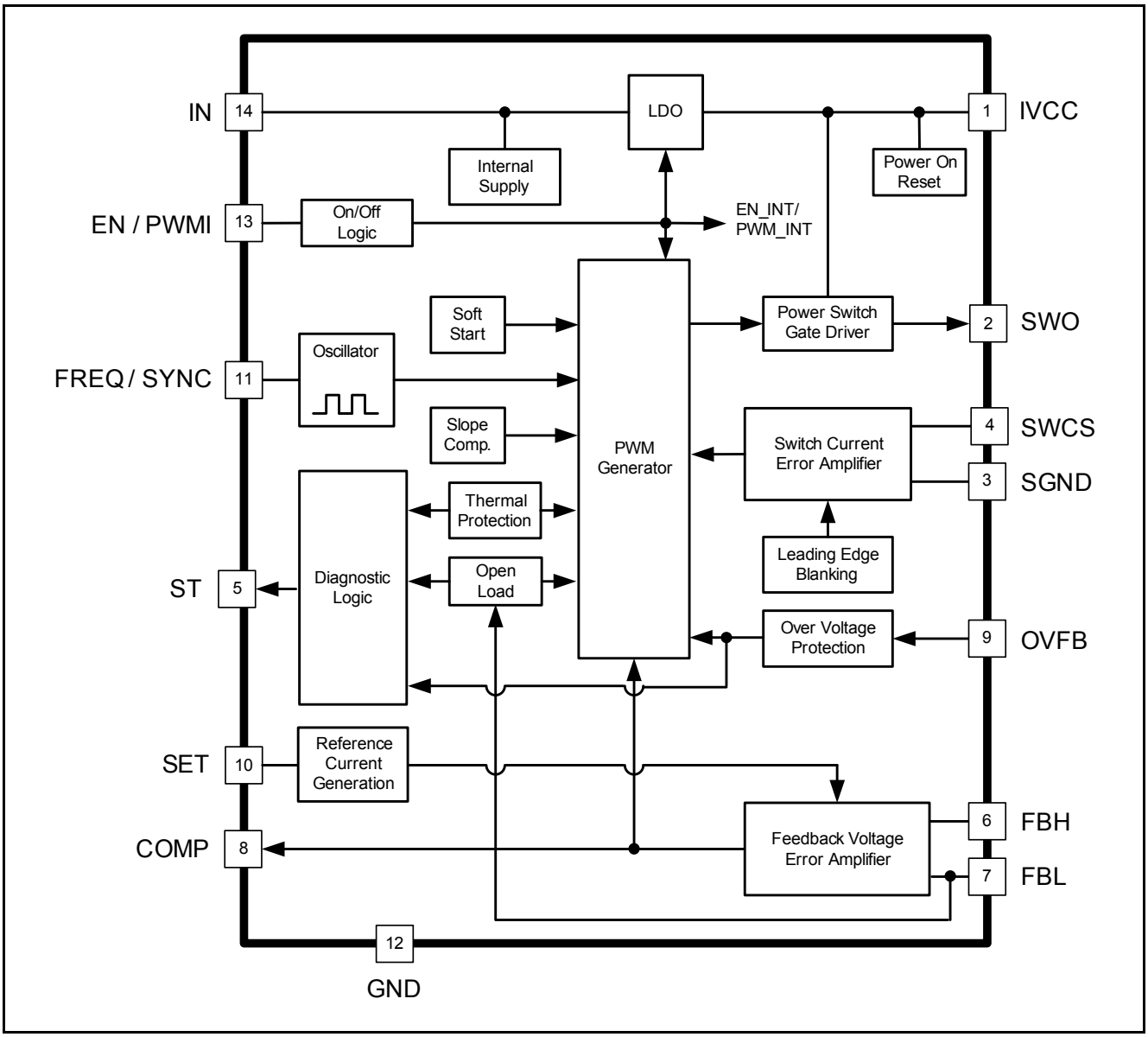



**Figure 2-1 Block Diagram TLD5097EL**

# 3 Pin Configuration

## 3.1 Pin Assignment

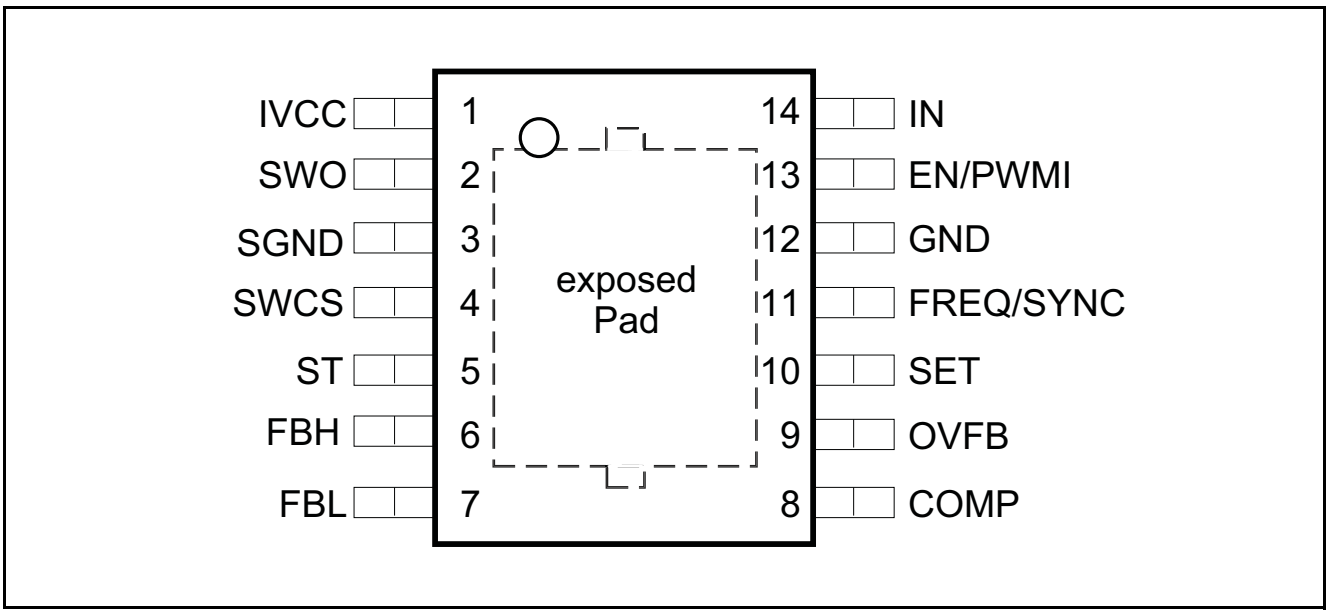



**Figure 3-1 Pin Configuration TLD5097EL**

## 3.2 Pin Definitions and Functions

**Table 3-1 Pin Definition and Function**

| # | Symbol | Direction | Type | Function |
|---|---|---|---|---|
| 1 | IVCC | | | **Internal LDO Output;** Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not be left open. |
| 2 | SWO | | | **Switch Output;** Connect to gate of external switching MOSFET |
| 3 | SGND | | | **Current Sense Ground;** Ground return for current sense switch |
| 4 | SWCS | | | **Current Sense Input;** Detects the peak current through switch |
| 5 | ST | | | **Status Output;**to indicate fualt conditions |
| 6 | FBH | | | **Voltage Feedback Positive;** Non inverting Input (+) |
| 7 | FBL | | | **Voltage Feedback Negative;** Inverting Input (-) |
| 8 | COMP | | | **Compensation Input;** Connect R and C network to pin for stability |

**Table 3-1 Pin Definition and Function**

| # | Symbol | Direction | Type | Function |
|---|---|---|---|---|
| 9 | OVFB | | | **Output Overvoltage Protection Feedback;** Connect to resistive voltage divider to set overvoltage threshold. |
| 10 | SET | | | **Analog Dimming Input;** Load current adjustment Pin. Pin must not be left open. If analog dimming feature is not used connect to IVCC pin. |
| 11 | FREQ / SYNC | | | **Frequency Select or Synchronization Input;** Connect external resistor to GND to set frequency. Or apply external clock signal for synchronization within frequency capture range. |
| 12 | GND | | | **Ground;** Connect to system ground. |
| 13 | EN / PWMI | | | **Enable or PWM Input;** Apply logic HIGH signal to enable device or PWM signal for dimming LED. |
| 14 | IN | | | **Supply Input;** Supply for internal biasing. |
| | EP | | | **Exposed Pad;** Connect to external heat spreading GND Cu area (e.g. inner GND layer of multilayer PCB with thermal vias) |

# 4 General Product Characteristics

## 4.1 Absolute Maximum Ratings

$T_j$ = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

**Table 4-1 Absolute Maximum Ratings[1)]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| IN<br>Supply Input | $V_{IN}$ | -0.3 | | 45 | V | | P_4.1.1 |
| EN / PWMI<br>Enable or PWM Input | $V_{EN}$ | -40 | | 45 | V | | P_4.1.2 |
| FBH-FBL;<br>Feedback Error Amplifier Differential | $V_{FBH}$-$V_{FBL}$ | -40 | | 61 | V | The maximum delta must not exceed 61V | P_4.1.3 |
| FBH;<br>Feedback Error Amplifier Positive Input | $V_{FBH}$ | -40 | | 61 | V | The difference between $V_{FBH}$ and $V_{FBL}$ must not exceed 61V, refer to Parameter 4.1.3 | P_4.1.4 |
| FBL<br>Feedback Error Amplifier Negative Input | $V_{FBL}$ | -40 | | 61 | V | The difference between $V_{FBH}$ and $V_{FBL}$ must not exceed 61V, refer to Parameter 4.1.3 | P_4.1.5 |
| FBH and FBL Current | $I_{FBL,FBH}$ | | 1 | | mA | t < 100ms, $V_{FBH}$-$V_{FBL}$ =0.3V | P_4.1.6 |
| OVFB<br>Over Voltage Feedback Input | $V_{OVP}$ | -0.3 | | 5.5 | V | | P_4.1.7 |
| OVFB<br>Over Voltage Feedback Input | $V_{OVP}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.8 |
| SWCS<br>Switch Current Sense Input | $V_{SWCS}$ | -0.3 | | 5.5 | V | | P_4.1.9 |
| SWCS<br>Switch Current Sense Input | $V_{SWCS}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.10 |

**Table 4-1 Absolute Maximum Ratings[1)]**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SWO<br>Switch Gate Drive Output | $V_{SWO}$ | -0.3 | | 5.5 | V | | P_4.1.11 |
| SWO<br>Switch Gate Drive Output | $V_{SWO}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.12 |
| SGND<br>Current Sense Switch GND | $V_{SGND}$ | -0.3 | | 0.3 | V | | P_4.1.13 |
| COMP<br>Compensation Input | $V_{COMP}$ | -0.3 | | 5.5 | V | | P_4.1.14 |
| COMP<br>Compensation Input | $V_{COMP}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.15 |
| FREQ / SYNC; Frequency and Synchronization Input | $V_{FREQ / SYNC}$ | -0.3 | | 5.5 | V | | P_4.1.16 |
| FREQ / SYNC; Frequency and Synchronization Input | $V_{FREQ / SYNC}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.17 |
| PWMO<br>PWM Dimming Output | $V_{PWMO}$ | -0.3 | | 5.5 | V | | P_4.1.18 |
| PWMO<br>PWM Dimming Output | $V_{PWMO}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.19 |
| ST | $V_{ST}$ | -0.3 | | 5.5 | V | | P_4.1.20 |
| ST | $V_{ST}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.21 |
| ST current | $I_{ST}$ | -2 | | 2 | mA | | P_4.1.22 |
| SET | $V_{SET}$ | -0.3 | | 45 | V | | P_4.1.23 |
| IVCC<br>Internal Linear Voltage Regulator Output | $V_{IVCC}$ | -0.3 | | 5.5 | V | | P_4.1.24 |
| IVCC<br>Internal Linear Voltage Regulator Output | $V_{IVCC}$ | -0.3 | | 6.2 | V | t < 10s | P_4.1.25 |
| **Temperatures** | | | | | | | |
| Junction Temperature | $T_j$ | -40 | | 150 | °C | | P_4.1.26 |
| Storage Temperature | $T_{stg}$ | -55 | | 150 | °C | | P_4.1.27 |
| **ESD Susceptibility** | | | | | | | |
| ESD Resistivity of all pins | $V_{ESD,HBM}$ | -2 | | 2 | kV | HBM[2)] | P_4.1.28 |
| ESD Resistivity of IN, EN/PWMI, FBH, FBL and SET pin to GND | $V_{ESD,HBM}$ | -4 | | 4 | kV | HBM[2)] | P_4.1.29 |

1) Not subject to production test, specified by design.

2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5kΩ, 100pF)

*Note:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 4-2 Functional Range**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Extended Supply Voltage Range | $V_{IN}$ | 4.5 | | 45[1)] | V | $V_{IVCC} > V_{IVCC,RTH,d}$; Parameter deviations possible | P_4.2.1 |
| Nominal Supply Voltage Range | $V_{IN}$ | 8 | | 34 | V | | P_4.2.2 |
| Feedback Voltage Input | $V_{FBH}$; $V_{FBL}$ | 3 | | 60 | V | | P_4.2.3 |
| Junction Temperature | $T_j$ | -40 | | 150 | °C | | P_4.2.4 |

1) Not subject to production test, specified by design

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

**Table 4-3 Thermal Resistance**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Junction to Case[1)2)] | $R_{thJC}$ | | 10 | | K/W | | P_4.3.1 |
| Junction to Ambient[3)] | $R_{thJA}$ | | 47 | | K/W | 2s2p | P_4.3.2 |
| Junction to Ambient | $R_{thJA}$ | | 54 | | K/W | 1s0p + 600mm$^2$ | P_4.3.3 |
| Junction to Ambient | $R_{thJA}$ | | 64 | | K/W | 1s0p + 300mm$^2$ | P_4.3.4 |

1) Not subject to production test, specified by design.

2) Specified $R_{thJC}$ value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta=25°C is dissipating 1W.

3) Specified $R_{thJA}$ value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5mm board. The 2s2p board has 2 outer copper layers (2 x 70µm Cu) and 2 inner copper layers (2 x 35µm Cu), A thermal via (diameter = 0.3mm and 25µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta=25°C, IC is dissipating 1W

# 5 Switching Regulator

## 5.1 Description

The TLD5097EL regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The switching regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs to an external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over $t_{SS}$ (Parameter 5.2.9) to minimize potential overvoltage at the output.

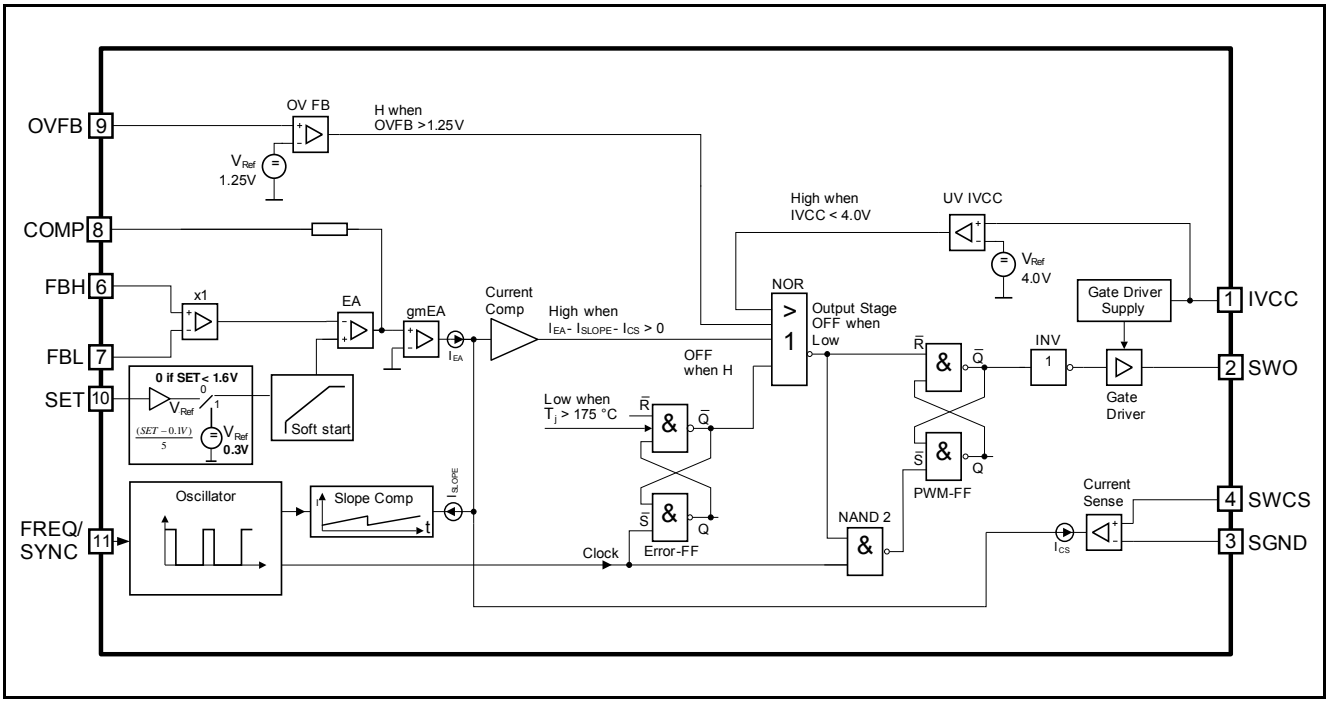



**Figure 5-1 Switching Regulator Block Diagram**

## 5.2 Electrical Characteristics

$V_{IN}$ = 8 V to 34 V; $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

**Table 5-1 Electrical Characteristics: Switching Regulator**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Regulator** | | | | | | | |
| Feedback Reference Voltage | $V_{REF}$ | 0.29 | 0.30 | 0.31 | V | refer to **Figure 11-11** $V_{REF}= V_{FBH} -V_{FBL}$ $V_{SET}$= 5V $I_{LED}$= 350 mA | P_5.2.1 |
| Feedback Reference Voltage | $V_{REF}$ | 0.057 | 0.06 | 0.063 | V | refer to **Figure 11-11** $V_{REF}= V_{FBH} -V_{FBL}$ $V_{SET}$= 0.4V $I_{LED}$= 70mA | P_5.2.2 |
| Feedback Reference Voltage Offset | $V_{REF\_offset}$ | – | – | 5 | mV | refer to **Figure 10-2** and **Figure 11-11** $V_{REF}= V_{FBH} -V_{FBL}$ $V_{SET}$= 0.1V $V_{OUT}>V_{IN}$ | P_5.2.3 |
| Voltage Line Regulation | $(\Delta V_{REF} / V_{REF}) / \Delta V_{IN}$ | – | – | 0.15 | %/V | refer to **Figure 11-11** $V_{IN}$ = 8V to 19V; $V_{SET}$ = 5V; $I_{LED}$ = 350mA | P_5.2.4 |
| Voltage Load Regulation | $(\Delta V_{REF} / V_{REF}) / \Delta I_{BO}$ | – | – | 5 | %/A | refer to **Figure 11-11** $V_{SET}$ = 5V; $I_{LED}$ = 100 to 500mA | P_5.2.5 |
| Switch Peak Over Current Threshold | $V_{SWCS}$ | 130 | 150 | 170 | mV | $V_{FBH} = V_{FBL}$ = 5 V VCOMP = 3.5V | P_5.2.6 |
| Maximum Duty Cycle | $D_{MAX,fixed}$ | 91 | 93 | 95 | % | Fixed frequency mode | P_5.2.7 |
| Maximum Duty Cycle | $D_{MAX,sync}$ | 88 | – | – | % | Synchronization mode | P_5.2.8 |
| Soft Start Ramp | $t_{SS}$ | 350 | 1000 | 1500 | µs | $V_{FB}$ rising from 5% to 95% of $V_{FB}$, typ. | P_5.2.9 |
| IFBH Feedback High Input Current | $I_{FBH}$ | 38 | 46 | 54 | µA | $V_{FBH} - V_{FBL}$ = 0.3 V | P_5.2.10 |

**Table 5-1 Electrical Characteristics: Switching Regulator**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| IFBL Feedback Low Input Current | $I_{FBL}$ | 15 | 21 | 27 | µA | $V_{FBH}$ - $V_{FBL}$ = 0.3 V | P_5.2.11 |
| Switch Current Sense Input Current | $I_{SWCS}$ | 10 | 50 | 100 | µA | $V_{SWCS}$ = 150 mV | P_5.2.12 |
| Input Undervoltage Shutdown | $V_{IN,off}$ | 3.5 | – | 4.5 | V | $V_{IN}$ decreasing | P_5.2.13 |
| Input Voltage Startup | $V_{IN,on}$ | – | – | 4.85 | V | $V_{IN}$ increasing | P_5.2.14 |
| **Gate Driver for External Switch** | | | | | | | |
| Gate Driver Peak Sourcing Current | $I_{SWO,SRC}$ | – | 380 | – | mA | 1)VSWO = 1 V to 4 V | P_5.2.15 |
| Gate Driver Peak Sinking Current | $I_{SWO,SNK}$ | – | 550 | – | mA | 1)VSWO = 4 V to 1 V | P_5.2.16 |
| Gate Driver Output Rise Time | $t_{R,SWO}$ | – | 30 | 60 | ns | 1)CL,SWO = 3.3 nF; VSWO = 1 V to 4 V | P_5.2.17 |
| Gate Driver Output Fall Time | $t_{F,SWO}$ | – | 20 | 40 | ns | 1)CL,SWO = 3.3 nF; VSWO = 4 V to 1 V | P_5.2.18 |
| Gate Driver Output Voltage | $V_{SWO}$ | 4.5 | – | 5.5 | V | 1)CL,SWO = 3.3 nF | P_5.2.19 |

1) Not subject to production test, specified by design

# 6 Oscillator and Synchronisation

## 6.1 Description

### R_OSC vs. switching frequency

The internal oscillator is used to determine the switching frequency of the boost regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

(6.1)

$$R_{FREQ} = \frac{1}{(141 \cdot 10^{-12}\left[\frac{s}{\Omega}\right]) \cdot \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - (3.5 \cdot 10^{3}\,[\Omega])\,[\Omega]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the boost regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

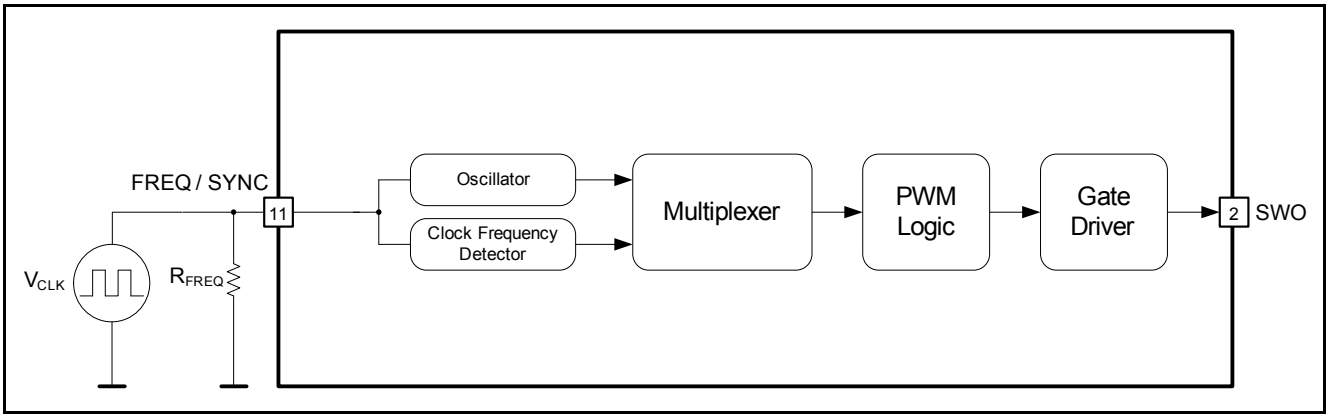



**Figure 6-1 Oscillator and Synchronization Block Diagram and Simplified Application Circuit**

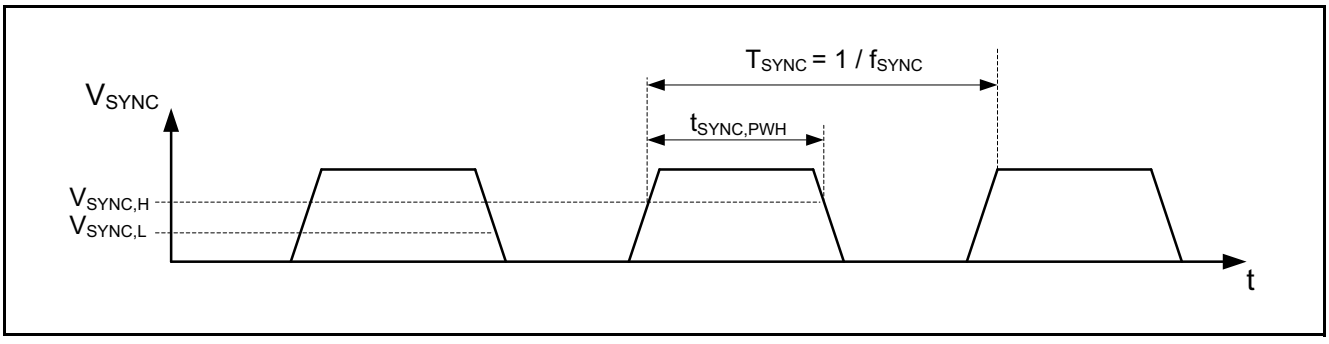



**Figure 6-2 Synchronization Timing Diagram**

## 6.2 Electrical Characteristics

$V_{IN}$ = 8 V to 34 V; $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

**Table 6-1 Electrical Characteristics: Oscillator and Synchronisation**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Oscillator** | | | | | | | |
| Oscillator Frequency | $f_{FREQ}$ | 250 | 300 | 350 | kHz | $R_{FREQ}$ = 20kΩ | P_6.2.1 |
| Oscillator Frequency Adjustment Range | $f_{FREQ}$ | 100 | – | 500 | kHz | | P_6.2.2 |
| FREQ / SYNC Supply Current | $I_{FREQ}$ | – | – | -700 | µA | $V_{FREQ}$ = 0 V | P_6.2.3 |
| Frequency Voltage | $V_{FREQ}$ | 1.16 | 1.24 | 1.32 | V | $f_{FREQ}$ = 100 kHz | P_6.2.4 |
| **Synchronisation** | | | | | | | |
| Synchronization Frequency Capture Range | $f_{SYNC}$ | 250 | – | 500 | kHz | | P_6.2.5 |
| Synchronization Signal High Logic Level Valid | $V_{SYNC,H}$ | 3.0 | – | – | V | 1)2) | P_6.2.6 |
| Synchronization Signal Low Logic Level Valid | $V_{SYNC,L}$ | – | – | 0.8 | V | 1)2) | P_6.2.7 |
| Synchronization Signal Logic High Pulse Width | $t_{SYNC,PWH}$ | 200 | – | – | ns | 1)2) | P_6.2.8 |

1) Synchronization of external PWM ON signal to falling edge

2) Not subject to production test, specified by design

## 6.3 Typical Performance Characteristics of Oscillator

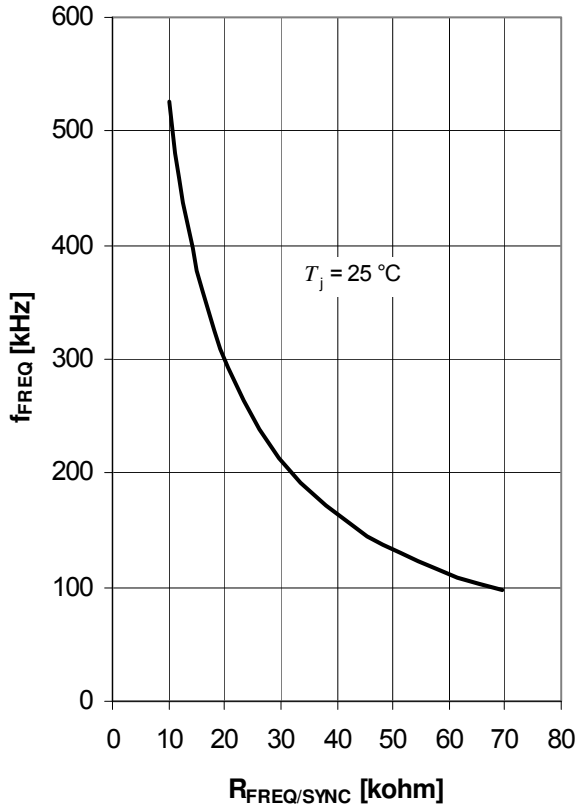



**Figure 6-3 Switching Frequency fSW versus Frequency Select Resistor to GND RFREQ/SYNC**

# 7 Enable and Dimming Function

## Description

The enable function powers ON or OFF the device. A valid logic LOW signal on enable pin EN/PWMI powers OFF the device and current consumption is less than $I_{q\_OFF}$ (Parameter 7.2.8). A valid logic HIGH enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is OFF in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to the internal gate driver. The EN/PWMI enables and disables the gate driver for the main switch during PWM operation. PWM dimming an LED is a commonly practiced dimming method and can prevent color shift in an LED light source.

The enable and PWM input function share the same pin. Therefore a valid logic LOW signal at the EN/PWMI pin needs to differentiate between an enable power OFF or an PWM dimming LOW signal. The device differentiates between enable OFF and PWM dimming signal by requiring the enable OFF at the EN/PWMI pin to stay LOW for the Enable Turn OFF Delay Time ($t_{EN,OFF,DEL}$ Parameter 7.2.6).

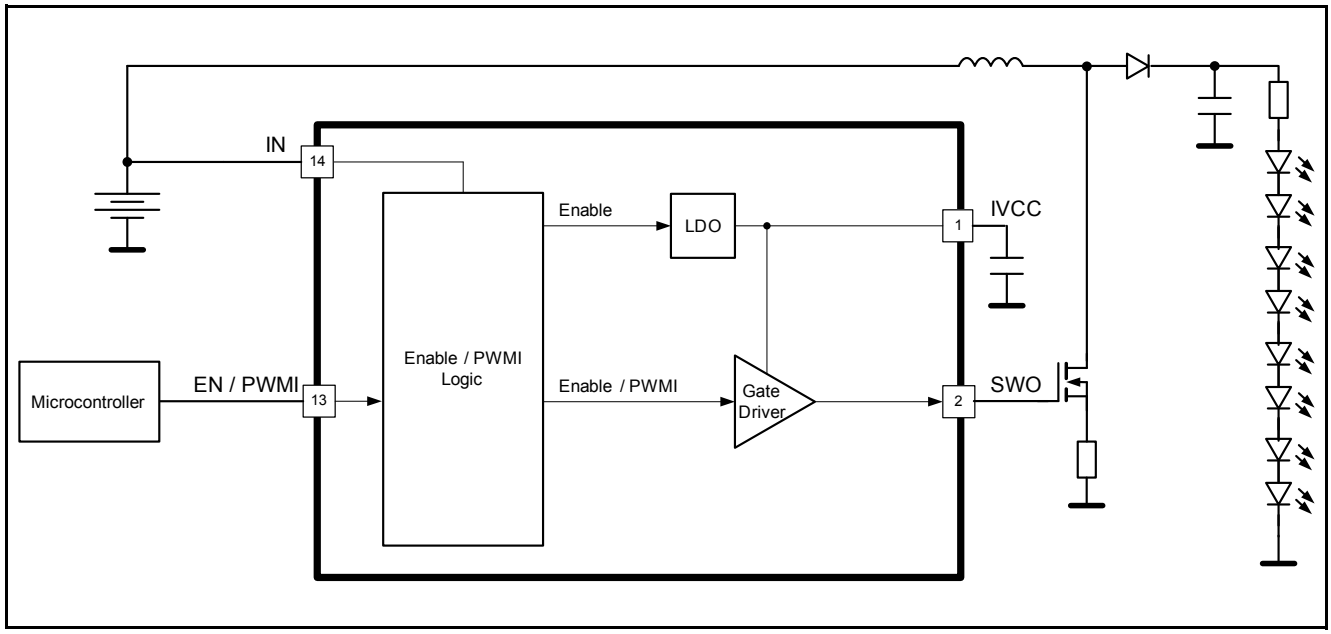



**Figure 7-1 Block Diagram and Simplified Application Circuit Enable and LED Dimming**

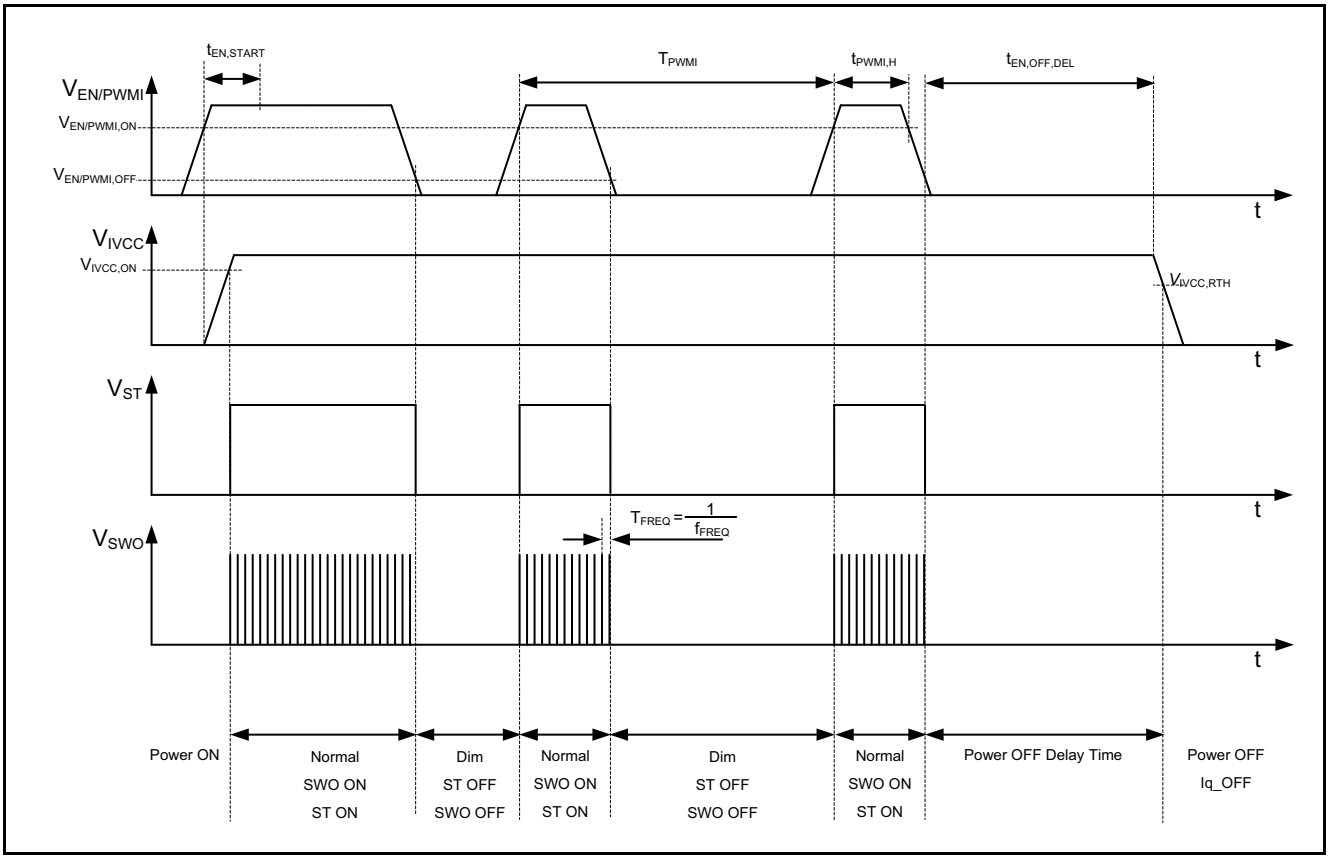



**Figure 7-2 Timing Diagram Enable and LED Dimming**

*Note: The ST signal is LOW during soft-start.*

## 7.1 Electrical Characteristics

VIN = 8V to 34V; $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

**Table 7-1 Electrical Characteristics: Enable and Dimming**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Enable / PWM Input** | | | | | | | |
| Enable/PWMI Turn On Threshold | $V_{EN/PWMI,ON}$ | 3.0 | – | | V | | P_7.1.1 |
| Enable/PWMI Turn Off Threshold | $V_{EN/PWMI,OFF}$ | – | – | 0.8 | V | | P_7.1.2 |
| Enable/PWMI Hysteresis | $V_{EN/PWMI,HYS}$ | 50 | 200 | 400 | mV | 1) | P_7.1.3 |
| Enable/PWMI High Input Current | $I_{EN/PWMI,H}$ | – | – | 30 | µA | $V_{EN/PWMI}$ = 16.0 V | P_7.1.4 |
| Enable/PWMI Low Input Current | $I_{EN/PWMI,L}$ | – | 0.1 | 1 | µA | $V_{EN/PWMI}$ = 0.5 V | P_7.1.5 |

**Table 7-1 Electrical Characteristics: Enable and Dimming**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Enable Turn Off Delay Time | $t_{EN,OFF,DEL}$ | 8 | 10 | 12 | ms | | P_7.1.6 |
| Enable Startup Time | $t_{EN,START}$ | 100 | – | – | µs | | P_7.1.7 |
| **Current Consumption** | | | | | | | |
| Current Consumption, Shutdown Mode | $I_{q\_OFF}$ | – | – | 10 | µA | $V_{EN/PWMI}$ = 0.8 V; $T_j \leq$ 105°C; $V_{IN}$ = 16V | P_7.1.8 |
| Current Consumption, Active Mode[2)] | $I_{q\_ON}$ | – | – | 7 | mA | $V_{EN/PWMI} \geq$ 4.75 V; $I_{BO}$ = 0 mA; $V_{SWO}$ = 0% Duty Cycle | P_7.1.9 |

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of external switches.

# 8 Linear Regulator

## Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM,min}$ (parameter **P_8.1.2**). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (parameter **P_8.1.5**) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

### Integrated Undervoltage Protection for the External Switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage ($V_{IVCC}$) and resets the device in case the output voltage falls below the IVCC undervoltage reset switch OFF threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

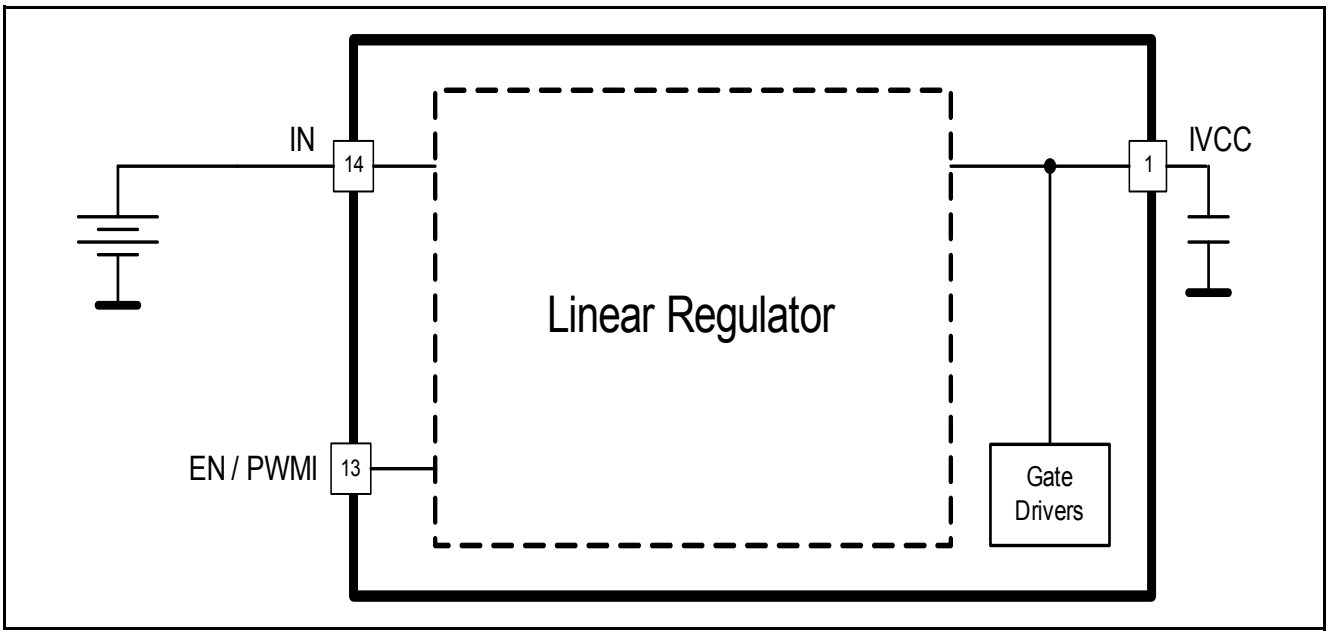



**Figure 8-1 Voltage Regulator Block Diagram and Simplified Application Circuit**

## 8.1 Electrical Characteristics

$V_{IN}$ = 8V to 34V; $T_j$ = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

**Table 8-1 Electrical Characteristics:Line Regulator**

| Parameter | Symbol | Values | | | Unit | Note or Test Condition | Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output Voltage | $V_{IVCC}$ | 4.85 | 5 | 5.15 | V | 6 V ≤ $V_{IN}$ ≤ 45 V<br>0.1 mA≤$I_{IVCC}$≤40mA | P_8.1.1 |
| Output Current Limitation | $I_{LIM}$ | 51 | | 90 | mA | $V_{IN}$ = 13.5 V<br>$V_{IVCC}$ = 4.5V | P_8.1.2 |
| Drop out Voltage | $V_{DR}$ | | | 0.5 | V | $V_{IN}$ = 4.5V<br>$I_{IVCC}$ = 25mA | P_8.1.3 |
| IVCC Buffer Capacitor | $C_{IVCC}$ | 0.47 | 1 | 100 | µF | 1)2) | P_8.1.4 |
| IVCC Buffer Capacitor ESR | $R_{IVCC,ESR}$ | – | – | 0.5 | Ω | 1) | P_8.1.5 |
| Undervoltage Reset Headroom | $V_{IVCC,HDRM}$ | 100 | – | – | mV | $V_{IVCC}$ decreasing<br>$V_{IVCC}$ - $V_{IVCC,RTH,d}$ | P_8.1.6 |
| IVCC Undervoltage Reset switch OFF Threshold | $V_{IVCC,RTH,d}$ | 3.6 | – | 4.0 | V | 3)$V_{IVCC}$ decreasing | P_8.1.7 |
| IVCC Undervoltage Reset switch ON Threshold | $V_{IVCC,RTH,i}$ | – | – | 4.5 | V | $V_{IVCC}$ increasing | P_8.1.8 |

1) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum.

3) Selection of external switching MOSFET is crucial and the $V_{IVCC,RTH,d}$ min. as worst case $V_{GS}$ must be considered.

# 9 Protection and Diagnostic Functions

## 9.1 Description

The TLD5097EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case of a fault condition, the SWO signal stops operation. The ST signal will change to an active logic LOW signal to communicate that a fault has occurred (detailed overview in **Figure 9-1**and **Figure 9-2** below). **Figure 9-3** illustrates the various open load and open feedback conditions. In case of an overtemperature condition the integrated thermal shutdown function turns off the gate driver and internal linear voltage regulator. The typical junction shutdown temperature is 175°C ($T_{j,SD}$ Parameter 9.2.3). After cooling down the IC will automatically restart. Thermal shutdown is an integrated protection function designed to prevent IC destruction and is not intended for continuous use in normal operation (**Figure 9-5**). To calculate the proper overvoltage protection resistor values an example is given in **Figure 9-6**.

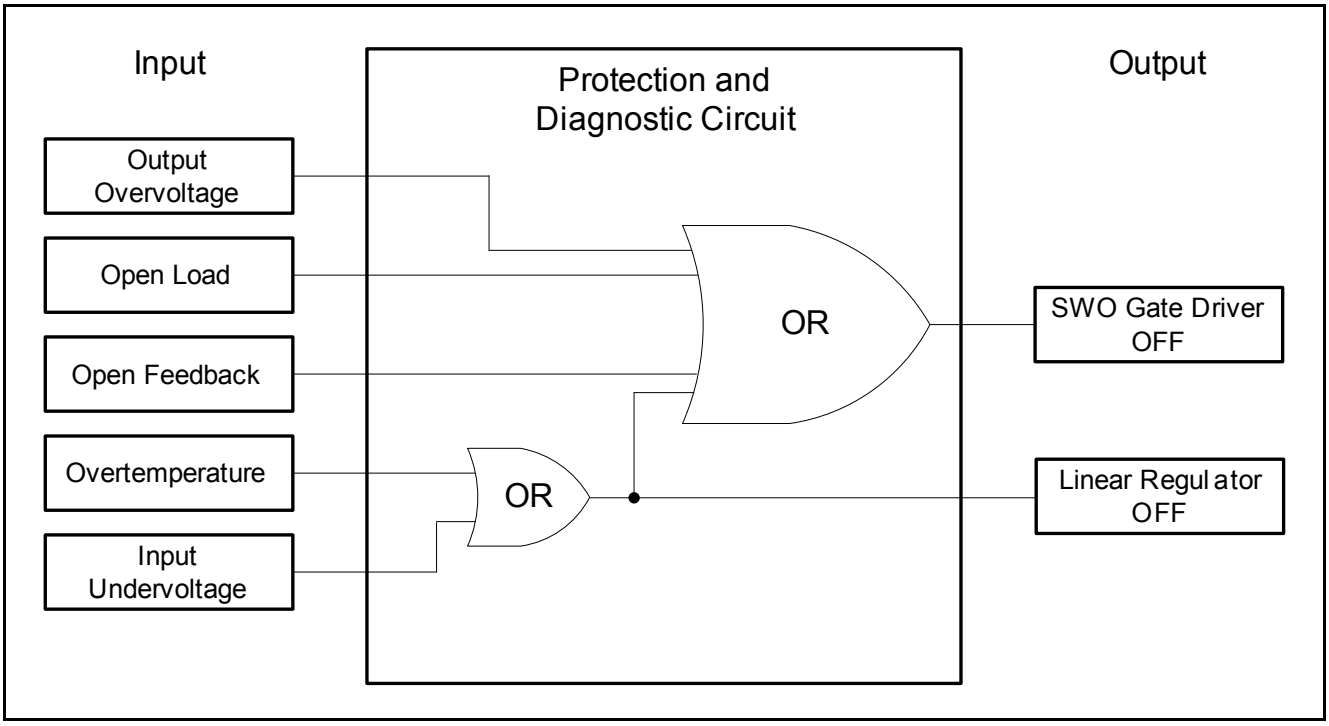
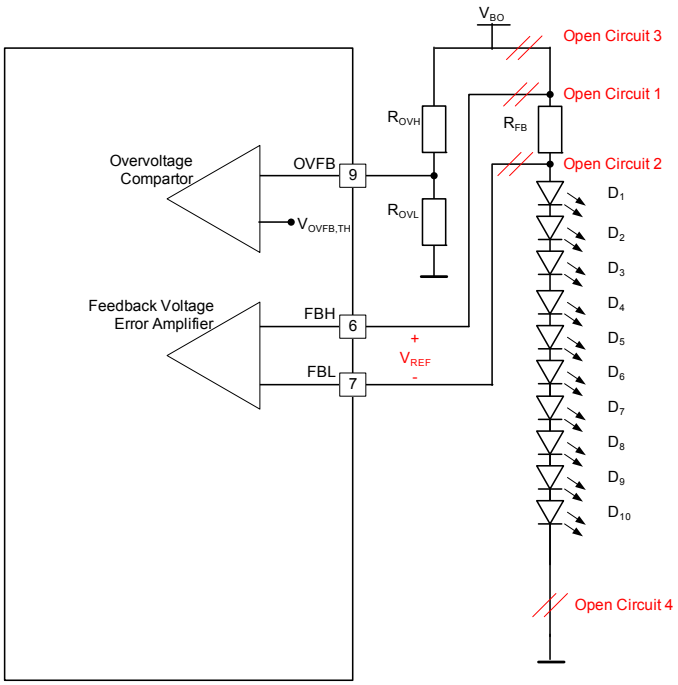



**Figure 9-1 Protection and Diagnostic Function Block Diagram**

| Input | | Output | | |
|---|---|---|---|---|
| Condition | Level* | ST | SWO | IVCC |
| Overvoltage @ Output | False | H or Sw* | Sw* | Active |
| | True | L | L | Active |
| Open Load | False | H or Sw* | Sw* | Active |
| | True | L | L | Active |
| Open Feedback | False | H or Sw* | Sw* | Active |
| | True | L | L | Active |
| Overtemperature | False | H or Sw* | Sw* | Active |
| | True | L | L | Shutdown |
| Undervoltage @ Input | False | H or Sw* | Sw* | Active |
| | True | L | L | Shutdown |

*Note:
Sw = Switching
False = Condition does not exist
True = Condition does exist

**Figure 9-2 Diagnosis Truth Table**




Output Open Circuit Conditions

| Open Circuit Condition | Fault Condition | Fault Threshold Voltage $V_{REF}$ |
|---|---|---|
| 1 | Open FBH | -20 to -100 mV |
| 2 | Open FBL | 0.5 to 1.0 V |
| 3 | Open VBO | -20 to -100 mV |
| 4 | Open LEDGND | Detected by overvoltage |

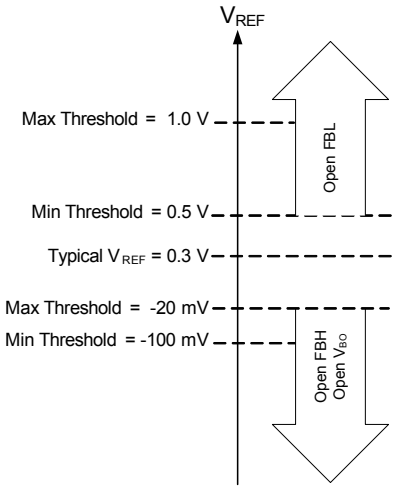



**Figure 9-3 Open Load and Open Feedback Conditions**

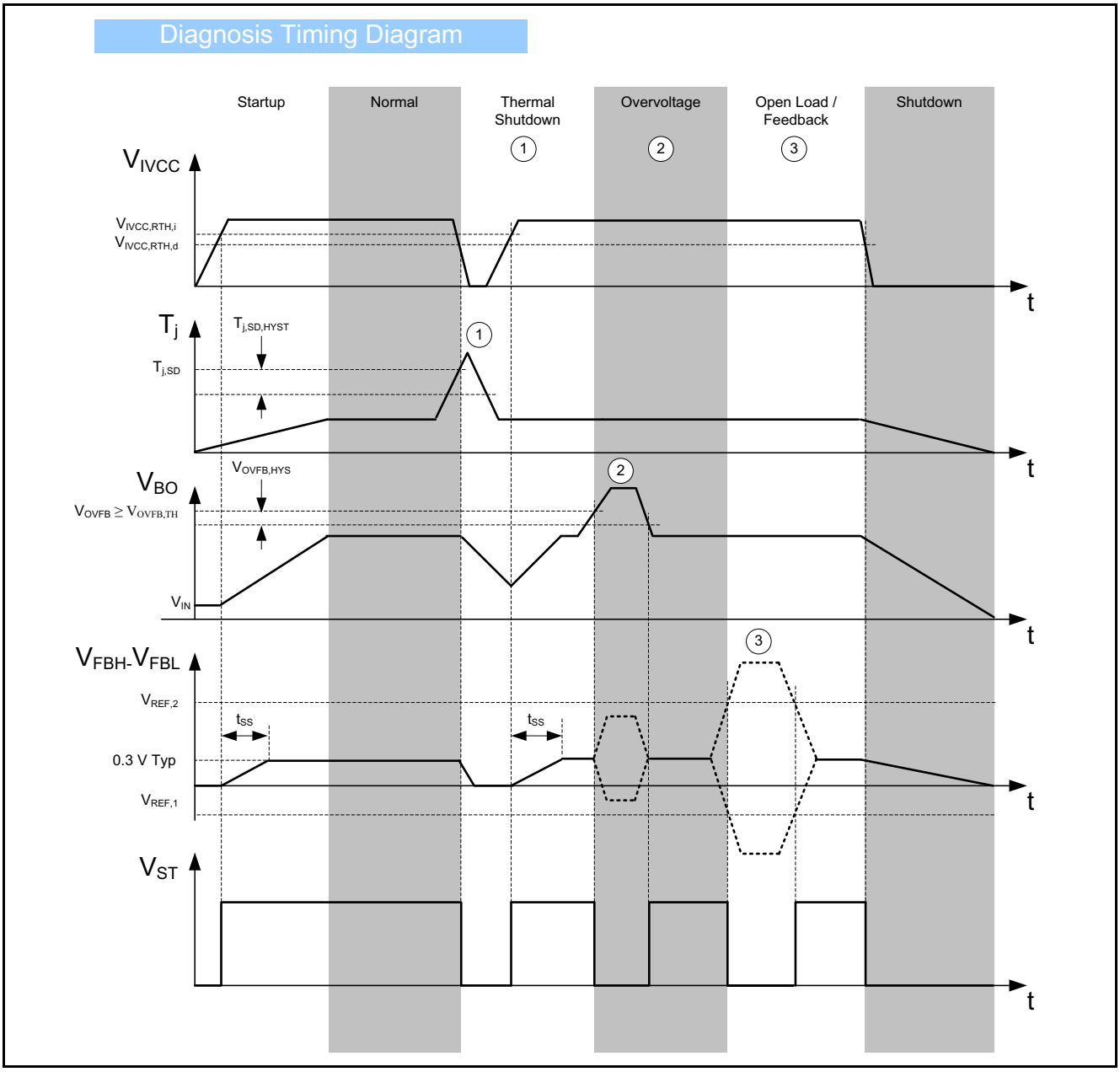



**Figure 9-4 Open load, Overvoltage and Overtemperature Timing Diagram**

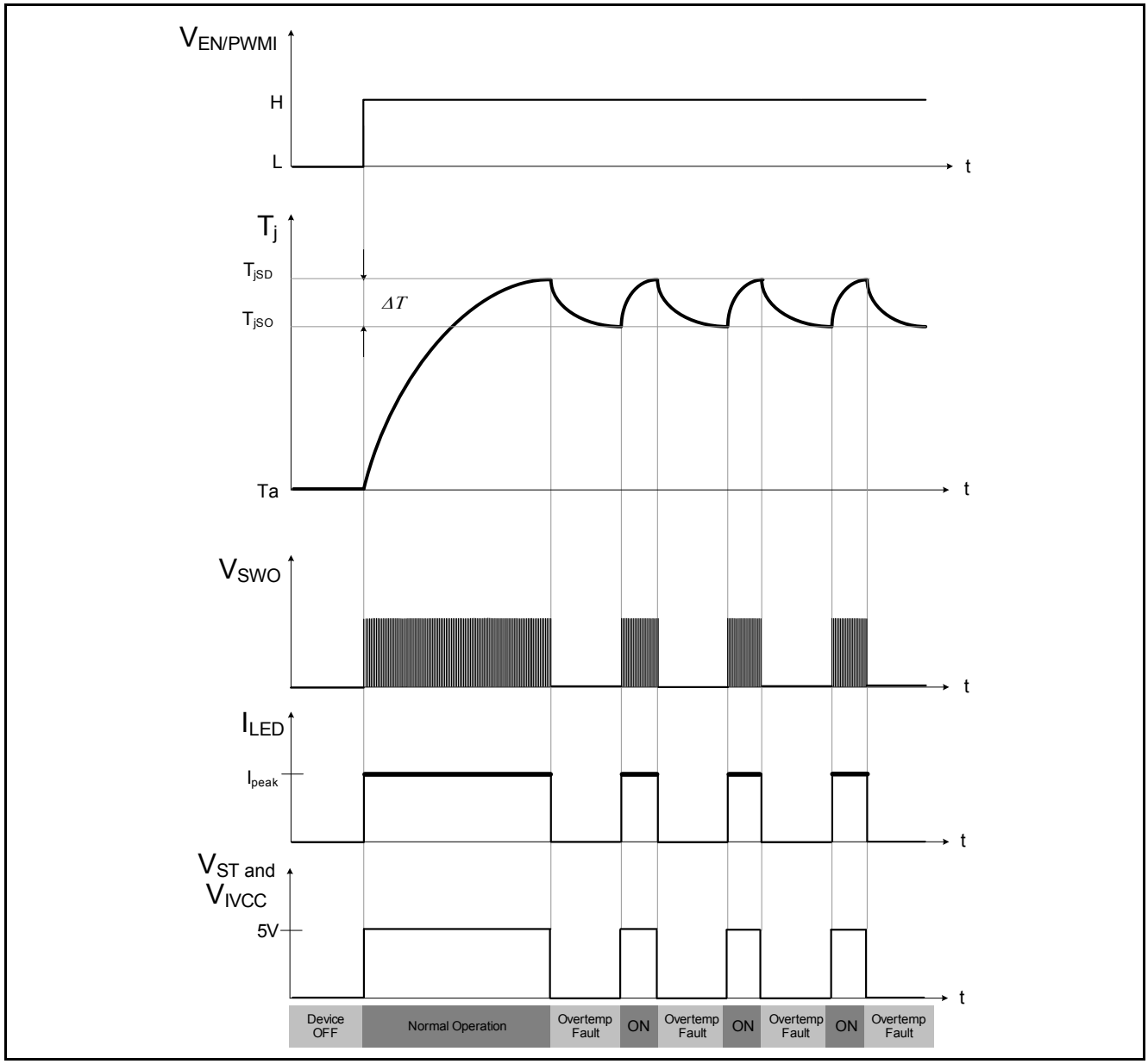



**Figure 9-5 Device Overtemperature Protection Behavior**

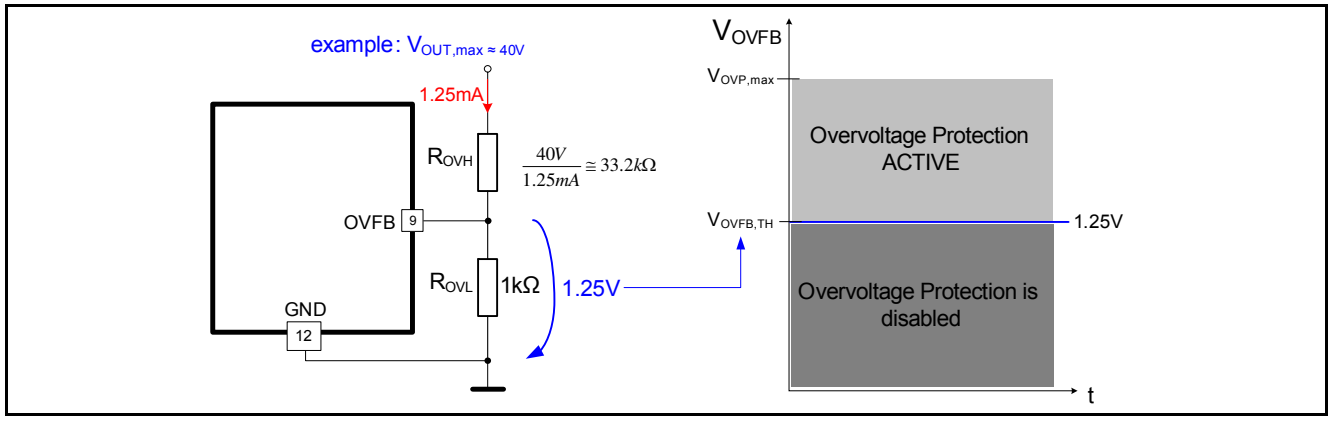



**Figure 9-6 Overvoltage Protection Description**