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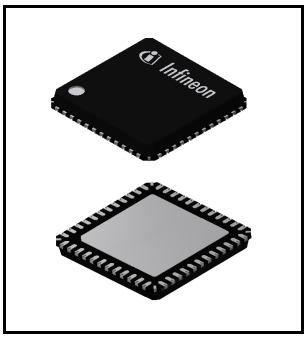
TLD5501-2QV

Dual SYNC Buck Controller with SPI Interface

Infineon® LITIX™ Power Flex

Package	PG-VQFN-48-31
Marking	TLD55012QV
Sales Name	TLD5501-2QV



1 Overview

Features

- Dual-Channel synchronous DC/DC Controller for HIGH POWER LED drivers
- Wide LED forward voltage Range (2 V up to 50 V)
- Wide VIN Range (IC 4.5 V to 40 V, Power 4.5 V to 55 V)
- Switching Frequency Range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum Efficiency in every condition (up to 96%)
- Constant Current (LED) and Constant Voltage Regulation
- Limp Home Function (Fail Safe Mode)
- EMC optimized device: Features an auto Spread Spectrum
- LED current sense with dedicated monitor Output
- Advanced protection features for device and load
- Enhanced Dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48-31 package
- Automotive AEC Qualified

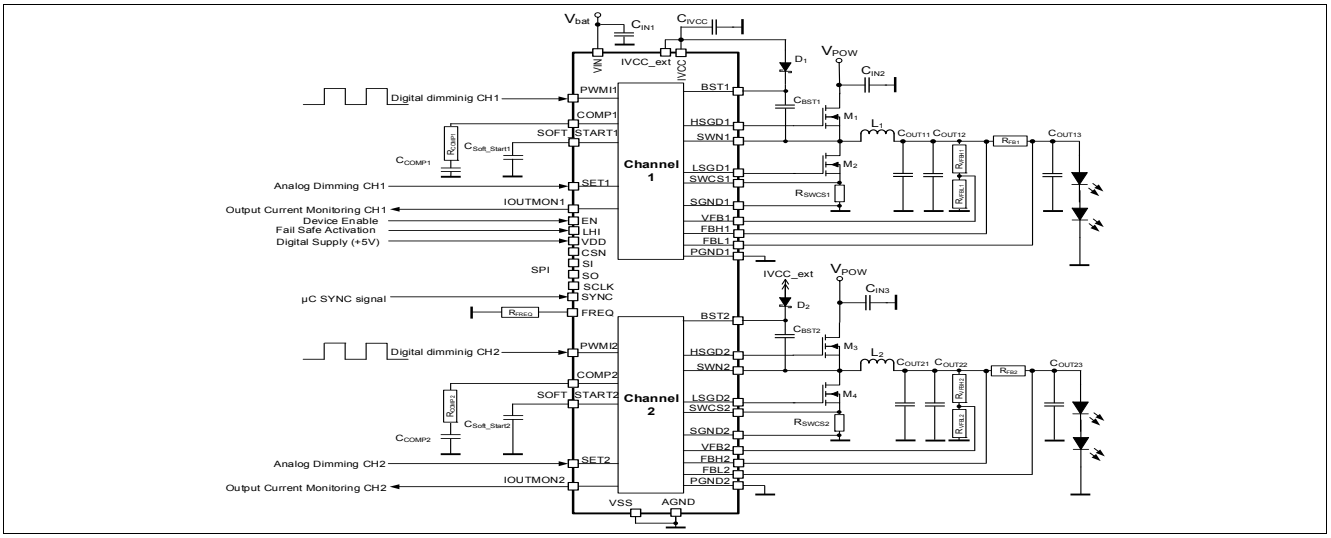


Figure 1 Application Drawing - TLD5501-2QV as current regulator

Overview

Description

The TLD5501-2QV is a synchronous DUAL Channel DC/DC buck controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5501-2QV offers both analog and digital (PWM) dimming.The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5501-2QV is suitable for use in the harsh automotive environment.

Table 1 Product Summary

Power Stage input voltage range	V_{POW}	4.5 V … 55 V
Device Input supply voltage range	V_{VIN}	4.5 V … 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	50 V
Switching Frequency range	f_{SW}	200 kHz... 700 kHz
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Up)	$R_{DS(ON\_PU)}$	2.3 Ω
Typical NMOS driver on-state resistance at T_j = 25°C (Gate Pull Down)	$R_{DS(ON\_PD)}$	1.2 Ω
SPI clock frequency	$f_{SCLK(MAX)}$	5 MHz

Protective Functions

- Over load protection of external MOSFETs
- Shorted load, output overvoltage and overcurrent protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in ON-state
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide I_{LED} information

Limp Home Function

- Limp Home activation via LHI pin

Applications

- Especially designed for driving high power LEDs in automotive applications
- Automotive Exterior Lighting: full LED headlamp assemblies (Low Beam, High Beam, Matrix Beam, Pixel Light)
- General purpose current/voltage controlled DC/DC buck LED driver

2 Block Diagram

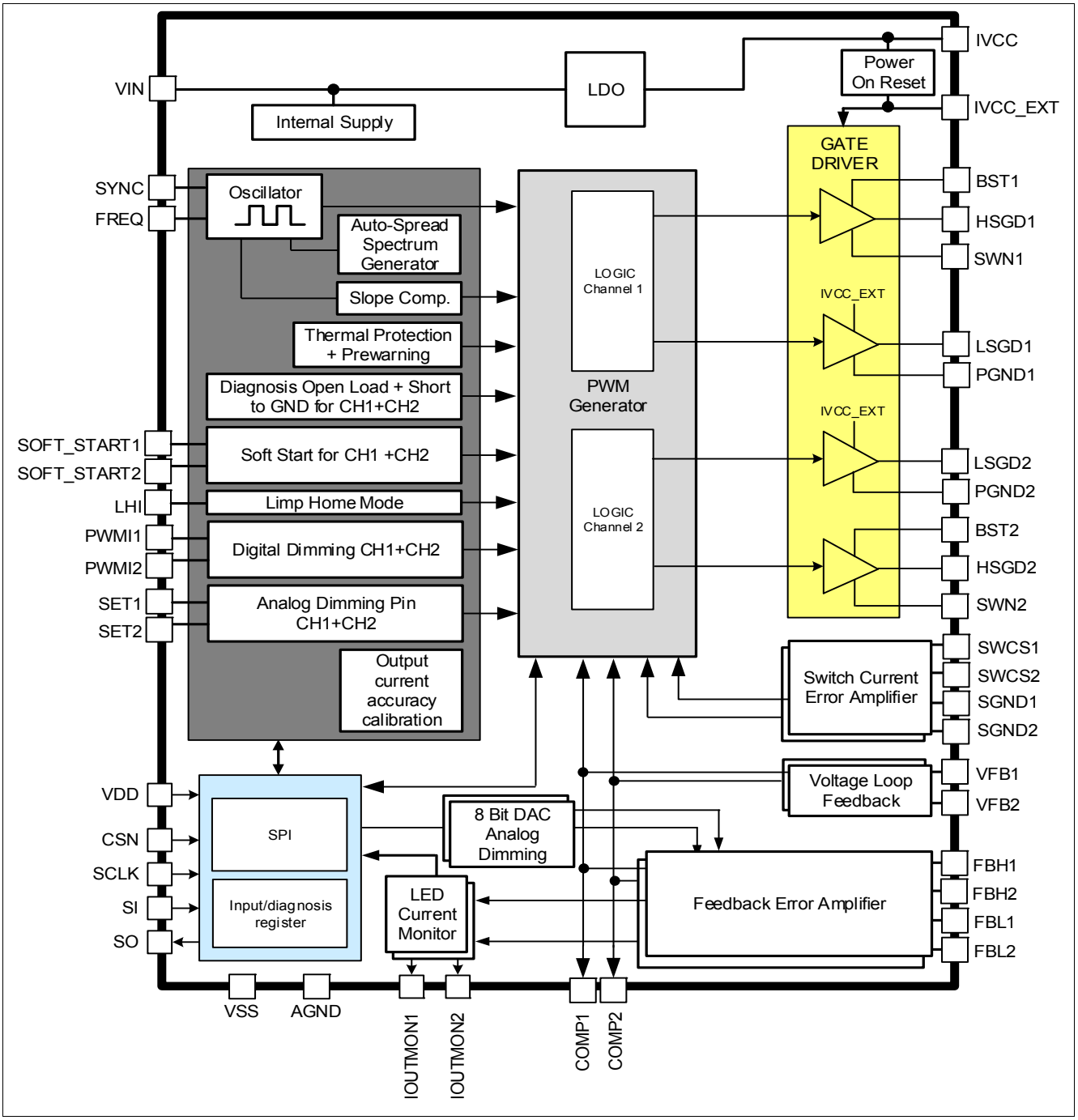


Figure 2 Block Diagram - TLD5501-2QV

3 Pin Configuration

3.1 Pin Assignment

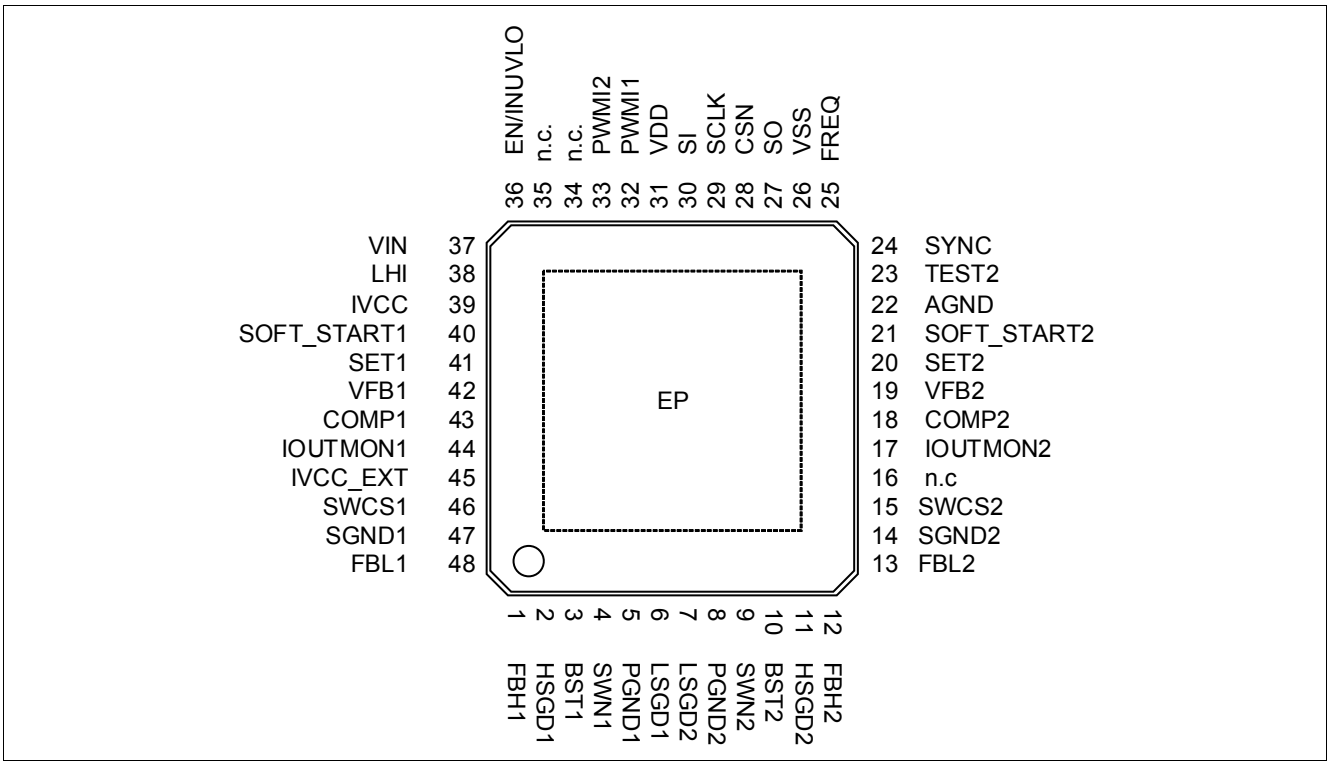


Figure 3 Pin Configuration - TLD5501-2QV

3.2 Pin Definitions and Functions

Pin	Symbol	I/O [1)]		Function
Power Supply				
16 , 34 ,35	n.c.	-		**Not connected, tie to AGND on the Layout;**
37	VIN	-		**Power Supply Voltage;** Supply for internal biasing.
31	VDD	-		**Digital GPIO Supply Voltage;** Connect to reverse voltage protected 5 V or 3.3 V supply.
45	IVCC_EXT	I	PD	**External LDO input;** Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.
5, 8	PGND1, 2	-		**Power Ground;** Ground for power potential. Connect externally close to the chip.
26	VSS	-		**Digital GPIO Ground;** Ground for GPIO pins.
22	AGND	-		**Analog Ground;** Ground Reference
-	EP	-		**Exposed Pad;** Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).
Gate Driver Stages				
2	HSGD1	O		**Highside Gate Driver Output 1;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET.
11	HSGD2	O		**Highside Gate Driver Output 2;** Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET.
6	LSGD1	O		**Lowside Gate Driver Output 1;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
7	LSGD2	O		**Lowside Gate Driver Output 2;** Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT}. Connect to gate of external switching MOSFET.
4	SWN1	IO		**Switch Node 1;**
9	SWN2	IO		**Switch Node 2;**
39	IVCC	O		**Internal LDO output;** Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.

Pin Configuration

Pin	Symbol	I/O [1)]		Function
Inputs and Outputs				
38	LHI	I	PD	**Limp Home Input Pin;** Used to enter in Limp Home state during Fail Safe condition.
23	TEST2	-		**Test Pin;** Used for Infineon end of line test, connect to GND in application.
36	EN/INUVLO	I	PD	**Enable/Input Under Voltage Lock Out;** Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open.
25	FREQ	I		**Frequency Select Input;** Connect external resistor to GND to set frequency.
24	SYNC	I	PD	**Synchronization Input;** Apply external clock signal for synchronization.
32	PWMI1	I	PD	**Control Input CH1;** Digital input 5 V or 3.3 V.
33	PWMI2	I	PD	**Control Input CH2;** Digital input 5 V or 3.3 V.
1	FBH1	I		**Output current Feedback Positive for CH1;** Non inverting Input (+) CH1.
12	FBH2	I		**Output current Feedback Positive for CH2;** Non inverting Input (+) CH2.
48	FBL1	I		**Output current Feedback Negative for CH1;** Inverting Input (-) CH1.
13	FBL2	I		**Output current Feedback Negative for CH2;** Inverting Input (-) CH2.
3	BST1	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.
10	BST2	IO		**Bootstrap capacitor;** Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.
46	SWCS1	I		**Current Sense Input for CH1;** Inductor current sense CH1 - Non Inverting Input (+).
15	SWCS2	I		**Current Sense Input for CH2;** Inductor current sense CH2 - Non Inverting Input (+).
47	SGND1	I		**Current Sense Ground for CH1;** Inductor current sense CH1 - Inverting Input (-). Route as Differential net with SWCS1 on the Layout.
14	SGND2	I		**Current Sense Ground for CH2;** Inductor current sense CH2 - Inverting Input (-). Route as Differential net with SWCS2 on the Layout.

Pin Configuration

Pin	Symbol	I/O [1]		Function
43	COMP1	O		**Compensation Network Pin for CH1;** Connect R and C network to pin for stability phase margin adjustment for CH1.
18	COMP2	O		**Compensation Network Pin for CH2;** Connect R and C network to pin for stability phase margin adjustment for CH2.
40	SOFT_START1	O		**Softstart configuration Pin for CH1;** Connect a capacitor C_{SOFT_START1} to GND to fix a soft start ramp default time.
21	SOFT_START2	O		**Softstart configuration Pin for CH2;** Connect a capacitor C_{SOFT_START2} to GND to fix a soft start ramp default time.
42	VFB1	I		**Voltage Feedback Pin for CH1;** VFB is intended to set output protection functions for CH1.
19	VFB2	I		**Voltage Feedback Pin for CH2;** VFB is intended to set output protection functions for CH2.
41	SET1	I		**Analog current sense adjustment Pin for CH1;**
20	SET2	I		**Analog current sense adjustment Pin for CH2;**
44	IOUTMON1	O	PD	**Output current monitor output 1;** Monitor pin that produces a linear function of I_{OUT} as a voltage.
17	IOUTMON2	O	PD	**Output current monitor output 2;** Monitor pin that produces a linear function of I_{OUT} as a voltage.
SPI				
30	SI	I	PD	**Serial data in;** Digital input 5 V or 3.3 V.
29	SCLK	I	PD	**Serial clock;** Digital input 5 V or 3.3 V.
28	CSN	I	PU	**SPI chip select;** Digital input 5 V or 3.3 V. Active LOW.
27	SO	O		**Serial data out;** Digital output, referenced to V_{DD}.

1) O: Output, I: Input,
PD: pull-down circuit integrated,
PU: pull-up circuit integrated

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1)]
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V_{VIN}	-0.3	–	60	V	–	P_4.1.1
VDD Digital supply voltage	V_{VDD}	-0.3	–	6	V	–	P_4.1.2
IVCC Internal Linear Voltage Regulator Output voltage	V_{IVCC}	-0.3	–	6	V	–	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V_{IVCC_EXT}	-0.3	–	6	V	–	P_4.1.4
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	$V_{LSGD1,2-PGND1,2}$	-0.3	–	5.5	V	–	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	$V_{HSGD1,2-SWN1,2}$	-0.3	–	5.5	V	–	P_4.1.55
SWN1, SWN2 switching node voltage	$V_{SWN1,2}$	-1	–	60	V	–	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Boostrap voltage	$V_{BST1,2-SWN1,2}$	-0.3	–	6	V	–	P_4.1.7
BST1, BST2 Boostrap voltage related to GND	$V_{BST1,2}$	-0.3	–	65	V	–	P_4.1.8
SWCS1,2 Switch Current Sense Input voltages	$V_{SWCS1,2}$	-0.3	–	0.3	V	–	P_4.1.42
SGND1,2 Switch Current Sense GND voltages	$V_{SGND1,2}$	-0.3	–	0.3	V	–	P_4.1.43
SWCS1,2-SGND1,2 Switch Current Sense differential voltages	$V_{SWCS1,2-SGND1,2}$	-0.5	–	0.5	V	–	P_4.1.44
PGND1,2 Power GND voltage	$V_{PGND1,2}$	-0.3	–	0.3	V	–	P_4.1.28
High voltage Pins							
FBH1,2; FBL1,2 Feedback Error Amplifier voltages	$V_{FBH1,2;FBL1,2}$	-0.3	–	60	V	–	P_4.1.45

Table 2 Absolute Maximum Ratings[1)] (cont'd)
***T_J* = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
FBH1,2-FBL1,2 Feedback Error Amplifier differential voltages	$V_{FBH1,2-FBL1,2}$	-0.5	–	0.5	V	–	P_4.1.47
EN/INUVLO Device enable/input undervoltage lockout	$V_{EN/INUVLO}$	-0.3	–	60	V	–	P_4.1.16
Digital (I/O) Pins							
PWMI1,2 Digital Input voltages	$V_{PWMI1,2}$	-0.3	–	5.5	V	–	P_4.1.49
CSN Voltage at Chip Select pin	V_{CSN}	-0.3	–	5.5	V	–	P_4.1.18
SCLK Voltage at Serial Clock pin	V_{SCLK}	-0.3	–	5.5	V	–	P_4.1.19
SI Voltage at Serial Input pin	V_{SI}	-0.3	–	5.5	V	–	P_4.1.20
SO Voltage at Serial Output pin	V_{SO}	-0.3	–	5.5	V	–	P_4.1.21
SYNC Synchronization Input voltage	V_{SYNC}	-0.3	–	5.5	V	–	P_4.1.22
LHI Limp Home Input Voltage	V_{LHI}	-0.3	–	5.5	V	–	P_4.1.58
LHI Limp Home Input Current	I_{LHI}	-5	–	–	mA	–	P_4.1.60
Analog Pins							
VFB1,2 Loop Input voltages	$V_{VFB1,2}$	-0.3	–	5.5	V	–	P_4.1.50
SET1,2 Analog dimming Input voltage	$V_{SET1,2}$	-0.3	–	5.5	V	–	P_4.1.56
COMP1,2 Compensation Input voltages	$V_{COMP1,2}$	-0.3	–	3.6	V	–	P_4.1.52
SOFT_START1,2 Softstart Voltages	$V_{SOFT\_START1,2}$	-0.3	–	3.6	V	–	P_4.1.53
FREQ Voltage at frequency selection pin	V_{FREQ}	-0.3	–	3.6	V	–	P_4.1.32
IOUTMON1,2 Voltages at output monitor pins	$V_{IOUTMON1,2}$	-0.3	–	5.5	V	–	P_4.1.59
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.35
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.36
ESD Susceptibility							

Table 2 Absolute Maximum Ratings[1] (cont'd)
T_J = -40°C to +150°C; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2]	P_4.1.37
ESD Resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[3]	P_4.1.38
ESD Resistivity of corner Pins to GND	V_{ESD,CDM_corner}	-750	–	750	V	CDM[3]	P_4.1.39

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	V_{VIN}	4.5	–	40	V	1)	P_4.2.1
Device Nominal Supply Voltage Range	V_{VIN}	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	V_{POW}	4.5	–	55	V	1)	P_4.2.5
Digital Supply Voltage	V_{DD}	3	–	5.5	V	–	P_4.2.3
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.9	–	K/W	1) 2)	P_4.3.1
Junction to Ambient	R_{thJA}	–	25	–	K/W	3) 2s2p	P_4.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). Ta = 25°C; The IC is dissipating 1 W.

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu). A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. Ta = 25°C; The IC is dissipating 1 W.

5 Power Supply

The TLD5501-2QV is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC_EXT is the supply for the low side driver stages. This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high side driver stages. If no external voltage is available this pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

The supply pins VIN, VDD and IVCC_EXT have undervoltage detections.

Undervoltage on VDD supply voltage prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC_EXT or IVCC voltages forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND .

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

Figure 4 shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC_EXT.

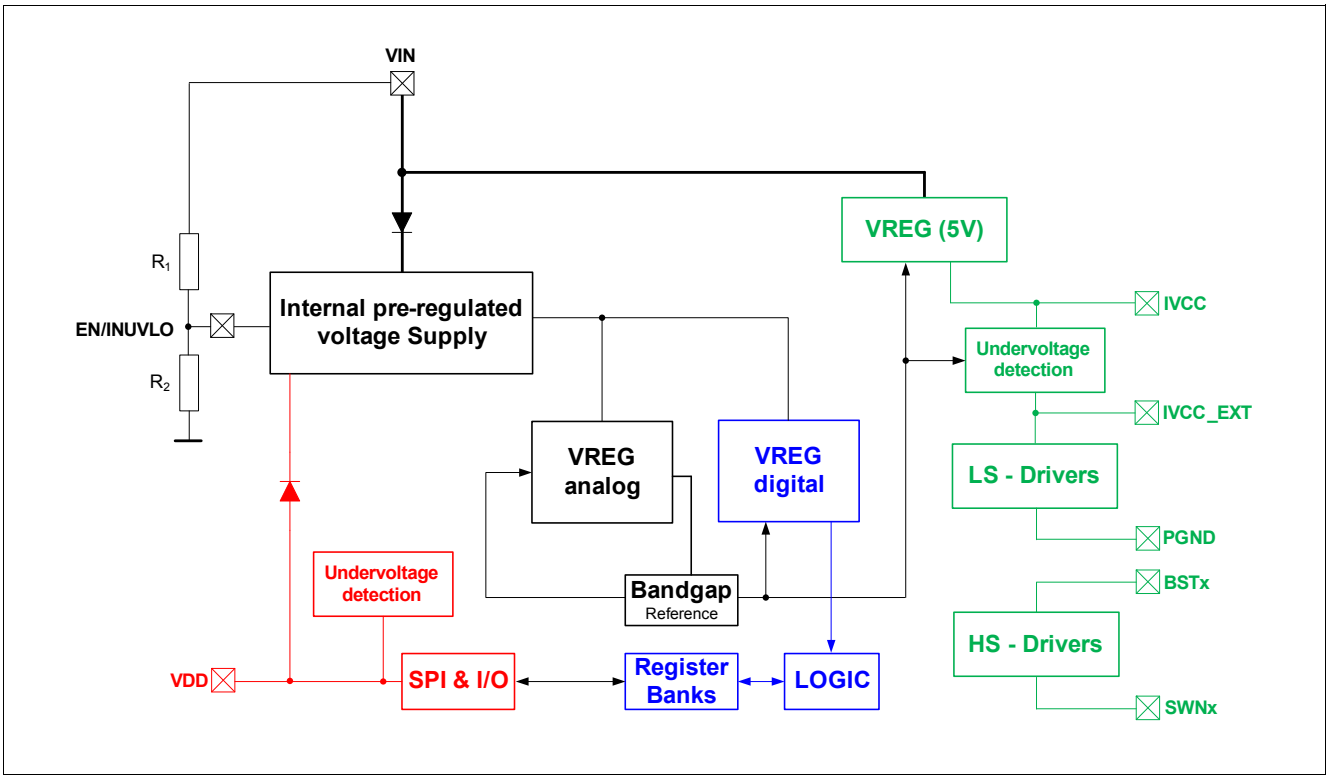


Figure 4 Power Supply Concept Drawing

Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold is fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a µC-port as shown in (B) (C).

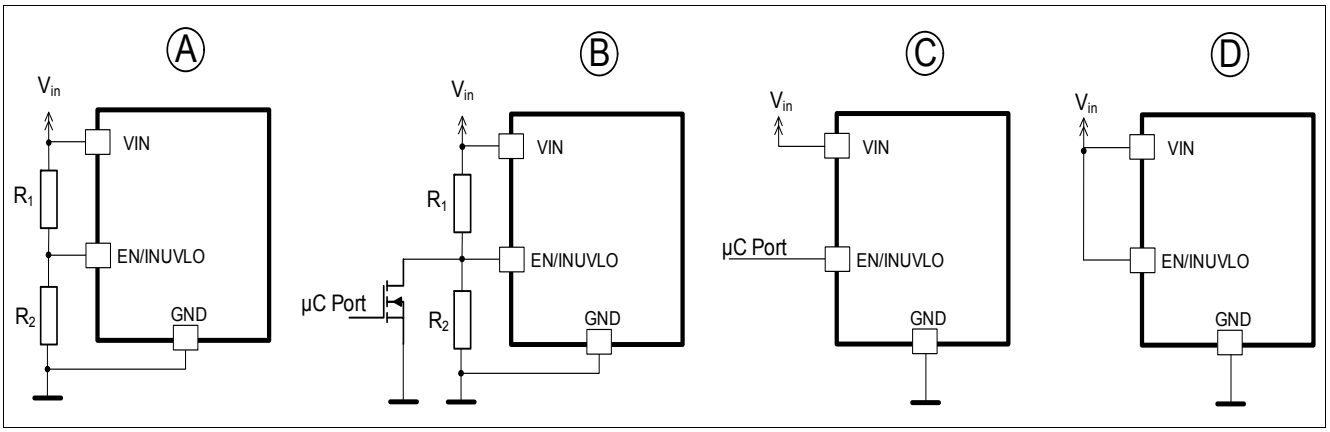


Figure 5 Usage of EN/INUVLO pin in different applications

5.1 Different Power States

TLD5501-2QV has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level
- VDD level
- LHI level
- `DVCCTRL.IDLE` bit state

The state diagram including the possible transitions is shown in **Figure 6**.

The Power-up condition is entered when the supply voltage V_{VIN} exceed its minimum supply voltage threshold $V_{VIN(ON)}$.

SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN , VDD, IVCC, and IVCC_EXT. The current consumption is low. Refer to parameters: $I_{VDD(SLEEP)}$, and $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE}.

IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter I_{VDD} (P_5.3.4). The internal voltage regulator is working. Not all diagnosis functions are available (refer to **Chapter 10** for additional informations). In this state there is no switching activity, independently from the supply voltages V_{IN}, V_{DD}, IVCC and IVCC_EXT. When V_{DD} is available, the SPI registers are working and SPI communication is possible.

Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the µC. For detailed info, refer to **Chapter 8**.

When Limp Home state is entered, SPI registers are reset to their default values. In order to regulate the output current/voltage, it is necessary that V_{IN} and IVCC_EXT are present and above their undervoltage threshold. If also VDD is above its undervoltage threshold, SPI communication is possible but only in read mode.

ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI1,2 = HIGH or `LOOPCTRL_CH1,2.PWM_1,2` = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level $V_{BST1,2}$ - $V_{SWN1,2}$ needs to be above the threshold $V_{BST1,2}$ - $V_{SWN1,2\_UVth}$. In order to recharge the bootstrap capacitor, sporadic switching activity could also be observed when PWMI1,2 = LOW and LOOPCTRL_CH1,2.PWM_1,2 =

LOW. In ACTIVE state the device current consumption via V_{IN} and V_{DD} is dependent on the external MOSFET used and the switching frequency f_{SW}.

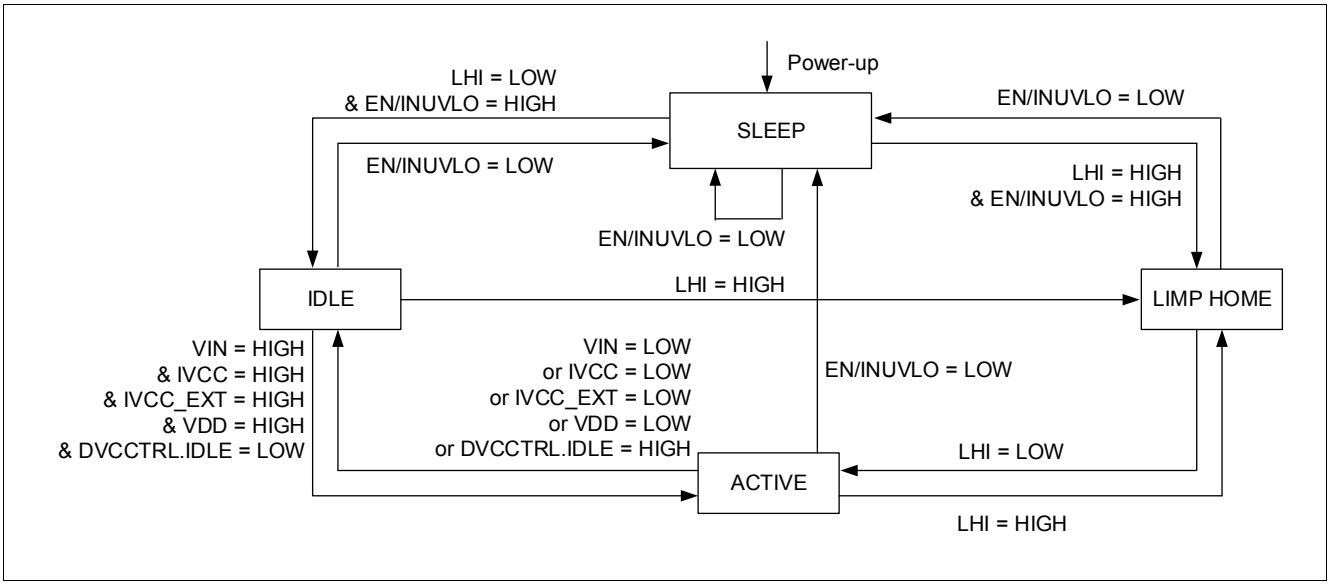


Figure 6 Simplified State Diagram

5.2 Different Possibilities to RESET the device

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (`TER`) is set to HIGH.

Under Voltage Reset:

EN/INUVLO: When EN/INUVLO is below $V_{EN/INUVLOth}$ (P_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

VDD: When V_{VDD} is below $V_{VDD(UV)}$ (P_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

Reset via SPI command:

There is a command (`DVCCTRL.SWRST` = HIGH) available to RESET all writeable registers to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when `LOOPCTRL_CH1,2.ENCAL_CH1,2` = HIGH, is not reset by the SWRST.

Reset via Limp Home:

When Limp Home state is detected the registers are reset to the default values.

5.3 Electrical Characteristics

Table 5 EC Power Supply

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply V_{IN}							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	V_{IN} increasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA;	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	V_{IN} decreasing; $V_{EN/INUVLO}$ = HIGH; V_{DD} = 5 V; IVCC = IVCC_EXT = 10 mA;	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	6.2	9	mA	[1)]ACTIVE mode; $V_{PWMI1,2}$ = 0 V;	P_5.3.2
V_{IN} Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT} = 0 V;	P_5.3.3
Digital Power Supply V_{DD}							
Digital supply current	I_{VDD}	–	–	0.5	mA	V_{IN} = 13.5 V; f_{SCLK} = 0 Hz; $V_{PWMI1,2}$ = 0 V; V_{EN} = V_{CSN} = V_{DD} = 5 V;	P_5.3.4
Digital Supply Sleep mode current	$I_{VDD(SLEEP)}$	–	–	1.5	µA	$V_{EN/INUVLO}$ = 0 V; V_{CSN} = V_{DD} = 5 V; V_{IN} = 13.5 V; V_{IVCC} = V_{IVCC_EXT} = 0 V;	P_5.3.5
Undervoltage shutdown threshold voltage	$V_{VDD(UV)}$	1	–	3	V	V_{CSN} = V_{DD}; V_{SI} = V_{SCLK} = 0 V; SO from LOW to HIGH impedance;	P_5.3.6
EN/INUVLO Pin characteristics							
Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.6	1.75	1.9	V	–	P_5.3.7
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	[1)]	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	µA	$V_{EN/INUVLO}$ = 0.8 V;	P_5.3.9

Table 5 EC Power Supply (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	µA	$V_{EN/INUVLO}$ = 2 V;	P_5.3.10
LHI Pin characteristics							
LOW level	$V_{LHI(L)}$	0	-	0.8	V	–	P_5.3.16
HIGH level	$V_{LHI(H)}$	2.0	-	5.5	V	–	P_5.3.17
L-Input pull-down current	$I_{LHI(L)}$	6	12	18	µA	V_{LHI} = 0.8 V;	P_5.3.18
H-Input pull-down current	$I_{LHI(H)}$	15	30	45	µA	V_{LHI} = 2.0 V;	P_5.3.19
Timings							
SLEEP mode to ACTIVE time	t_{ACTIVE}	–	–	0.7	ms	1) $V_{IVCC} = V_{IVCC\_EXT}$; C_{IVCC} = 10 µF; V_{IN} = 13.5 V; V_{DD} = 5 V;	P_5.3.11

1) Not subject to production test, specified by design.

6 Regulator Description

The TLD5501-2QV includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to **Chapter 6.5**).

In deep buck applications, due to duty cycle limitations (D_{BUCK_MIN}) the device will enter pulse skipping mode in order to keep regulating the average output current, the ouptut ripple may increase.

The minimum duty cycle is dependent by the f_{sw}.

6.1 Regulator Diagram Description

An analog current control loop (A5, A4 with complessive gain = $IFBx_{gm}$) connected to the sensing pins FBL1,2, FBH1,2 regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (R_{COMP}, C_{COMP}) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the R_{SWCS} resistor.

R_{SWCS} is used also to limit the maximum external switches / inductor current.

If the Voltage across R_{SWCS} exceeds its overcurrent threshold ($V_{SWCS1,2\_buck}$) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC_CHx) provides a PWM signal to two internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs. Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in **Figure 7** shows a typical constant current application. The voltage across R_{FB} sets the output current.

The output current is fixed via the SPI parameter (`LEDCURRADIM_CH1,2.ADIMVAL_CH1,2` = 11110000_B = default at 100%) plus an offset trimming (`LEDCURRCAL_CH1,2.CALIBVAL_CH1,2` = 0000_B = default in the middle of the range). Refer to **Chapter 8.1** for more details.

Regulator Description

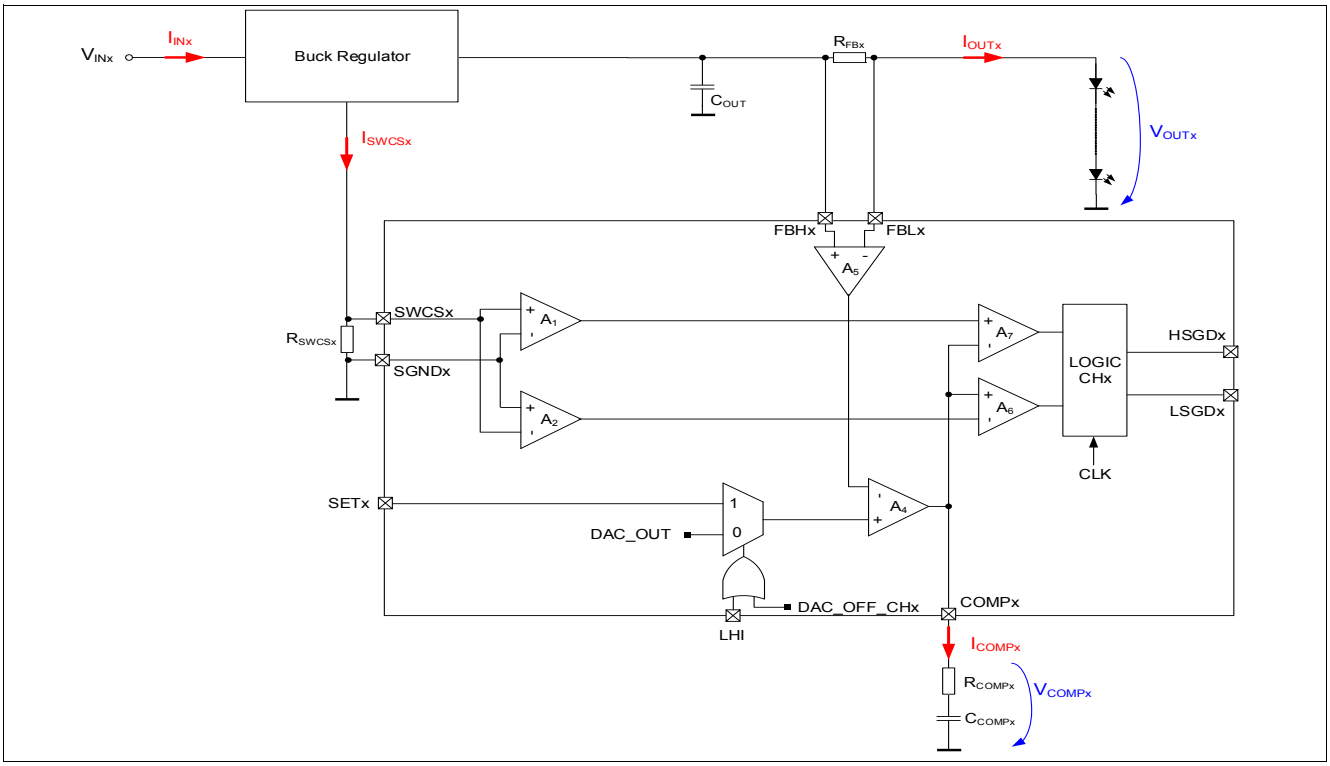


Figure 7 Regulator Block Diagram (similar for both Channels) - TLD5501-2QV

6.2 Adjustable Soft Start Ramp

The soft start routine limits the current through the inductor and the external MOSFET switches during initialization to minimize potential overshoots at the output.

The soft start routine is applied:

- At first turn on (first PWM rise after EN = High)
- After Output Short to GND detection
- After channel stop via low analog dimming value (see **Chapter 8** for details)

The soft start rising edge gradually increases the current of the inductor (L_{OUT}) over $t_{SOFT\_START1,2}$ by clamping the COMP1,2 voltage . The soft start ramp is defined by a capacitor placed at the SOFT_START1,2 pin.

Selection of the SOFT_START1,2 capacitor ($C_{SOFT\_START1,2}$) can be done according to the approximate formula described in **Equation (6.1)**:

$$t_{SOFT\_START\,1,2} = \frac{0.9V}{I_{SOFT\_START\,1,2(PU)}} \cdot C_{SOFT\_START\,1,2} \tag{6.1}$$

The SOFT START1,2 pins are also used to implement a fault mask and wait-before-retry time, on rising and falling edge respectively, see **Figure 8** and chapter **Chapter 10.2** for details.

If a short on the output is detected, a pull-down current source $I_{SOFT\_START1,2\_PD}$ (P_6.4.59) is activated. This current brings down the $V_{SOFT\_START1,2}$ until $V_{SOFT\_START1,2\_RESET}$ (P_6.4.61) is reached, then the pull-up current source $I_{SOFT\_START1,2\_PU}$ (P_6.4.58) turns on again. If the fault condition hasn't been removed until $V_{SOFT\_START1,2\_LOFF}$ (P_6.4.60) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.

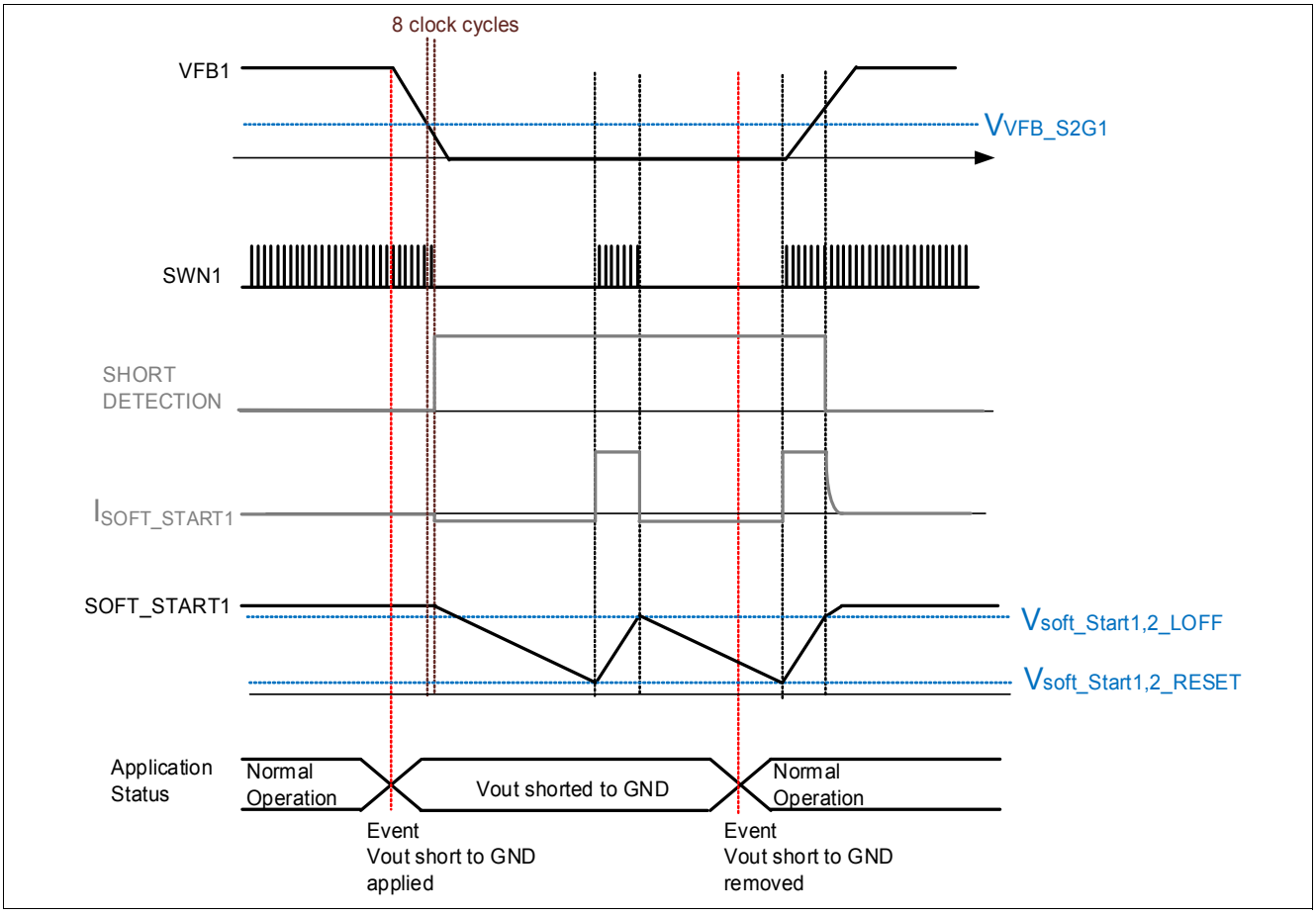


Figure 8 Soft Start timing diagram on a short to ground detected by the VFB1 pin

6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter **Chapter 11.2**. Select the switching frequency with an external resistor according to the graph in **Figure 9** or the following approximate formulas.

$$f_{SW}[kHz] = 5375 * (R_{FREQ}[k\Omega])^{-0.8} \quad (6.2)$$

$$R_{FREQ}[k\Omega] = 46023 * (f_{SW}[kHz])^{-1.25} \quad (6.3)$$

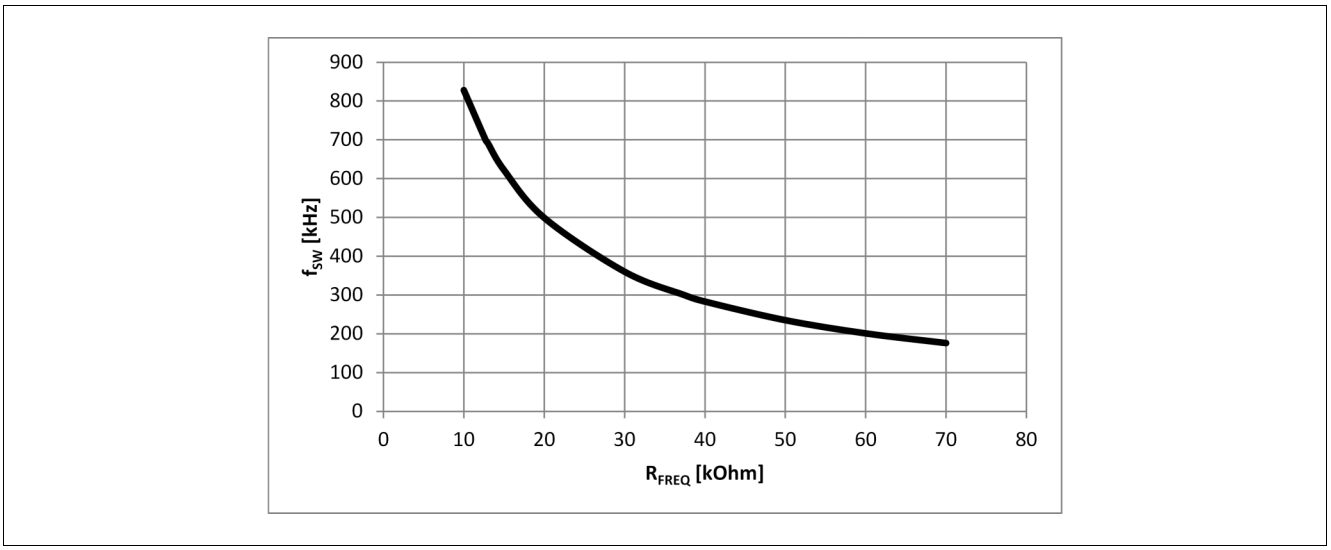


Figure 9 Switching Frequency f_{SW} versus Frequency Select Resistor to GND R_{FREQ}

6.4 Flexible current sense

The flexible current sense implementation enables highside and lowside current sensing.

The **Figure 10** displays the application examples for the highside and lowside current sense concept.

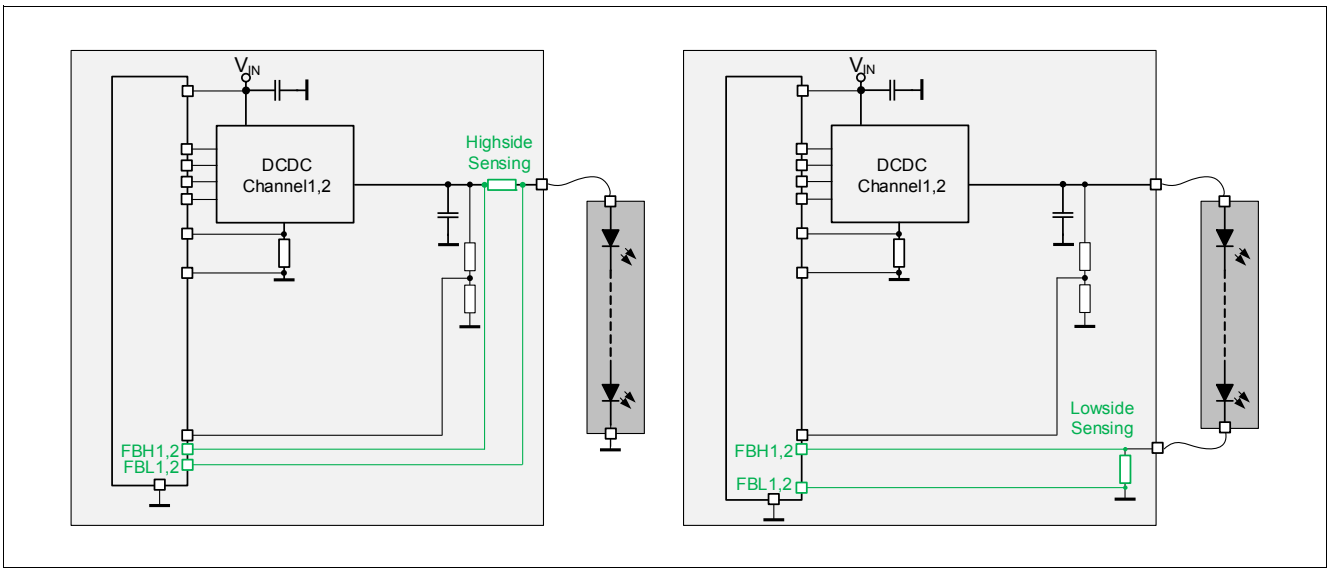


Figure 10 Highside and lowside current sensing - TLD5501-2QV

6.5 Programming Output Voltage (Constant Voltage Regulation)

For a voltage regulator, the output voltage can be set by selecting the values R_{FBx1}, R_{FBx2} and R_{FBx3} according to the following **Equation (6.4)**:

$$V_{OUT1,2} = \left(I_{FBH1,2} + \frac{V_{FBH1,2-FBL1,2}}{R_{FB21,2}} \right) \cdot R_{FB11,2} + \left(\frac{V_{FBH1,2-FBL1,2}}{R_{FB21,2}} - I_{FBL1,2} \right) \cdot R_{FB31,2} + V_{FBH1,2-FBL1,2} \quad (6.4)$$

After the output voltage is fixed via the resistor divider, the value can be changed via the Analog Dimming bits `ADIMVAL_CH1,2`.

If Analog dimming is performed, due to the variations on the I_{FBL} ($I_{FBL1,2\_HSS}$ (P_6.4.52) and $I_{FBL1,2\_LSS}$ (P_6.4.54)) current on the entire voltage spanning, a non linearity on the output voltage may be observed. To minimize this effect RFBx resistors should be properly dimensioned.

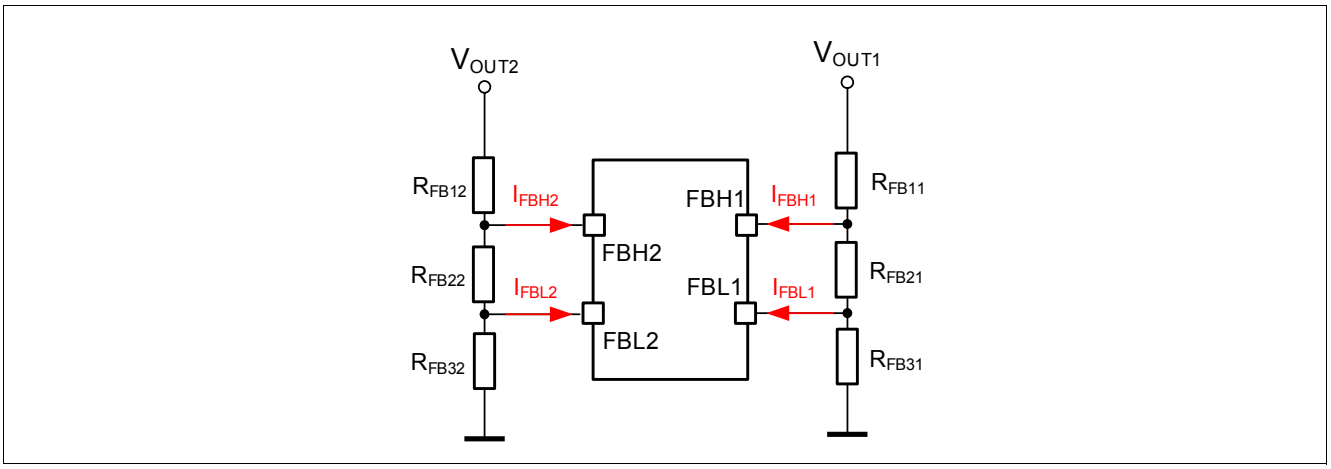


Figure 11 Programming Output Voltage (Constant Voltage Regulation)

6.6 Electrical Characteristics

Table 6 EC Regulator

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator:							
$V_{(FBH1,2-FBL1,2)}$ thresholds	$V_{(FBH1,2-FBL1,2)}$	145.5	150	154.5	mV	ADIM.ADIMVAL_CH1,2 = 11110000_B;	P_6.4.43
$V_{(FBH1,2-FBL1,2)}$ thresholds @ analog dimming 10%	$V_{(FBH1,2-FBL1,2)\_10}$	12	15	18	mV	ADIM.ADIMVAL_CH1,2 = 00011000_B; Calibration Procedure not performed	P_6.4.47
FBH1,2 Bias currents @ highside sensing setup	$I_{FBH1,2\_HSS}$	65	100	156	µA	$V_{FBL1,2}$ = 7 V; $V_{FBH1,2 - FBL1,2}$ = 150 mV;	P_6.4.51
FBL1,2 Bias currents @ highside sensing setup	$I_{FBL1,2\_HSS}$	17	30	45	µA	$V_{FBL1,2}$ = 7 V; $V_{FBH1,2 - FBL1,2}$ = 150 mV;	P_6.4.52
FBH1,2 Bias currents @ lowside sensing setup	$I_{FBH1,2\_LSS}$	-7.5	-4	-2.5	µA	$V_{FBL1,2}$ = 0 V; $V_{FBH1,2 - FBL1,2}$ = 150 mV;	P_6.4.53
FBL1,2 Bias currents @ lowside sensing setup	$I_{FBL1,2\_LSS}$	-45	-30	-20	µA	$V_{FBL1,2}$ = 0 V; $V_{FBH1,2 - FBL1,2}$ = 150 mV;	P_6.4.54
FBH-FBL High Side sensing entry threshold	$V_{FBH\_HSS\_inc}$	1.9	2	2.1	V	1) $V_{FBH1,2}$ increasing;	P_6.9.1
FBH-FBL High Side sensing exit threshold	$V_{FBH\_HSS\_dec}$	1.65	1.75	1.85	V	1) $V_{FBH1,2}$ decreasing;	P_6.9.2
OUT Current sense Amplifier g_m	$IFBx_{gm}$	–	890	–	µS	1)	P_6.4.10
Output Monitor Voltages	$V_{IOUTMON1,2}$	1.33	1.4	1.47	V	$V_{FBH1,2 - FBL1,2}$ = 150 mV;	P_6.5.1
Minimum BUCK Duty Cycle	D_{BUCK_MIN}	–	4	5.5	%	1) f_{sw} = 300 kHZ;	P_6.8.2
Maximum BUCK Duty Cycle	D_{BUCK_MAX}	90.5	92	94	%	1) f_{sw} = 300 kHZ;	P_6.5.2
Switch Peak Over Current Thresholds - BUCK	$V_{SWCS1,2\_buck}$	-60	-50	-40	mV	1)	P_10.8.25
Soft Start							
Soft Start1,2 pull up currents	$I_{Soft\_Start1,2\_PU}$	21	27	34	µA	$V_{Soft\_Start1,2}$ = 1 V;	P_6.4.58
Soft Start1,2 pull down currents	$I_{Soft\_Start1,2\_PD}$	2.1	2.7	3.4	µA	$V_{Soft\_Start1,2}$ = 1 V;	P_6.4.59

Table 6 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Soft Start1,2 Latch-OFF Thresholds	$V_{Soft\_Start1,2\_LOFF}$	1.65	1.75	1.85	V	–	P_6.4.60
Soft Start1,2 Reset Thresholds	$V_{Soft\_Start1,2\_RESET}$	0.1	0.2	0.3	V	–	P_6.4.61
Soft Start1,2 Voltage during regulation	$V_{Soft\_Start\_reg}$	1.9	2	2.1	V	[1] No Faults	P_6.9.3
Oscillator							
Switching Frequency	f_{SW}	285	300	315	kHz	T_j = 25°C; R_{FREQ}= 37.4 kΩ; ENSPREAD = LOW	P_6.4.23
SYNC Frequency	f_{SYNC}	200	–	700	kHz	–	P_6.4.24
SYNC Turn On Threshold	$V_{SYNC,ON}$	2	–	–	V	–	P_6.4.25
SYNC Turn Off Threshold	$V_{SYNC,OFF}$	–	–	0.8	V	–	P_6.4.26
SYNC High Input Current	$I_{SYNC,H}$	15	30	45	µA	V_{SYNC} = 2.0 V;	P_6.4.62
SYNC Low Input Current	$I_{SYNC,L}$	6	12	18	µA	V_{SYNC} = 0.8 V;	P_6.4.63
Gate Driver for external Switch							
Gate Driver undervoltage threshold VBST1,2-VSWN1,2_UVth	$V_{BST1,2}$- $V_{SWN1,2\_UVth}$	3.4	–	4	V	$V_{BST1,2}$ - $V_{SWN1,2}$ decreasing;	P_6.4.64
HSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)HS}$	1.4	2.3	3.7	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{source} = 100 mA;	P_6.4.28
HSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)HS}$	0.6	1.2	2.2	Ω	$V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V; I_{sink} = 100 mA;	P_6.4.29
LSGD1,2 NMOS driver on-state resistance (Gate Pull Up)	$R_{DS(ON\_PU)LS}$	1.4	2.3	3.7	Ω	V_{IVCC_EXT} = 5 V; I_{source} = 100 mA;	P_6.4.30
LSGD1,2 NMOS driver on-state resistance (Gate Pull Down)	$R_{DS(ON\_PD)LS}$	0.4	1.2	1.8	Ω	V_{IVCC_EXT} = 5 V; I_{sink} = 100 mA;	P_6.4.31
HSGD1,2 Gate Driver peak sourcing current	$I_{HSGD1,2\_SRC}$	380	–	–	mA	[1] $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 1 V to 4 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.32
HSGD1,2 Gate Driver peak sinking current	$I_{HSGD1,2\_SNK}$	410	–	–	mA	[1] $V_{HSGD1,2}$ - $V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2}$ - $V_{SWN1,2}$ = 5 V	P_6.4.33

Table 6 EC Regulator (cont'd)

V_{IN} = 8 V to 36 V, T_J = -40°C to +150°C, all voltages with respect to AGND (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
LSGD1,2 Gate Driver peak sourcing current	$I_{LSGD1,2\_SRC}$	370	–	–	mA	1) $V_{LSGD1,2}$ = 1 V to 4 V; V_{IVCC_EXT} = 5 V;	P_6.4.34
LSGD1,2 Gate Driver peak sinking current	$I_{LSGD1,2\_SNK}$	550	–	–	mA	1) $V_{LSGD1,2}$ = 4 V to 1 V; V_{IVCC_EXT} = 5 V;	P_6.4.35
LSGD1,2 OFF to HSGD ON delay	$t_{LSOFF-HSON\_delay}$	15	30	40	ns	1)	P_6.4.36
HSGD1,2 OFF to LSGD ON delay	$t_{HSOFF-LSON\_delay}$	35	65	95	ns	1)	P_6.4.37

1) Not subject to production test, specified by design