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TLD5541-1

H-Bridge DC/DC Controller with SPI Interface

Infineon® LITIX™ Power Flex



Package	PG-VQFN-48-31	PG-TQFP-48-9
Marking	TLD55411QV	TLD55411QU
Sales Name	TLD5541-1QV	TLD5541-1QU

1 Overview

Features

- Single Inductor high power Buck-Boost controller
- Wide LED forward voltage Range (2 V up to 55 V)
- Wide VIN Range (IC 4.5 V to 40 V, Power 4.5 V to 55 V)
- Switching Frequency Range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum Efficiency in every condition (up to 96%)
- Constant Current (LED) and Constant Voltage Regulation
- Drives Multiple Load with a single IC thanks to the Fast Output Discharge operation
- Limp Home Function (Fail Safe Mode)
- EMC optimized device: Features an auto Spread Spectrum
- LED and Input current sense with dedicated monitor Outputs
- Advanced protection features for device and load
- Enhanced Dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48-31 or PG-TQFP-48-9 package
- Automotive AEC Qualified

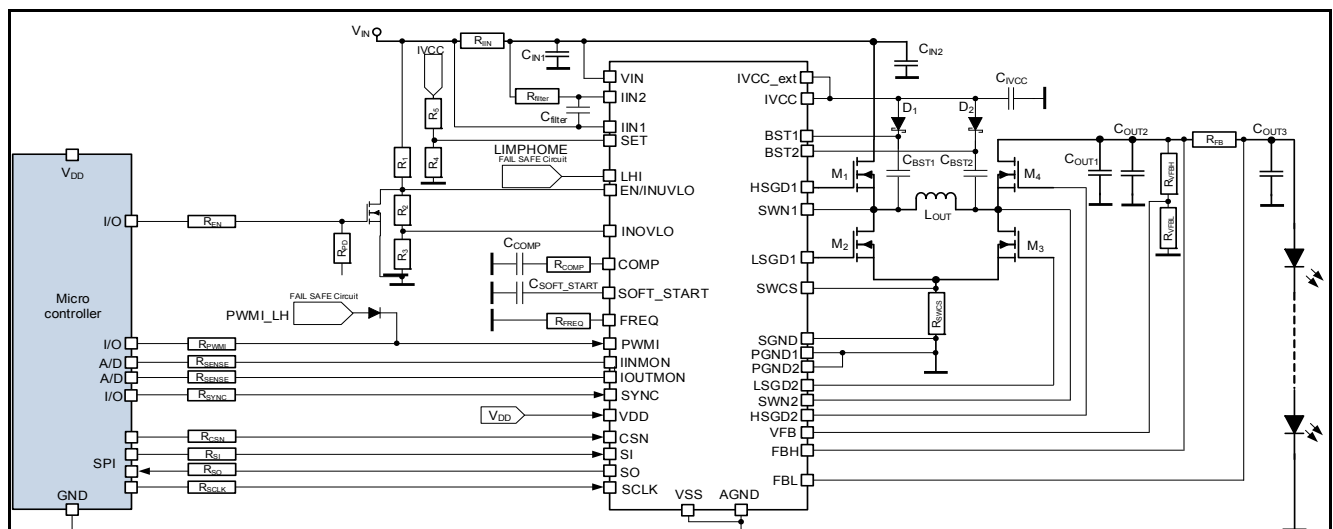
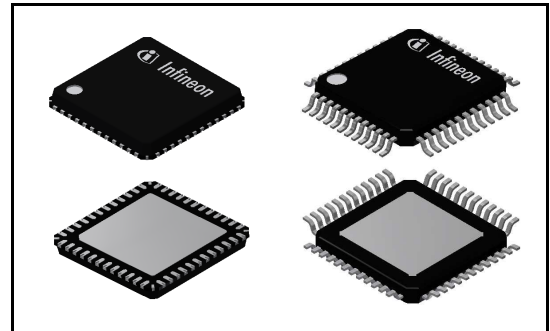


Figure 1 Application Drawing - TLD5541-1 as current regulator

Overview

Description

The TLD5541-1 is a synchronous MOSFET H-Bridge DC/DC controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5541-1 offers both analog and digital (PWM) dimming. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programmable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5541-1 is suitable for use in the harsh automotive environment.

Table 1 Product Summary

Power Stage input voltage range	V_{POW}	4.5 V ... 55 V
Device Input supply voltage range	V_{VIN}	4.5 V ... 40 V
Maximum output voltage (depending by the application conditions)	$V_{OUT(max)}$	55 V as LED Driver Boost Mode 50 V as LED Driver Buck Mode 50 V as Voltage regulator
Switching Frequency range	f_{SW}	200 kHz... 700 kHz
Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Up)	$R_{DS(ON_PU)}$	2.3 Ω
Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Down)	$R_{DS(ON_PD)}$	1.2 Ω
SPI clock frequency	$f_{SCLK(MAX)}$	5 MHz

Protective Functions

- Over load protection of external MOSFETs
- Shorted load, open load, output overvoltage protection
- Input overvoltage and undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in ON-state
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide I_{LED} and I_{IN} information

Limp Home Function

- Limp Home activation via LHI pin

Applications

- Especially designed for driving high power LEDs in automotive applications
- Automotive Exterior Lighting: full LED headlamp assemblies (Low Beam, High Beam, Matrix Beam, Pixel Light)
- General purpose current/voltage controlled DC/DC LED driver

Block Diagram

2 Block Diagram

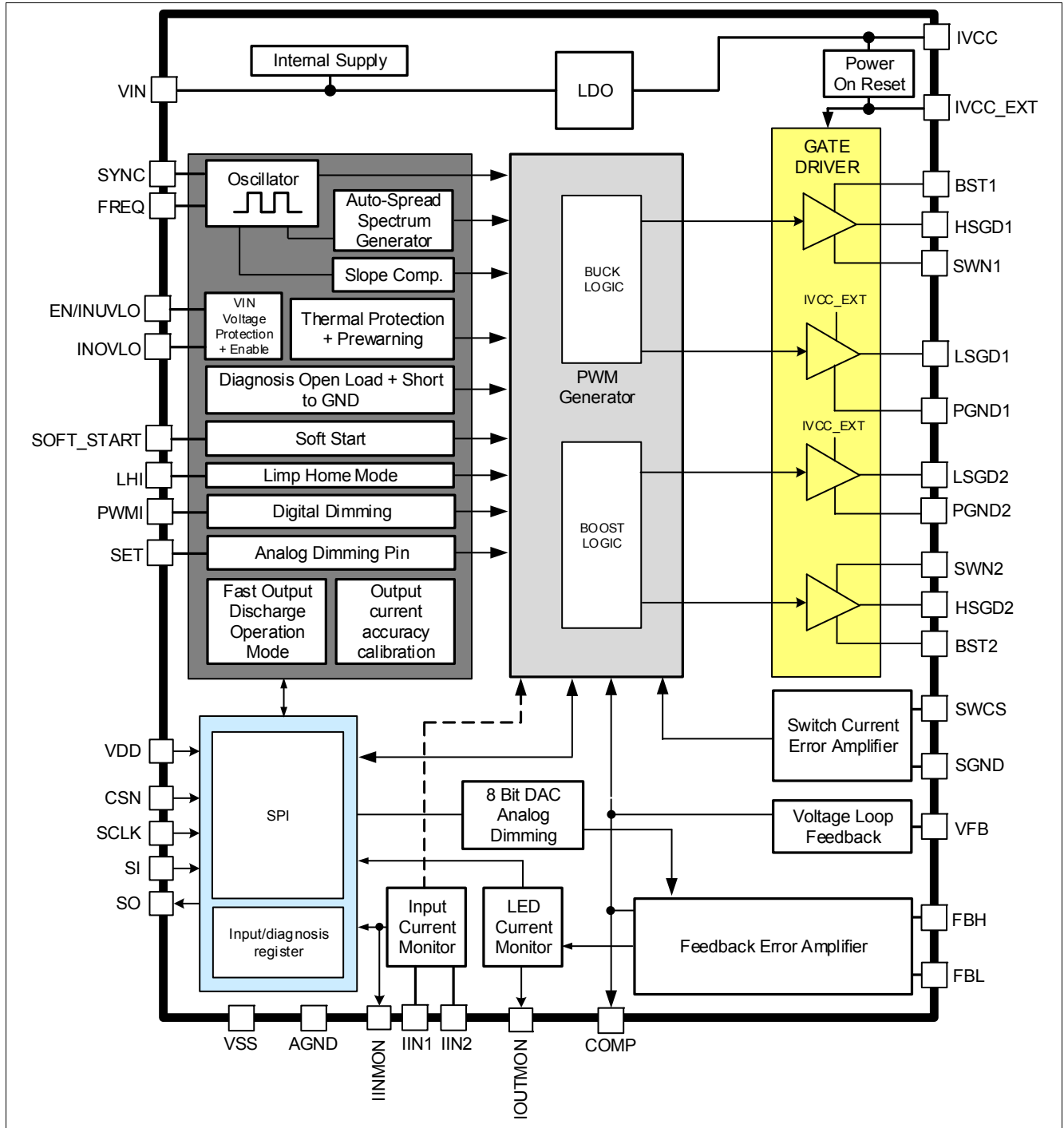


Figure 2 Block Diagram - TLD5541-1

Pin Configuration

3 Pin Configuration

3.1 Pin Assignment

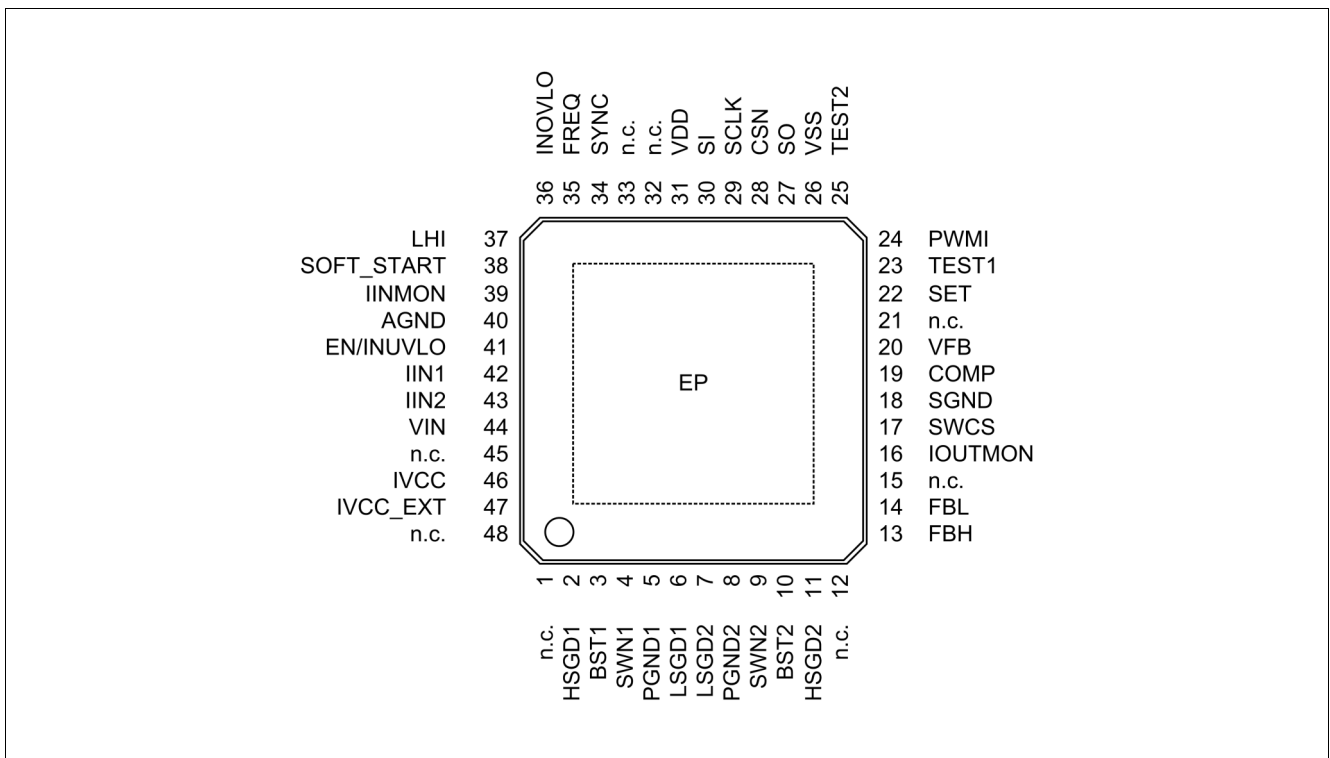


Figure 3 Pin Configuration - TLD5541-1

Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O ¹⁾		Function
Power Supply				
1, 12, 15, 21, 32, 33, 45, 48	n.c.	-		Not connected, tie to AGND on the Layout;
44	VIN	-		Power Supply Voltage; Supply for internal biasing.
31	VDD	-		Digital GPIO Supply Voltage; Connect to reverse voltage protected 5 V or 3.3 V supply.
47	IVCC_EXT	I	PD	External LDO input; Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.
5, 8	PGND1, 2	-		Power Ground; Ground for power potential. Connect externally close to the chip.
26	VSS	-		Digital GPIO Ground; Ground for GPIO pins.
40	AGND	-		Analog Ground; Ground Reference
-	EP	-		Exposed Pad; Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).
Gate Driver Stages				
2	HSGD1	O		Highside Gate Driver Output 1; Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET.
11	HSGD2	O		Highside Gate Driver Output 2; Drives the top n-channel MOSFET with a voltage equal to V_{IVCC_EXT} superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET.
6	LSGD1	O		Lowside Gate Driver Output 1; Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT} . Connect to gate of external switching MOSFET.
7	LSGD2	O		Lowside Gate Driver Output 2; Drives the lowside n-channel MOSFET between GND and V_{IVCC_EXT} . Connect to gate of external switching MOSFET.
4	SWN1	IO		Switch Node 1; SWN1 pin swings from a diode voltage drop below ground up to V_{IN} .
9	SWN2	IO		Switch Node 2; SWN2 pin swings from ground up to a diode voltage drop above V_{OUT} .

Pin Configuration

Pin	Symbol	I/O ¹⁾	Function
46	IVCC	O	Internal LDO output; Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.

Inputs and Outputs

37	LHI	I	PD	Limp Home Input Pin; Used to enter in Limp Home state during Fail Safe condition.
23	TEST1	-		Test Pin; Used for Infineon end of line test, connect to GND in application.
25	TEST2	-		Test Pin; Used for Infineon end of line test, connect to GND in application.
41	EN/INUVLO	I	PD	Enable/Input Under Voltage Lock Out; Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open.
35	FREQ	I		Frequency Select Input; Connect external resistor to GND to set frequency.
34	SYNC	I	PD	Synchronization Input; Apply external clock signal for synchronization.
24	PWMI	I	PD	Control Input; Digital input 5 V or 3.3 V.
13	FBH	I		Output current Feedback Positive; Non inverting Input (+).
14	FBL	I		Output current Feedback Negative; Inverting Input (-).
3	BST1	IO		Bootstrap capacitor; Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.
10	BST2	IO		Bootstrap capacitor; Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.
17	SWCS	I		Current Sense Input; Inductor current measurement - Non Inverting Input (+).
18	SGND	I		Current Sense Ground; Inductor current sense - Inverting Input (-). Route as Differential net with SWCS on the Layout.
42	IIN1	I		Input Current Monitor Positive; Non Inverting Input (+), connect to VIN if input current monitor is not needed.
43	IIN2	I		Input Current Monitor Negative; Inverting Input (-), connect to VIN if input current monitor is not needed.
19	COMP	O		Compensation Network Pin; Connect R and C network to pin for stability phase margin adjustment.

Pin Configuration

Pin	Symbol	I/O ¹⁾	Function
38	SOFT_START	O	Softstart configuration Pin; Connect a capacitor C_{SOFT_START} to GND to fix a soft start ramp default time.
36	INOVLO	I	Input Overvoltage Protection Pin; Define an upper voltage threshold and switches OFF the device in case of overvoltages on the VIN supply. Must not be left open.
20	VFB	I	Voltage Loop Feedback Pin; VFB is intended to set output protection functions.
22	SET	I	Analog current sense adjustment Pin;
39	IINMON	O	Input current monitor output; Monitor pin that produces a voltage that is 20 times the voltage $V_{IIN1-IIN2}$. IINMON will be equal 1 V when $V_{IIN1}-V_{IIN2} = 50$ mV.
16	IOUTMON	O	Output current monitor output; Monitor pin that produces a voltage that is 200 mV + 8 times the voltage $V_{FBH-FBL}$. IOUTMON will be equal 1.4 V when $V_{FBH-FBL} = 150$ mV.

SPI

30	SI	I	PD	Serial data in; Digital input 5 V or 3.3 V.
29	SCLK	I	PD	Serial clock; Digital input 5 V or 3.3 V.
28	CSN	I	PU	SPI chip select; Digital input 5 V or 3.3 V. Active LOW.
27	SO	O		Serial data out; Digital output, referenced to V_{DD} .

- 1) O: Output, I: Input,
PD: pull-down circuit integrated,
PU: pull-up circuit integrated

General Product Characteristics

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings¹⁾
 $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
VIN Supply Input	V_{VIN}	-0.3	-	60	V	-	P_4.1.1
VDD Digital supply voltage	V_{VDD}	-0.3	-	6	V	-	P_4.1.2
IVCC Internal Linear Voltage Regulator Output voltage	V_{IVCC}	-0.3	-	6	V	-	P_4.1.3
IVCC_EXT External Linear Voltage Regulator Input voltage	V_{IVCC_EXT}	-0.3	-	6	V	-	P_4.1.4
Gate Driver Stages							
LSGD1,2 - PGND1,2 Lowside Gatedriver voltage	$V_{LSGD1,2-}$ PGND1,2	-0.3	-	5.5	V	-	P_4.1.54
HSGD1,2 - SWN1,2 Highside Gatedriver voltage	$V_{HSGD1,2-}$ SWN1,2	-0.3	-	5.5	V	-	P_4.1.55
SWN1, SWN2 switching node voltage	$V_{SWN1,2}$	-1	-	60	V	-	P_4.1.6
(BST1-SWN1), (BST2-SWN2) Bootstrap voltage	$V_{BST1,2-}$ SWN1,2	-0.3	-	6	V	-	P_4.1.7
BST1, BST2 Bootstrap voltage related to GND	$V_{BST1,2}$	-0.3	-	65	V	-	P_4.1.8
SWCS Switch Current Sense Input voltage	V_{SWCS}	-0.3	-	0.3	V	-	P_4.1.9
SGND Switch Current Sense GND voltage	V_{SGND}	-0.3	-	0.3	V	-	P_4.1.10
SWCS-SGND Switch Current Sense differential voltage	V_{SWCS-} SGND	-0.5	-	0.5	V	-	P_4.1.11
PGND1,2 Power GND voltage	$V_{PGND1,2}$	-0.3	-	0.3	V	-	P_4.1.28
High voltage Pins							
IIN1, IIN2 Input Current monitor voltage	$V_{IIN1,2}$	-0.3	-	60	V	-	P_4.1.12

General Product Characteristics

Table 2 Absolute Maximum Ratings¹⁾ (cont'd)
 $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IIN1-IIN2 Input Current monitor differential voltage	$V_{IIN1-IIN2}$	-0.5	-	0.5	V	-	P_4.1.13
FBH, FBL Feedback Error Amplifier voltage	$V_{FBH, FBL}$	-0.3	-	60	V	-	P_4.1.14
FBH-FBL Feedback Error Amplifier differential voltage	$V_{FBH-FBL}$	-0.5	-	0.5	V	-	P_4.1.15
EN/INUVLO Device enable/input undervoltage lockout	$V_{EN/INUVLO}$	-0.3	-	60	V	-	P_4.1.16

Digital (I/O) Pins

PWMI Digital Input voltage	V_{PWMI}	-0.3	-	5.5	V	-	P_4.1.17
CSN Voltage at Chip Select pin	V_{CSN}	-0.3	-	5.5	V	-	P_4.1.18
SCLK Voltage at Serial Clock pin	V_{SCLK}	-0.3	-	5.5	V	-	P_4.1.19
SI Voltage at Serial Input pin	V_{SI}	-0.3	-	5.5	V	-	P_4.1.20
SO Voltage at Serial Output pin	V_{SO}	-0.3	-	5.5	V	-	P_4.1.21
SYNC Synchronization Input voltage	V_{SYNC}	-0.3	-	5.5	V	-	P_4.1.22
LHI Limp Home Input Voltage	V_{LHI}	-0.3	-	5.5	V	-	P_4.1.58

Analog Pins

VFB Loop Input voltage	V_{VFB}	-0.3	-	5.5	V	-	P_4.1.25
INOVLO Input overvoltage lockout	V_{INOVLO}	-0.3	-	5.5	V	-	P_4.1.26
SET Analog dimming Input voltage	V_{SET}	-0.3	-	5.5	V	-	P_4.1.29
COMP Compensation Input voltage	V_{COMP}	-0.3	-	3.6	V	-	P_4.1.30
SOFT_START Softstart Voltage	V_{SOFT_STAR}	-0.3	-	3.6	V	-	P_4.1.31
FREQ Voltage at frequency selection pin	V_{FREQ}	-0.3	-	3.6	V	-	P_4.1.32

General Product Characteristics

Table 2 Absolute Maximum Ratings¹⁾ (cont'd)
 $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; all voltages with respect to AGND, (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IINMON Voltage at input monitor pin	V_{IINMON}	-0.3	–	3.6	V	–	P_4.1.33
IOUTMON Voltage at output monitor pin	$V_{IOUTMON}$	-0.3	–	5.5	V	–	P_4.1.34

Temperatures

Junction Temperature	T_J	-40	–	150	$^{\circ}\text{C}$	–	P_4.1.35
Storage Temperature	T_{stg}	-55	–	150	$^{\circ}\text{C}$	–	P_4.1.36

ESD Susceptibility

ESD Resistivity of all Pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM ²⁾	P_4.1.37
ESD Resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM ³⁾	P_4.1.38
ESD Resistivity of corner Pins to GND	V_{ESD,CDM_corner}	-750	–	750	V	CDM ³⁾	P_4.1.39

- 1) Not subject to production test, specified by design.
- 2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 k Ω , 100 pF)
- 3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Device Extended Supply Voltage Range	V_{VIN}	4.5	–	40	V	1)	P_4.2.1
Device Nominal Supply Voltage Range	V_{VIN}	8	–	36	V	–	P_4.2.2
Power Stage Voltage Range	V_{POW}	4.5	–	55	V	1)	P_4.2.5
Digital Supply Voltage	V_{DD}	3	–	5.5	V	–	P_4.2.3
Junction Temperature	T_J	-40	–	150	$^{\circ}\text{C}$	–	P_4.2.4

- 1) Not subject to production test, specified by design.

General Product Characteristics

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

Table 4

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	0.9	–	K/W	^{1) 2)}	P_4.3.1
Junction to Ambient	R_{thJA}	–	25	–	K/W	³⁾ 2s2p	P_4.3.2

- 1) Not subject to production test, specified by design.
- 2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). $T_a = 25^\circ\text{C}$; The IC is dissipating 1 W.
- 3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 μm Cu) and 2 inner copper layers (2 x 35 μm Cu). A thermal via (diameter = 0.3 mm and 25 μm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. $T_a = 25^\circ\text{C}$; The IC is dissipating 1 W.

Power Supply

5 Power Supply

The TLD5541-1 is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC_EXT is the supply for the low side driver stages. This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high side driver stages. If no external voltage is available this pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

The supply pins VIN, VDD and IVCC_EXT have undervoltage detections.

Undervoltage on VDD supply voltage prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC_EXT or IVCC voltages forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND (refer to [Chapter 10.3](#)).

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

Figure 4 shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC_EXT.

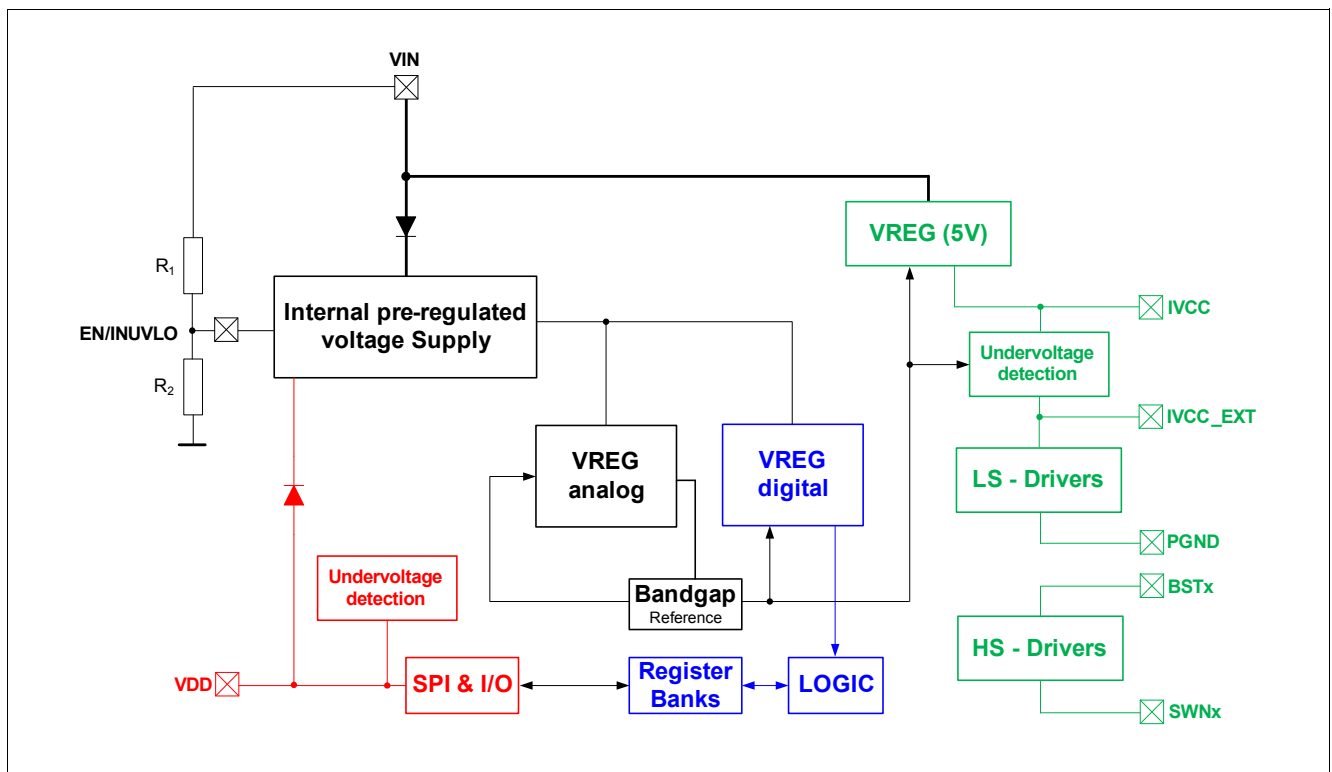


Figure 4 Power Supply Concept Drawing

Power Supply

Usage of EN/INUVLO pin in different applications

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold should be fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a μC -port as shown in (B).

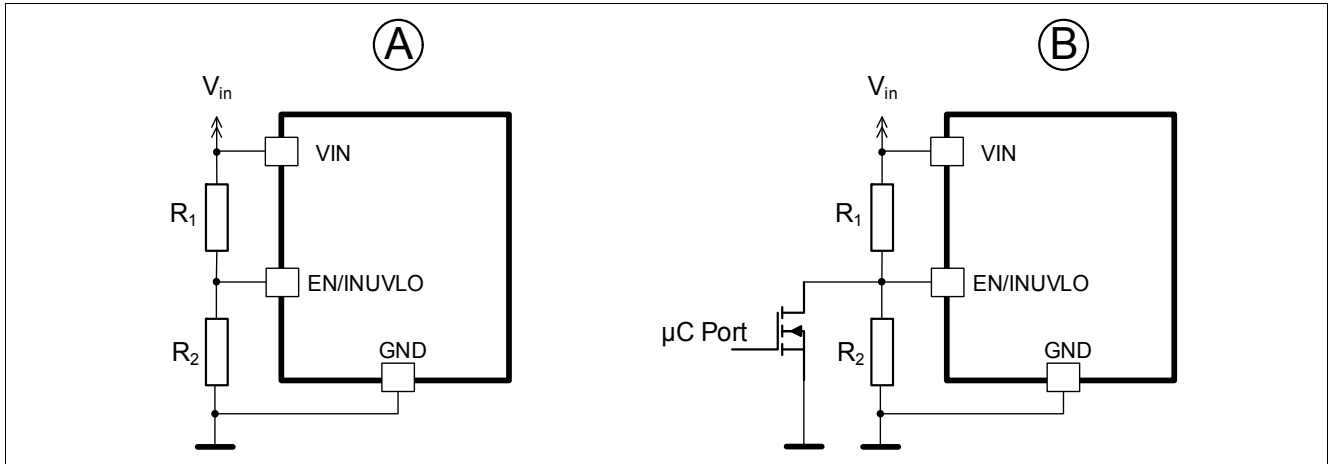


Figure 5 Usage of EN/INUVLO pin in different applications

Power Supply

5.1 Different Power States

TLD5541-1 has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level
- VDD level
- LHI level
- DVCCTRL.IDLE bit state

The state diagram including the possible transitions is shown in [Figure 6](#).

The Power-up condition is entered when the supply voltage V_{VIN} exceed its minimum supply voltage threshold $V_{VIN(ON)}$.

SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN , VDD, IVCC, and IVCC_EXT. The current consumption is low. Refer to parameters: $I_{VDD(SLEEP)}$ and $I_{VIN(SLEEP)}$.

The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE} .

IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter I_{VDD} (P_5.3.4). The internal voltage regulator is working. Not all diagnosis functions are available (refer to [Chapter 10](#) for additional informations). In this state there is no switching activity, independently from the supply voltages V_{IN} , V_{DD} , IVCC and IVCC_EXT. When V_{DD} is available, the SPI registers are working and SPI communication is possible.

Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the μC . For detailed info, refer to [Chapter 8](#).

When Limp Home state is entered, SPI registers are reset to their default values and SPI communication is possible but only in read mode (SPI registers can be read but cannot be written). In order to regulate the output current/voltage, it is necessary that V_{IN} and IVCC_EXT are present and above their undervoltage threshold.

ACTIVE

In active state the device will start switching activity to provide power at the output only when PWMI = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level $V_{BST1,2} - V_{SWN1,2}$ needs to be above the threshold

Power Supply

$V_{BST1,2} - V_{SWN1,2_UVth}$. In ACTIVE state the device current consumption via V_{IN} and V_{DD} is dependent on the external MOSFET used and the switching frequency f_{SW} .

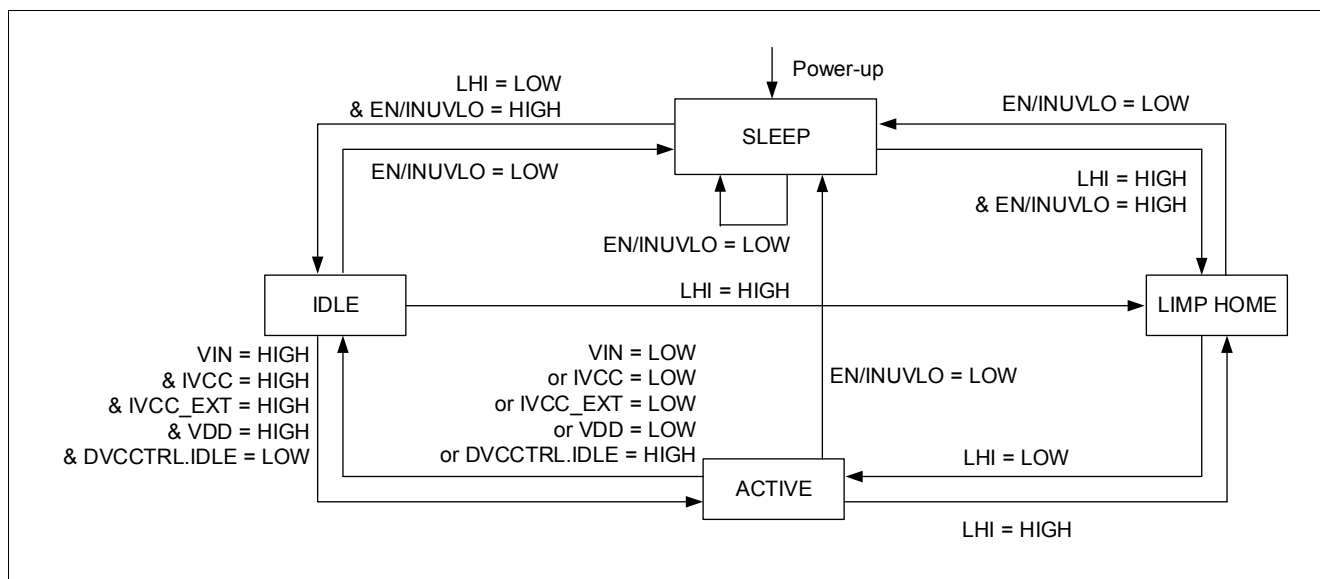


Figure 6 Simplified State Diagram

5.2 Different Possibilities to RESET the device

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (TER) is set to HIGH.

Under Voltage Reset:

EN/INUVLO: When EN/INUVLO is below $V_{EN/INUVLOth}$ (P_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

VDD: When V_{VDD} is below $V_{VDD(UV)}$ (P_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

Reset via SPI command:

There is a command (DVCCTRL.SWRST = HIGH) available to RESET all writable registers to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when DVCCTRL.ENCAL = HIGH, is not reset by the SWRST.

Reset via Limp Home:

When Limp Home state is detected the registers are reset to the default values.

Power Supply

5.3 Electrical Characteristics

Table 5 EC Power Supply

$V_{IN} = 8\text{ V to }36\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply V_{IN}							
Input Voltage Startup	$V_{VIN(ON)}$	–	–	4.7	V	V_{IN} increasing; $V_{EN/INUVLO} = \text{HIGH}$; $V_{DD} = 5\text{ V}$; $IVCC = IVCC_EXT = 10\text{ mA}$;	P_5.3.1
Input Undervoltage switch OFF	$V_{VIN(OFF)}$	–	–	4.5	V	V_{IN} decreasing; $V_{EN/INUVLO} = \text{HIGH}$; $V_{DD} = 5\text{ V}$; $IVCC = IVCC_EXT = 10\text{ mA}$;	P_5.3.14
Device operating current	$I_{VIN(ACTIVE)}$	–	4.4	6	mA	¹⁾ ACTIVE mode; $V_{PWMI} = 0\text{ V}$;	P_5.3.2
V_{IN} Sleep mode supply current	$I_{VIN(SLEEP)}$	–	–	1.5	μA	$V_{EN/INUVLO} = 0\text{ V}$; $V_{CSN} = V_{DD} = 5\text{ V}$; $V_{IN} = 13.5\text{ V}$; $V_{IVCC} = V_{IVCC_EXT} = 0\text{ V}$;	P_5.3.3

Digital Power Supply V_{DD}

Digital supply current	I_{VDD}	–	–	0.5	mA	$V_{IN} = 13.5\text{ V}$; $f_{SCLK} = 0\text{ Hz}$; $V_{PWMI} = 0\text{ V}$; $V_{EN} = V_{CSN} = V_{DD} = 5\text{ V}$;	P_5.3.4
Digital Supply Sleep mode current	$I_{VDD(SLEEP)}$	–	–	1.5	μA	$V_{EN/INUVLO} = 0\text{ V}$; $V_{CSN} = V_{DD} = 5\text{ V}$; $V_{IN} = 13.5\text{ V}$; $V_{IVCC} = V_{IVCC_EXT} = 0\text{ V}$;	P_5.3.5
Undervoltage shutdown threshold voltage	$V_{VDD(UV)}$	1	–	3	V	$V_{CSN} = V_{DD}$; $V_{SI} = V_{SCLK} = 0\text{ V}$; SO from LOW to HIGH impedance;	P_5.3.6

EN/INUVLO Pin characteristics

Input Undervoltage falling Threshold	$V_{EN/INUVLOth}$	1.6	1.75	1.9	V	–	P_5.3.7
EN/INUVLO Rising Hysteresis	$V_{EN/INUVLO(hyst)}$	–	90	–	mV	¹⁾	P_5.3.8
EN/INUVLO input Current LOW	$I_{EN/INUVLO(LOW)}$	0.45	0.89	1.34	μA	$V_{EN/INUVLO} = 0.8\text{ V}$;	P_5.3.9

Power Supply

Table 5 EC Power Supply (cont'd)

$V_{IN} = 8\text{ V to }36\text{ V}$, $T_J = -40^\circ\text{C to }+150^\circ\text{C}$, all voltages with respect to AGND; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN/INUVLO input Current HIGH	$I_{EN/INUVLO(HIGH)}$	1.1	2.2	3.3	μA	$V_{EN/INUVLO} = 2\text{ V};$	P_5.3.10

LHI Pin characteristics

LOW level	$V_{LHI(L)}$	0	-	0.8	V	-	P_5.3.16
HIGH level	$V_{LHI(H)}$	2.0	-	5.5	V	-	P_5.3.17
L-Input pull-down current	$I_{LHI(L)}$	6	12	18	μA	$V_{LHI} = 0.8\text{ V};$	P_5.3.18
H-Input pull-down current	$I_{LHI(H)}$	15	30	45	μA	$V_{LHI} = 2.0\text{ V};$	P_5.3.19

Timings

SLEEP mode to ACTIVE time	t_{ACTIVE}	-	-	0.7	ms	1) $V_{IVCC} = V_{IVCC_EXT};$ $C_{IVCC} = 10\ \mu\text{F};$ $V_{IN} = 13.5\text{ V};$ $V_{DD} = 5\text{ V};$	P_5.3.11
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1) Not subject to production test, specified by design.

6 Regulator Description

The TLD5541-1 includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to [Chapter 6.7](#)).

It is designed to control 4 gate driver outputs in a H-Bridge topology by using only one inductor and 4 external MOSFETs. This topology is able to operate in high power BOOST, BUCK-BOOST and BUCK mode applications with maximum efficiency.

The transition between the different regulation modes is done automatically by the device itself, with respect to the application boundary conditions.

The transition phase between modes is seamless.

A SPI flag provides mode feedback to the μC (refer to SPI bits `REGUSETMON` . `REGUMODFB`).

6.1 Regulator Diagram Description

The TLD5541-1 includes two analog current control inputs (IIN1, IIN2) to limit the maximum Input current (Block A1 and A7 in [Figure 7](#)).

A second analog current control loop (A5, A6 with compressive gain = $IFBx_{gm}$) connected to the sensing pins FBL, FBH regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network (R_{COMP} , C_{COMP}) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the R_{SWCS} resistor.

R_{SWCS} is used also to limit the maximum external switches / inductor current.

If the Voltage across R_{SWCS} exceeds its overcurrent threshold (V_{SWCS_buck} or V_{SWCS_boost} for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-Bridge setup . Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in [Figure 7](#) shows a typical constant current application. The voltage across R_{FB} sets the output current. R_{IN} is used to fix the maximum input current.

The output current is fixed via the SPI parameter (`LEDCURRADIM` . `ADIMVAL` = 11110000_B = default at 100%) plus an offset trimming (`LEDCURRCAL` . `CALIBVAL` = 0000_B = default in the middle of the range). Refer to [Chapter 8.1](#) for more details.

Regulator Description

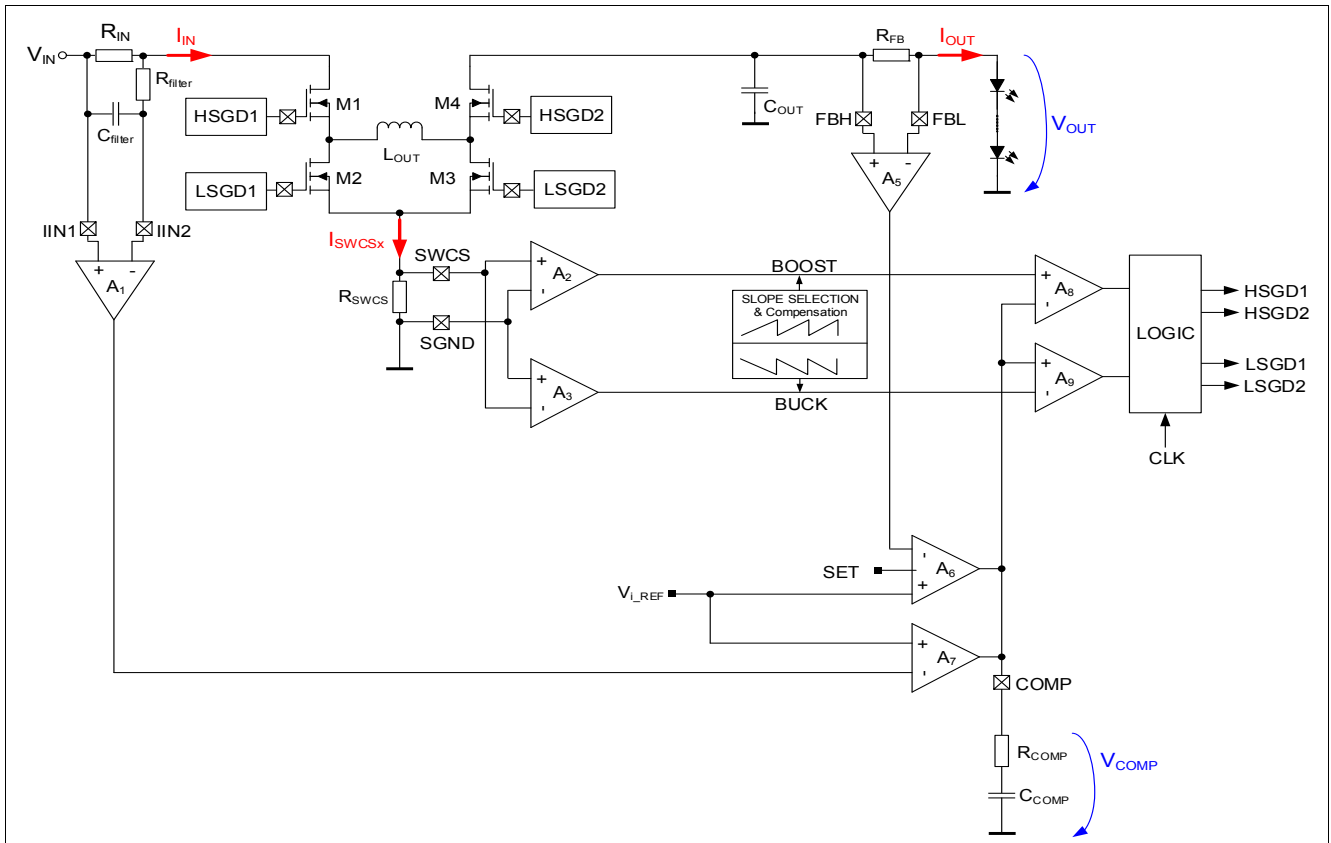


Figure 7 Regulator Block Diagram - TLD5541-1

Regulator Description

6.2 Adjustable Soft Start Ramp

The soft start routine limits the current through the inductor and the external MOSFET switches during initialization to minimize potential overshoots at the output.

The soft start routine is applied:

- At first turn on (first PWM rise after EN = High)
- After Output Short to GND or Open Load detection
- After Input Overvoltage detection

The soft start rising edge gradually increases the current of the inductor (L_{OUT}) over t_{SOFT_START} by clamping the COMP voltage. The soft start ramp is defined by a capacitor placed at the SOFT_START pin.

Selection of the SOFT_START capacitor (C_{SOFT_START}) can be done according to the approximate formula described in [Equation \(6.1\)](#):

$$t_{SOFT_START} = \frac{V_{ss_th_eff}}{I_{SOFT_START(PU)}} \cdot C_{SOFT_START} \quad (6.1)$$

Note: $V_{ss_th_eff}$ is the soft start effectiveness threshold, that depends on load condition. Its value is about 0.7 V for the buck mode and 1.4 V for the boost mode

The SOFT START pin is also used to implement a fault mask and wait-before-retry time, on rising and falling edge respectively, see and chapter [Chapter 10.2](#) for details.

If an open load or a short on the output is detected, a pull-down current source $I_{SOFT_START_PD}$ (P_6.4.20) is activated. This current brings down the V_{SOFT_START} until $V_{SOFT_START_RESET}$ (P_6.4.22) is reached, then the pull-up current source $I_{SOFT_START_PU}$ (P_6.4.19) turns on again. If the fault condition hasn't been removed until $V_{SOFT_START_LOFF}$ (P_6.4.21) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.

If an input overvoltage is detected the soft start is kept low as long as the overvoltage remains.

At first PWM rise after EN = High, the internal PWM is extended till one of the 2 following condition is reached:

- Until V_{SOFT_START} exceeds $V_{Soft_Start1,2_LOFF}$
- Until V_{FBH_FBL} exceeds $V_{FBH_FBL_OL}$

Regulator Description

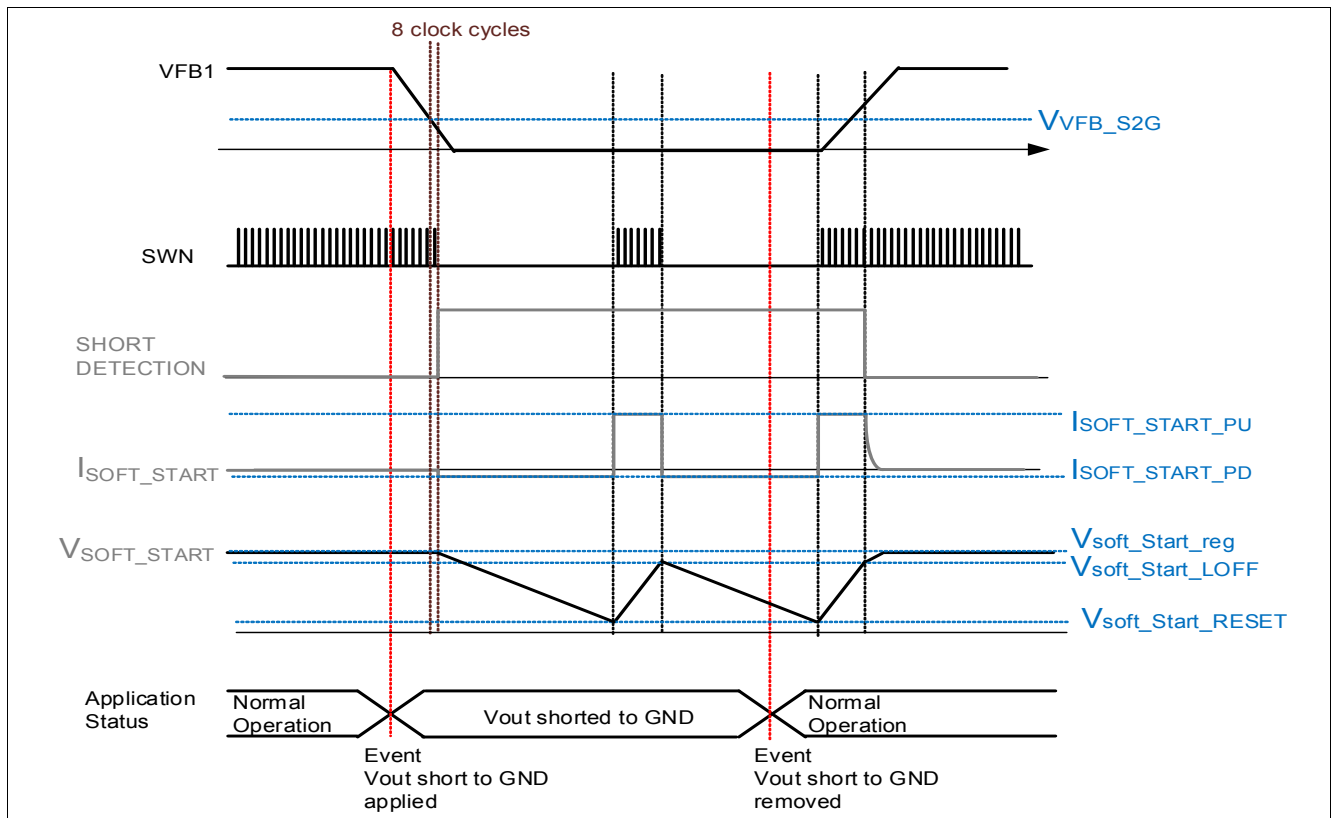


Figure 8 Soft Start timing diagram on a short to ground detected by the VFB pin

6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter [Chapter 11.2](#). Select the switching frequency with an external resistor according to the graph in [Figure 9](#) or the following approximate formulas.

$$f_{SW} [kHz] = 5375 * (R_{FREQ} [k\Omega])^{-0.8} \tag{6.2}$$

$$R_{FREQ} [k\Omega] = 46023 * (f_{SW} [kHz])^{-1.25} \tag{6.3}$$

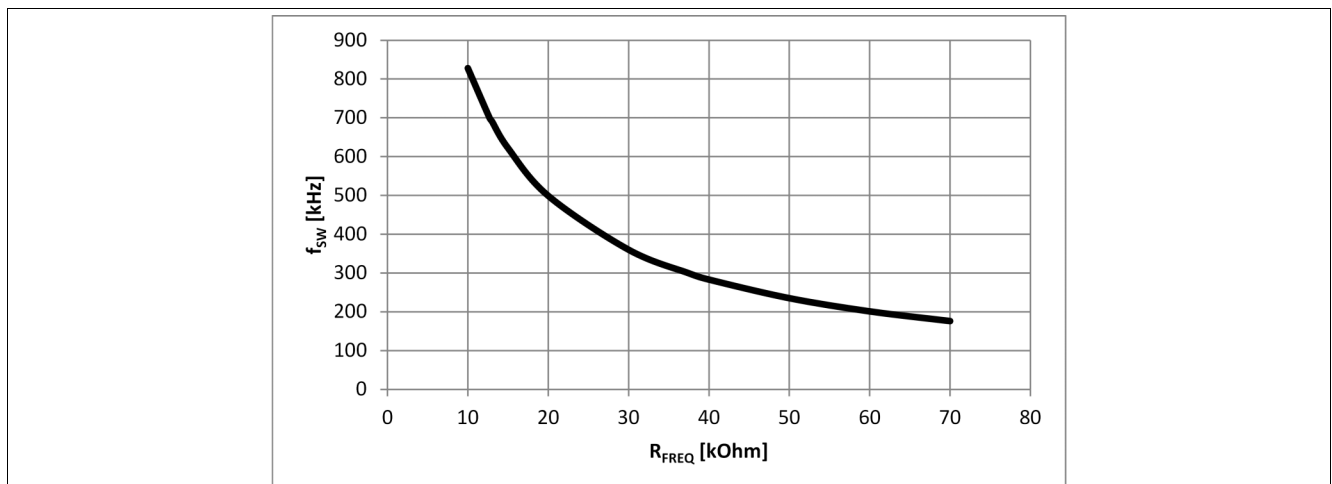


Figure 9 Switching Frequency f_{SW} versus Frequency Select Resistor to GND R_{FREQ}

Regulator Description

6.4 Operation of 4 switches H-Bridge architecture

Inductor L_{OUT} connects in an H-Bridge configuration with 4 external N channel MOSFETs (M1, M2, M3 & M4)

- Transistor M1 and M3 provides a path between V_{IN} and ground through L_{OUT} in one direction (Driven by top and bottom gate drivers HSGD1 and LSGD2)
- Transistor M2 and M4 provides a path between V_{OUT} and ground through L_{OUT} in the other direction (Driven by top and bottom gate drivers HSGD2 and LSGD1)
- Nodes SWN1, SWN2, voltage across R_{SWCS} , input and load currents are also monitored by the TLD5541-1

	BOOST MODE	BUCK-BOOST MODE	BUCK MODE
M1	ON	PWM	PWM
M2	OFF	PWM	PWM
M3	PWM	PWM	OFF
M4	PWM	PWM	ON

Figure 10 4 switches H-Bridge architecture Transistor Status summary

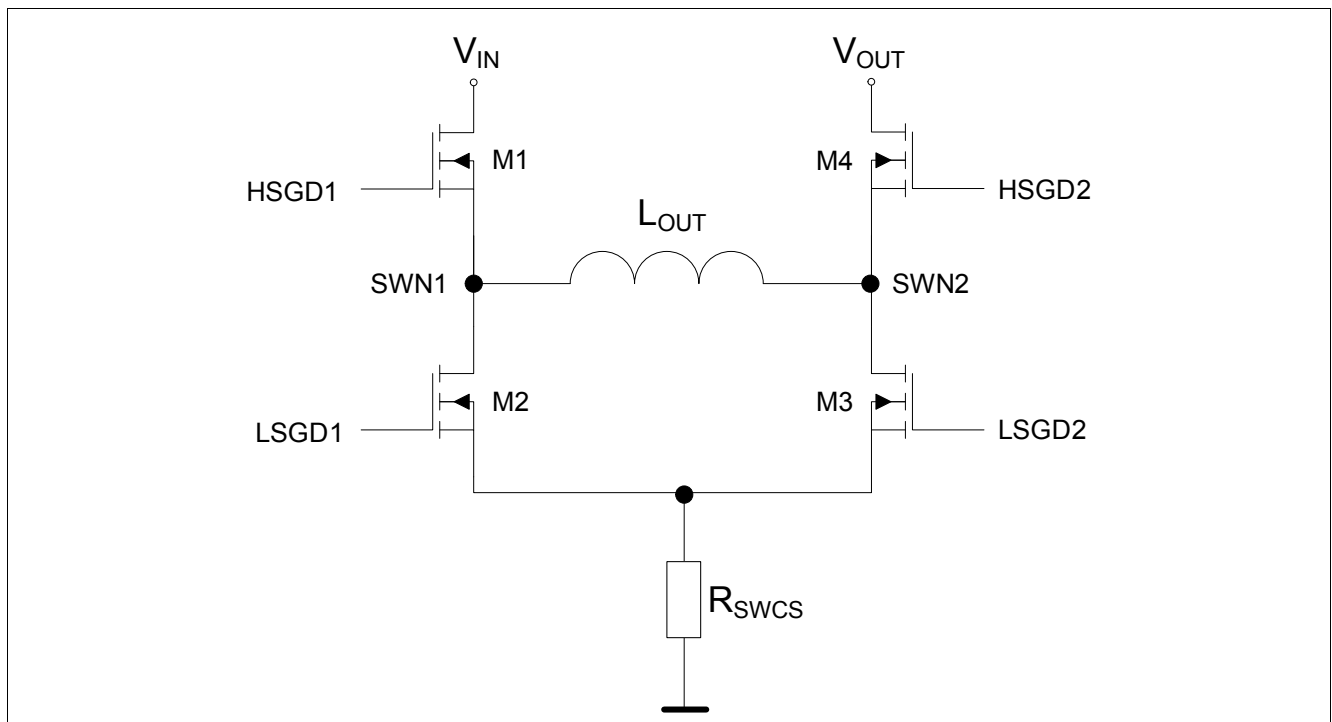


Figure 11 4 switches H-Bridge architecture overview

6.4.1 Boost mode ($V_{IN} < V_{OUT}$)

- M1 is always ON, M2 is always OFF
- Every cycle M3 turns ON first and inductor current is sensed (peak current control)
- M3 stays ON until the upper reference threshold is reached across R_{SWCS} (Energizing)

Regulator Description

- M3 turns OFF, M4 turns ON until the end of the cycle (Recirculation)
- Switches M3 and M4 alternate, behaving like a typical synchronous boost Regulator (see [Figure 12](#))

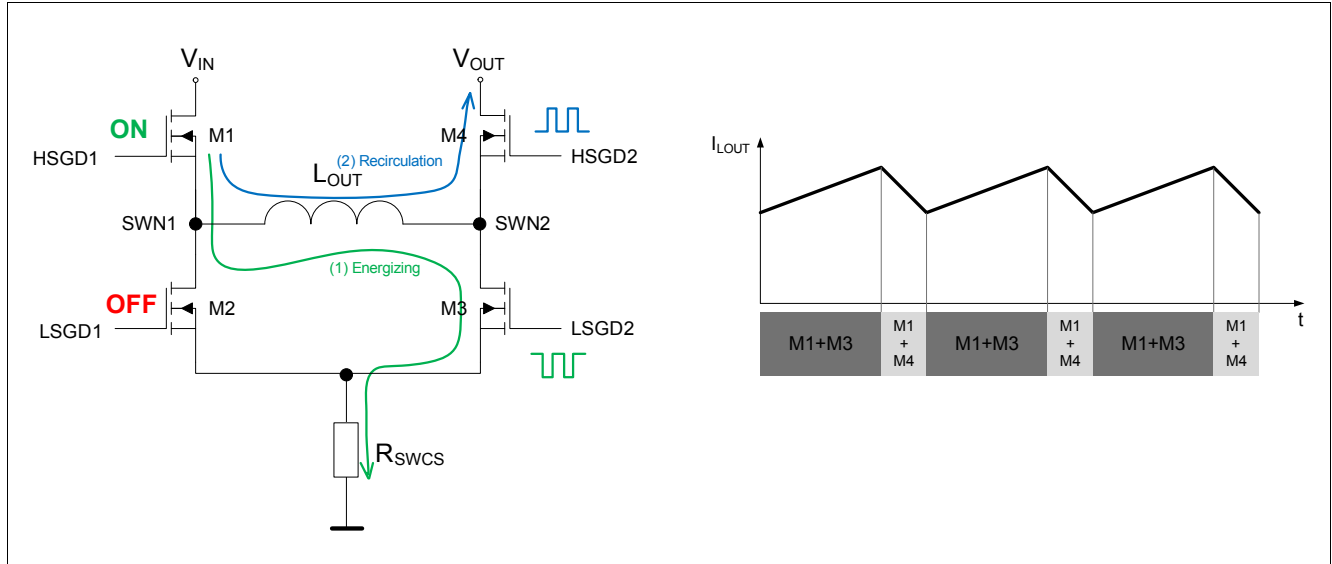


Figure 12 4 switches H-Bridge architecture in BOOST mode

Simplified comparison of 4 switches H-Bridge architecture to traditional asynchronous Boost approach.

- M2 is always OFF in this mode (open)
- M1 is always ON in this mode (closed connection of inductor to V_{IN})
- M4 acts as a synchronous diode, with significantly lower conduction power losses ($I^2 \times R_{DS(ON)}$ vs. $0.7 V \times I$)

Note: Diode is source of losses and lower system efficiency!

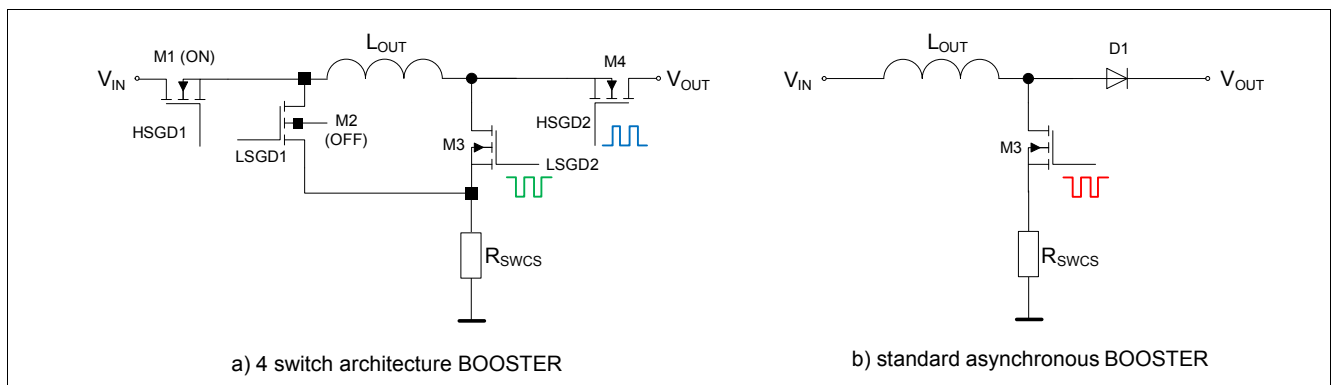


Figure 13 4 switches H-Bridge architecture in BOOST mode compared to standard async Booster

6.4.2 Buck mode ($V_{IN} > V_{OUT}$)

- M4 is always ON, M3 is always OFF
- Every cycle M2 turns ON and inductor current is sensed (valley current control)
- M2 stays ON until the lower reference threshold is reached across R_{SWCS} (Recirculation)

Regulator Description

- M2 turns OFF, M1 turns ON until the end of the cycle (Energizing)
- Switches M1 and M2 alternate, behaving like a typical synchronous BUCK Regulator (see [Figure 14](#))

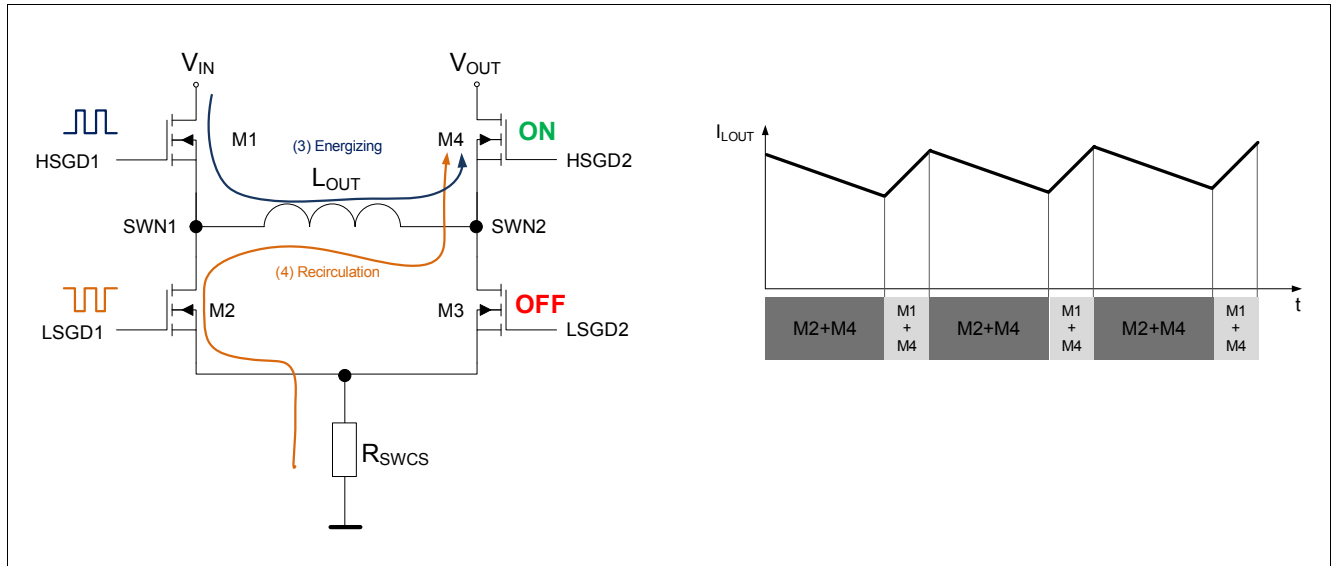


Figure 14 4 switches H-Bridge architecture in BUCK mode

Simplified comparison of 4 switches architecture to traditional asynchronous Buck approach.

- M3 is always OFF in this mode (open).
- M4 is always ON in this mode (closed connection inductor to V_{OUT}).
- M2 acts as a synchronous diode, with significantly lower conduction losses ($I^2 \times R_{DS(ON)}$ vs. $0.7 V \times I$)

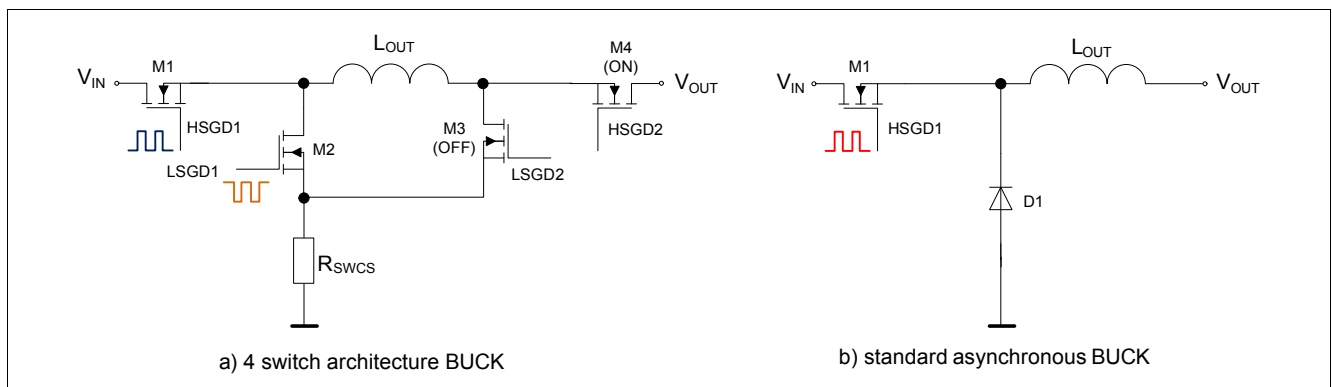


Figure 15 4 switches H-Bridge architecture in BUCK mode compared to standard async BUCK

6.4.3 Buck-Boost mode ($V_{IN} \sim V_{OUT}$)

- When V_{IN} is close to V_{OUT} the controller is in Buck-Boost operation
- All switches are switching in buck-boost operation. The direct energy transfer from the Input to the output ($M1+M4 = ON$) is beneficial to reduce ripple current and improves the energy efficiency of the Buck-Boost control scheme
- The two buck boost waveforms and switching behaviors are displayed in [Figure 16](#) below

Regulator Description

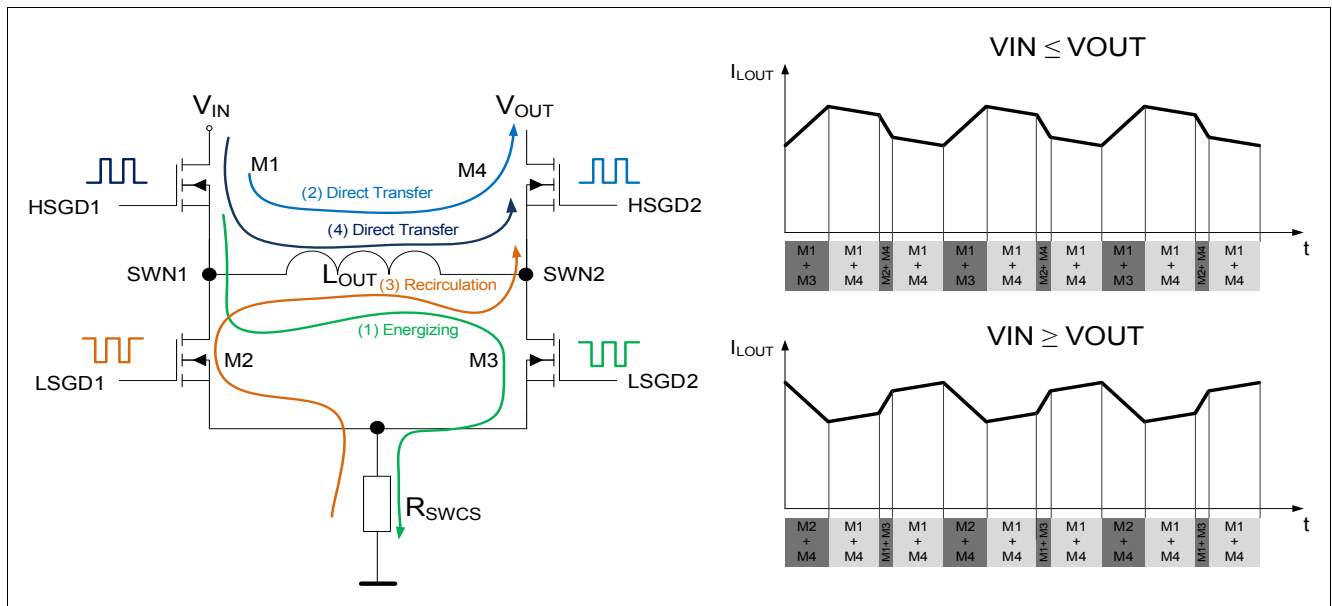


Figure 16 4 switches H-Bridge architecture in BUCK-BOOST mode

6.5 Fast Output Discharge Operation Mode - Multi Floating Switches Topology

Multiple light functions can be driven by a single DC/DC converter adopting a Multi Floating Switch (MFS) topology. In a MFS topology, each LED Function is connected in series and can be independently turned off via a bypass switch. Because of the series connections, all the functions are driven with the same current. Different brightness can be achieved with individual PWM duty cycles.

In order to drive different LED functions in this topology, a Buck Boost converter is probably needed. A single stage buck boost topology has high efficiency but requires several μF of output capacitance (C_{OUT}). The extra voltage present on this capacitor, when shorting one function to turn it off, may create a current spike in the LEDs that have to remain on.

The TLD5541-1 has a dedicated state machine which controls a fast discharge of the output cap to a desired fraction of the initial output voltage. This Fast Output Discharge feature (F.D.), if carefully configured, limits the current spike during load jump events preventing LED damage.

An Example of the Multi Floating Switch topology architecture and operation are shown in [Figure 17](#)

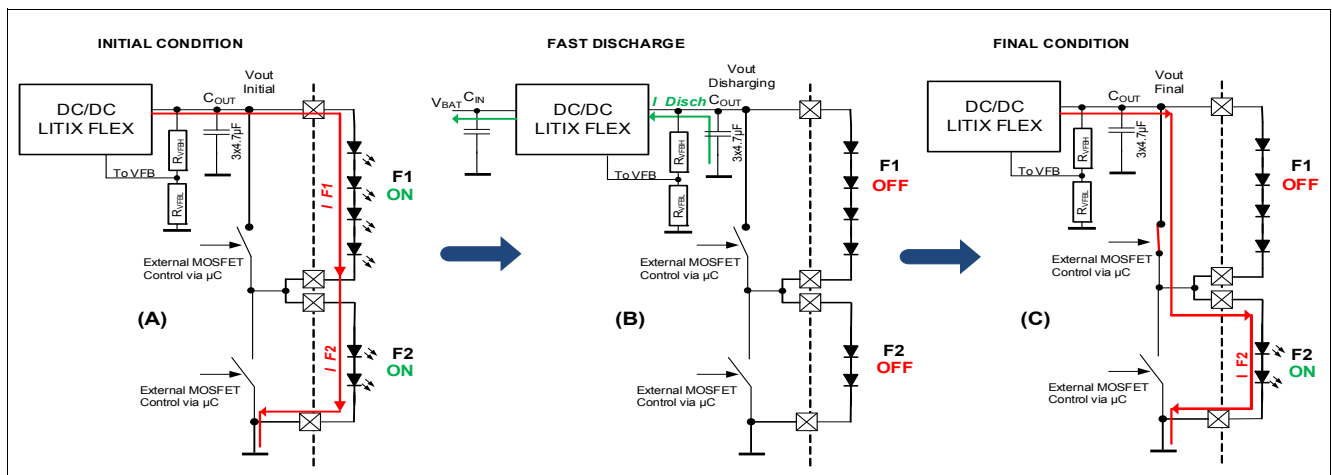


Figure 17 Multi Floating Switch topology: operation sequence on 2 Functions: (F1+F2) to (F2)