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# TLD5541-2QV

Dual SYNC DC/DC Controller with SPI Interface

Infineon® LITIX™ Power Flex



|                   |               |
|-------------------|---------------|
| <b>Package</b>    | PG-VQFN-48-31 |
| <b>Marking</b>    | TLD55412QV    |
| <b>Sales Name</b> | TLD5541-2QV   |

## 1 Overview

### Features

- Dual-Channel synchronous DC/DC Controller for HIGH POWER LED drivers
- Wide LED forward voltage Range (2 V up to 55 V)
- Wide VIN Range (IC 4.5 V to 40 V, Power 4.5 V to 55 V)
- Switching Frequency Range from 200 kHz to 700 kHz
- SPI for diagnostics and control
- Maximum Efficiency in every condition (up to 96%)
- Multitopology constant Current (LED) and Constant Voltage Regulation
- Drives Multiple Load with a single IC thanks to the Fast Output Discharge operation
- Limp Home Function (Fail Safe Mode)
- EMC optimized device: Features an auto Spread Spectrum
- LED current sense with dedicated monitor Output
- Advanced protection features for device and load
- Enhanced Dimming features: Analog and PWM dimming
- LED current accuracy +/- 3%
- Available in a small thermally enhanced PG-VQFN-48-31 package
- Automotive AEC Qualified

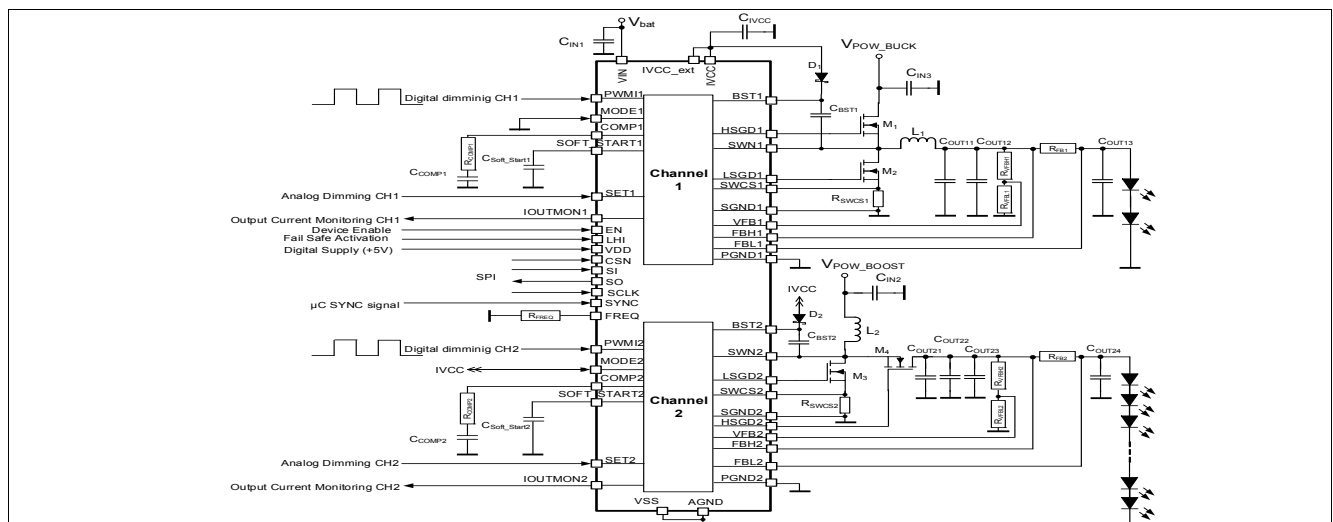
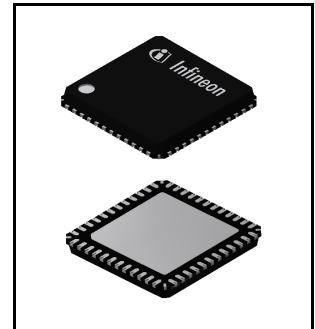


Figure 1 Application Drawing - TLD5541-2QV as current regulator

## Overview

### Description

The TLD5541-2QV is a synchronous DUAL Channel DC/DC controller with built in protection features and SPI interface. This concept is beneficial for driving high power LEDs with maximum system efficiency and minimum number of external components. The TLD5541-2QV offers both analog and digital (PWM) dimming. The switching frequency is adjustable in the range of 200 kHz to 700 kHz. It can be synchronized to an external clock source. A built in programmable Spread Spectrum switching frequency modulation and the forced continuous current regulation mode improve the overall EMC behavior. Furthermore the current mode regulation scheme provides a stable regulation loop maintained by small external compensation components. The adjustable soft start feature limits the current peak as well as voltage overshoot at start-up. The TLD5541-2QV is suitable for use in the harsh automotive environment.

**Table 1 Product Summary**

|  |                  |                                   |
|--|------------------|-----------------------------------|
| Power Stage input voltage range  | $V_{POW}$        | 4.5 V ... 55 V                    |
| Device Input supply voltage range  | $V_{VIN}$        | 4.5 V ... 40 V                    |
| Maximum output voltage (depending by the application conditions)                     | $V_{OUT(max)}$   | 55 V Boost Mode<br>50 V Buck Mode |
| Switching Frequency range  | $f_{SW}$         | 200 kHz... 700 kHz                |
| Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Up)   | $R_{DS(ON\_PU)}$ | 2.3 $\Omega$                      |
| Typical NMOS driver on-state resistance at $T_j = 25^\circ\text{C}$ (Gate Pull Down) | $R_{DS(ON\_PD)}$ | 1.2 $\Omega$                      |
| SPI clock frequency  | $f_{SCLK(MAX)}$  | 5 MHz                             |

### Protective Functions

- Over load protection of external MOSFETs
- Shorted load, output overvoltage and overcurrent protection
- Input undervoltage protection
- Thermal shutdown of device with autorestart behavior
- Electrostatic discharge protection (ESD)

### Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in ON-state
- Device Overtemperature shutdown and Temperature Prewarning
- Smart monitoring and advanced functions provide  $I_{LED}$  information

### Limp Home Function

- Limp Home activation via LHI pin

### Applications

- Especially designed for driving high power LEDs in automotive applications
- Automotive Exterior Lighting: full LED headlamp assemblies (Low Beam, High Beam, Matrix Beam, Pixel Light)
- General purpose current/voltage controlled DC/DC LED driver

Block Diagram

2 Block Diagram

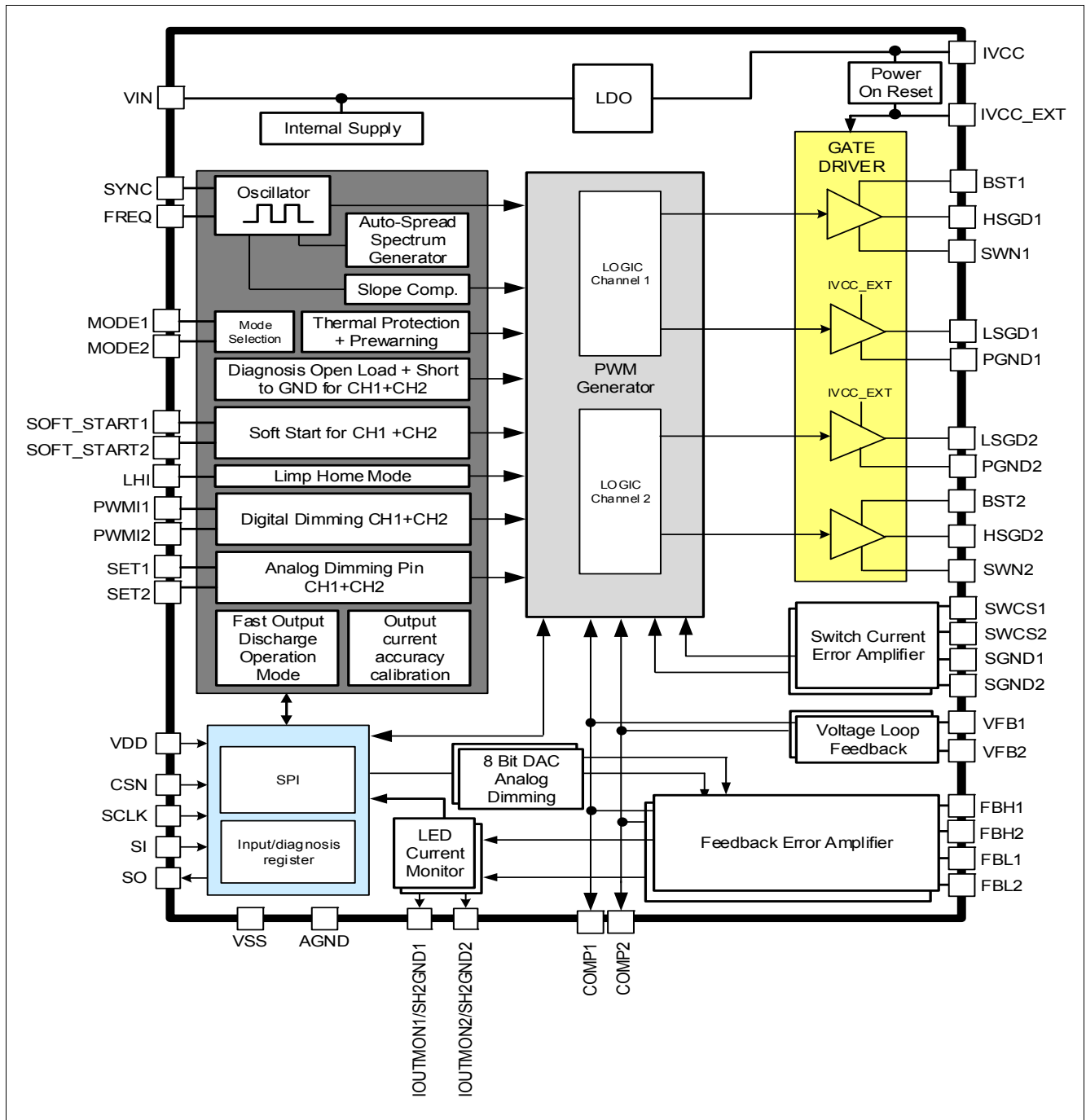
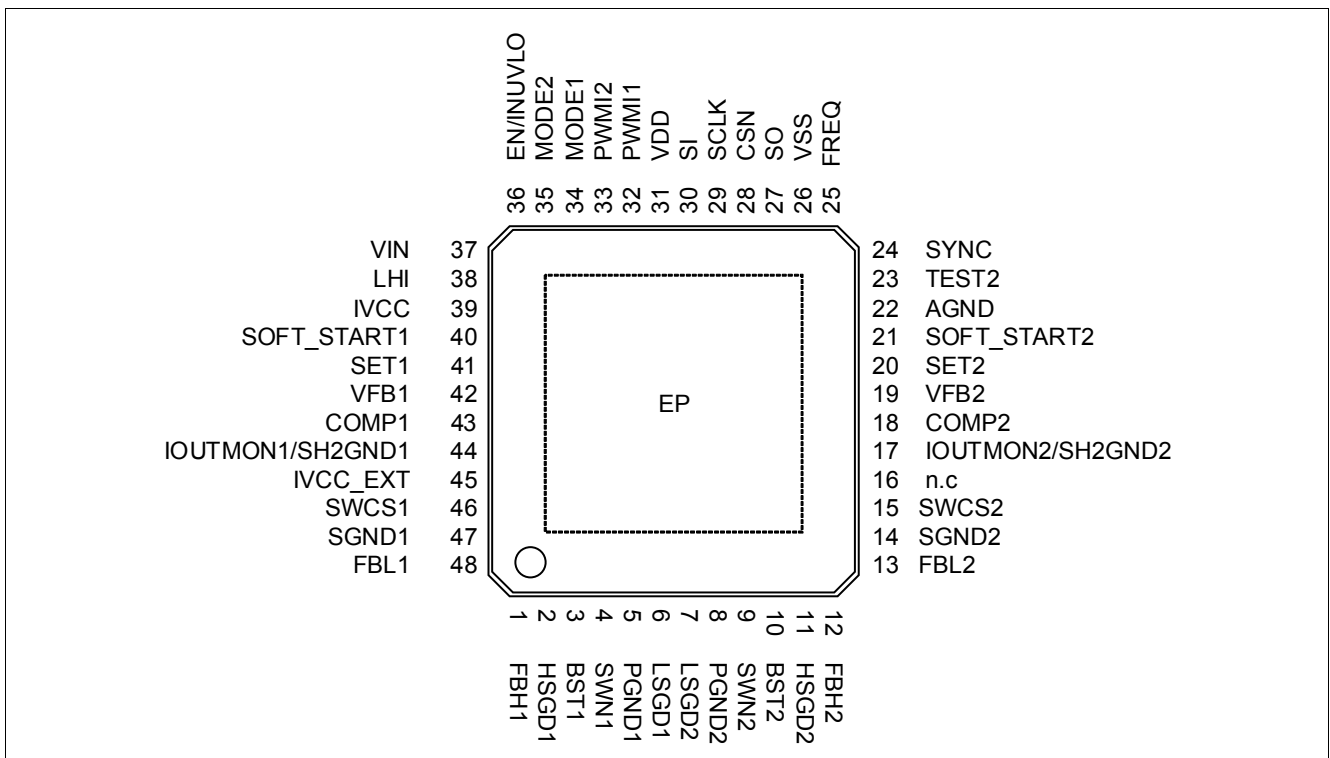


Figure 2 Block Diagram - TLD5541-2QV

**Pin Configuration**

**3 Pin Configuration**

**3.1 Pin Assignment**



**Figure 3 Pin Configuration -TLD5541-2QV**

**Pin Configuration**

**3.2 Pin Definitions and Functions**

| Pin                       | Symbol   | I/O <sup>1)</sup> |    | Function   |
|---------------------------|----------|-------------------|----|--|
| <b>Power Supply</b>       |          |                   |    |  |
| 16                        | n.c.     | -                 |    | <b>Not connected, tie to AGND on the Layout;</b>   |
| 37                        | VIN      | -                 |    | <b>Power Supply Voltage;</b><br>Supply for internal biasing.   |
| 31                        | VDD      | -                 |    | <b>Digital GPIO Supply Voltage;</b><br>Connect to reverse voltage protected 5 V or 3.3 V supply.   |
| 45                        | IVCC_EXT | I                 | PD | <b>External LDO input;</b><br>Input to alternatively supply internal Gate Drivers via an external LDO. Connect to IVCC pin to use internal LDO to supply gate drivers. Must not be left open.                |
| 5, 8                      | PGND1, 2 | -                 |    | <b>Power Ground;</b><br>Ground for power potential. Connect externally close to the chip.  |
| 26                        | VSS      | -                 |    | <b>Digital GPIO Ground;</b><br>Ground for GPIO pins.   |
| 22                        | AGND     | -                 |    | <b>Analog Ground;</b><br>Ground Reference  |
| -                         | EP       | -                 |    | <b>Exposed Pad;</b><br>Connect to external heatspreading Cu area (e.g. inner GND layer of multilayer PCB with thermal vias).   |
| <b>Gate Driver Stages</b> |          |                   |    |  |
| 2                         | HSGD1    | O                 |    | <b>Highside Gate Driver Output 1;</b><br>Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC\_EXT}$ superimposed on the switch node voltage SWN1. Connect to gate of external switching MOSFET. |
| 11                        | HSGD2    | O                 |    | <b>Highside Gate Driver Output 2;</b><br>Drives the top n-channel MOSFET with a voltage equal to $V_{IVCC\_EXT}$ superimposed on the switch node voltage SWN2. Connect to gate of external switching MOSFET. |
| 6                         | LSGD1    | O                 |    | <b>Lowside Gate Driver Output 1;</b><br>Drives the lowside n-channel MOSFET between GND and $V_{IVCC\_EXT}$ . Connect to gate of external switching MOSFET.  |
| 7                         | LSGD2    | O                 |    | <b>Lowside Gate Driver Output 2;</b><br>Drives the lowside n-channel MOSFET between GND and $V_{IVCC\_EXT}$ . Connect to gate of external switching MOSFET.  |
| 4                         | SWN1     | IO                |    | <b>Switch Node 1;</b>  |
| 9                         | SWN2     | IO                |    | <b>Switch Node 2;</b>  |
| 39                        | IVCC     | O                 |    | <b>Internal LDO output;</b><br>Used for internal biasing and gate driver supply. Bypass with external capacitor close to the pin. Pin must not be left open.   |

**Pin Configuration**

| Pin                       | Symbol    | I/<br>O | <sup>1)</sup> | Function   |
|---------------------------|-----------|---------|---------------|--|
| <b>Inputs and Outputs</b> |           |         |               |  |
| 38                        | LHI       | I       | PD            | <b>Limp Home Input Pin;</b><br>Used to enter in Limp Home state during Fail Safe condition.  |
| 23                        | TEST2     | -       |               | <b>Test Pin;</b><br>Used for Infineon end of line test, connect to GND in application.   |
| 36                        | EN/INUVLO | I       | PD            | <b>Enable/Input Under Voltage Lock Out;</b><br>Used to put the device in a low current consumption mode, with additional capability to fix an undervoltage threshold via external components. Pin must not be left open. |
| 25                        | FREQ      | I       |               | <b>Frequency Select Input;</b><br>Connect external resistor to GND to set frequency.   |
| 24                        | SYNC      | I       | PD            | <b>Synchronization Input;</b><br>Apply external clock signal for synchronization.  |
| 32                        | PWMI1     | I       | PD            | <b>Control Input CH1;</b> Digital input 5 V or 3.3 V.  |
| 33                        | PWMI2     | I       | PD            | <b>Control Input CH2;</b> Digital input 5 V or 3.3 V.  |
| 1                         | FBH1      | I       |               | <b>Output current Feedback Positive for CH1;</b><br>Non inverting Input (+) CH1.   |
| 12                        | FBH2      | I       |               | <b>Output current Feedback Positive for CH2;</b><br>Non inverting Input (+) CH2.   |
| 48                        | FBL1      | I       |               | <b>Output current Feedback Negative for CH1;</b><br>Inverting Input (-) CH1.   |
| 13                        | FBL2      | I       |               | <b>Output current Feedback Negative for CH2;</b><br>Inverting Input (-) CH2.   |
| 3                         | BST1      | IO      |               | <b>Bootstrap capacitor;</b><br>Used for internal biasing and to drive the Highside Switch HSGD1. Bypass to SWN1 with external capacitor close to the pin. Pin must not be left open.                                     |
| 10                        | BST2      | IO      |               | <b>Bootstrap capacitor;</b><br>Used for internal biasing and to drive the Highside Switch HSGD2. Bypass to SWN2 with external capacitor close to the pin. Pin must not be left open.                                     |
| 46                        | SWCS1     | I       |               | <b>Current Sense Input for CH1;</b><br>Inductor current sense CH1 - Non Inverting Input (+).   |
| 15                        | SWCS2     | I       |               | <b>Current Sense Input for CH2;</b><br>Inductor current sense CH2 - Non Inverting Input (+).   |
| 47                        | SGND1     | I       |               | <b>Current Sense Ground for CH1;</b><br>Inductor current sense CH1 - Inverting Input (-).<br>Route as Differential net with SWCS1 on the Layout.   |
| 14                        | SGND2     | I       |               | <b>Current Sense Ground for CH2;</b><br>Inductor current sense CH2 - Inverting Input (-).<br>Route as Differential net with SWCS2 on the Layout.   |

**Pin Configuration**

| Pin | Symbol           | I/O | <sup>1)</sup> | Function  |
|-----|------------------|-----|---------------|---|
| 43  | COMP1            | O   |               | <b>Compensation Network Pin for CH1;</b><br>Connect R and C network to pin for stability phase margin adjustment for CH1.   |
| 18  | COMP2            | O   |               | <b>Compensation Network Pin for CH2;</b><br>Connect R and C network to pin for stability phase margin adjustment for CH2.   |
| 40  | SOFT_START1      | O   |               | <b>Softstart configuration Pin for CH1;</b><br>Connect a capacitor $C_{SOFT\_START1}$ to GND to fix a soft start ramp default time.   |
| 21  | SOFT_START2      | O   |               | <b>Softstart configuration Pin for CH2;</b><br>Connect a capacitor $C_{SOFT\_START2}$ to GND to fix a soft start ramp default time.   |
| 42  | VFB1             | I   |               | <b>Voltage Feedback Pin for CH1;</b><br>VFB is intended to set output protection functions for CH1.   |
| 19  | VFB2             | I   |               | <b>Voltage Feedback Pin for CH2;</b><br>VFB is intended to set output protection functions for CH2.   |
| 41  | SET1             | I   |               | <b>Analog current sense adjustment Pin for CH1;</b>   |
| 20  | SET2             | I   |               | <b>Analog current sense adjustment Pin for CH2;</b>   |
| 44  | IOUTMON1/SH2GND1 | O   | PD            | <b>Output current monitor output 1/Short to ground Flag 1;</b><br>MODE1=LOW: Monitor pin that produces a linear function of $I_{OUT}$ as a voltage.<br>MODE1=HIGH: Short to ground error flag.<br>Pin configuration is forced to Output current monitor when $CURRMON\_CH1 . IOUTMON\_CH1=HIGH$ . |
| 17  | IOUTMON2/SH2GND2 | O   | PD            | <b>Output current monitor output 2/Short to ground Flag 2;</b><br>MODE2=LOW: Monitor pin that produces a linear function of $I_{OUT}$ as a voltage.<br>MODE2=HIGH: Short to ground error flag.<br>Pin configuration is forced to Output current monitor when $CURRMON\_CH2 . IOUTMON\_CH2=HIGH$ . |
| 34  | MODE1            | I   | PD            | <b>Regulation Mode selection Pin for CH1;</b><br>LOW: BUCK Regulation<br>HIGH: BOOST Regulation.  |
| 35  | MODE2            | I   | PD            | <b>Regulation Mode selection Pin for CH2;</b><br>LOW: BUCK Regulation<br>HIGH: BOOST Regulation.  |

**SPI**

|    |      |   |    |  |
|----|------|---|----|--|
| 30 | SI   | I | PD | <b>Serial data in;</b> Digital input 5 V or 3.3 V.               |
| 29 | SCLK | I | PD | <b>Serial clock;</b> Digital input 5 V or 3.3 V.                 |
| 28 | CSN  | I | PU | <b>SPI chip select;</b> Digital input 5 V or 3.3 V. Active LOW.  |
| 27 | SO   | O |    | <b>Serial data out;</b> Digital output, referenced to $V_{DD}$ . |



**Pin Configuration**

- 1) O: Output, I: Input,  
PD: pull-down circuit integrated,  
PU: pull-up circuit integrated

**General Product Characteristics**

**4 General Product Characteristics**

**4.1 Absolute Maximum Ratings**

**Table 2 Absolute Maximum Ratings<sup>1)</sup>**  
 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

| Parameter  | Symbol                    | Values |      |      | Unit | Note or Test Condition | Number   |
|--|---------------------------|--------|------|------|------|------------------------|----------|
|  |                           | Min.   | Typ. | Max. |      |                        |          |
| <b>Supply Voltages</b>   |                           |        |      |      |      |                        |          |
| VIN<br>Supply Input  | $V_{VIN}$                 | -0.3   | –    | 60   | V    | –                      | P_4.1.1  |
| VDD<br>Digital supply voltage                                    | $V_{VDD}$                 | -0.3   | –    | 6    | V    | –                      | P_4.1.2  |
| IVCC<br>Internal Linear Voltage Regulator<br>Output voltage      | $V_{IVCC}$                | -0.3   | –    | 6    | V    | –                      | P_4.1.3  |
| IVCC_EXT<br>External Linear Voltage Regulator Input<br>voltage   | $V_{IVCC\_EXT}$           | -0.3   | –    | 6    | V    | –                      | P_4.1.4  |
| <b>Gate Driver Stages</b>  |                           |        |      |      |      |                        |          |
| LSGD1,2 - PGND1,2<br>Lowside Gatedriver voltage                  | $V_{LSGD1,2-}$<br>PGND1,2 | -0.3   | –    | 5.5  | V    | –                      | P_4.1.54 |
| HSGD1,2 - SWN1,2<br>Highside Gatedriver voltage                  | $V_{HSGD1,2-}$<br>SWN1,2  | -0.3   | –    | 5.5  | V    | –                      | P_4.1.55 |
| SWN1, SWN2<br>switching node voltage                             | $V_{SWN1,2}$              | -1     | –    | 60   | V    | –                      | P_4.1.6  |
| (BST1-SWN1), (BST2-SWN2)<br>Bootstrap voltage                    | $V_{BST1,2-}$<br>SWN1,2   | -0.3   | –    | 6    | V    | –                      | P_4.1.7  |
| BST1, BST2<br>Bootstrap voltage related to GND                   | $V_{BST1,2}$              | -0.3   | –    | 65   | V    | –                      | P_4.1.8  |
| SWCS1,2<br>Switch Current Sense Input voltages                   | $V_{SWCS1,2}$             | -0.3   | –    | 0.3  | V    | –                      | P_4.1.42 |
| SGND1,2<br>Switch Current Sense GND voltages                     | $V_{SGND1,2}$             | -0.3   | –    | 0.3  | V    | –                      | P_4.1.43 |
| SWCS1,2-SGND1,2<br>Switch Current Sense differential<br>voltages | $V_{SWCS1,2-}$<br>SGND1,2 | -0.5   | –    | 0.5  | V    | –                      | P_4.1.44 |
| PGND1,2<br>Power GND voltage                                     | $V_{PGND1,2}$             | -0.3   | –    | 0.3  | V    | –                      | P_4.1.28 |
| <b>High voltage Pins</b>   |                           |        |      |      |      |                        |          |
| FBH1,2; FBL1,2<br>Feedback Error Amplifier voltages              | $V_{FBH1,2;}$<br>FBL1,2   | -0.3   | –    | 60   | V    | –                      | P_4.1.45 |

**General Product Characteristics**

**Table 2 Absolute Maximum Ratings<sup>1)</sup> (cont'd)**  
 $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

| Parameter   | Symbol                       | Values |      |      | Unit | Note or Test Condition | Number   |
|---|------------------------------|--------|------|------|------|------------------------|----------|
|   |                              | Min.   | Typ. | Max. |      |                        |          |
| FBH1,2-FBL1,2<br>Feedback Error Amplifier differential voltages | $V_{\text{FBH1,2-FBL1,2}}$   | -0.5   | -    | 0.5  | V    | -                      | P_4.1.47 |
| EN/INUVLO<br>Device enable/input undervoltage lockout           | $V_{\text{EN/INUVLO}}$       | -0.3   | -    | 60   | V    | -                      | P_4.1.16 |
| <b>Digital (I/O) Pins</b>                                       |                              |        |      |      |      |                        |          |
| PWM1,2<br>Digital Input voltages                                | $V_{\text{PWM1,2}}$          | -0.3   | -    | 5.5  | V    | -                      | P_4.1.49 |
| CSN<br>Voltage at Chip Select pin                               | $V_{\text{CSN}}$             | -0.3   | -    | 5.5  | V    | -                      | P_4.1.18 |
| SCLK<br>Voltage at Serial Clock pin                             | $V_{\text{SCLK}}$            | -0.3   | -    | 5.5  | V    | -                      | P_4.1.19 |
| SI<br>Voltage at Serial Input pin                               | $V_{\text{SI}}$              | -0.3   | -    | 5.5  | V    | -                      | P_4.1.20 |
| SO<br>Voltage at Serial Output pin                              | $V_{\text{SO}}$              | -0.3   | -    | 5.5  | V    | -                      | P_4.1.21 |
| SYNC<br>Synchronization Input voltage                           | $V_{\text{SYNC}}$            | -0.3   | -    | 5.5  | V    | -                      | P_4.1.22 |
| MODE1, 2<br>Regulation Mode selection Input voltages            | $V_{\text{MODE1,2}}$         | -0.3   | -    | 5.5  | V    | -                      | P_4.1.57 |
| LHI<br>Limp Home Input Voltage                                  | $V_{\text{LHI}}$             | -0.3   | -    | 5.5  | V    | -                      | P_4.1.58 |
| LHI<br>Limp Home Input Current                                  | $I_{\text{LHI}}$             | -5     | -    | -    | mA   | -                      | P_4.1.60 |
| <b>Analog Pins</b>  |                              |        |      |      |      |                        |          |
| VFB1,2<br>Loop Input voltages                                   | $V_{\text{VFB1,2}}$          | -0.3   | -    | 5.5  | V    | -                      | P_4.1.50 |
| SET1,2<br>Analog dimming Input voltage                          | $V_{\text{SET1,2}}$          | -0.3   | -    | 5.5  | V    | -                      | P_4.1.56 |
| COMP1,2<br>Compensation Input voltages                          | $V_{\text{COMP1,2}}$         | -0.3   | -    | 3.6  | V    | -                      | P_4.1.52 |
| SOFT_START1,2<br>Softstart Voltages                             | $V_{\text{SOFT\_STAR T1,2}}$ | -0.3   | -    | 3.6  | V    | -                      | P_4.1.53 |
| FREQ<br>Voltage at frequency selection pin                      | $V_{\text{FREQ}}$            | -0.3   | -    | 3.6  | V    | -                      | P_4.1.32 |
| IOUTMON1,2/SH2GND1,2<br>Voltages at output monitor pins         | $V_{\text{IOUTMON1, 2}}$     | -0.3   | -    | 5.5  | V    | -                      | P_4.1.59 |
| <b>Temperatures</b>   |                              |        |      |      |      |                        |          |

**General Product Characteristics**

**Table 2 Absolute Maximum Ratings<sup>1)</sup> (cont'd)**  
 $T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to AGND, (unless otherwise specified)

| Parameter                             | Symbol                       | Values |      |      | Unit               | Note or Test Condition | Number   |
|---------------------------------------|------------------------------|--------|------|------|--------------------|------------------------|----------|
|                                       |                              | Min.   | Typ. | Max. |                    |                        |          |
| Junction Temperature                  | $T_j$                        | -40    | –    | 150  | $^{\circ}\text{C}$ | –                      | P_4.1.35 |
| Storage Temperature                   | $T_{\text{stg}}$             | -55    | –    | 150  | $^{\circ}\text{C}$ | –                      | P_4.1.36 |
| <b>ESD Susceptibility</b>             |                              |        |      |      |                    |                        |          |
| ESD Resistivity of all Pins           | $V_{\text{ESD,HBM}}$         | -2     | –    | 2    | kV                 | HBM <sup>2)</sup>      | P_4.1.37 |
| ESD Resistivity to GND                | $V_{\text{ESD,CDM}}$         | -500   | –    | 500  | V                  | CDM <sup>3)</sup>      | P_4.1.38 |
| ESD Resistivity of corner Pins to GND | $V_{\text{ESD,CDM\_corner}}$ | -750   | –    | 750  | V                  | CDM <sup>3)</sup>      | P_4.1.39 |

- 1) Not subject to production test, specified by design.
- 2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kV, 100 pF)
- 3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 3 Functional Range**

| Parameter                            | Symbol           | Values |      |      | Unit               | Note or Test Condition | Number  |
|--------------------------------------|------------------|--------|------|------|--------------------|------------------------|---------|
|                                      |                  | Min.   | Typ. | Max. |                    |                        |         |
| Device Extended Supply Voltage Range | $V_{\text{VIN}}$ | 4.5    | –    | 40   | V                  | 1)                     | P_4.2.1 |
| Device Nominal Supply Voltage Range  | $V_{\text{VIN}}$ | 8      | –    | 36   | V                  | –                      | P_4.2.2 |
| Power Stage Voltage Range            | $V_{\text{POW}}$ | 4.5    | –    | 55   | V                  | 1)                     | P_4.2.5 |
| Digital Supply Voltage               | $V_{\text{DD}}$  | 3      | –    | 5.5  | V                  | –                      | P_4.2.3 |
| Junction Temperature                 | $T_j$            | -40    | –    | 150  | $^{\circ}\text{C}$ | –                      | P_4.2.4 |

- 1) Not subject to production test, specified by design.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

**General Product Characteristics**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4**

| Parameter           | Symbol     | Values |      |      | Unit | Note or Test Condition | Number  |
|---------------------|------------|--------|------|------|------|------------------------|---------|
|                     |            | Min.   | Typ. | Max. |      |                        |         |
| Junction to Case    | $R_{thJC}$ | –      | 0.9  | –    | K/W  | <sup>1) 2)</sup>       | P_4.3.1 |
| Junction to Ambient | $R_{thJA}$ | –      | 25   | –    | K/W  | <sup>3)</sup> 2s2p     | P_4.3.2 |

- 1) Not subject to production test, specified by design.
- 2) Specified  $R_{thJC}$  value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature).  $T_a = 25^\circ\text{C}$ ; The IC is dissipating 1 W.
- 3) Specified  $R_{thJA}$  value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; The device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70  $\mu\text{m}$  Cu) and 2 inner copper layers (2 x 35  $\mu\text{m}$  Cu). A thermal via (diameter = 0.3 mm and 25  $\mu\text{m}$  plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB.  $T_a = 25^\circ\text{C}$ ; The IC is dissipating 1 W.

**Power Supply**

**5 Power Supply**

The TLD5541-2QV is supplied by the following pins:

- VIN (main supply voltage)
- VDD (digital supply voltage)
- IVCC\_EXT (supply for internal gate driver stages)

The VIN supply, in combination with the VDD supply, provides internal supply voltages for the analog and digital blocks. In situations where VIN voltage drops below VDD voltage, an increased current consumption may be observed at the VDD pin.

The SPI and IO interfaces are supplied by the VDD pin.

IVCC\_EXT is the supply for the low side driver stages. This supply is used also to charge, through external Schottky diodes, the bootstrap capacitors which provide supply voltages to the high side driver stages. If no external voltage is available this pin must be shorted to IVCC, which is the output of an internal 5 V LDO.

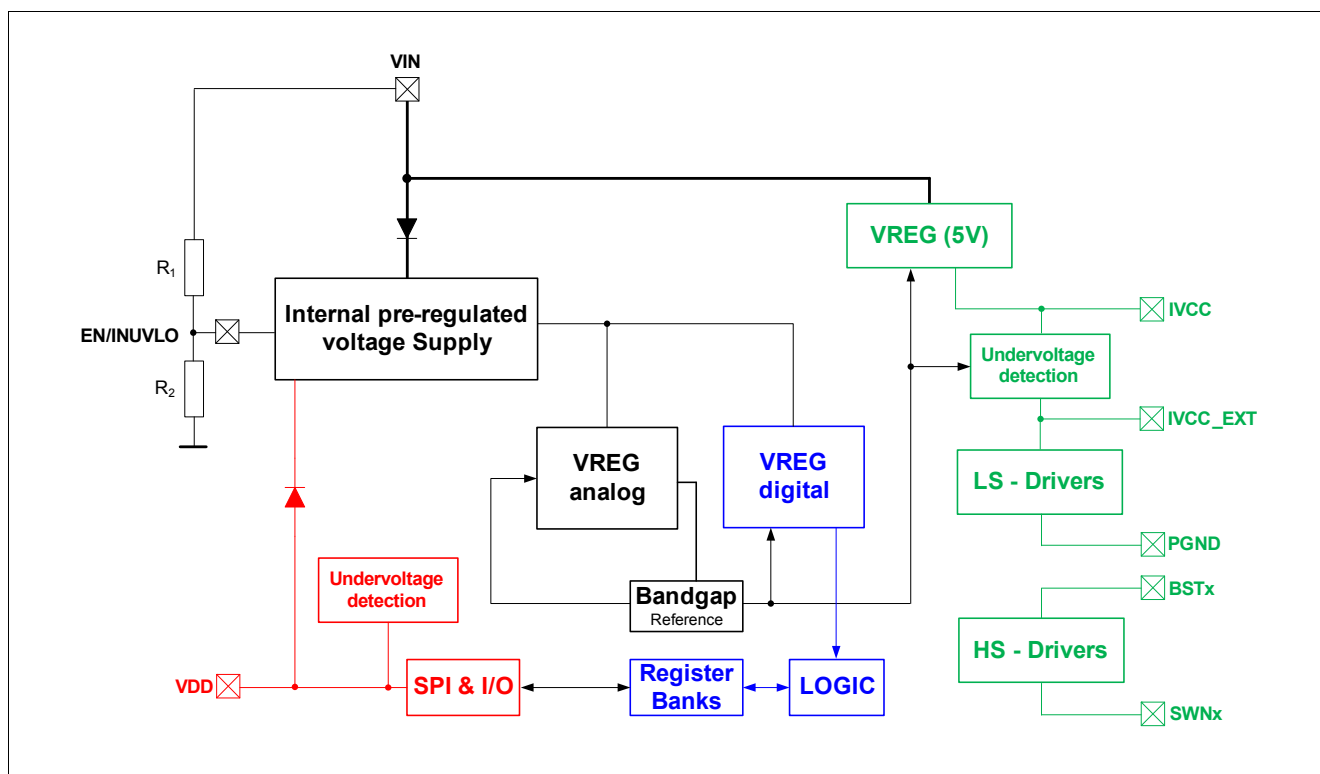
The supply pins VIN, VDD and IVCC\_EXT have undervoltage detections.

Undervoltage on VDD supply voltage prevents the activation of the gate driver stages and any SPI communication (the SPI registers are reset). Undervoltage on IVCC\_EXT or IVCC voltages forces a deactivation of the driver stages, thus stopping the switching activity, but has no effect on the SPI register settings.

Moreover the double function pin EN/INUVLO can be used as an input undervoltage protection by placing a resistor divider from VIN to GND .

If EN/INUVLO undervoltage is detected, it will turn-off the IVCC voltage regulator, stop switching, stop communications and reset all the registers.

**Figure 4** shows a basic concept drawing of the supply domains and interactions among pins VIN, VDD and IVCC/IVCC\_EXT.

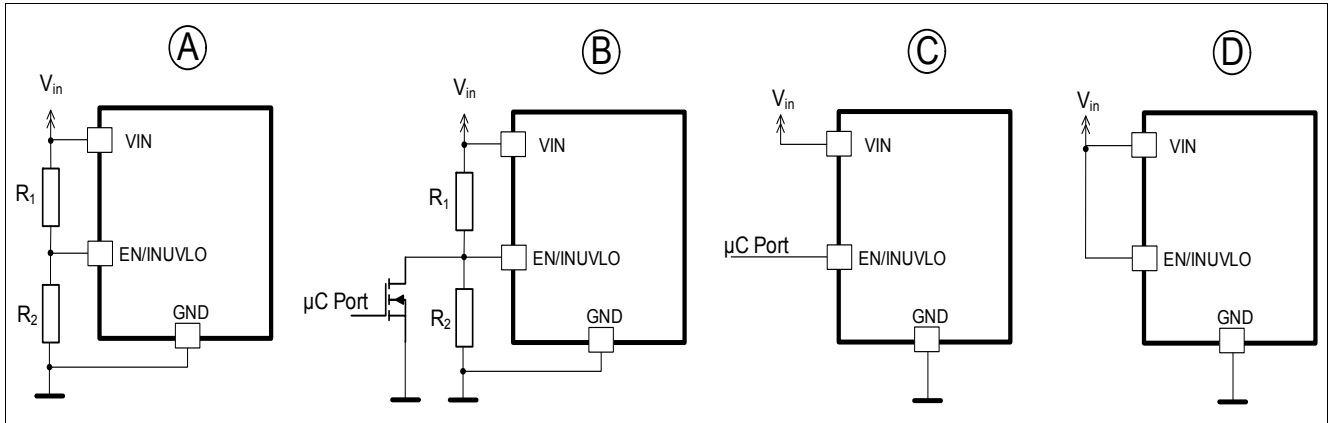


**Figure 4 Power Supply Concept Drawing**

**Power Supply**

**Usage of EN/INUVLO pin in different applications**

The pin EN/INUVLO is a double function pin and can be used to put the device into a low current consumption mode. An undervoltage threshold is fixed by placing an external resistor divider (A) in order to avoid low voltage operating conditions. This pin can be driven by a  $\mu$ C-Port as shown in (B) (C).



**Figure 5 Usage of EN/INUVLO pin in different applications**

## Power Supply

### 5.1 Different Power States

TLD5541-2QV has the following power states:

- SLEEP state
- IDLE state
- LIMP HOME state
- ACTIVE state

The transition between the power states is determined according to these variables after a filter time of max. 3 clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC\_EXT level
- VDD level
- LHI level
- DVCCTRL.IDLE bit state

The state diagram including the possible transitions is shown in [Figure 6](#).

The Power-up condition is entered when the supply voltage  $V_{VIN}$  exceed its minimum supply voltage threshold  $V_{VIN(ON)}$ .

#### SLEEP

When the device is powered it enters the SLEEP state, all outputs are OFF and the SPI registers are reset, independently from the supply voltages at the pins VIN, VDD, IVCC, and IVCC\_EXT. The current consumption is low. Refer to parameters:  $I_{VDD(SLEEP)}$  and  $I_{VIN(SLEEP)}$ .

The transition from SLEEP to ACTIVE state requires a specified time:  $t_{ACTIVE}$ .

#### IDLE

In IDLE state, the current consumption of the device can reach the limits given by parameter  $I_{VDD}$  (P\_5.3.4). The internal voltage regulator is working. Not all diagnosis functions are available (refer to [Chapter 10](#) for additional informations). In this state there is no switching activity, independently from the supply voltages  $V_{IN}$ ,  $V_{DD}$ , IVCC and IVCC\_EXT. When  $V_{DD}$  is available, the SPI registers are working and SPI communication is possible.

#### Limp Home

The Limp Home state is beneficial to fulfill system safety requirements and provides the possibility to maintain a defined current/voltage level on the output via a backup control circuitry. The backup control circuitry turns on required loads during a malfunction of the  $\mu C$ . For detailed info, refer to [Chapter 8](#).

When Limp Home state is entered, SPI registers are reset to their default values. In order to regulate the output current/voltage, it is necessary that  $V_{IN}$  and IVCC\_EXT are present and above their undervoltage threshold. If also VDD is above its undervoltage threshold, SPI communication is possible but only in read mode.

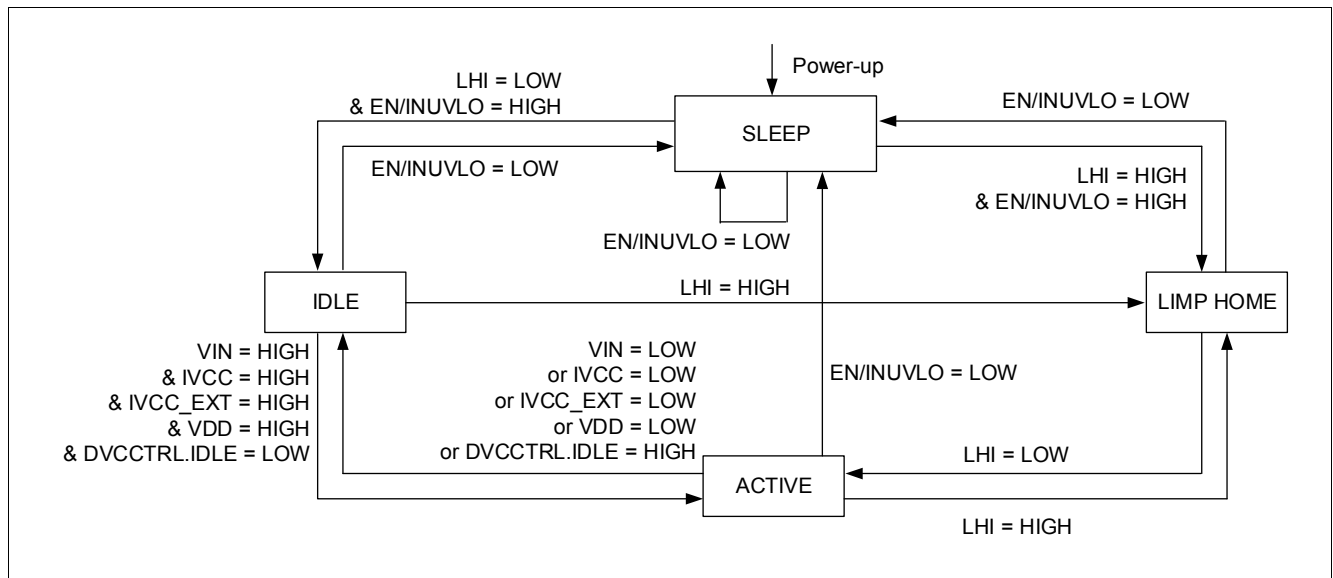
#### ACTIVE

In active state the device will start switching activity to provide power at the output only when PWM1,2 = HIGH or LOOPCTRL.CH1,2.PWM\_1,2 = HIGH. To start the Highside gate drivers HSGD1,2 the voltage level  $V_{BST1,2} - V_{SWN1,2}$  needs to be above the threshold  $V_{BST1,2} - V_{SWN1,2\_UVth}$ . In order to recharge the bootstrap capacitor, sporadic switching activity could also be observed when PWM1,2 = LOW and LOOPCTRL.CH1,2.PWM\_1,2 =



**Power Supply**

LOW. In ACTIVE state the device current consumption via  $V_{IN}$  and  $V_{DD}$  is dependent on the external MOSFET used and the switching frequency  $f_{SW}$ .



**Figure 6 Simplified State Diagram**

**5.2 Different Possibilities to RESET the device**

There are several reset triggers implemented in the device.

After any kind of reset, the Transmission Error Flag (TER) is set to HIGH.

**Under Voltage Reset:**

EN/INUVLO: When EN/INUVLO is below  $V_{EN/INUVLOth}$  (P\_5.3.7), the SPI interface is not working and all the registers are reset to their default values. In addition, the device enters SLEEP mode and the current consumption is minimized.

VDD: When  $V_{VDD}$  is below  $V_{VDD(UV)}$  (P\_5.3.6), the SPI interface is not working and all the registers are reset to their default values.

**Reset via SPI command:**

There is a command (DVCCTRL.SWRST = HIGH) available to RESET all writeable registers to their default values. Note that the result coming from the Calibration routine, which is readable by the SPI when LOOPCTRL\_CH1,2.ENCAL\_CH1,2 = HIGH, is not reset by the SWRST.

**Reset via Limp Home:**

When Limp Home state is detected the registers are reset to the default values.

**Power Supply**

**5.3 Electrical Characteristics**

**Table 5 EC Power Supply**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

| Parameter                                       | Symbol                | Values |      |      | Unit          | Note or Test Condition   | Number   |
|---|-----------------------|--------|------|------|---------------|--|----------|
|   |                       | Min.   | Typ. | Max. |               |  |          |
| <b>Power Supply <math>V_{IN}</math></b>         |                       |        |      |      |               |  |          |
| Input Voltage Startup                           | $V_{VIN(ON)}$         | –      | –    | 4.7  | V             | $V_{IN}$ increasing;<br>$V_{EN/INUVLO} = \text{HIGH}$ ;<br>$V_{DD} = 5\text{ V}$ ;<br>$IVCC = IVCC\_EXT = 10\text{ mA}$ ;                      | P_5.3.1  |
| Input Undervoltage switch OFF                   | $V_{VIN(OFF)}$        | –      | –    | 4.5  | V             | $V_{IN}$ decreasing;<br>$V_{EN/INUVLO} = \text{HIGH}$ ;<br>$V_{DD} = 5\text{ V}$ ;<br>$IVCC = IVCC\_EXT = 10\text{ mA}$ ;                      | P_5.3.14 |
| Device operating current                        | $I_{VIN(ACTIVE)}$     | –      | 6.2  | 9    | mA            | <sup>1)</sup> ACTIVE mode;<br>$V_{PWM1,2} = 0\text{ V}$ ;  | P_5.3.2  |
| $V_{IN}$ Sleep mode supply current              | $I_{VIN(SLEEP)}$      | –      | –    | 1.5  | $\mu\text{A}$ | $V_{EN/INUVLO} = 0\text{ V}$ ;<br>$V_{CSN} = V_{DD} = 5\text{ V}$ ;<br>$V_{IN} = 13.5\text{ V}$ ;<br>$V_{IVCC} = V_{IVCC\_EXT} = 0\text{ V}$ ; | P_5.3.3  |
| <b>Digital Power Supply <math>V_{DD}</math></b> |                       |        |      |      |               |  |          |
| Digital supply current                          | $I_{VDD}$             | –      | –    | 0.5  | mA            | $V_{IN} = 13.5\text{ V}$ ;<br>$f_{SCLK} = 0\text{ Hz}$ ;<br>$V_{PWM1,2} = 0\text{ V}$ ;<br>$V_{EN} = V_{CSN} = V_{DD} = 5\text{ V}$ ;          | P_5.3.4  |
| Digital Supply Sleep mode current               | $I_{VDD(SLEEP)}$      | –      | –    | 1.5  | $\mu\text{A}$ | $V_{EN/INUVLO} = 0\text{ V}$ ;<br>$V_{CSN} = V_{DD} = 5\text{ V}$ ;<br>$V_{IN} = 13.5\text{ V}$ ;<br>$V_{IVCC} = V_{IVCC\_EXT} = 0\text{ V}$ ; | P_5.3.5  |
| Undervoltage shutdown threshold voltage         | $V_{VDD(UV)}$         | 1      | –    | 3    | V             | $V_{CSN} = V_{DD}$ ;<br>$V_{SI} = V_{SCLK} = 0\text{ V}$ ;<br>SO from LOW to HIGH impedance;   | P_5.3.6  |
| <b>EN/INUVLO Pin characteristics</b>            |                       |        |      |      |               |  |          |
| Input Undervoltage falling Threshold            | $V_{EN/INUVLOth}$     | 1.6    | 1.75 | 1.9  | V             | –  | P_5.3.7  |
| EN/INUVLO Rising Hysteresis                     | $V_{EN/INUVLO(hyst)}$ | –      | 90   | –    | mV            | <sup>1)</sup>  | P_5.3.8  |
| EN/INUVLO input Current LOW                     | $I_{EN/INUVLO(LOW)}$  | 0.45   | 0.89 | 1.34 | $\mu\text{A}$ | $V_{EN/INUVLO} = 0.8\text{ V}$ ;   | P_5.3.9  |

**Power Supply**

**Table 5 EC Power Supply (cont'd)**

$V_{IN} = 8\text{ V to }36\text{ V}$ ,  $T_J = -40^\circ\text{C to }+150^\circ\text{C}$ , all voltages with respect to AGND; (unless otherwise specified)

| Parameter                    | Symbol                | Values |      |      | Unit          | Note or Test Condition        | Number   |
|------------------------------|-----------------------|--------|------|------|---------------|-------------------------------|----------|
|                              |                       | Min.   | Typ. | Max. |               |                               |          |
| EN/INUVLO input Current HIGH | $I_{EN/INUVLO(HIGH)}$ | 1.1    | 2.2  | 3.3  | $\mu\text{A}$ | $V_{EN/INUVLO} = 2\text{ V};$ | P_5.3.10 |

**LHI Pin characteristics**

|                           |              |     |    |     |               |                           |          |
|---------------------------|--------------|-----|----|-----|---------------|---------------------------|----------|
| LOW level                 | $V_{LHI(L)}$ | 0   | -  | 0.8 | V             | -                         | P_5.3.16 |
| HIGH level                | $V_{LHI(H)}$ | 2.0 | -  | 5.5 | V             | -                         | P_5.3.17 |
| L-Input pull-down current | $I_{LHI(L)}$ | 6   | 12 | 18  | $\mu\text{A}$ | $V_{LHI} = 0.8\text{ V};$ | P_5.3.18 |
| H-Input pull-down current | $I_{LHI(H)}$ | 15  | 30 | 45  | $\mu\text{A}$ | $V_{LHI} = 2.0\text{ V};$ | P_5.3.19 |

**Timings**

|                           |              |   |   |     |    |   |          |
|---------------------------|--------------|---|---|-----|----|---|----------|
| SLEEP mode to ACTIVE time | $t_{ACTIVE}$ | - | - | 0.7 | ms | 1)<br>$V_{IVCC} = V_{IVCC\_EXT};$<br>$C_{IVCC} = 10\ \mu\text{F};$<br>$V_{IN} = 13.5\text{ V};$<br>$V_{DD} = 5\text{ V};$ | P_5.3.11 |
|---------------------------|--------------|---|---|-----|----|---|----------|

1) Not subject to production test, specified by design.

## Regulator Description

### 6 Regulator Description

The TLD5541-2QV includes all of the functions necessary to provide constant current to the output as usually required to drive LEDs. A voltage mode regulation can also be implemented (Refer to [Chapter 6.6](#)).

In deep buck applications, due to duty cycle limitations ( $D_{\text{BUCK\_MIN}}$ ) the device will enter pulse skipping mode in order to keep regulating the average output current, the output ripple may increase.

The minimum duty cycle is dependent by the  $f_{\text{sw}}$ .

A SPI flag provides mode feedback to the  $\mu\text{C}$  (refer to SPI bits `FAULTS_CH1, 2.REGUMODFB_CH1, 2`).

#### 6.1 Regulator Diagram Description

An analog current control loop (A5, A4 with compressive gain =  $IFBx_{\text{gm}}$ ) connected to the sensing pins FBL1,2, FBH1,2 regulates the output current.

The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current.

An external compensation network ( $R_{\text{COMP}}, C_{\text{COMP}}$ ) is used to adjust the control loop to various application boundary conditions.

The inductor current for the current mode loop is sensed by the  $R_{\text{SWCS}}$  resistor.

$R_{\text{SWCS}}$  is used also to limit the maximum external switches / inductor current.

If the Voltage across  $R_{\text{SWCS}}$  exceeds its overcurrent threshold ( $V_{\text{SWCS1,2\_buck}}$  or  $V_{\text{SWCS1,2\_boost}}$  for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit.

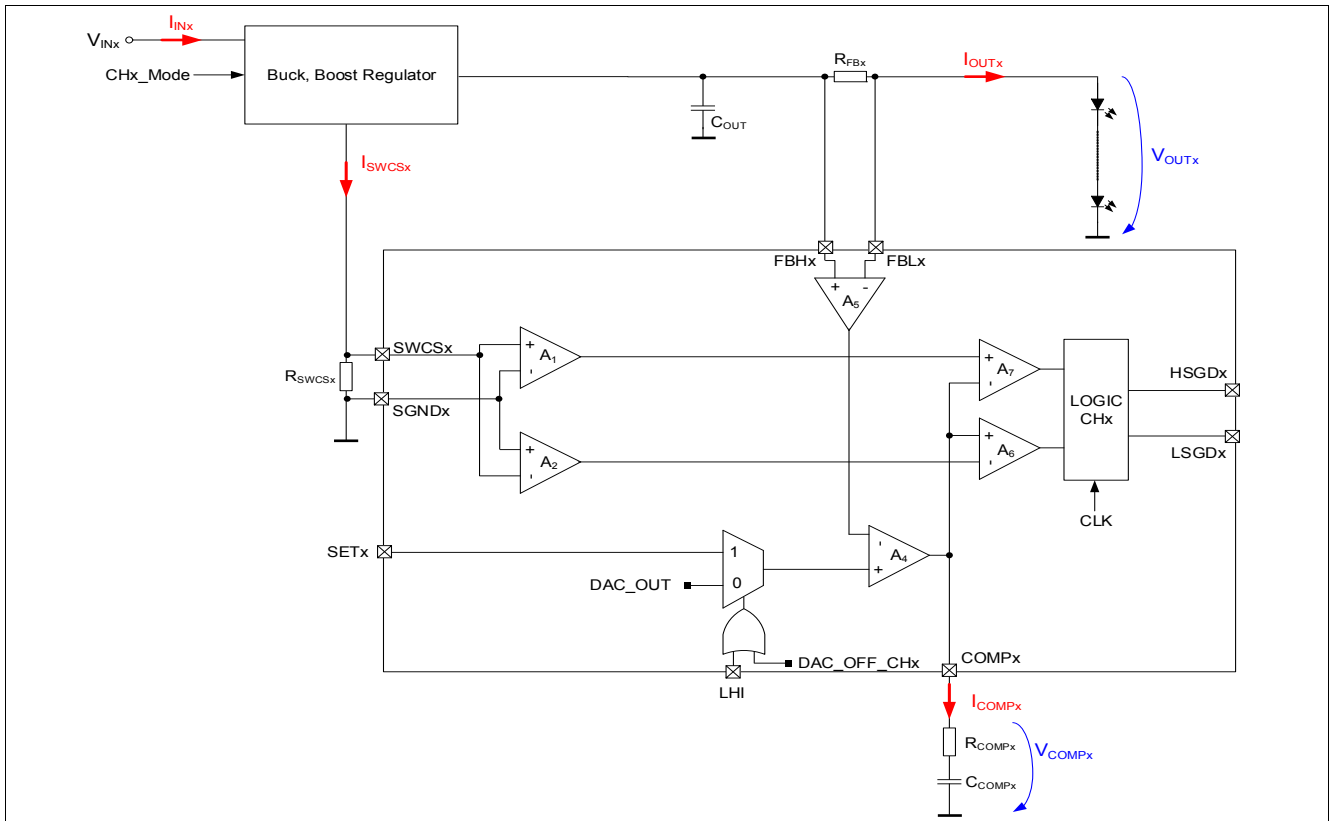
The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations.

The control loop logic block (LOGIC\_CHx) provides a PWM signal to two internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in a multitopology configuration. Once the soft start expires a forced CCM regulation mode is performed.

The control loop block diagram displayed in [Figure 7](#) shows a typical constant current application. The voltage across  $R_{\text{FB}}$  sets the output current.

The output current is fixed via the SPI parameter (`LEDCURRADIM_CH1, 2.ADIMVAL_CH1, 2 = 11110000B` = default at 100%) plus an offset trimming (`LEDCURRCAL_CH1, 2.CALIBVAL_CH1, 2 = 0000B` = default in the middle of the range). Refer to [Chapter 8.1](#) for more details.

**Regulator Description**



**Figure 7 Regulator Block Diagram (similar for both Channels) - TLD5541-2QV**

**Regulator Description**

**6.2 Adjustable Soft Start Ramp**

The soft start routine limits the current through the inductor and the external MOSFET switches during initialization to minimize potential overshoots at the output.

The soft start routine is applied:

- At first turn on (first PWM rise after EN = High)
- After Output Short to GND detection
- After channel stop via low analog dimming value (see [Chapter 8](#) for details)

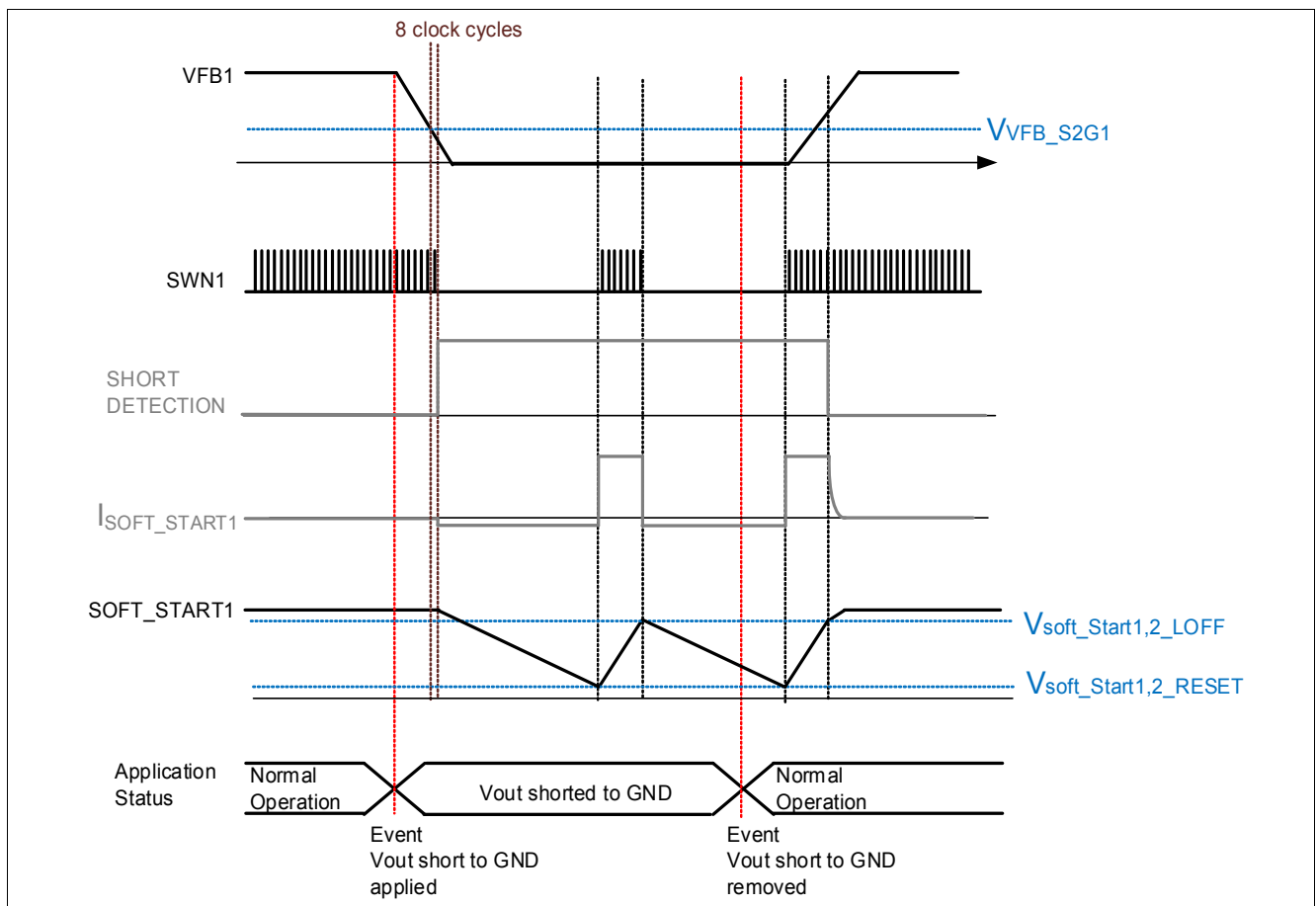
The soft start rising edge gradually increases the current of the inductor ( $L_{OUT}$ ) over  $t_{SOFT\_START1,2}$  by clamping the COMP1,2 voltage. The soft start ramp is defined by a capacitor placed at the SOFT\_START1,2 pin.

Selection of the SOFT\_START1,2 capacitor ( $C_{SOFT\_START1,2}$ ) can be done according to the approximate formula described in [Equation \(6.1\)](#):

$$t_{SOFT\_START1,2} = \frac{0.9V}{I_{SOFT\_START1,2(PU)}} \cdot C_{SOFT\_START1,2} \tag{6.1}$$

The SOFT\_START1,2 pins are also used to implement a fault mask and wait-before-retry time, on rising and falling edge respectively, see [Figure 8](#) and chapter [Chapter 10.2](#) for details.

If a short on the output is detected, a pull-down current source  $I_{SOFT\_START1,2\_PD}$  (P\_6.4.59) is activated. This current brings down the  $V_{SOFT\_START1,2}$  until  $V_{SOFT\_START1,2\_RESET}$  (P\_6.4.61) is reached, then the pull-up current source  $I_{SOFT\_START1,2\_PU}$  (P\_6.4.58) turns on again. If the fault condition hasn't been removed until  $V_{SOFT\_START1,2\_LOFF}$  (P\_6.4.60) is reached, the pull-down current source turns back on again, initiating a new cycle. This will continue until the fault is removed.



**Figure 8 Soft Start timing diagram on a short to ground detected by the VFB1 pin**

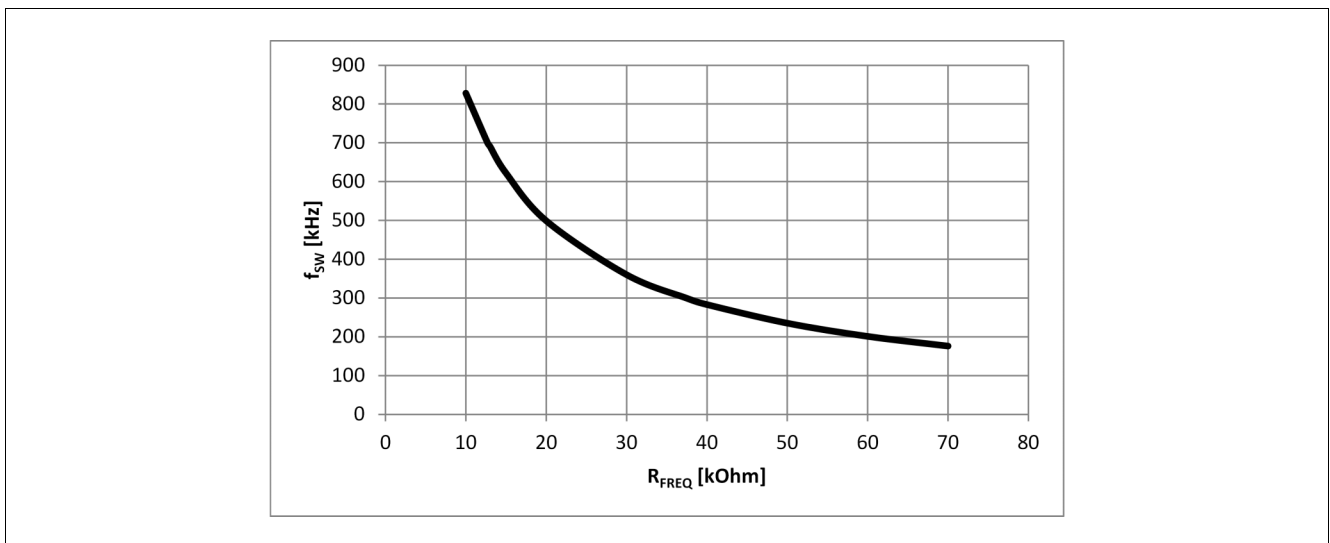
## Regulator Description

### 6.3 Switching Frequency setup

The switching frequency can be set from 200 kHz to 700 kHz by an external resistor connected from the FREQ pin to GND or by supplying a sync signal as specified in chapter [Chapter 11.2](#). Select the switching frequency with an external resistor according to the graph in [Figure 9](#) or the following approximate formulas.

$$f_{SW} [kHz] = 5375 * (R_{FREQ} [k\Omega])^{-0.8} \quad (6.2)$$

$$R_{FREQ} [k\Omega] = 46023 * (f_{SW} [kHz])^{-1.25} \quad (6.3)$$



**Figure 9** Switching Frequency  $f_{SW}$  versus Frequency Select Resistor to GND  $R_{FREQ}$

### 6.4 Fast Output Discharge Operation Mode

During load changes in a multi-floating switches (MFS) application (series connection of LEDs with parallel short circuit switches for each LED) the voltage on the output capacitor ( $C_{OUT}$ ) will create a current spike at the output. The fast output discharge feature limits the current spike during load jump events and prevents a damage to the LED chain connected at the output.

The TLD5541-2QV has a dedicated state machine which ensures a safe and fast dynamic load step transition in Multifloatswitch applications.

After a trigger command via SPI (`MFSSETUP1_CH1, 2.SOMFS_CH1, 2 = HIGH`), the TLD5541-2QV stops regulating the output current and enters a voltage regulation via VFB1,2 which actively “discharges” the output capacitor ( $C_{OUT}$ ). The new output voltage target value is automatically calculated by the TLD5541-2QV, using the information of the new load connected to the output, sent by the  $\mu C$  via a 4Bit command (`MFSSETUP1_CH1, 2.LEDCHAIN_CH1, 2`).

An adjustable preparation time  $t_{prep}$  (`MFSSETUP2_CH1, 2.MFSDLY_CH1, 2`) is used to drive the load.

#### Calculation of preparation time $t_{prep}$ :

The [Equation \(6.4\)](#) below describes the relationship between the switching frequency  $f_{SW}$  and the content of `MFSSETUP2_CH1, 2.MFSDLY_CH1, 2` register.

$$t_{prep} = \frac{1}{f_{SW}} \cdot [2 + (MFSDLY\_CH1, 2)_{dec}] \quad (6.4)$$

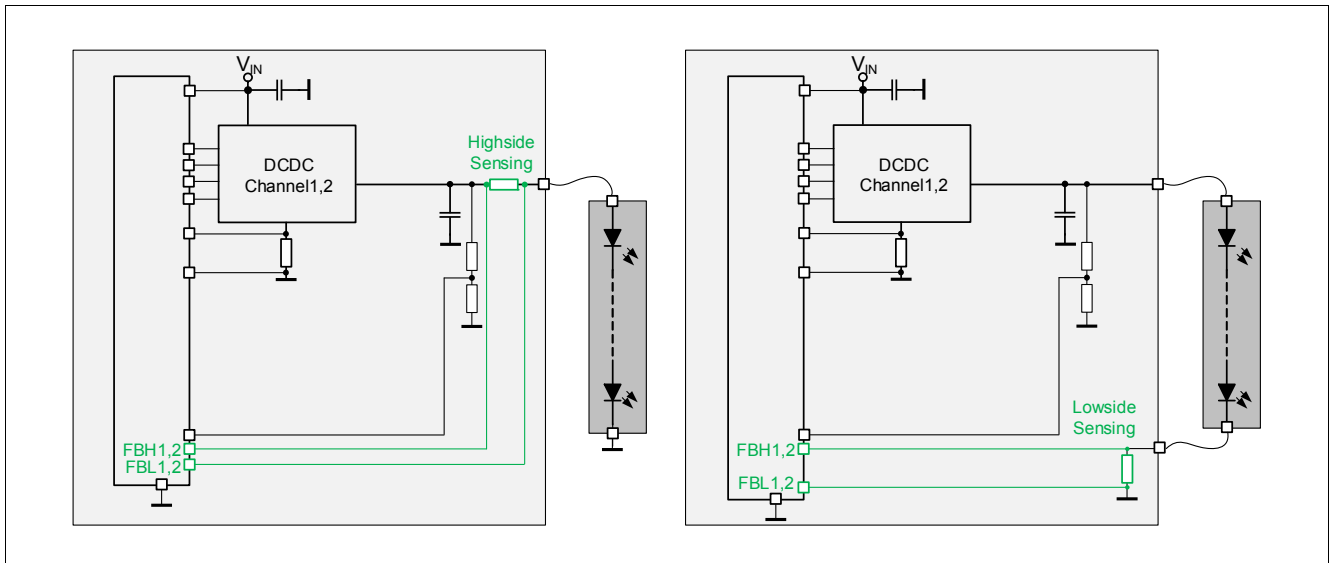
**Regulator Description**

**6.5 Flexible current sense (Buck Only)**

The flexible current sense implementation enables highside and lowside current sensing when the device operates in buck mode.

Due to the short circuit protection threshold  $V_{FBH\_S2G}$  the low side sensing is not possible (and not recommended) in boost to ground applications.

The **Figure 10** displays the application examples for the highside and lowside current sense concept.



**Figure 10 Highside and lowside current sensing - TLD5541-2QV**



**Regulator Description**

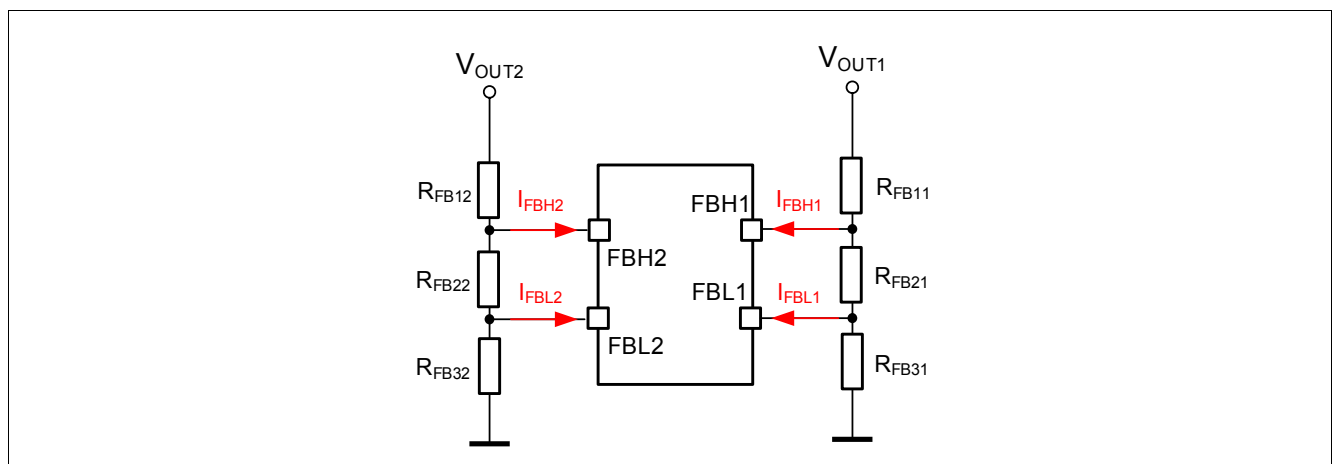
**6.6 Programming Output Voltage (Constant Voltage Regulation)**

For a voltage regulator, the output voltage can be set by selecting the values  $R_{FBx1}$ ,  $R_{FBx2}$  and  $R_{FBx3}$  according to the following **Equation (6.5)**:

$$V_{OUT1,2} = \left( I_{FBH1,2} + \frac{V_{FBH1,2} - V_{FBL1,2}}{R_{FB21,2}} \right) \cdot R_{FB1,2} + \left( \frac{V_{FBH1,2} - V_{FBL1,2}}{R_{FB21,2}} - I_{FBL1,2} \right) \cdot R_{FB31,2} + V_{FBH1,2} - V_{FBL1,2} \quad (6.5)$$

After the output voltage is fixed via the resistor divider, the value can be changed via the Analog Dimming bits ADIMVAL\_CH1, 2.

If Analog dimming is performed, due to the variations on the  $I_{FBL}$  ( $I_{FBL1,2\_HSS}$  (P\_6.4.52) and  $I_{FBL1,2\_LSS}$  (P\_6.4.54)) current on the entire voltage spanning, a non linearity on the output voltage may be observed. To minimize this effect RFBx resistors should be properly dimensioned.



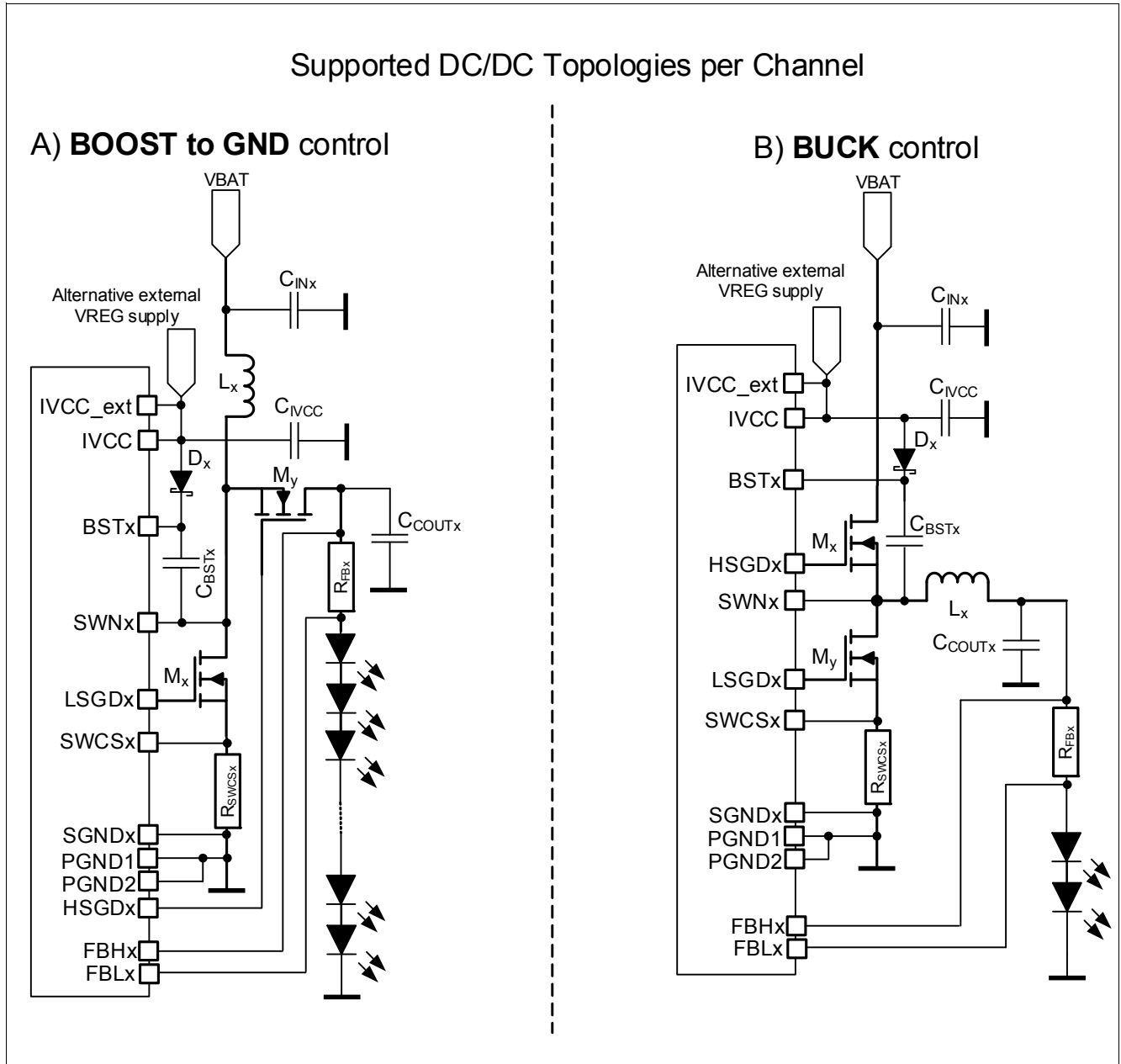
**Figure 11 Programming Output Voltage (Constant Voltage Regulation)**

**Regulator Description**

**6.7 Topologies for Dual Channel SYNC**

Each channel of the TLD5541-2QV can be used in BOOST and BUCK topologies. A voltage and current regulation can be configured. Furthermore a multiphase operation can be achieved via a parallel connection of the two outputs.

The **Figure 12** displays the supported DC/DC topologies per channel.



**Figure 12 Supported DC/DC topologies per channel**