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TLE4253

Low Dropout Voltage Tracking Regulator

Automotive Power

Never stop thinking

Low Dropout Voltage Tracking Regulator   **TLE4253GS**
TLE4253

1 Overview

Features

- Tight output tracking tolerance to reference
- Output voltage adjust down to 2.0 V
- Stable with ceramic output capacitor
- Flexibility of output voltage adjust higher or lower than reference, proportional to the reference voltage
- 250 mA output current capability
- Low dropout voltage
- Combined tracking / enable input
- Very low current consumption in OFF mode
- PG-DSO-8 packages with lowest thermal resistance
- Wide input voltage range -42 V $\leq V_I \leq$ 45 V
- Wide temperature range: -40 °C $\leq T_j \leq$ 150 °C
- Output protected against short circuit to GND and battery
- Overtemperature protection
- Reverse polarity proof
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)
- AEC Qualified
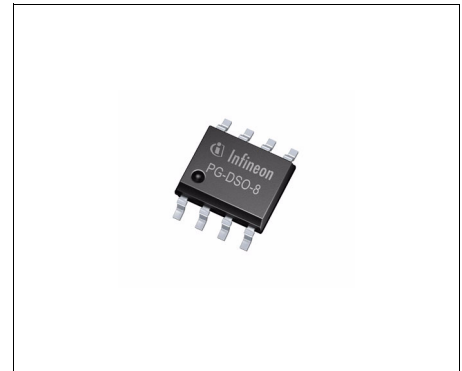
PG-DSO-8
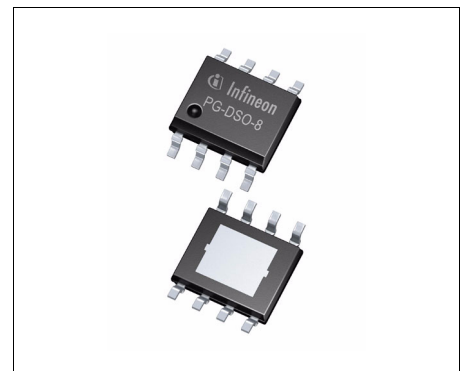
PG-DSO-8 exposed pad

Functional Description

The TLE4253 is a monolithic integrated low-dropout voltage tracking regulator in small PG-DSO-8 packages. The exposed pad (EP) package variant PG-DSO-8 exposed pad offers extremely low thermal resistance. The IC is designed to supply off-board systems, e. g. sensors in engine management systems under the severe conditions of automotive applications. Therefore, the IC is equipped with additional protection functions against reverse polarity and short circuit to GND and battery.

With supply voltages up to 40 V, the output voltage follows a reference voltage applied at the adjust input with high accuracy. The reference voltage applied directly to the adjust input or by an e. g. external resistor divider can be 2.0 V at minimum.

The output is able to drive loads up to 250 mA at minimum while the device follows the e. g. 5 V output of a main voltage regulator acting as reference with high accuracy.

The TLE4253 tracker can be set into shutdown mode in order to reduce the quiescent current to an extremly low value. This makes the IC suitable to low power battery applications.

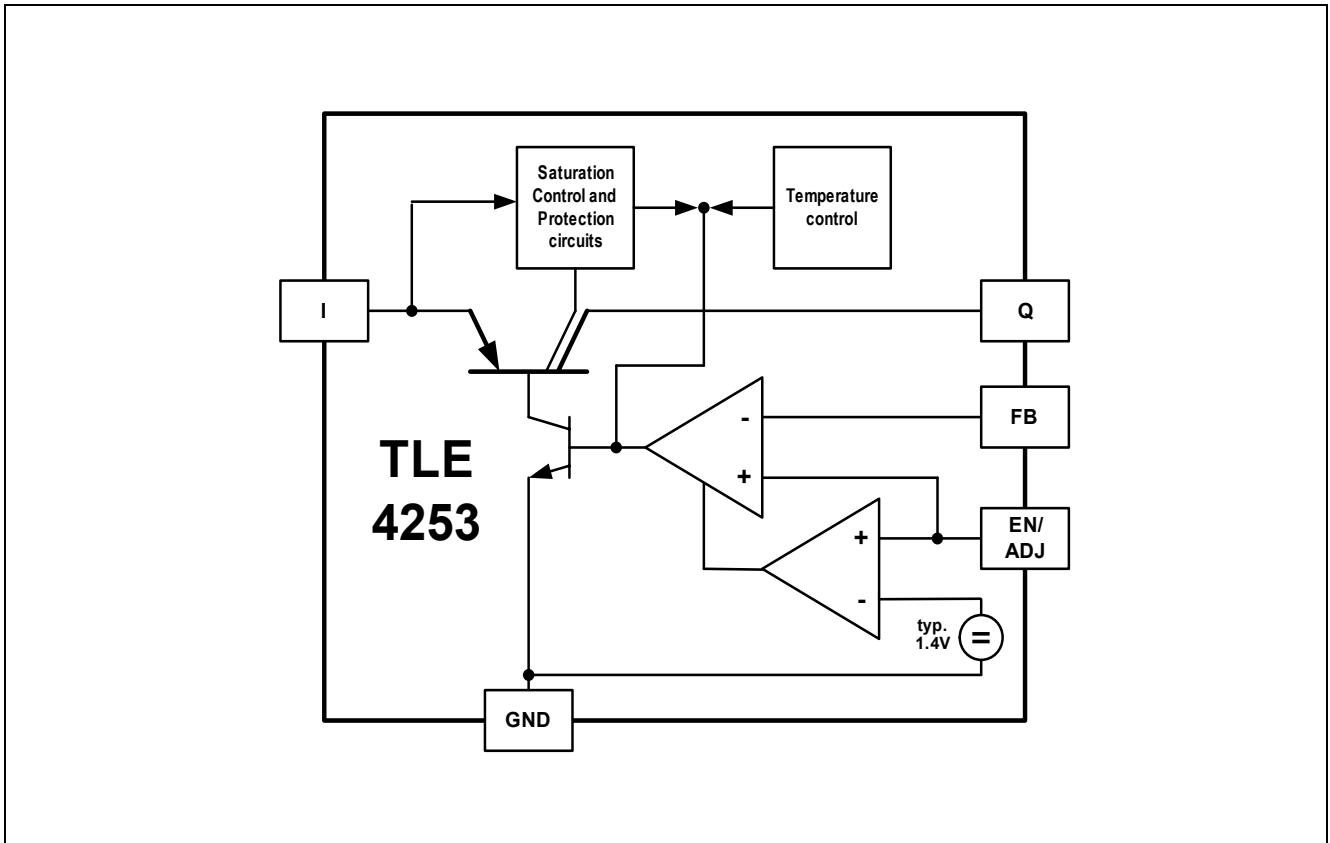| Type	Package	Marking
TLE4253GS	PG-DSO-8	4253
TLE4253E	PG-DSO-8 exposed pad	4253E

2 Block Diagram

Figure 1   Block Diagram

3 Pin Configuration

3.1 Pin Assignment
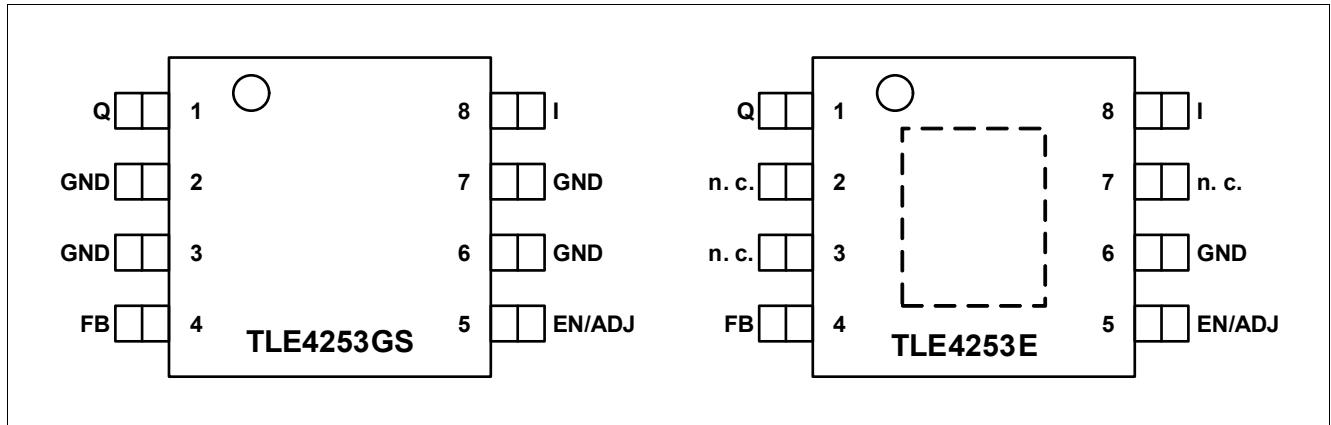
Figure 2 Pin Configuration and Block Diagram

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	Q	**Tracker Output.** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table "Functional Range".
2, 3, 6, 7	GND	**Ground reference** (version TLE4253GS only)**.** Interconnect the pins on PCB. Connect to heatsink area.
6	GND	**Ground** (version TLE4253E only)**.** Connect to exposed pad.
2, 3, 7	n. c.	**Not connected** (version TLE4253E only)**.** Connect to GND externally.
4	FB	**Feedback input for tracker.** Non inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage and connect a voltage divider for higher output voltages than the reference (see application information).
5	EN/ADJ	**Adjust / Enable.** Connect the reference to this pin. The active high signal of the reference turns on the device, with active low the tracker is disabled. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see application information).
8	I	**Input.** IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.
–	EP	**Exposed pad** (version TLE4253E only)**.** Attach the exposed pad on package bottom to the heatsink area on circuit board. Connect to GND.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

-40 °C $\leq T_j \leq$ 150 °C; all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	**Max.**		
Voltages						
4.1.1	Input voltage	V_I	-42	45	V	–
4.1.2	Output voltage	V_Q	-2	45	V	–
4.1.3	Adjust / Enable Input	$V_{ADJ/EN}$	-42	45	V	–
4.1.4	Feedback Input	V_{FB}	-42	45	V	–
Temperature						
4.1.5	Junction Temperature	T_j	-40	150	°C	–
4.1.6	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Rating						
4.1.7	ESD Susceptibility	$V_{ESD,HBM}$	-4	4	kV	HBM[2]
4.1.8		$V_{ESD,CDM}$	-1	1	kV	CDM[3]

1) Not subject to production test, specified by design.
2) ESD susceptibility Human Body Model "HBM" according to EIA/JESD 22-A 114B.
3) ESD susceptibility Charged Device Model "CDM" according to EIA/JESD22-C101 or ESDA STM5.3.1.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage	V_I	3.5	40	V	$V_I \geq V_Q + V_{dr}$
4.2.1	Adjust / Enable Input Voltage (Voltage Tracking Range)	$V_{ADJ/EN}$	2.0	–	V	–
4.2.2	Junction Temperature	T_j	-40	150	°C	–
4.2.3	Output Capacitor Requirements	C_Q	10		µF	–[1]
4.2.4		ESR_{CQ}	–	5	Ω	–[2]

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

2) relevant ESR value at f = 10 kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Value			Unit	Conditions
			Min.	Typ.	Max.		

PG-DSO-8:

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
4.3.1	Junction to Soldering Point	R_{thJSP}	–	39	–	K/W	Pins 2 - 3 and 6 - 7 fixed to T_A
4.3.2	Junction to Ambient	R_{thJA}	–	150	–	K/W	Footprint only [1]
4.3.3			–	91	–	K/W	300 mm^2 PCB heatsink area [1]
4.3.4			–	81	–	K/W	600 mm^2 PCB heatsink area [1]
4.3.5			–	65	–	K/W	2s2p board[2]

PG-DSO-8 exposed pad:

Pos.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
4.3.6	Junction to Case Bottom	R_{thJC}	–	9	–	K/W	Measured to exposed bottom pad
4.3.7	Junction to Ambient	R_{thJA}	–	169	–	K/W	Footprint only [1]
4.3.8			–	64	–	K/W	300 mm^2 PCB heatsink area [1]
4.3.9			–	55	–	K/W	600 mm^2 PCB heatsink area [1]
4.3.10			–	49	–	K/W	2s2p board[2]

1) Package mounted on PCB FR4; 80 x 80 x 1.5 mm; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow.
Not subject to production test; specified by design.

2) Specified R_{thJA} value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).
Where applicable a thermal via array under the package contacted the first inner copper layer.

5 Electrical Characteristics

5.1 Tracking Regulator

The output voltage V_Q is controlled by comparing it to the voltage applied at pin ADJ/EN and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Functional Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor C_I is strongly recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages.

An overtemperature protection circuit prevents the IC from immediate destruction under fault conditions (e. g. output continuously short-circuited to GND) by reducing the output current. A thermal balance below 200 °C junction temperature is established. Please note that a junction temperature above 150 °C is outside the maximum ratings and reduces the IC lifetime.

The TLE4253 allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance graph. The thermal protection circuit is not operating during reverse polarity condition.

Table 1   Electrical Characteristics Tracking Regulator

V_I = 13.5 V; $V_{ADJ/EN} \geq 2.0$ V; $V_{FB} = V_Q$; -40 °C $\leq T_j \leq$ 150 °C;
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.1.1	Output Voltage Tracking Accuracy	ΔV_Q	-5	–	5	mV	I_Q = 30 mA; $V_{ADJ/EN}$ = 5 V
5.1.2	$\Delta V_Q = V_{EN/ADJ} - V_Q$		-10	–	10	mV	0.1 mA $\leq I_Q \leq$ 200 mA; 3.5 V $\leq V_I \leq$ 32 V; $V_{ADJ/EN}$ = 2 V
5.1.3			-15	–	15	mV	0.1 mA $\leq I_Q \leq$ 250 mA; 9 V $\leq V_I \leq$ 32 V; $V_{ADJ/EN}$ = 5 V
5.1.4	Load Regulation steady-state	$|dV_{Q,load}|$	–	–	10	mV	I_Q = 0.1 mA to 200 mA; $V_{ADJ/EN}$ = 5 V
5.1.5	Line Regulation steady-state	$|dV_{Q,line}|$	–	–	10	mV	V_I = 6 V to 32 V; I_Q = 10 mA; $V_{ADJ/EN}$ = 5 V
5.1.6	Power Supply Ripple Rejection	$PSRR$	60	–	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; C_Q = 10 µF, ceramic type [1]

Table 1   Electrical Characteristics Tracking Regulator

V_I = 13.5 V; $V_{ADJ/EN} \geq 2.0$ V; $V_{FB} = V_Q$; -40 °C $\leq T_j \leq$ 150 °C;
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.1.7	Dropout Voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	280	600	mV	I_Q = 200 mA [2]
5.1.8	Output Current Limitation	$I_{Q,max}$	251	400	600	mA	$V_Q = (V_{ADJ}$ - 0.1 V); $V_{ADJ/EN}$ = 5 V
5.1.9	Reverse Current	I_Q	-10	-5.5	–	mA	V_I = 0 V; V_Q = 16 V; $V_{ADJ/EN}$ = 5 V
5.1.10	Reverse Current at Negative Input Voltage	I_I	-5	-2	–	mA	V_I = -16 V; V_Q = 0 V; $V_{ADJ/EN}$ = 5 V
Feedback Input FB:							
5.1.11	Feedback Input Biasing Current	I_{FB}		0.1	0.5	µA	V_{FB} = 5 V
Overtemperature Protection:							
5.1.12	Junction Temperature Equilibrium	$T_{j,eq}$	151	–	200	°C	T_j increasing due to power dissipation generated by the IC[1]

1) Parameter not subject to production test; specified by design.
2) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

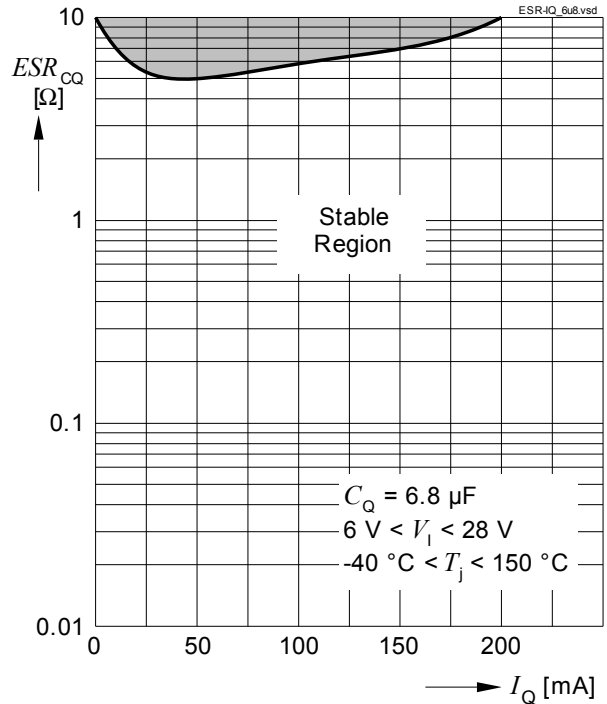**Typical Performance Characteristics Tracking Regulator**

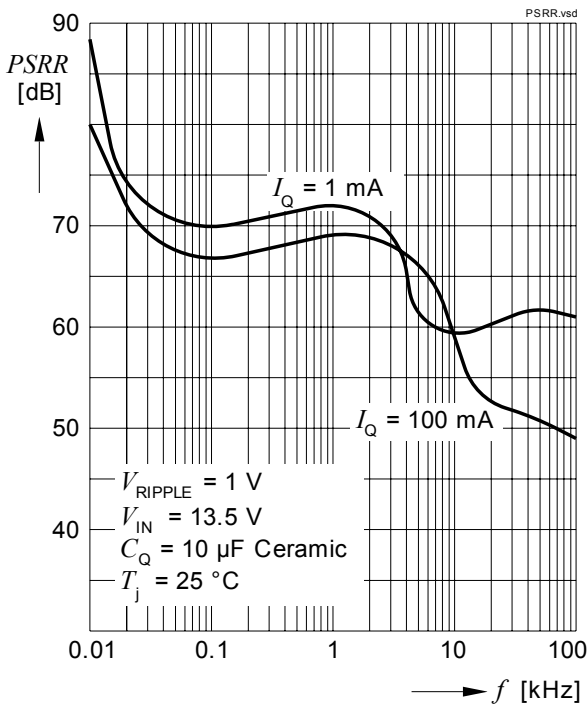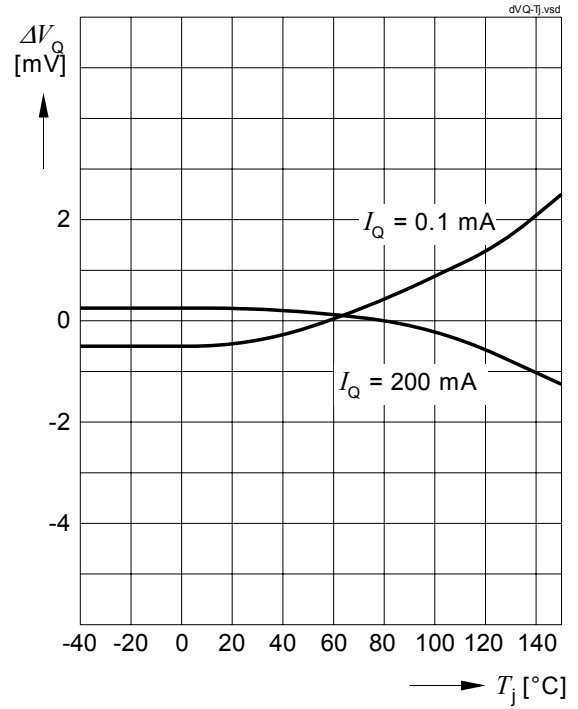$V_{ADJ/EN}$ = 5 V; V_{FB} = V_Q (unless otherwise noted)

Output Voltage V_Q vs.
**Adjust Voltage V_{ADJ}**

VQ-VADJ.vsd

V_Q [V]

V_I = 13.5 V

T_j = 150 °C

T_j = -40 °C

V_{ADJ} [V]
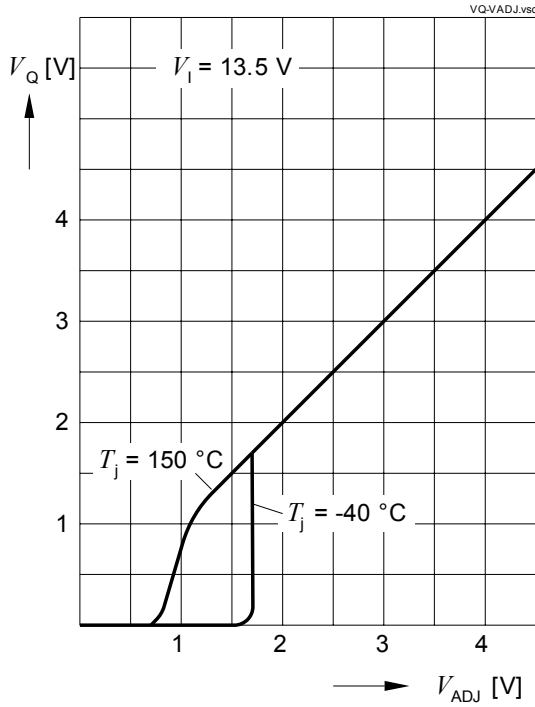
Output Voltage V_Q vs.
Input Voltage V_I

VQ-VI.vsd

V_Q [V]

V_{dr}

V_{ADJ} = 5 V

T_j = -40 °C

T_j = 150 °C

V_I [V]
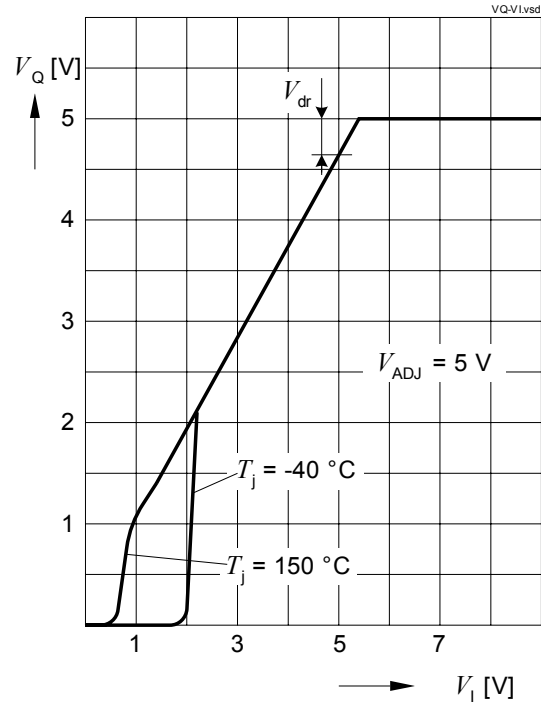
Output Current Limitation $I_{Q,max}$ vs.
Input Voltage V_I

SOA.VSD

I_Q [mA]

T_j = 25 °C

T_j = 125 °C

V_{ADJ} = 5 V

V_I [V]
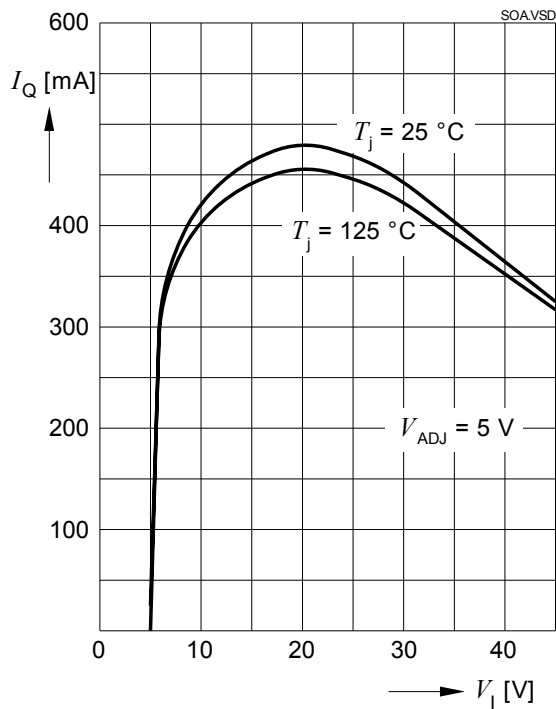
Output Current Limitation $I_{Q,max}$ vs.
Output Voltage V_Q
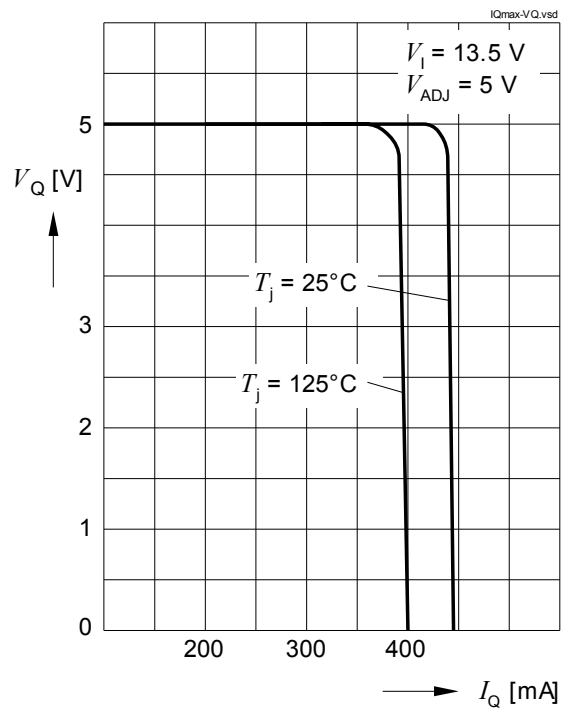
IQmax-VQ.vsd

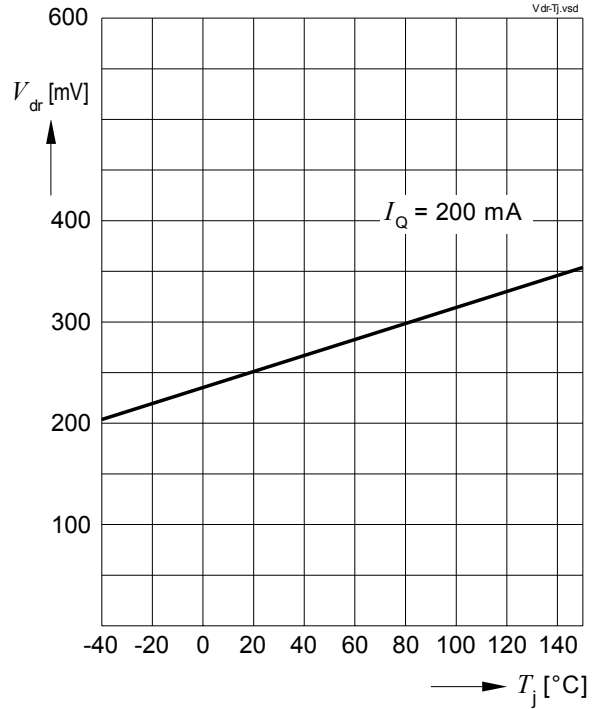V_I = 13.5 V
V_{ADJ} = 5 V

V_Q [V]

T_j = 25°C

T_j = 125°C

I_Q [mA]

Typical Performance Characteristics Tracking Regulator

$V_{ADJ/EN}$ = 5 V; V_{FB} = V_Q (unless otherwise noted)

Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q
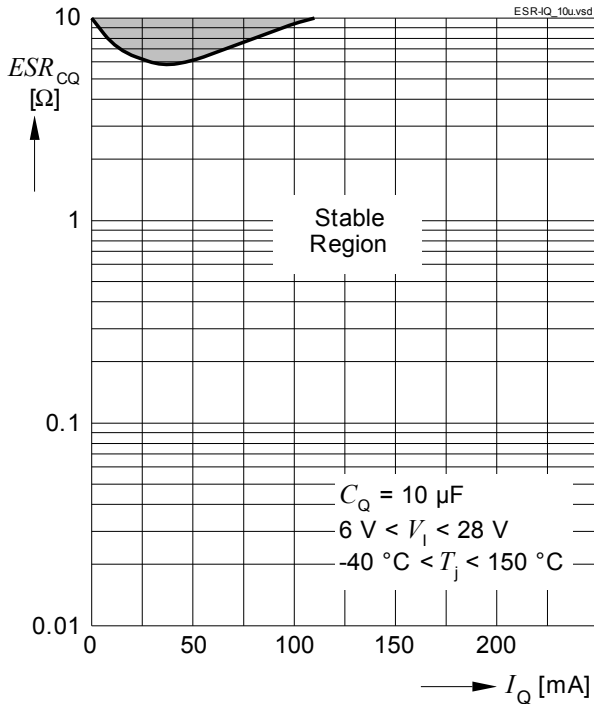
C_Q = 10 µF
6 V < V_I < 28 V
-40 °C < T_j < 150 °C

Output Capacitor Series Resistor ESR_{CQ} vs. Output Current I_Q

C_Q = 6.8 µF
6 V < V_I < 28 V
-40 °C < T_j < 150 °C

Power Supply Ripple Rejection $PSRR$

I_Q = 1 mA

I_Q = 100 mA

V_{RIPPLE} = 1 V
V_{IN} = 13.5 V
C_Q = 10 µF Ceramic
T_j = 25 °C

Line Regulation d$V_{Q,line}$ vs. Input Voltage Change dV_I
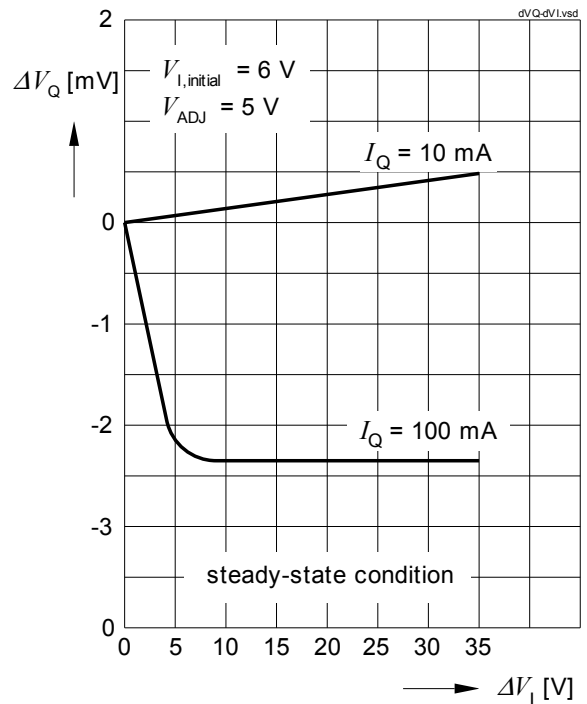
$V_{I,initial}$ = 6 V
V_{ADJ} = 5 V

I_Q = 10 mA

I_Q = 100 mA

steady-state condition

Typical Performance Characteristics Tracking Regulator

$V_{\text{ADJ/EN}}$ = 5 V; V_{FB} = V_Q (unless otherwise noted)

Load Regulation d$V_{\text{Q,line}}$ vs. Output Current Change dI_Q
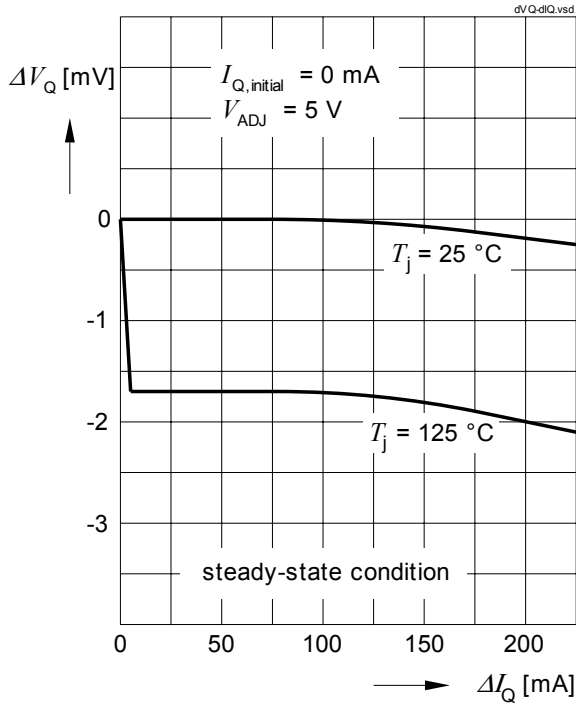
Tracking Accuracy ΔV_Q vs. Junction Temperature T_j

Line Transient Response
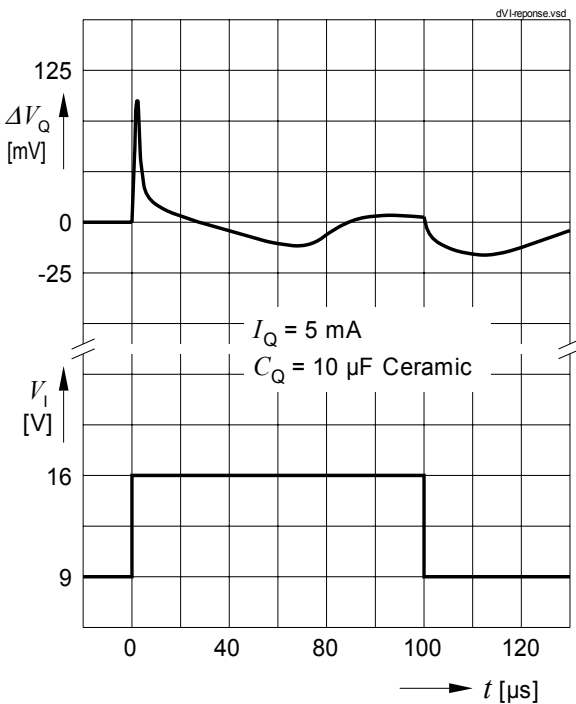
Load Transient Response
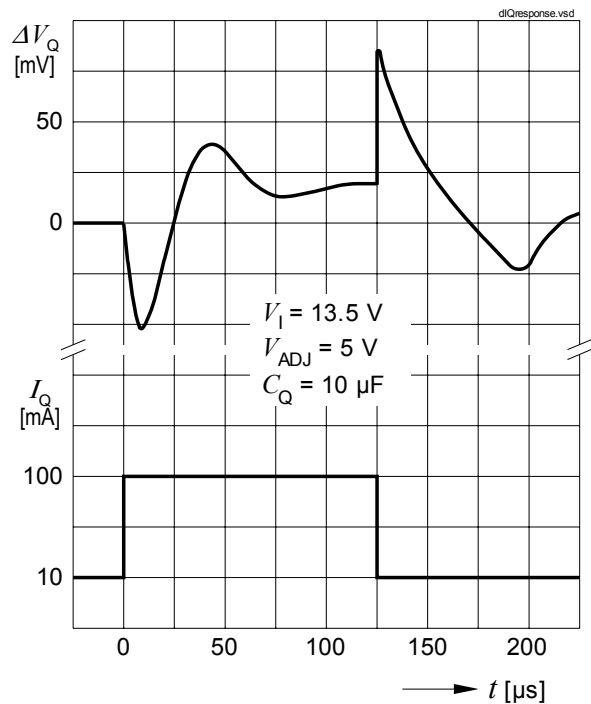
Typical Performance Characteristics Tracking Regulator

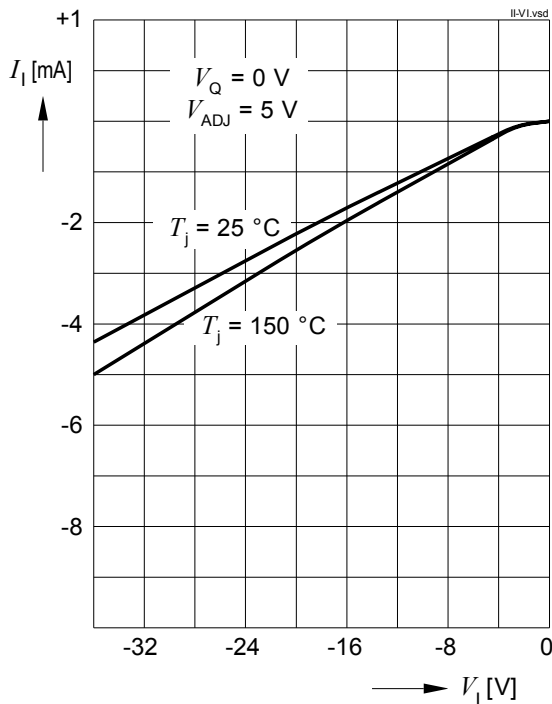$V_{ADJ/EN}$ = 5 V; V_{FB} = V_Q (unless otherwise noted)

Dropout Voltage V_{dr} vs.
Output Current I_Q
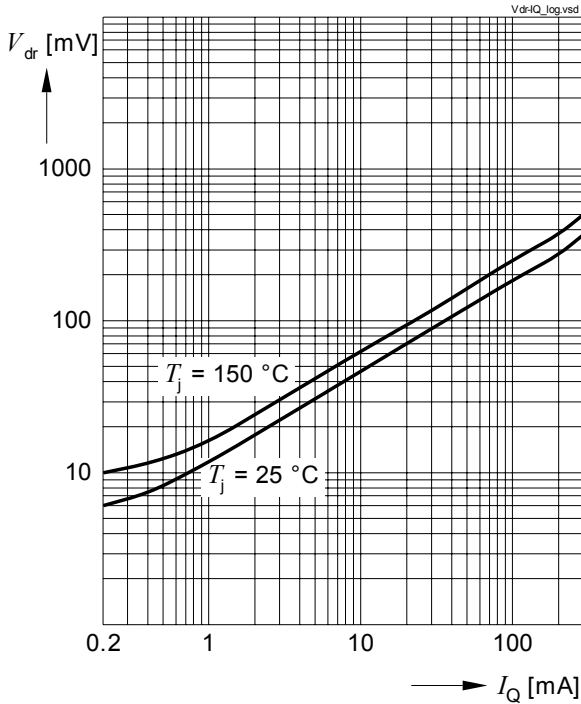
Dropout Voltage V_{dr} vs.
Junction Temperature T_j

Reverse Current I_I vs.
Input Voltage V_I

Reverse Output Current I_Q vs.
Output Voltage V_Q
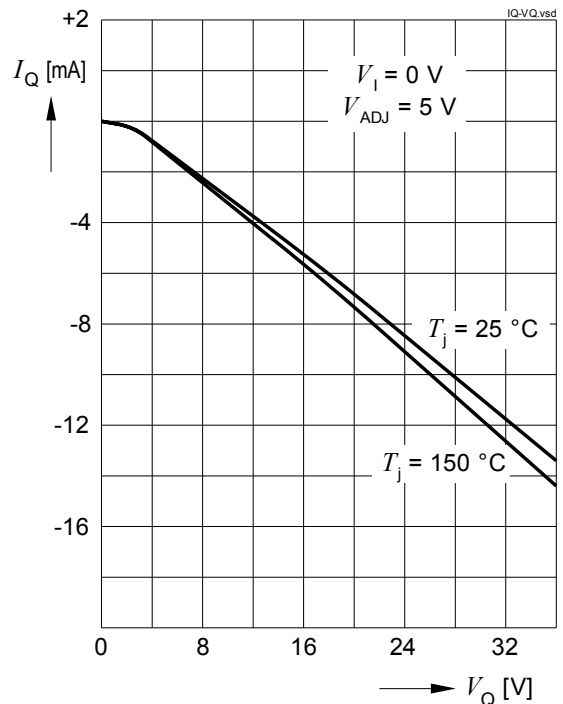
5.2 Current Consumption

**Table 2   Electrical Characteristics Current Consumption**

V_I = 13.5 V; $V_{ADJ/EN} \geq$ 2.0 V; $V_{FB} = V_Q$; -40 °C $\leq T_j \leq$ 150 °C;
all voltages with respect to ground (unless otherwise specified).

| Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.1	Quiescent Current Stand-by Mode	I_{q1}	–	0	2	µA	V_Q = 0 V; $V_{ADJ/EN} \leq$ 0.4 V; $T_j \leq$ 85 °C
5.2.2	Current Consumption $I_q = I_I - I_Q$	I_{q2}	–	120	150	µA	$I_Q \leq$ 100 µA; $V_{ADJ/EN}$ = 5 V; $T_j \leq$ 85 °C
5.2.3			–	7	15	mA	$I_Q \leq$ 200 mA; $V_{ADJ/EN}$ = 5 V
5.2.4	Current Consumption Dropout Region; $I_q = I_I - I_Q$	I_{q3}	–	1	3	mA	$V_{ADJ} = V_I$ = 5 V; I_Q = 0 mA

Typical Performance Characteristics Tracking Regulator

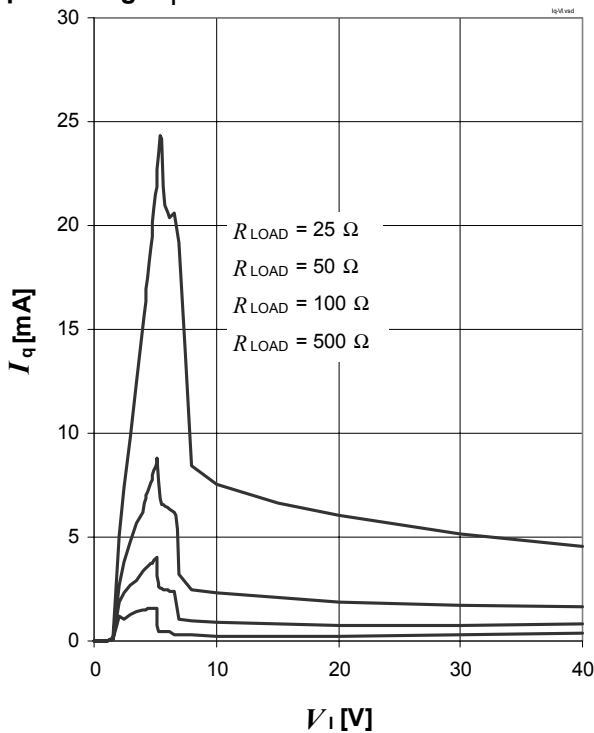$V_{ADJ/EN}$ = 5 V; V_{FB} = V_Q (unless otherwise noted)

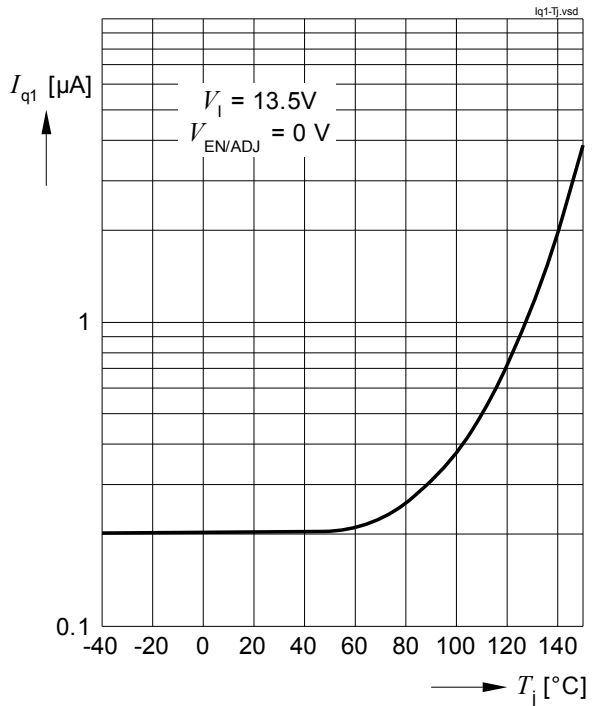### Current Consumption I_{q2} vs. Junction Temperature T_j
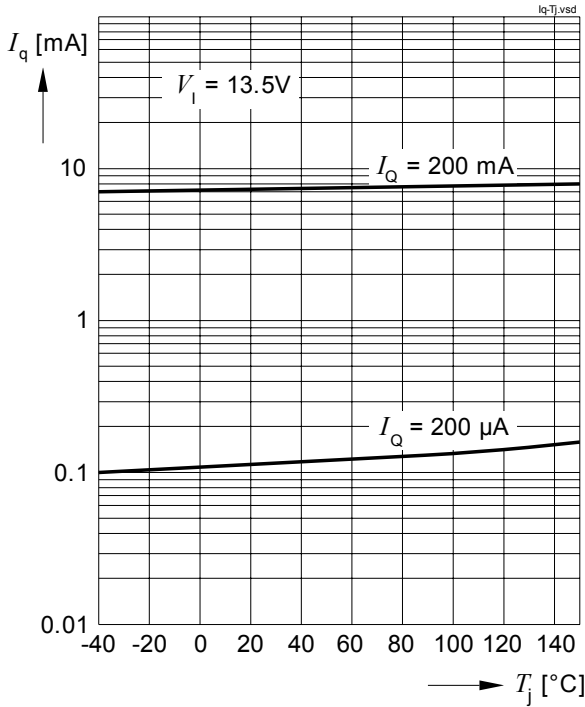
Current Consumption I_q vs. Output Current I_Q
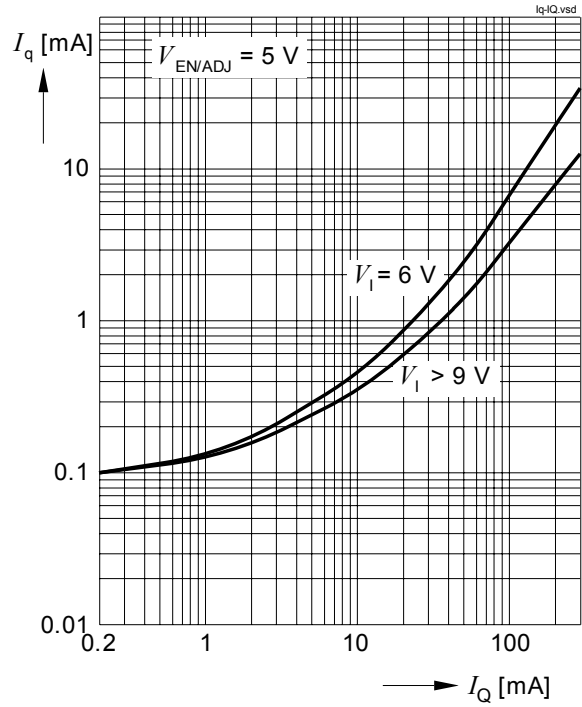
Current Consumption I_q vs. Input Voltage V_I

Quiescent Current I_{q1} vs. Junction Temperature T_j

5.3 Adjust / Enable Input

In order to reduce the quiescent current to a minimum, the TLE4253 can be switched to stand-by mode by setting the adjust/enable input "ADJ/EN" to "low".

In case the pin "ADJ/EN is left open, an internal pull-down resistor keeps the voltage at the pin low and therefore ensures that the regulator is switched off.

Table 3 Electrical Characteristics Adjust / Enable

V_I = 13.5 V; $V_{ADJ/EN} \geq 2.0$ V; $V_{FB} = V_Q$; -40 °C $\leq T_j \leq$ 150 °C;
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	**Typ.**	**Max.**		
5.3.1	Adjust / Enable Low Signal Valid	$V_{ADJ/EN,low}$	–	–	0.4	V	V_Q = 0 V; I_I < 2 µA; $T_j \leq$ 85 °C
5.3.2	Adjust / Enable High Signal Valid (Tracking Region)	$V_{ADJ/EN,high}$	2	–	–	V	V_Q settled: $\|V_Q - V_{ADJ/EN}\|$ < 10 mV; I_Q = 10 mA
5.3.3	Adjust / Enable Input Current	$I_{ADJ/EN}$	–	3.8	5.5	µA	$V_{ADJ/EN}$ = 5 V;
5.3.4	Adjust / Enable internal pull-down resistor	$R_{ADJ/EN}$	1	1.5	2	MΩ	

Typical Performance Characteristics Tracking Regulator

$V_{ADJ/EN}$ = 5 V; $V_{FB} = V_Q$ (unless otherwise noted)

Startup Sequence
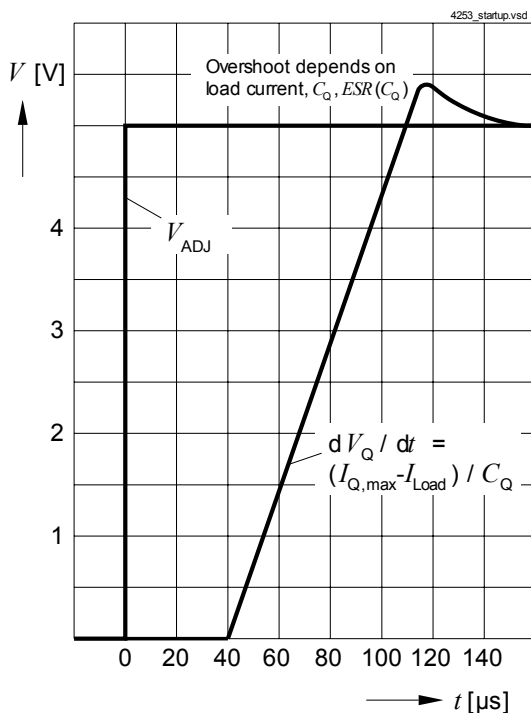
6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.
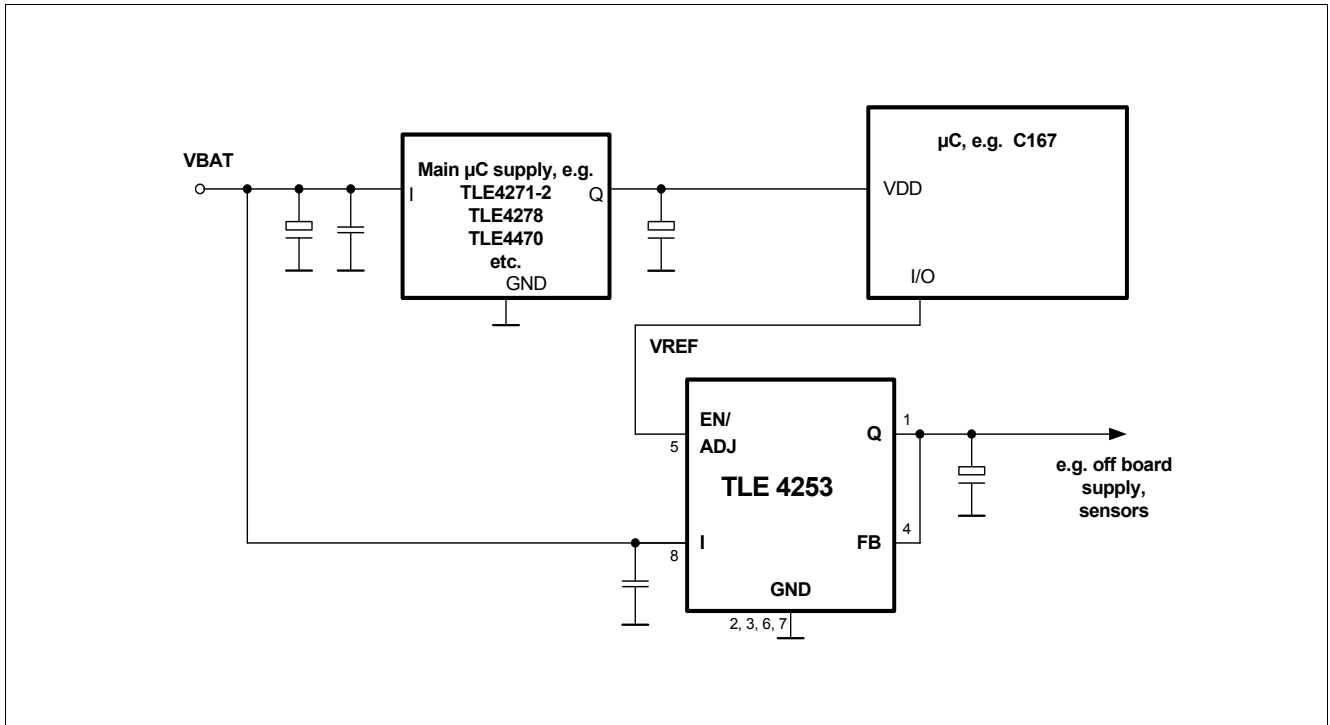*The application circuits shown are simplified examples. The function must be verified in the real application.*

Figure 3 Application circuit: Output voltage V_Q equal to reference voltage V_{REF}

Figure 3 shows the typical schematic for applications where the tracker output voltage equals the reference voltage V_{REF} applied to the pin "EN/ADJ". The pin "FB" is connected directly to the output. The reference voltage is directly applied "EN/ADJ".
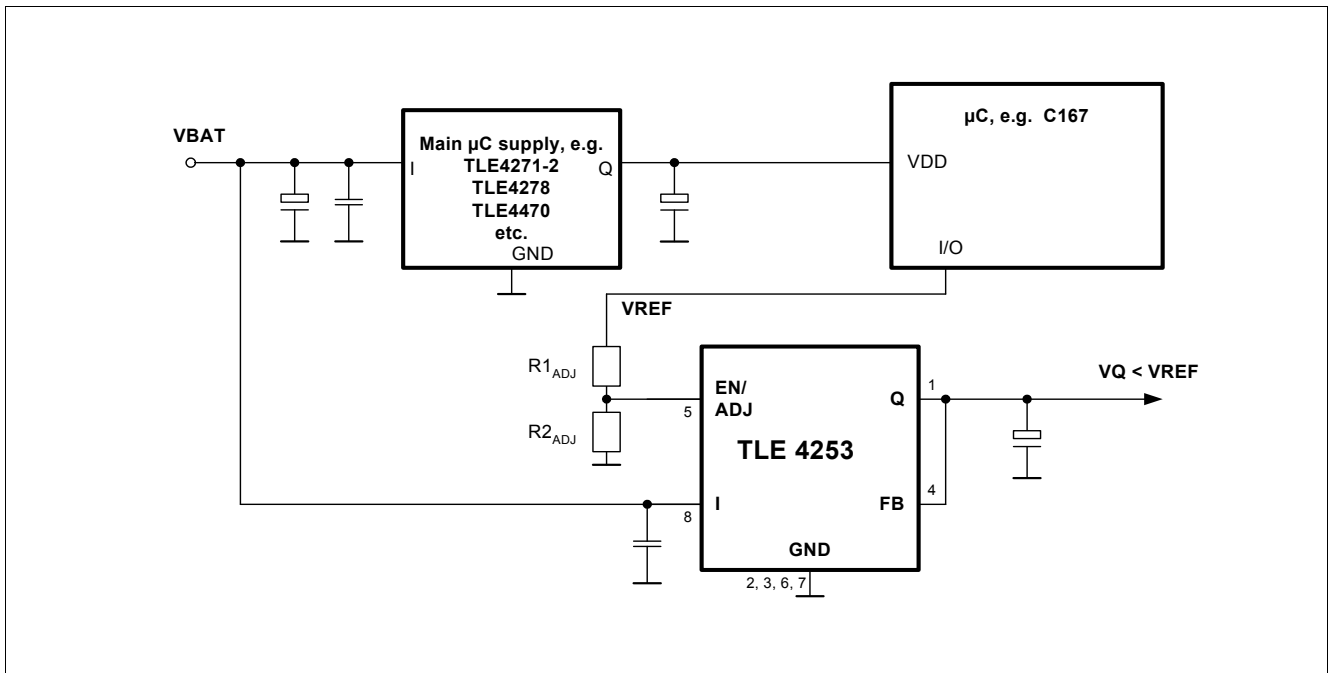
Figure 4 **Application circuit: Output voltage V_Q lower than reference voltage V_{REF}**

In order to obtain a lower output voltage V_Q at the tracker output than the reference voltage V_{REF}, a voltage divider according to Figure 4 has to be used. The output voltage V_Q then calculates:

$$V_Q = V_{REF} \cdot \left(\frac{R2_{ADJ}}{R1_{ADJ} + R2_{ADJ}} \right)$$

With a given reference voltage V_{REF}, the desired output voltage V_Q and the resistor value $R1_{ADJ}$, the resistor value for $R2_{ADJ}$ is given by:

$$R2_{ADJ} = R1_{ADJ} \cdot \left(\frac{V_Q}{V_{REF} - V_Q} \right)$$

Taking into consideration also the effect of the internal EN/ADJ pull-down resistor, the external resistor divider's $R2_{ADJ}$ has to be selected to:

$$R2_{ADJ,select} = \left(\frac{R2_{ADJ} \cdot R_{PullDown,min}}{R_{PullDown,min} - R2_{ADJ}} \right)$$
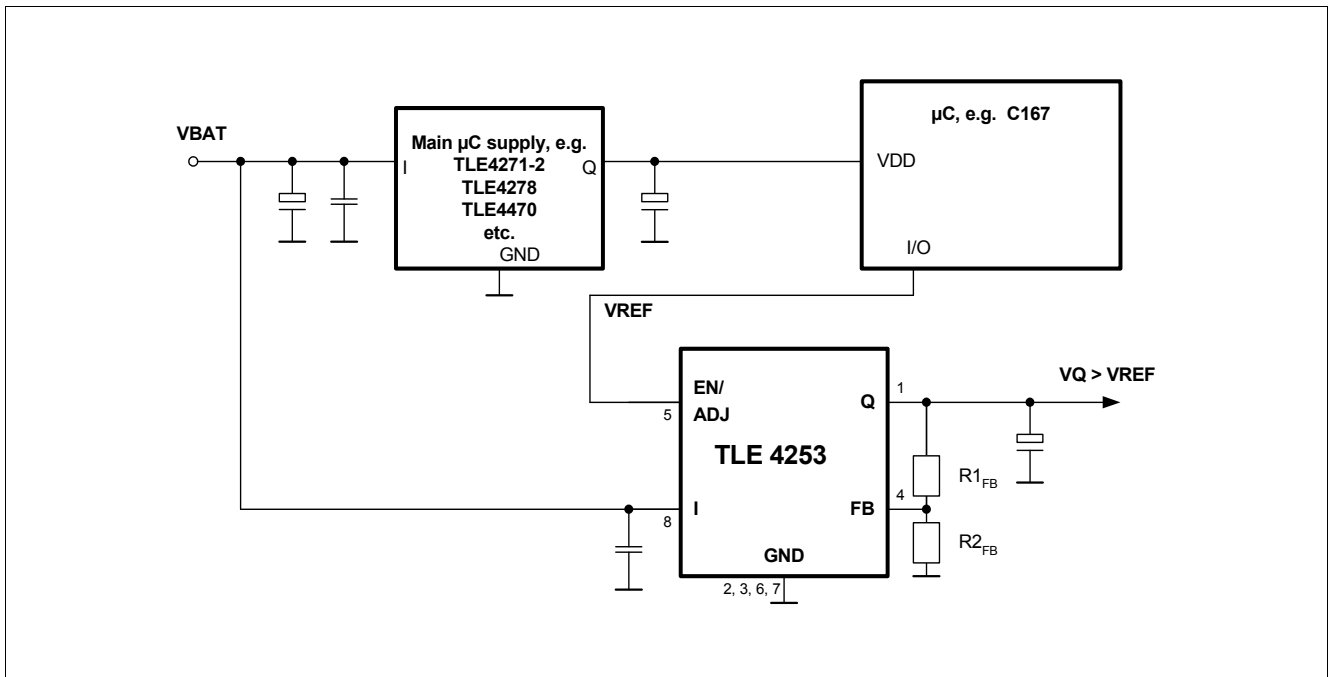
Figure 5 **Application circuit: Output voltage V_Q higher than reference voltage V_{REF}**

For output voltages higher than the reference voltage, the voltage divider has to be applied between the feedback and the output according to Figure 5. The equation for the output voltage with respect to the reference voltage is given by:

$$V_Q = V_{REF} \cdot \left(\frac{R1_{FB} + R2_{FB}}{R2_{FB}} \right)$$

Keep in mind that the input voltage has to be at minimum equal to the output voltage plus the dropout voltage of the regulator.
With a given reference voltage V_{REF}, the desired output voltage V_Q and the resistor value $R1_{FB}$, the resistor value for $R2_{FB}$ is given by:

$$R2_{FB} = R1_{FB} \cdot \left(\frac{V_{REF}}{V_Q - V_{REF}} \right)$$
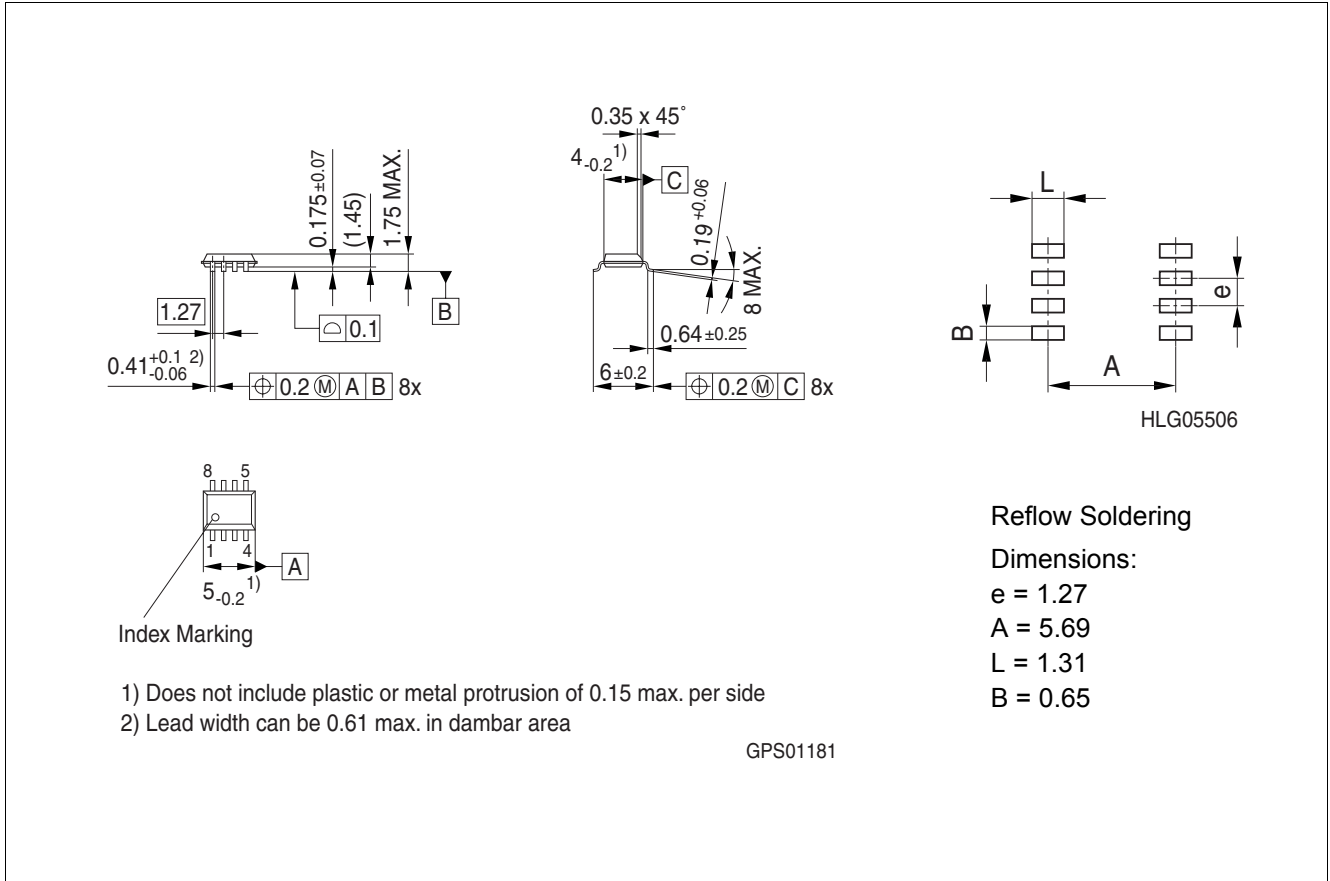
7 Package Outlines

Figure 6   Outline and Footprint PG-DSO-8

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Find all packages, sorts of packing and others at the Infineon Internet Page "Packages":
http://www.infineon.com/packages.
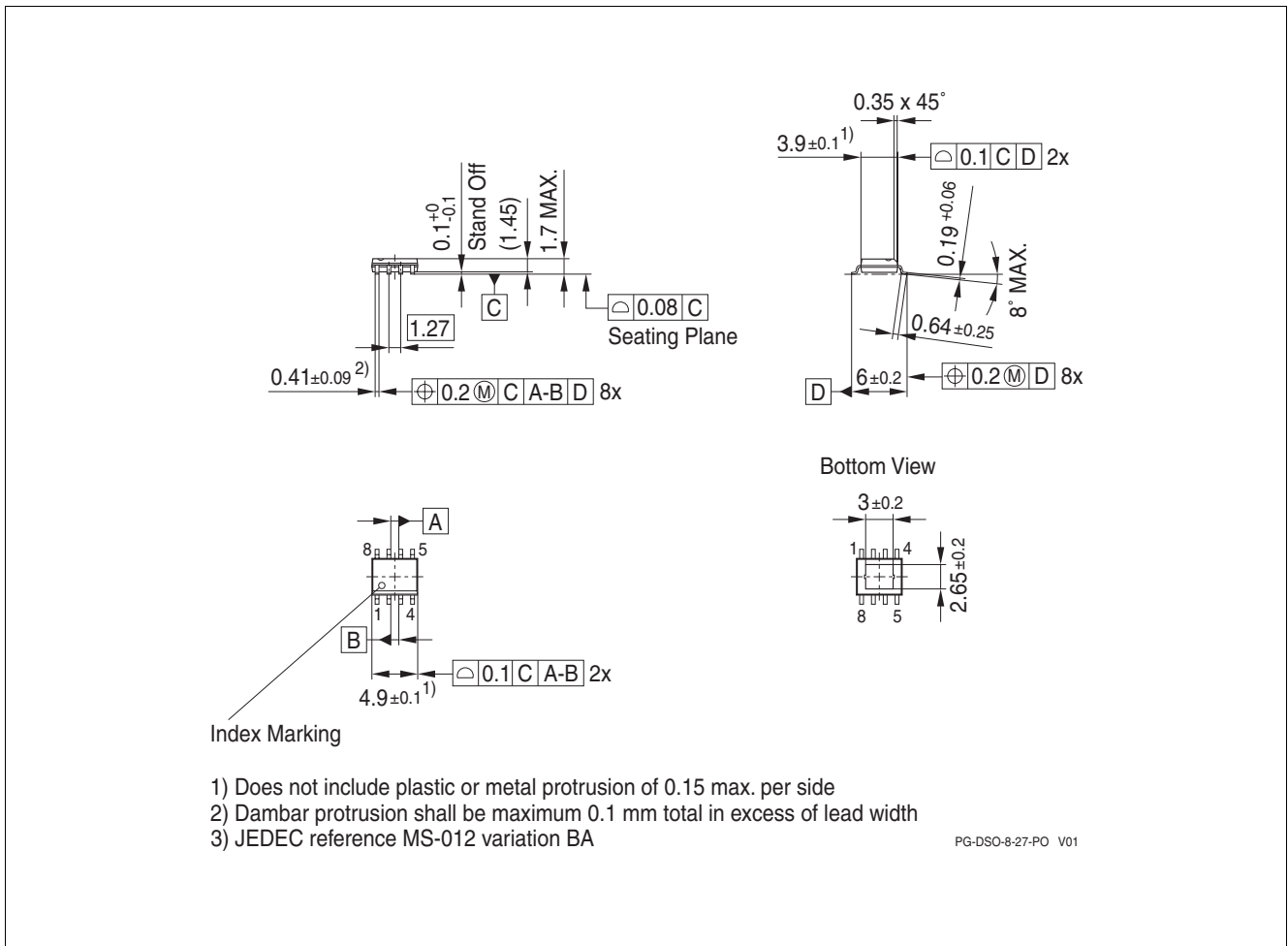
Dimensions in mm

Figure 7   Outline and footprint PG-DSO-8 exposed pad (exposed pad)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Find all packages, sorts of packing and others at the Infineon Internet Page "Packages":
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.2	2009-11-09	Updated Version Data Sheet, version TLE4253E in PG-DSO-8 exposed pad and all related description added:
		In **"Overview" on Page 2** picture for package PG-DSO-8 updated
		In **"Features" on Page 2** "package" replaced by "packages"
		In **"Functional Description" on Page 2** "a small PG-DSO-8 package" replaced by "small PG-DSO-8 packages"; "The exposed pad (EP) package variant PG-DSO-8 exposed pad offers extremely low thermal resistance." added; "suits" replaces by "makes"
		In **"Pin Assignment" on Page 4**, package PG-DSO-8 exposed pad added
		In **"Pin Definitions and Functions" on Page 4** all definition for package PG-DSO-8 exposed pad added
		In **"Thermal Resistance" on Page 6** all values for package PG-DSO-8 exposed pad added (**Item 4.3.6** - **Item 4.3.10**)
		In **"Adjust / Enable Input" on Page 15** typo corrected: "resistors" replaced by "resistor"
		In **"Package Outlines" on Page 19** package PG-DSO-8 exposed pad added
1.1	2008-08-19	Updated Version Final Datasheet for TLE4253GS:
		"Package Outlines" on Page 19 updated;
		In **"Typical Performance Characteristics Tracking Regulator" on Page 14** Graph **"Current Consumption Iq vs. Input VoltageVI" on Page 14** added
1.0	2007-07-10	Initial Final Datasheet for TLE4253GS.
		• For the TLE4253ES (exposed pad) product variant, please refer to the respective datasheet
0.41	2006-01-27	Target Datasheet

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.