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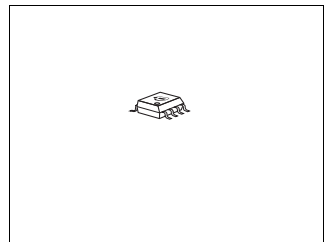
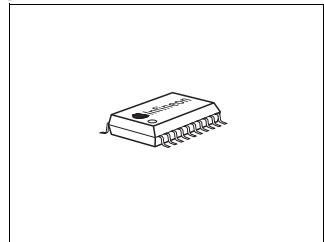
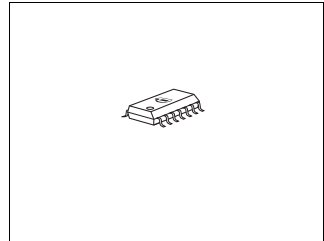
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## Features

- Output voltage tolerance  $\leq \pm 2\%$
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics
- Green Product (RoHS compliant)
- AEC Qualified



## Functional Description

TLE 4263 is a 5-V low drop voltage regulator in a SMD package PG-DSO-14, PG-DSO-20, or PG-DSO-8. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and incorporates temperature protection which turns off the IC at overtemperature.

The IC regulates an input voltage  $V_I$  in the range of  $6\text{ V} < V_I < 45\text{ V}$  to  $V_{Q,nom} = 5.0\text{ V}$ . A reset signal is generated for an output voltage of  $V_{Q,rt} < 4.5\text{ V}$ . This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally by a capacitor. The integrated watchdog logic supervises the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 900  $\mu\text{A}$  to typical 0  $\mu\text{A}$ .

Type	Package	Type	Package
TLE 4263 GS	PG-DSO-8	TLE 4263 GM	PG-DSO-14
TLE 4263 G	PG-DSO-20		

### Choosing External Components

The input capacitor  $C_1$  is necessary for compensation of line influences. Using a resistor of approx.  $1 \Omega$  in series with  $C_1$ , the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values  $\geq 22 \mu\text{F}$  and an ESR of  $\leq 3 \Omega$  within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

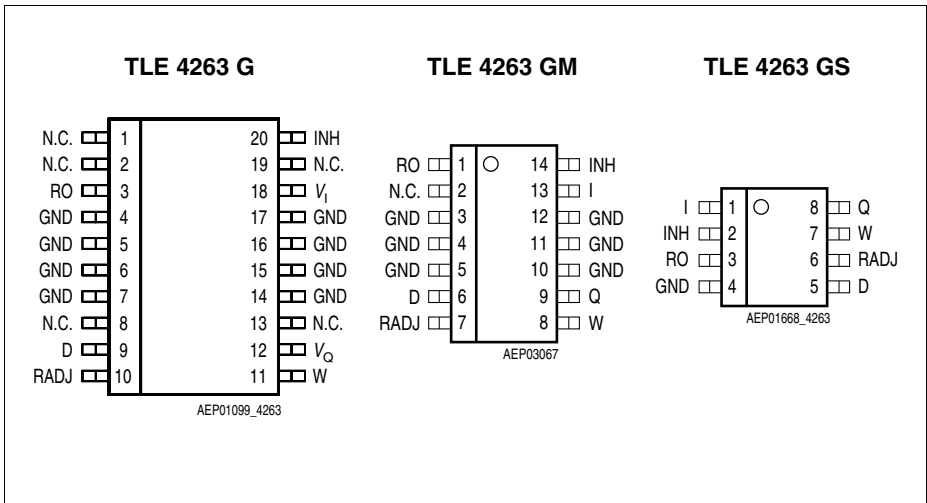


Figure 1 Pin Configuration (top view)

**Table 1 Pin Definitions and Functions**

Pin PG-DSO-14	Pin PG-DSO-20	Pin PG-DSO-8	Symbol	Function
1	3	3	RO	<b>Reset output;</b> open-collector output connected to the output via a resistor of 30 k $\Omega$ .
2	1, 2, 19, 13	–	N.C.	Not connected
3 - 5, 10 - 12	4-7, 14-17	4	GND	Ground
6	9	5	D	<b>Reset delay;</b> connected to ground with a capacitor.
7	10	6	RADJ	<b>Reset threshold;</b> to adjust the switching threshold connect a voltage divider (output to GND) to the pin. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
8	11	7	W	<b>Watchdog;</b> rising edge triggered input for monitoring a microcontroller.
9	12	8	Q	<b>5-V output voltage;</b> block to ground with a capacitor, $C \geq 22 \mu\text{F}$ , $\text{ESR} \leq 3 \Omega$ at 10 kHz
13	18	1	I	<b>Input voltage;</b> block to ground directly at the IC with a ceramic capacitor.
14	20	2	INH	<b>Inhibit;</b> TTL-compatible, low-active input.

### Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold  $V_{DRL}$ , a reset signal occurs at the reset output and is held until the upper threshold  $V_{DU}$  is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typ. 4.65 V. A connected microcontroller will be monitored through the watchdog logic. In case of missing pulses at pin W, the reset output is set to low. The pulse sequence time can be set in a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

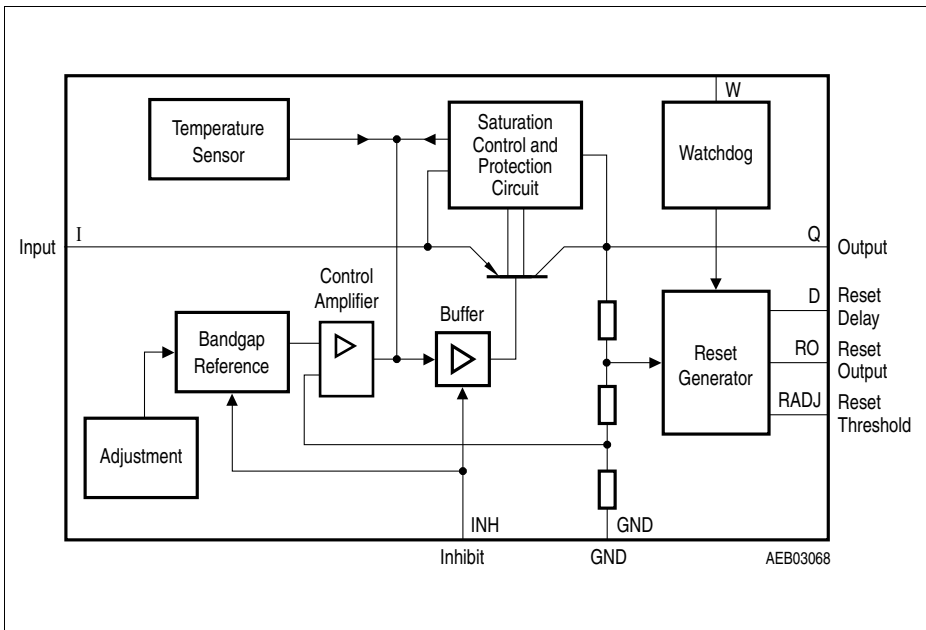


Figure 2 Block Diagram

**Table 2 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
<b>Input I</b>					
Input voltage	$V_I$	-42	45	V	–
Input current	$I_I$	–	–	–	internally limited
<b>Reset Output RO</b>					
Voltage	$V_R$	-0.3	42	V	–
Current	$I_R$	–	–	–	internally limited
<b>Reset Threshold RADJ</b>					
Voltage	$V_{RADJ}$	-0.3	6	V	–
<b>Reset Delay D</b>					
Voltage	$V_D$	-0.3	42	V	–
Current	$I_D$	–	–	–	internally limited
<b>Output Q</b>					
Voltage	$V_Q$	-0.3	7	V	–
Current	$I_Q$	–	–	–	internally limited
<b>Inhibit INH</b>					
Voltage	$V_{INH}$	-42	45	V	–
<b>Watchdog W</b>					
Voltage	$V_W$	-0.3	6	V	–
<b>Ground GND</b>					
Current	$I_{GND}$	-0.5	–	A	–
<b>Temperature</b>					
Junction temperature	$T_j$	–	150	°C	–
Storage temperature	$T_{stg}$	-50	150	°C	–
<b>Operating Range</b>					
Input voltage	$V_I$	–	45	V	–
Junction temperature	$T_j$	-40	150	°C	–

**Table 2 Absolute Maximum Ratings (cont'd)**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
<b>Thermal Resistance</b>					
Junction-ambient	$R_{thj-a}$	–	112	K/W	PG-DSO-14 <sup>1)</sup> ; Footprint only
		–	92	K/W	PG-DSO-14 <sup>1)</sup> ; 300 mm <sup>2</sup> Heat sink
		–	185	K/W	PG-DSO-8 <sup>1)</sup> ; Footprint only
		–	164	K/W	PG-DSO-8 <sup>1)</sup> ; 300 mm <sup>2</sup> Heat sink
Junction-pin	$R_{thj-p}$	–	32	K/W	PG-DSO-14 <sup>2)</sup>

1) Worst case; package mounted on PCB 80 × 80 × 1.5 mm<sup>3</sup>; 35μ Cu; 5μ Sn; zero airflow.

2) Measured to pin 4.

**Table 3 Characteristics**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}; V_{\text{INH}} > 3.5 \text{ V};$  (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
<b>Normal Operation</b>						
Output voltage	$V_Q$	4.90	5.00	5.10	V	$5 \text{ mA} \leq I_Q \leq 150 \text{ mA};$ $6 \text{ V} \leq V_I \leq 28 \text{ V}$
Output voltage	$V_Q$	4.90	5.00	5.10	V	$6 \text{ V} \leq V_I \leq 32 \text{ V};$ $I_Q = 100 \text{ mA};$ $T_j = 100 \text{ }^\circ\text{C}$
Output current	$I_Q$	200	250	400	mA	<sup>1)</sup>
Current consumption; $I_q = I_I - I_Q$	$I_q$	–	0	50	$\mu\text{A}$	$V_{\text{INH}} = 0$
	$I_q$	–	900	1300	$\mu\text{A}$	$I_Q = 0 \text{ mA}$
	$I_q$	–	10	18	mA	$I_Q = 150 \text{ mA}$
	$I_q$	–	15	23	mA	$I_Q = 150 \text{ mA}; V_I = 4.5 \text{ V}$
Drop voltage	$V_{\text{dr}}$	–	0.35	0.50	V	$I_Q = 150 \text{ mA}^{1)}$
Load regulation	$\Delta V_{Q,\text{lo}}$	–	–	25	mV	$I_Q = 5 \text{ mA to } 150 \text{ mA}$
Line regulation	$\Delta V_{Q,\text{li}}$	–	3	25	mV	$V_I = 6 \text{ V to } 28 \text{ V};$ $I_Q = 150 \text{ mA}$
Power Supply Ripple Rejection	$PSRR$	–	54	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 0.5 \text{ Vpp}$
<b>Reset Generator</b>						
Switching threshold	$V_{Q,\text{rt}}$	4.5	4.65	4.8	V	$V_{\text{RADJ}} = 0 \text{ V}$
Reset adjust threshold	$V_{\text{RADJ,th}}$	1.26	1.35	1.44	V	$V_Q > 3.5 \text{ V}$
Reset low voltage	$V_{\text{RO,l}}$	–	0.10	0.40	V	$I_{\text{RO}} = 1 \text{ mA}$
Saturation voltage	$V_{\text{D,sat}}$	–	50	100	mV	$V_Q < V_{\text{R,th}}$
Upper timing threshold	$V_{\text{DU}}$	1.45	1.70	2.05	V	–
Lower reset timing threshold	$V_{\text{DRL}}$	0.20	0.35	0.55	V	–
Charge current	$I_{\text{D,ch}}$	40	60	85	$\mu\text{A}$	–
Reset delay time	$t_{\text{rd}}$	1.3	2.8	4.1	ms	$C_{\text{D}} = 100 \text{ nF}$
Reset reaction time	$t_{\text{rr}}$	0.5	1.2	4	$\mu\text{s}$	$C_{\text{D}} = 100 \text{ nF}$

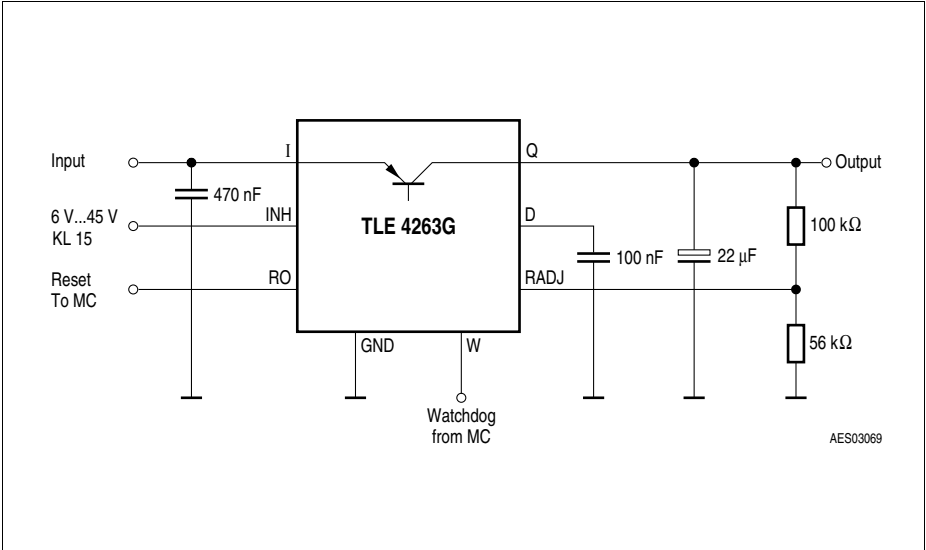


**Table 3 Characteristics (cont'd)**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 125 \text{ }^\circ\text{C}; V_{\text{INH}} > 3.5 \text{ V};$  (unless specified otherwise)

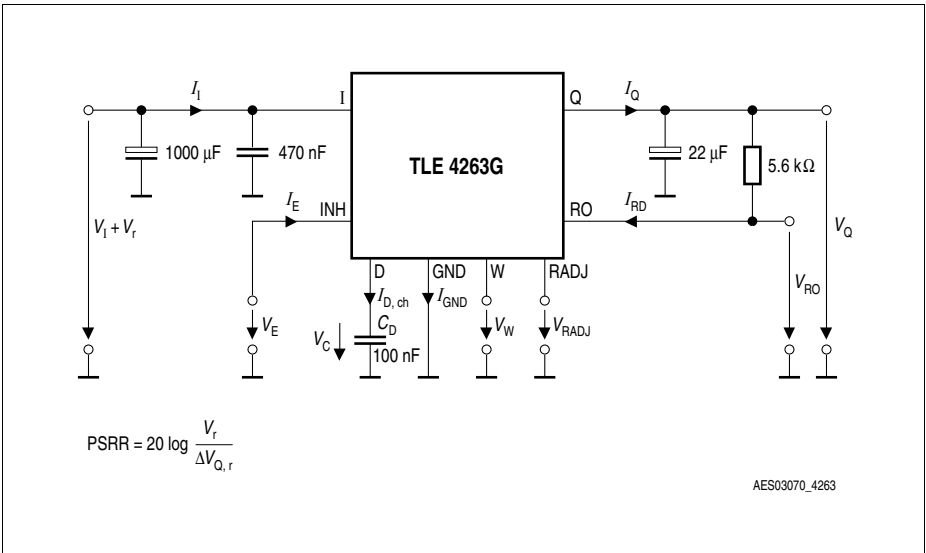
Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
<b>Watchdog</b>						
Discharge current	$I_{\text{D,wd}}$	4.40	6.25	9.10	$\mu\text{A}$	$V_{\text{D}} = 1.0 \text{ V}$
Upper timing threshold	$V_{\text{DU}}$	1.45	1.70	2.05	V	–
Lower timing threshold	$V_{\text{DWL}}$	0.20	0.35	0.55	V	–
Watchdog trigger time	$T_{\text{WI,tr}}$	16	22.5	27	ms	$C_{\text{D}} = 100 \text{ nF}$
<b>Inhibit</b>						
Switching voltage	$V_{\text{INH,ON}}$	3.6	–	–	V	IC turned on
Turn-OFF voltage	$V_{\text{INH,OFF}}$	–	–	0.8	V	IC turned off
Input current	$I_{\text{INH}}$	5	10	25	$\mu\text{A}$	$V_{\text{INH}} = 5 \text{ V}$

1) Drop voltage =  $V_i - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input).

*Note: The reset output is low within the range  $V_Q = 1 \text{ V}$  to  $V_{Q,rt}$ .*



**Figure 3 Application Circuit**



**Figure 4 Test Circuit**

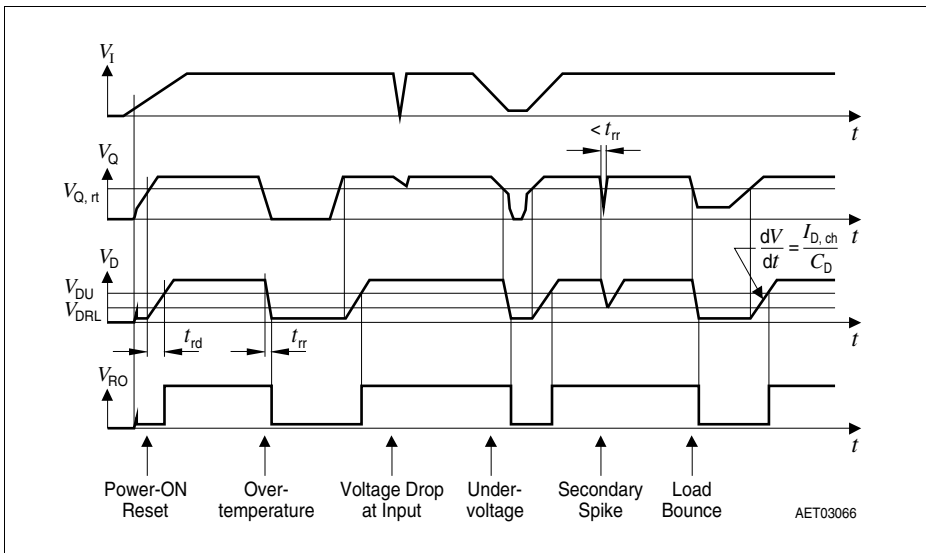
### Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor  $C_D$  which can be calculated as follows:

$$C_D = (t_{rd} \times I_{D,ch}) / \Delta V \tag{1}$$

Definitions:

- $C_D$  = delay capacitor
- $t_{rd}$  = reset delay time
- $I_{D,ch}$  = charge current, typical 60  $\mu$ A
- $\Delta V$  =  $V_{DU}$ , typical 1.70 V
- $V_{DU}$  = upper delay switching threshold at  $C_D$  for reset delay time



**Figure 5 Time Response, Watchdog with High-Frequency Clock**

### Reset Switching Threshold

The present default value is typ. 4.65 V. When using the TLE 4263 the reset threshold can be set to  $3.5\text{ V} < V_{Q,rt} < 4.6\text{ V}$  by connecting an external voltage divider to pin RADJ. The calculation can be easily done since the reset adjust input current can be neglected. If this feature is not needed, the pin has to be connected to GND.

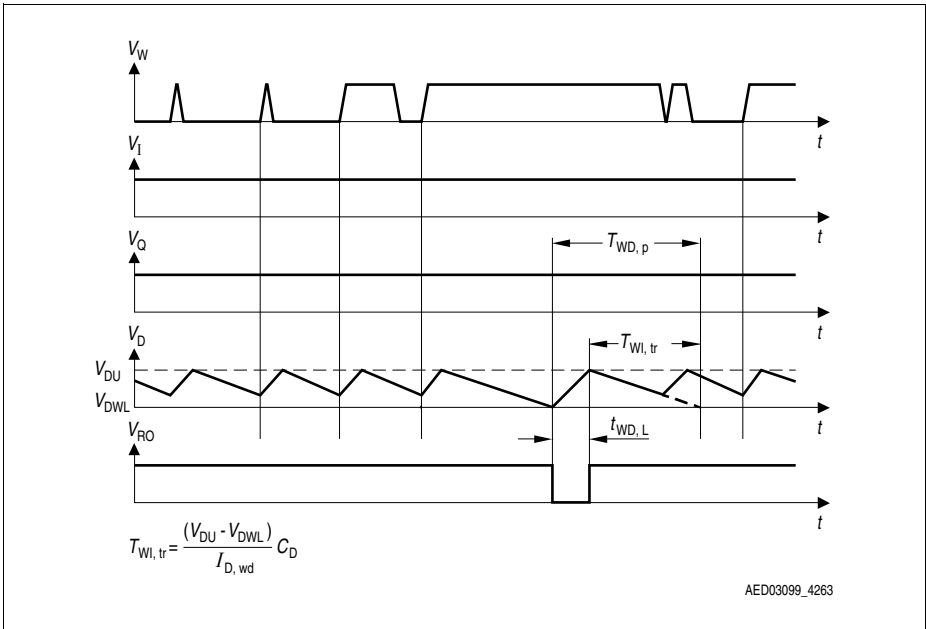
$$V_{Q,rt} = (1 + R_1/R_2) \times V_{RADJ,th} \tag{2}$$

Definitions:

- $V_{Q,rt}$  = reset threshold
- $V_{RADJ,th}$  = comparator reference voltage, typical 1.35 V

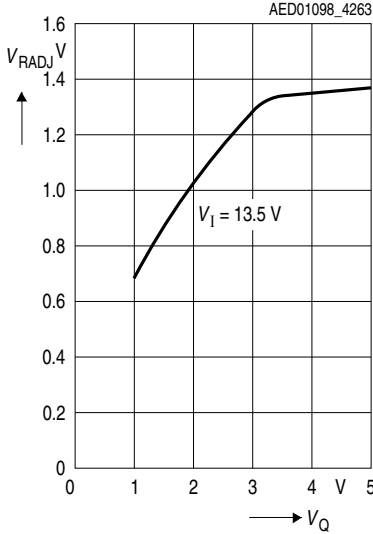
### Watchdog Timing

The frequency of the watchdog pulses has to be higher than the minimum pulse sequence which is set by the external reset delay capacitor  $C_D$ . Calculation can be done according to the formula given in [Figure 6](#).

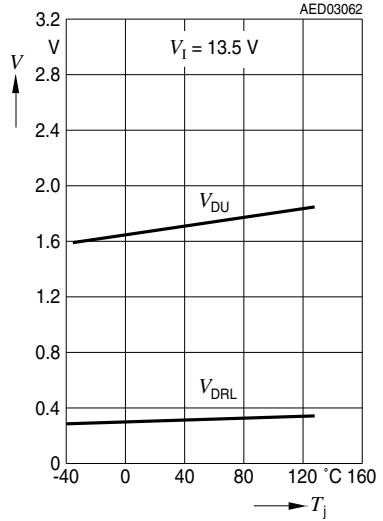


**Figure 6** Timing of the Watchdog Function Reset

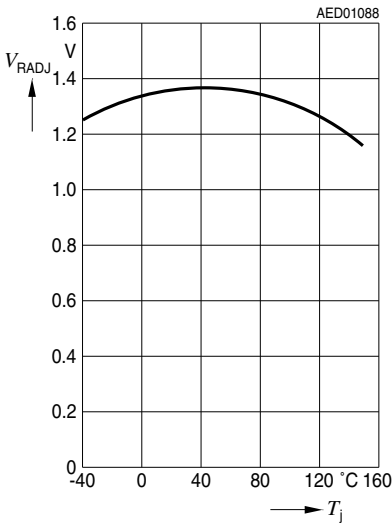
**Reset Switching Threshold versus Output Voltage**



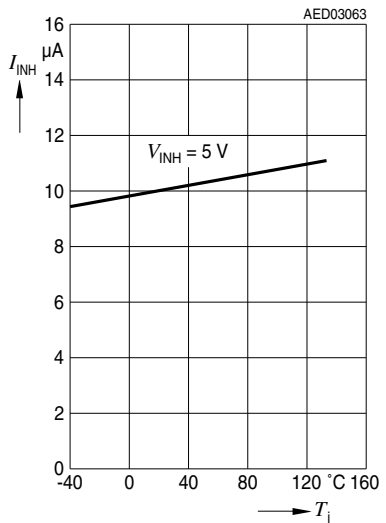
**Timing Threshold Voltage V<sub>DU</sub> and V<sub>DRL</sub> versus Temperature**



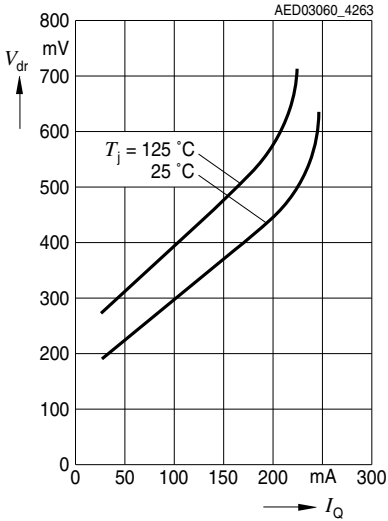
**Reset Switching Threshold versus Temperature**



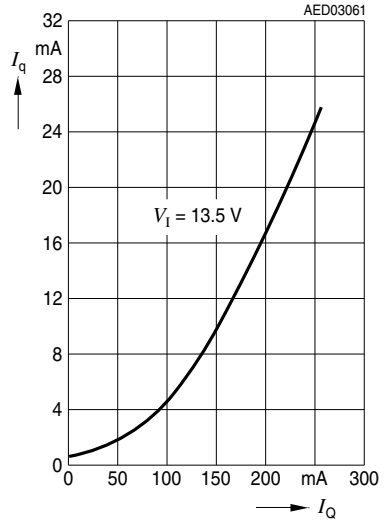
**Current Consumption of Inhibit versus Temperature**



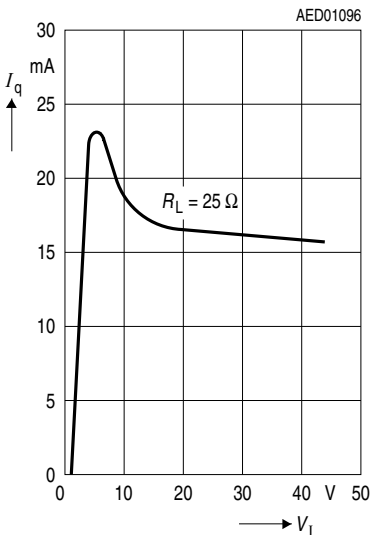
**Drop Voltage versus Output Current**



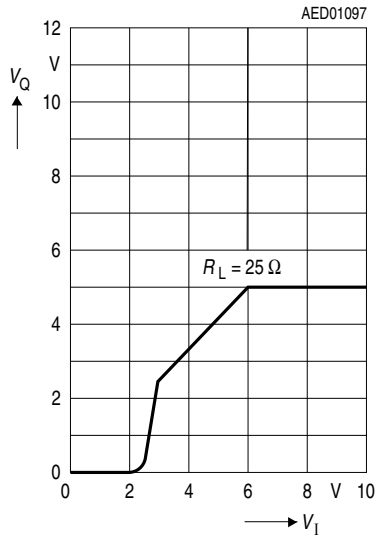
**Current Consumption versus Output Current**



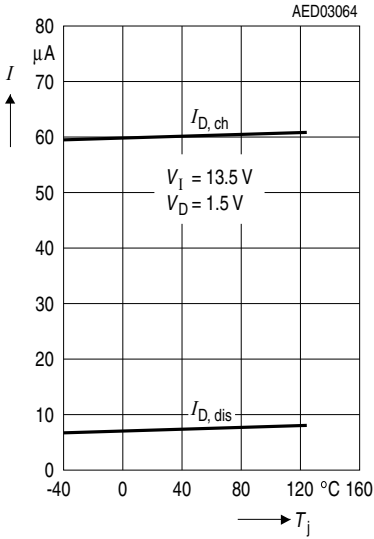
**Current Consumption versus Input Voltage**



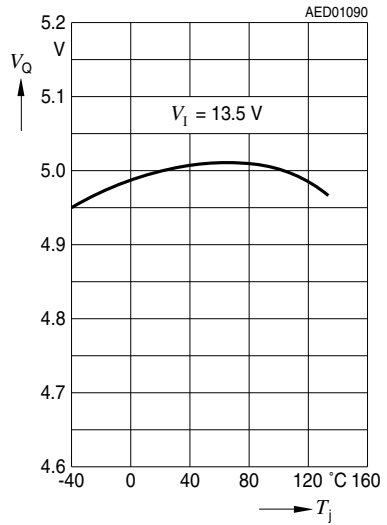
**Output Voltage versus Input Voltage**



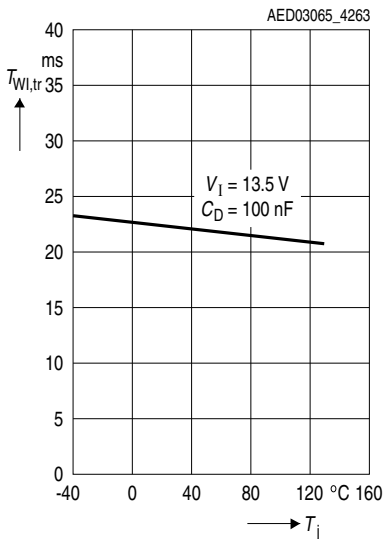
**Charge Current and Discharge Current versus Temperature**



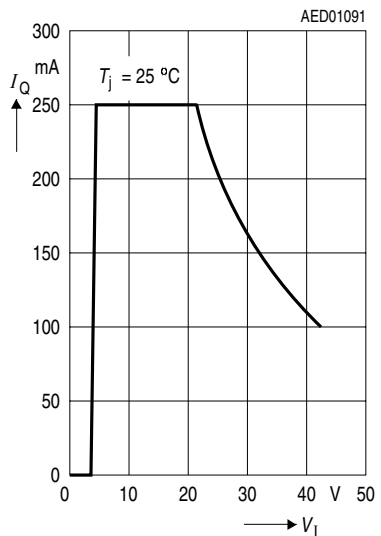
**Output Voltage versus Temperature**



**Pulse Time versus Temperature**



**Output Current versus Input Voltage**



Package Outlines

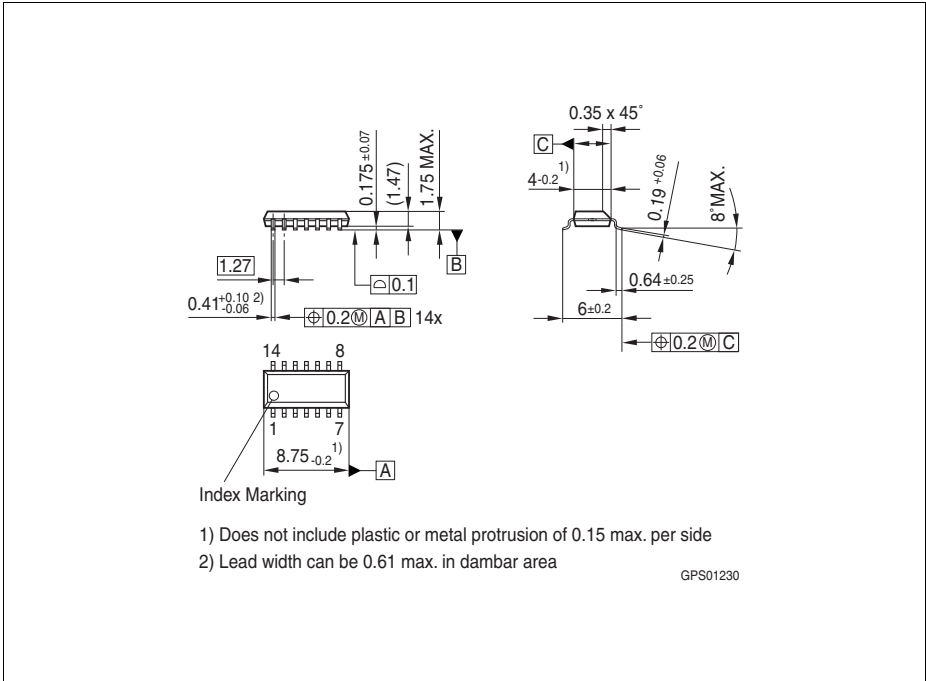


Figure 7 PG-DSO-14 (Plastic Dual Small Outline)

Green Product (RoHS compliant)

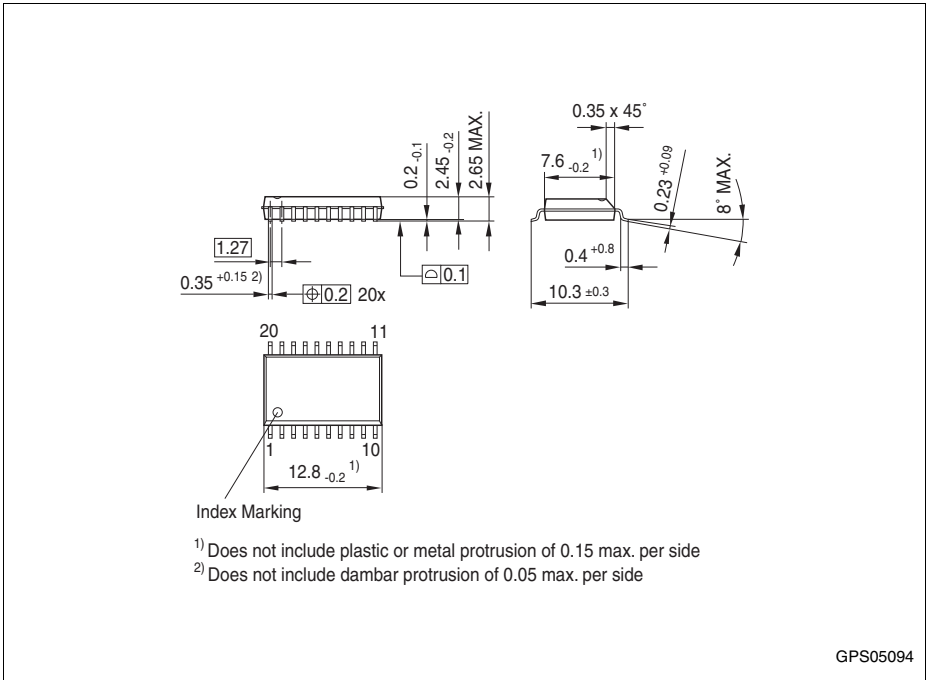
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SMD = Surface Mounted Device

Dimensions in mm





**Figure 8 PG-DSO-20 (Plastic Dual Small Outline)**

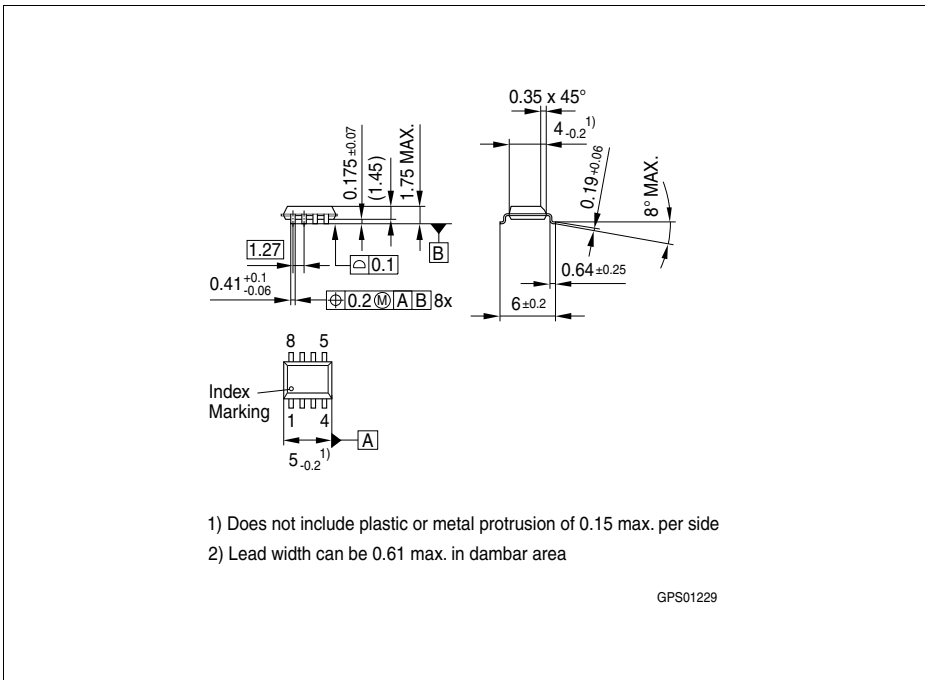
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SMD = Surface Mounted Device

Dimensions in mm



**Figure 9 PG-DSO-8 (Plastic Dual Small Outline)**

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SMD = Surface Mounted Device

Dimensions in mm

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**Revision History**

<b>Version</b>	<b>Date</b>	<b>Changes</b>
Rev. 2.9	2013-11-25	Package version changed: - PG-DSO-20-35 to PG-DSO-20 Package naming harmonized according to Infineon standards: - PG-DSO-8-16 to PG-DSO-8 - PG-DSO-14-30 to PG-DSO-14
Rev. 2.8	2007-03-20	Initial version of RoHS-compliant derivate of TLE 4263 <b>Page 1</b> : AEC certified statement added <b>Page 1</b> and <b>Page 15</b> ff:RoHS compliance statement and Green product feature added <b>Page 1</b> and <b>Page 15</b> ff: Package changed to RoHS compliant version Legal Disclaimer updated

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