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TLE42994

Low Dropout Fixed Voltage Regulator

TLE42994G
TLE42994GM
TLE42994E

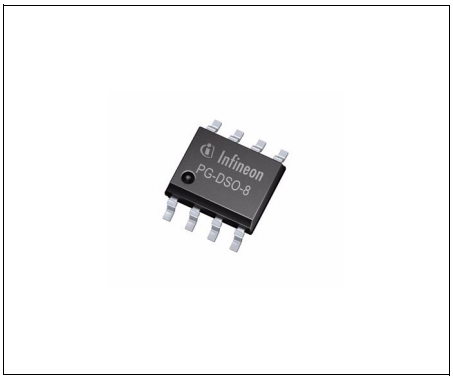
Data Sheet

Rev. 1.2, 2014-07-03

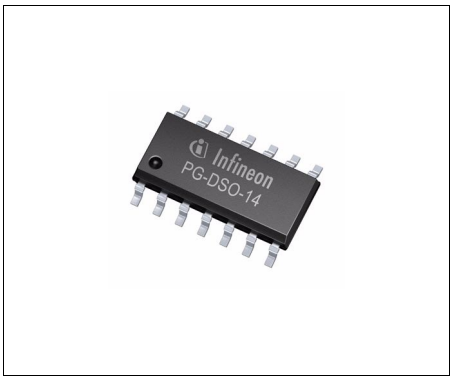
Automotive Power

AEC Qualified RoHS

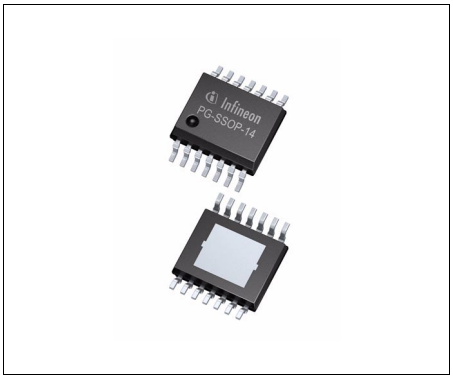
1 Overview



PG-DSO-8



PG-DSO-14



PG-SSOP-14 exposed pad

Features

- Output Voltage 5 V ± 2%
- Ouput Current up to 150 mA
- Extreme Low Current Consumption In ON State
- Enable Function: Below 1 µA Current Consumption In OFF State
- Early Warning
- Power-on and Undervoltage Reset with Programmable Delay Time
- Reset Low Down to V_Q = 1 V
- Adjustable Reset Threshold
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Protection
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Input Voltage Range from -42 V to 45 V
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE42994 is a monolithic integrated low dropout voltage regulator, especially designed for automotive applications that need to be in ON state during the car's engine is turned off. An input voltage up to 45 V is regulated to an output voltage of 5.0 V. The component is able to drive loads up to 150 mA. It is short-circuit protected by the implemented current limitation and has an integrated overtemperature shutdown. A reset signal is generated for an output voltage $V_{Q,rt}$ of typically 4.65 V. This threshold can be decreased by an external

Type	Package	Marking
TLE42994G	PG-DSO-8	42994G
TLE42994GM	PG-DSO-14	42994GM
TLE42994E	PG-SSOP-14 exposed pad	42994E

resistor divider. The power-on reset delay time can be programmed by the external delay capacitor. The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an under-voltage condition is indicated by setting the comparator's output to low. The TLE42994GM (PG-DSO-14 package) and TLE42994E (PG-SSOP-14 exposed pad package) include additionally an Enable function permitting enabling/disabling the regulator. In case the regulator is disabled it consumes less current than 1 µA.

Dimensioning Information on External Components

The input capacitor C_{I} is recommended for compensation of line influences. The output capacitor C_{Q} is necessary for the stability of the control loop.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The component also has a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

2 Block Diagram

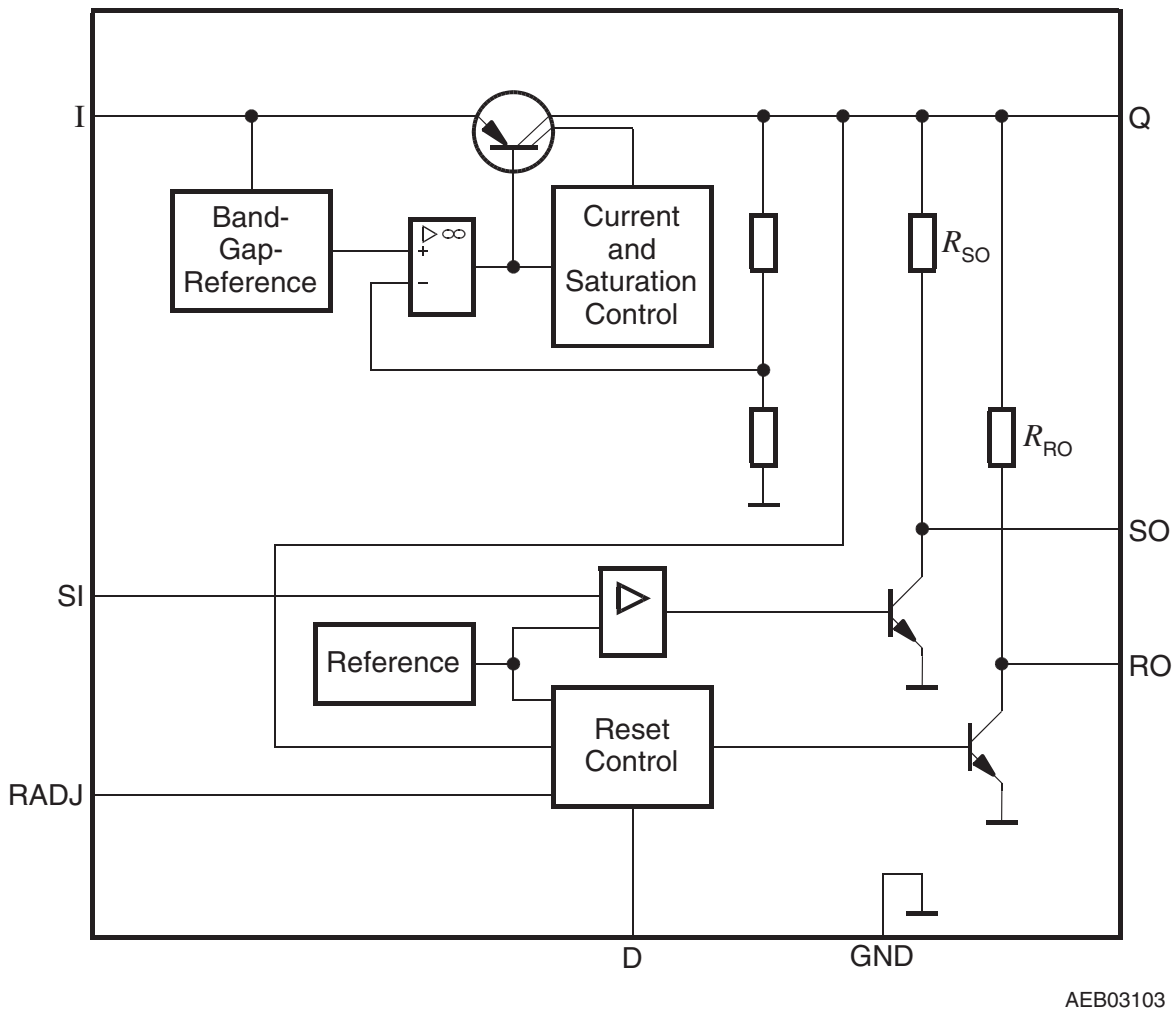


Figure 1 Block Diagram TLE42994G (package PG-DSO-8)

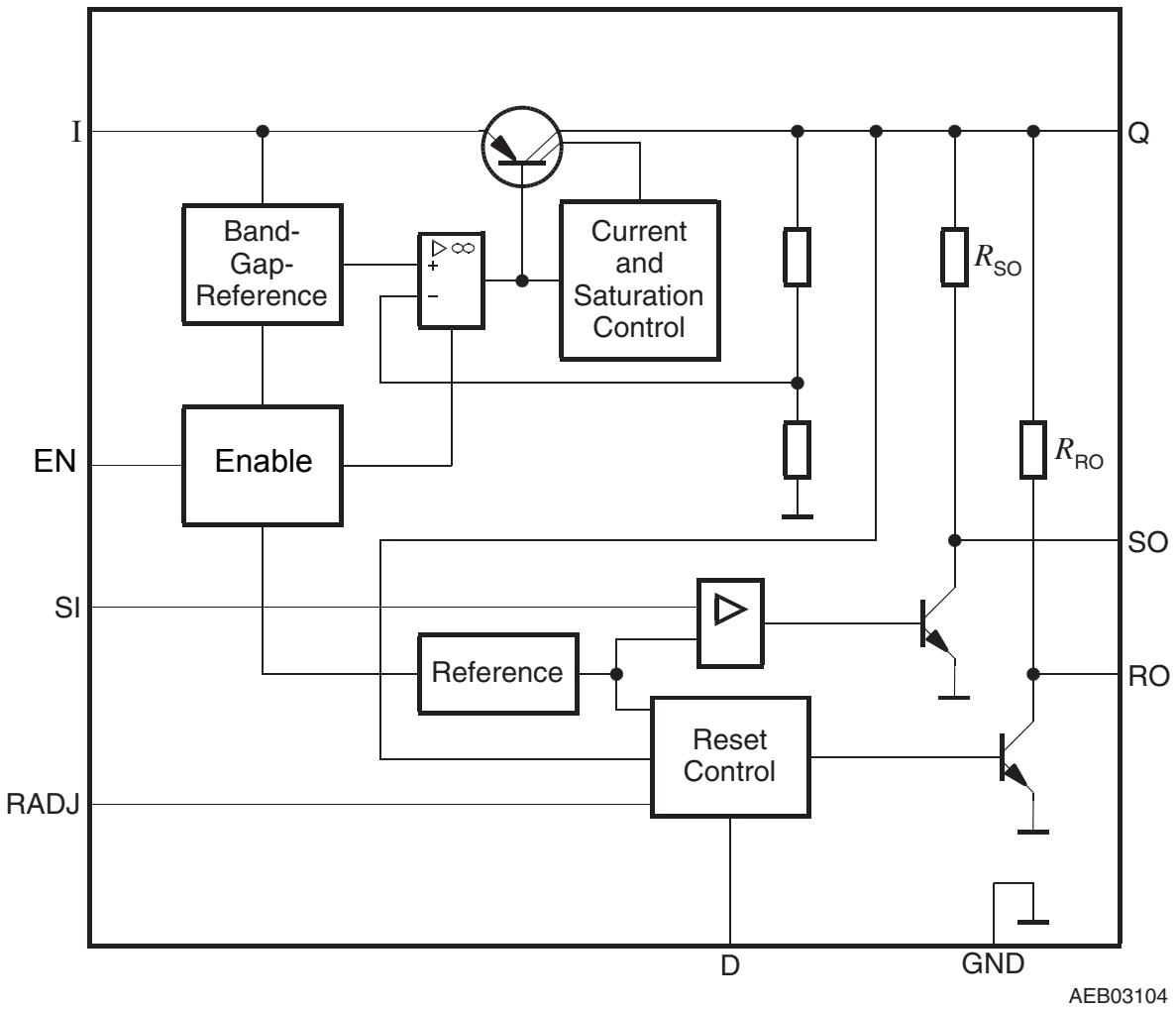


Figure 2 Block Diagram TLE42994GM, TLE42994E (packages PG-DSO-14, PG-SSOP-14 exposed pad)

3 Pin Configuration

3.1 Pin Assignment TLE42994G (PG-DSO-8)

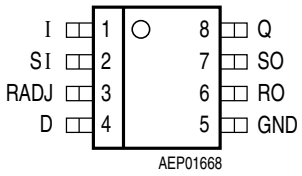


Figure 3 Pin Configuration (top view)

3.2 Pin Definitions and Functions TLE42994G (PG-DSO-8)

Pin	Symbol	Function
1	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
2	SI	**Sense Input** connect the voltage to be monitored; connect to Q if the sense comparator is not needed
3	RADJ	**Reset Threshold Adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
4	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
5	GND	**Ground**
6	RO	**Reset Output** open collector output; internally linked to the output via a 20 kΩ pull-up resistor; leave open if the reset function is not needed
7	SO	**Sense Output** open collector output; internally linked to the output via a 20 kΩ pull-up resistor; leave open if the sense comparator is not needed
8	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in **“Functional Range” on Page 12**

3.3 Pin Assignment TLE42994GM (PG-DSO-14)

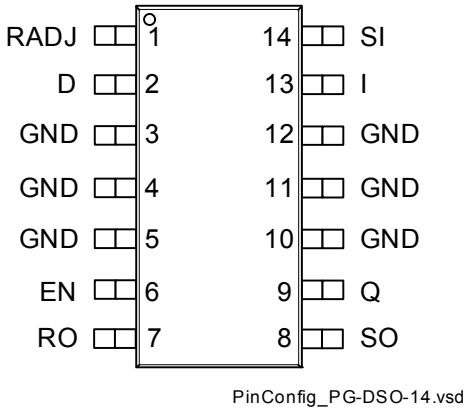


Figure 4 Pin Configuration (top view)

3.4 Pin Definitions and Functions TLE42994GM (PG-DSO-14)

Pin	Symbol	Function
1	RADJ	**Reset Threshold Adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
3, 4, 5	GND	**Ground** connect all pins to PCB and heatsink area
6	EN	**Enable** high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	**Reset Output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	**Sense Output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **“Functional Range” on Page 12**
10, 11, 12	GND	**Ground** connect all pins to PCB and heatsink area

Pin	Symbol	Function
13	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended
14	SI	**Sense Input** connect the voltage to be monitored; connect to Q if the sense comparator is not needed

3.5 Pin Assignment TLE42994E (PG-SSOP-14 exposed pad)

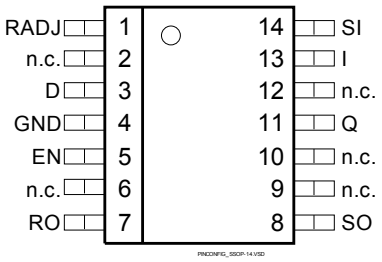


Figure 5 Pin Configuration (top view)

3.6 Pin Definitions and Functions TLE42994E (PG-SSOP-14 exposed pad)

Pin	Symbol	Function
1	RADJ	**Reset Threshold Adjust** connect an external voltage divider to adjust reset threshold; connect to GND for using internal threshold
2, 6	n.c.	**not connected** leave open or connect to GND
3	D	**Reset Delay Timing** connect a ceramic capacitor to GND for adjusting the reset delay time; leave open if the reset function is not needed
4	GND	**Ground** connect all pins to PCB and heatsink area
5	EN	**Enable** high signal enables the regulator; low signal disables the regulator; connect to I if the Enable function is not needed
7	RO	**Reset Output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the reset function is not needed
8	SO	**Sense Output** open collector output; internally linked to the output via a 20kΩ pull-up resistor; leave open if the sense comparator is not needed
9, 10, 12	n.c.	**not connected** leave open or connect to GND
11	Q	**Output** block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance C_Q and ESR in the table **“Functional Range” on Page 12**
13	I	**Input** for compensating line influences, a capacitor to GND close to the IC terminals is recommended

Pin	Symbol	Function
14	SI	**Sense Input** connect the voltage to be monitored; connect to Q if the sense comparator is not needed
PAD	–	**Exposed Pad** attach the exposed pad on package bottom to the heatsink area on circuit board; connect to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

-40 °C ≤ T_j ≤ 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable Input EN, Sense Input SI							
Voltage	V_I, V_{EN}, V_{SI}	-40	–	45	V	–	P_4.1.1
Output Q, Reset Output RO, Sense Output SO							
Voltage	V_Q, V_{RO}, V_{SO}	-0.3	–	7	V	–	P_4.1.2
Reset Delay D, Reset Threshold RADJ							
Voltage	V_D, V_{RADJ}	-0.3	–	7	V	–	P_4.1.3
Temperature							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage Temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD Absorption							
ESD Absorption	$V_{ESD,HBM}$	-2	–	2	kV	Human Body Model (HBM)[2)]	P_4.1.6
ESD Absorption	$V_{ESD,CDM}$	-500	–	500	V	Charge Device Model (CDM)[3)]	P_4.1.7
ESD Absorption	$V_{ESD,CDM}$	-750	–	750	V	Charge Device Model (CDM)[3)] at corner pins	P_4.1.8

1) not subject to production test, specified by design

2) ESD susceptibility Human Body Model “HBM” according to AEC-Q100-002 - JESD22-A114

3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage	V_I	5.5	–	45	V	–	P_4.2.1
Output Capacitor's Requirements for Stability	C_Q	22	–	–	µF	–[1)]	P_4.2.2
Output Capacitor's Requirements for Stability	$ESR(C_Q)$	–	–	3	Ω	–[2)]	P_4.2.3
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
TLE42994G (PG-DSO-8)							
Junction to Soldering Point[1)]	R_{thJSP}	–	–	60	K/W	measured to pin 5	P_4.3.1
Junction to Ambient[1)]	R_{thJA}	–	113	–	K/W	FR4 2s2p board[2)]	P_4.3.2
Junction to Ambient[1)]	R_{thJA}	–	185	–	K/W	FR4 1s0p board, footprint only[3)]	P_4.3.3
Junction to Ambient[1)]	R_{thJA}	–	142	–	K/W	FR4 1s0p board, 300mm^2 heatsink area on PCB[3)]	P_4.3.4
Junction to Ambient[1)]	R_{thJA}	–	136	–	K/W	FR4 1s0p board, 600mm^2 heatsink area on PCB[3)]	P_4.3.5
TLE42994GM (PG-DSO-14)							
Junction to Soldering Point[1)]	R_{thJSP}	–	–	30	K/W	measured to all GND pins	P_4.3.6
Junction to Ambient[1)]	R_{thJA}	–	63	–	K/W	FR4 2s2p board[2)]	P_4.3.7
Junction to Ambient[1)]	R_{thJA}	–	112	–	K/W	FR4 1s0p board, footprint only[3)]	P_4.3.8
Junction to Ambient[1)]	R_{thJA}	–	73	–	K/W	FR4 1s0p board, 300mm^2 heatsink area on PCB[3)]	P_4.3.9
Junction to Ambient[1)]	R_{thJA}	–	65	–	K/W	FR4 1s0p board, 600mm^2 heatsink area on PCB[3)]	P_4.3.10
TLE42994E (PG-SSOP-14 exposed pad)							
Junction to Case[1)]	R_{thJC}	–	10	–	K/W	–	P_4.3.11
Junction to Ambient[1)]	R_{thJA}	–	47	–	K/W	FR4 2s2p board[2)]	P_4.3.12
Junction to Ambient[1)]	R_{thJA}	–	140	–	K/W	FR4 1s0p board, footprint only[3)]	P_4.3.13
Junction to Ambient[1)]	R_{thJA}	–	63	–	K/W	FR4 1s0p board, 300mm^2 heatsink area on PCB[3)]	P_4.3.14
Junction to Ambient[1)]	R_{thJA}	–	53	–	K/W	FR4 1s0p board, 600mm^2 heatsink area on PCB[3)]	P_4.3.15

1) not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Block Description and Electrical Characteristics

5.1 Voltage Regulator

The output voltage V_Q is controlled by comparing a portion of it to an internal reference and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table **"Functional Range" on Page 12** have to be maintained. For details see also the typical performance graph **"Output Capacitor Series Resistor ESR(C_Q) versus Output Current I_Q" on Page 17**. As the output capacitor also has to buffer load steps it should be sized according to the application's needs.

An input capacitor C_I is strongly recommended to compensate line influences. Connect the capacitors close to the component's terminals.

A protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. These safeguards contain an output current limitation, a reverse polarity protection as well as a thermal shutdown in case of overtemperature.

To avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at input voltages above V_I = 22 V.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behaviour of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

The TLE42994 allows a negative supply voltage. In this fault condition, small currents are flowing into the IC, increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity conditions.

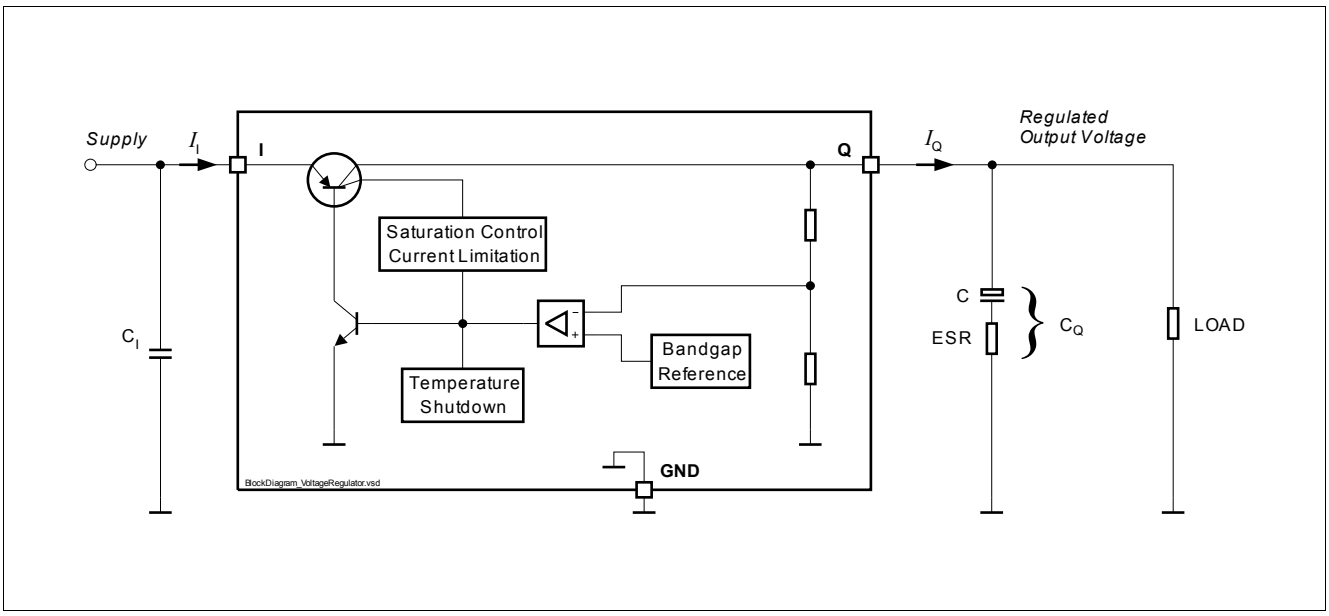


Figure 6 Voltage Regulator

Table 4 Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Voltage	V_Q	4.9	5.0	5.1	V	100 µA < I_Q < 100 mA 6 V < V_I < 18 V	P_5.1.1
Output Voltage	V_Q	4.85	5.0	5.15		100 µA < I_Q < 150 mA 6 V < V_I < 18 V	P_5.1.2
Output Current Limitation	$I_{Q,max}$	150	400	500	mA	V_Q = 4.8V	P_5.1.3
Load Regulation steady-state	$\Delta V_{Q,\ load}$	-30	-5	–	mV	I_Q = 1 mA to 100 mA V_I = 6 V	P_5.1.4
Line Regulation steady-state	$\Delta V_{Q,\ line}$	–	10	25	mV	V_I = 6 V to 32 V I_Q = 1 mA	P_5.1.5
Dropout Voltage[1] V_{dr} = V_I - V_Q	V_{dr}	–	220	500	mV	I_Q = 100 mA	P_5.1.6
Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[2]	P_5.1.7
Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	15	–	°C	T_j decreasing[2]	P_5.1.8
Power Supply Ripple Rejection[3]	$PSRR$	–	66	–	dB	f_{ripple} = 100 Hz V_{ripple} = 1 Vpp I_Q = 100 mA	P_5.1.9

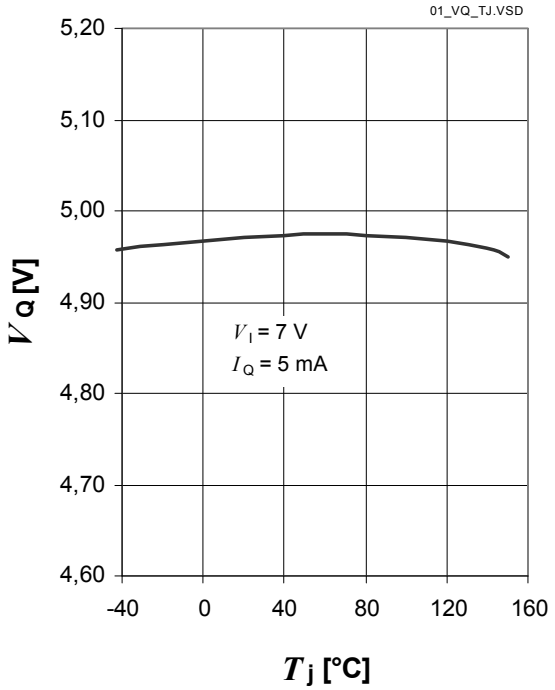
1) measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V

2) not subject to production test, specified by design

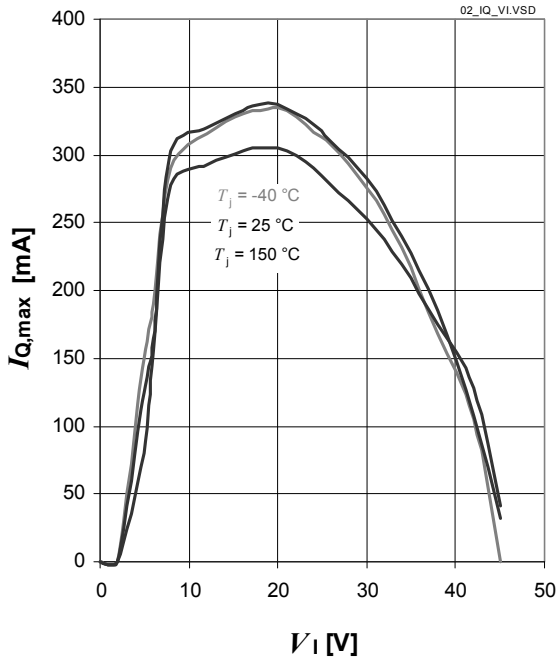
3) not subject to production test, specified by design

5.2 Typical Performance Characteristics Voltage Regulator

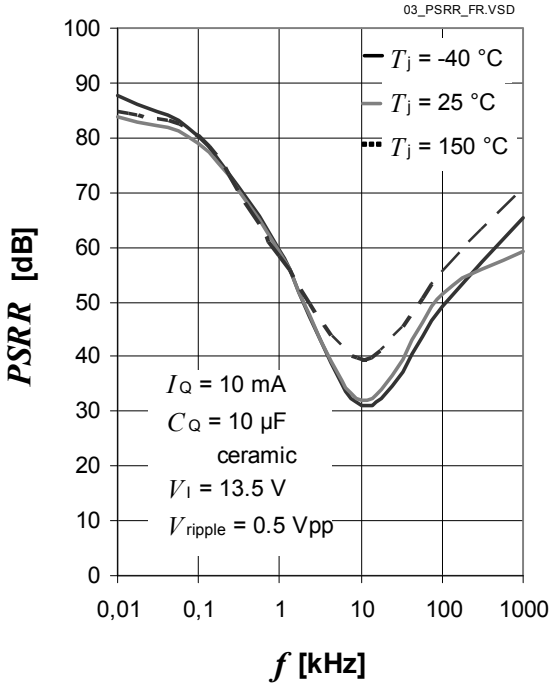
Output Voltage V_Q versus Junction Temperature T_J



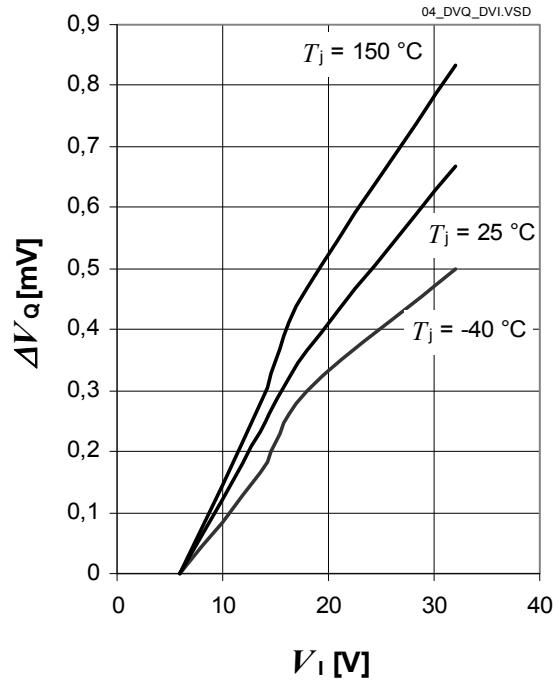
Output Current I_Q versus Input Voltage V_I



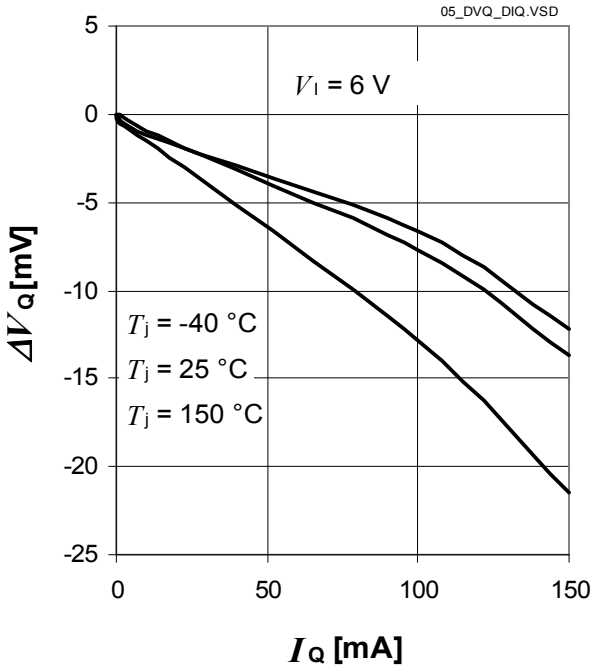
Power Supply Ripple Rejection $PSRR$ versus ripple frequency f_r



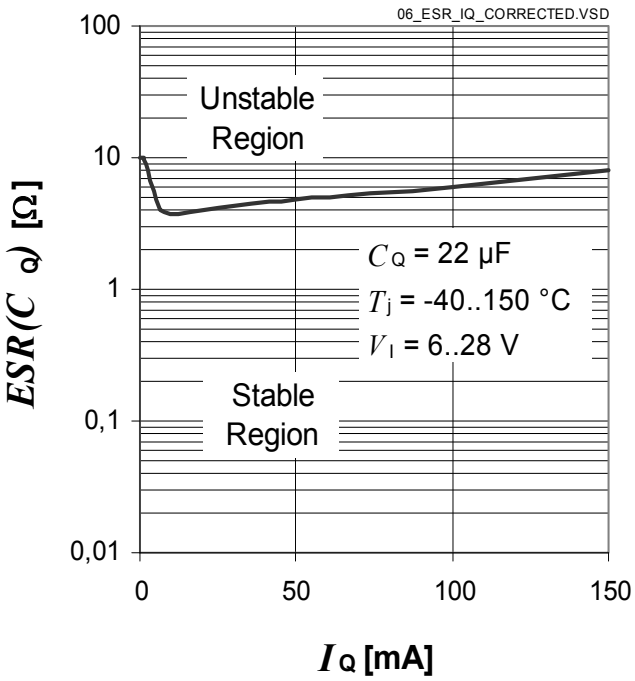
Line Regulation $\Delta V_{Q,line}$ versus Input Voltage Change ΔV_I



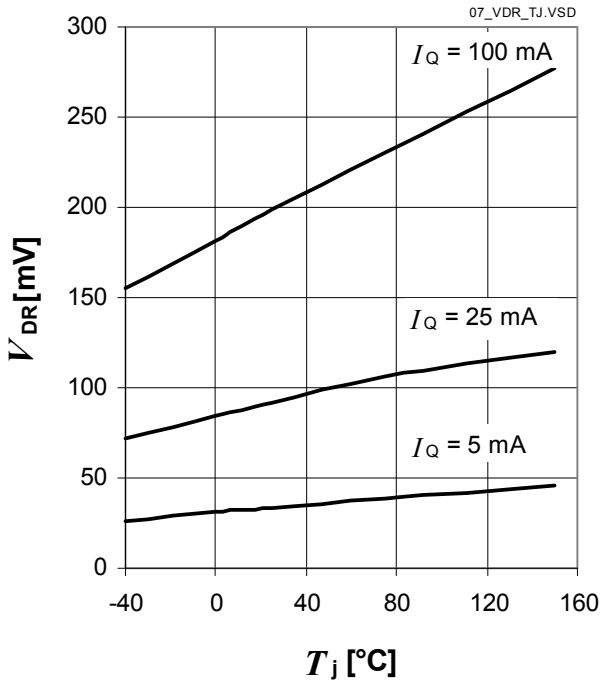
Load Regulation $\Delta V_{Q,load}$ versus Output Current Change ΔI_Q



Output Capacitor Series Resistor $ESR(C_Q)$ versus Output Current I_Q



Dropout Voltage V_{dr} versus Junction Temperature T_j



5.3 Current Consumption

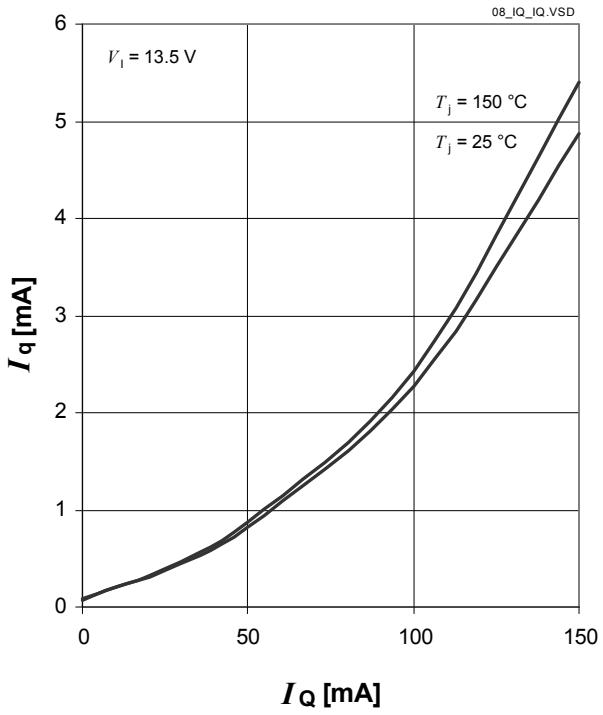
Table 5 Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

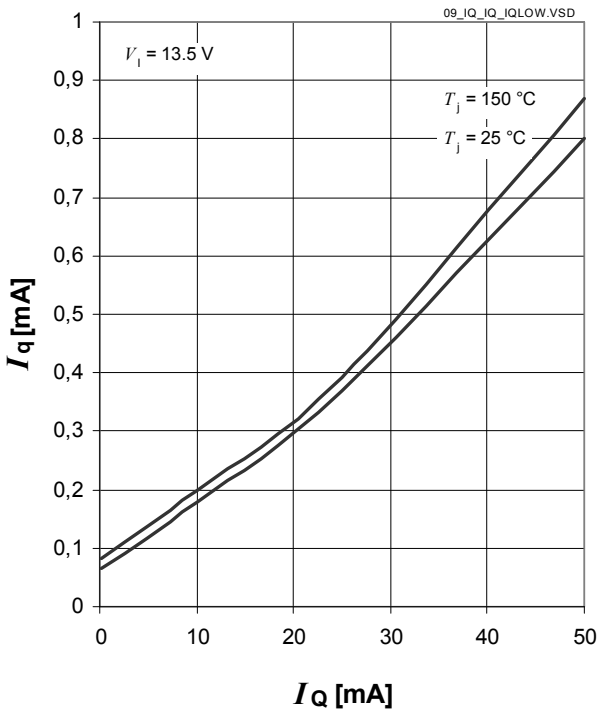
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption $I_q = I_I - I_Q$	I_q	–	–	1	µA	V_{EN} = 0 V TLE42994GM and TLE42994E only T_j = 25 °C	P_5.4.1
Current Consumption $I_q = I_I - I_Q$	I_q	–	65	100	µA	Enable HIGH I_Q = 100 µA, T_j = 25 °C	P_5.4.2
Current Consumption $I_q = I_I - I_Q$	I_q	–	65	105	µA	Enable HIGH I_Q = 100 µA, T_j ≤ 85 °C	P_5.4.3
Current Consumption $I_q = I_I - I_Q$	I_q	–	0.17	0.5	mA	Enable HIGH I_Q = 10 mA	P_5.4.4
Current Consumption $I_q = I_I - I_Q$	I_q	–	0.7	2	mA	Enable HIGH I_Q = 50 mA	P_5.4.5

5.4 Typical Performance Characteristics Current Consumption

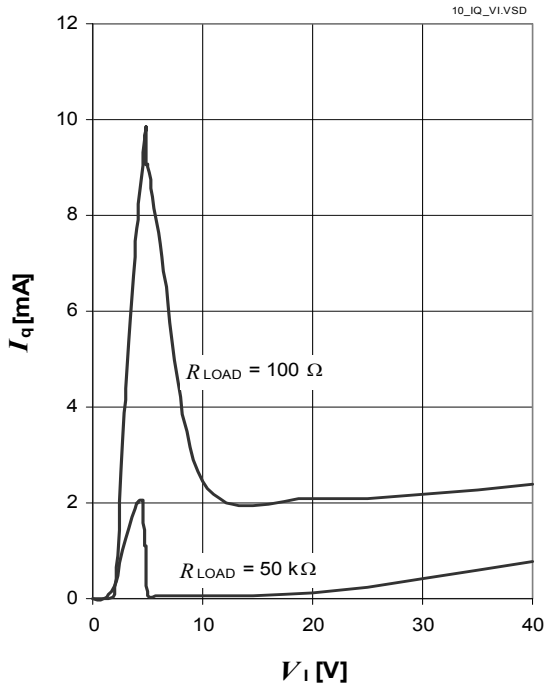
Current Consumption I_q versus Output Current I_Q



Current Consumption I_q versus Output Current I_Q (I_Q low)



Current Consumption I_q versus Input Voltage V_I



5.5 Enable Function (only TLE42994GM and TLE42994E)

Table 6 Electrical Characteristics Voltage Regulator

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable OFF Voltage Range	$V_{EN,OFF}$	–	–	0.8	V	–	P_5.6.1
Enable ON Voltage Range	$V_{EN,ON}$	3.5	–	–	V	–	P_5.6.2
Enable OFF Input Current	$I_{EN,OFF}$	–	0.5	2	µA	V_{EN} = 0 V	P_5.6.3
Enable ON Input Current	$I_{EN,ON}$	–	3	5	µA	V_{EN} = 5 V	P_5.6.4

5.6 Reset Function

The reset function provides several features:

Output Undervoltage Reset:

An output undervoltage condition is indicated by setting the Reset Output RO to “low”. This signal might be used to reset a microcontroller during low supply voltage.

Power-On Reset Delay Time:

The power-on reset delay time trd allows a microcontoller and oscillator to start up. This delay time is the time frame from exceeding the reset switching threshold V_{RT} until the reset is released by switching the reset output “RO” from “low” to “high”. The power-on reset delay time t_{rd} is defined by an external delay capacitor C_D connected to pin D charged by the delay capacitor charge current $I_{D,ch}$ starting from V_D = 0 V.

If the application needs a power-on reset delay time trd different from the value given in **Power On Reset Delay Time**, the delay capacitor’s value can be derived from the specified values in **Power On Reset Delay Time** and the desired power-on delay time:

(1)

$$C_D = \frac{t_{rd,new}}{t_{rd}} \times 100\text{nF}$$

with

- C_D: capacitance of the delay capacitor to be chosen
- $t_{rd,new}$: desired power-on reset delay time
- t_{rd}: power-on reset delay time specified in this datasheet

For a precise calculation also take the delay capacitor’s tolerance into consideration.

Reset Reaction Time:

The reset reaction time avoids that short undervoltage spikes trigger an unwanted reset “low” signal. The reset reaction rime t_{rr} considers the internal reaction time $t_{rr,int}$ and the discharge time $t_{rr,d}$ defined by the external delay capacitor C_D (see typical performance graph for details). Hence, the total reset reaction time becomes:

(2)

$$t_{rr} = t_{rd,int} + t_{rr,d}$$

with

- t_{rr}: reset reaction time
- $t_{rr,int}$: internal reset reaction time
- $t_{rr,d}$: reset discharge

Optional Reset Output Pull-Up Resistor $R_{RO,ext}$:

The Reset Output RO is an open collector output with an integrated pull-up resistor. If needed, an external pull-up resistor to the output Q can be added. In **Table 7 “Electrical Characteristics Reset Function” on Page 24** a minimum value for the external resistor $R_{RO,ext}$ is given.

Reset Adjust Function

The undervoltage reset switching threshold can be adjusted according to the application's needs by connecting an external voltage divider (R_{ADJ1}, R_{ADJ2}) at pin RADJ. For selecting the default threshold connect pin RADJ to GND.

When dimensioning the voltage divider, take into consideration that there will be an additional current constantly flowing through the resistors.

With a voltage divider connected, the reset switching threshold $V_{RT,new}$ is calculated as follows:

(3)

$$V_{RT,new} = \frac{R_{ADJ,1} + R_{ADJ,2}}{R_{ADJ,2}} \times V_{RADJ,th}$$

with

- $V_{RT,new}$: the desired new reset switching threshold
- R_{ADJ1}, R_{ADJ2}: resistors of the external voltage divider
- $V_{RADJ,th}$: reset adjust switching threshold given in **Table 7 "Electrical Characteristics Reset Function" on Page 24**

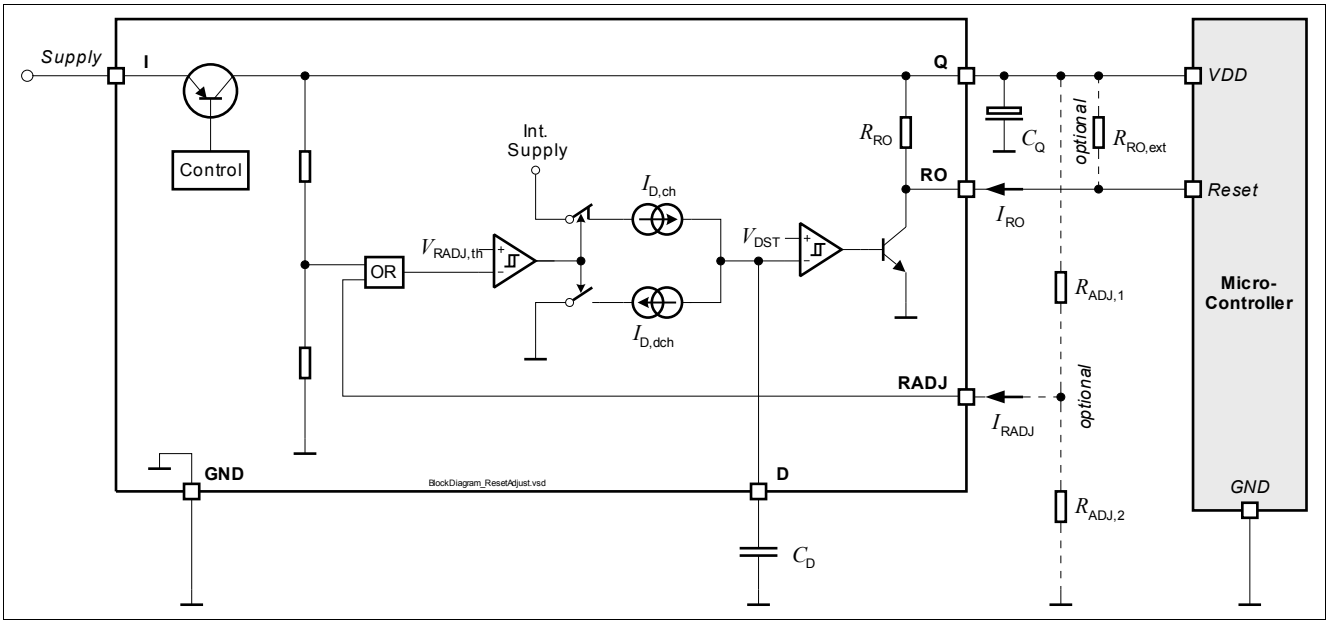


Figure 7 Block Diagram Reset Function

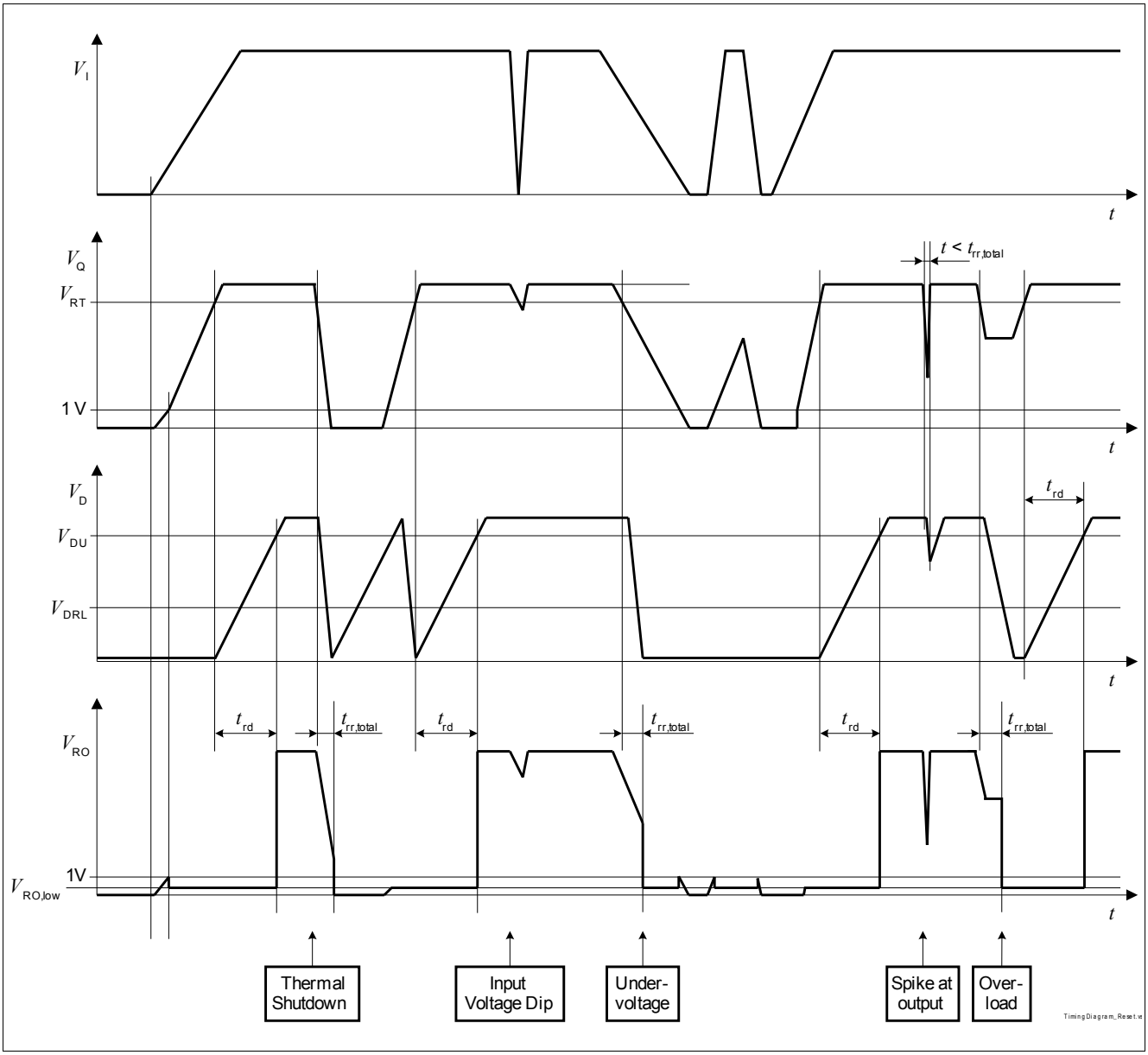


Figure 8 Timing Diagram Reset

Table 7 Electrical Characteristics Reset Function

V_I = 13.5 V, -40 °C ≤ T_j ≤ 150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

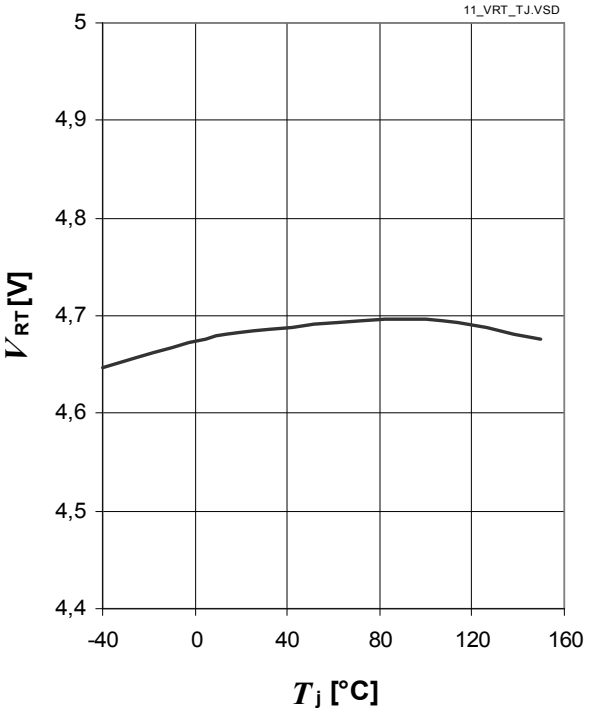
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Undervoltage Reset							
Default Output Undervoltage Reset Switching Thresholds	V_{RT}	4.5	4.65	4.8	V	V_Q decreasing	P_5.7.1
Output Undervoltage Reset Threshold Adjustment							
Reset Adjust Switching Threshold	$V_{RADJ,th}$	1.26	1.36	1.44	V	3.5 V ≤ V_Q < 5 V	P_5.7.2
Reset Adjustment Range[1)]	$V_{RT,range}$	3.50	–	4.65	V	–	P_5.7.3
Reset Output RO							
Reset Output Low Voltage	$V_{RO,low}$	–	0.1	0.4	V	1 V ≤ V_Q ≤ V_{RT} no external $R_{RO,ext}$	P_5.7.4
Reset Output Internal Pull-up Resistor to V_Q	R_{RO}	10	20	40	kΩ	–	P_5.7.5
Optional Reset Output External Pull-up Resistor to V_Q	$R_{RO,ext}$	5.6	–	–	kΩ	1 V ≤ V_Q ≤ V_{RT} ; V_{RO} ≤ 0.4 V	P_5.7.6
Reset Delay Timing							
Delay Pin Output Voltage	V_D	–	–	5	V	–	P_5.7.7
Power On Reset Delay Time	t_{rd}	17	28	35	ms	C_D = 100 nF Calculated Value: $t_{rd} = C_D * V_{DU} / I_{D,ch}$	P_5.7.8
Upper Delay Switching Threshold	V_{DU}	–	1.85	–	V	–	P_5.7.9
Lower Delay Switching Threshold	V_{DL}	–	0.50	–	V	–	P_5.7.10
Delay Capacitor Charge Current	$I_{D,ch}$	–	8.0	–	µA	V_D = 1 V	P_5.7.11
Delay Capacitor Reset Discharge Current	$I_{D,dch}$	–	70	–	mA	V_D = 1 V	P_5.7.12
Delay Capacitor Discharge Time	$t_{rr,\ d}$	–	1.9	3	µs	Calculated Value: $t_{rr,\ d} = C_D*(V_{DU} - V_{DL})/ I_{D,dch}$ C_D = 100 nF	P_5.7.13
Internal Reset Reaction Time	$t_{rr,\ int}$	–	14	20	µs	C_D = 0 nF [2)]	P_5.7.14
Reset Reaction Time	$t_{rr,\ total}$	–	15.9	23	µs	Calculated Value: $t_{rr,\ total} = t_{rr,\ int} + t_{rr,d}$ C_D = 100 nF	P_5.7.15

1) V_{RT} is scaled linearly, in case the Reset Switching Threshold is modified

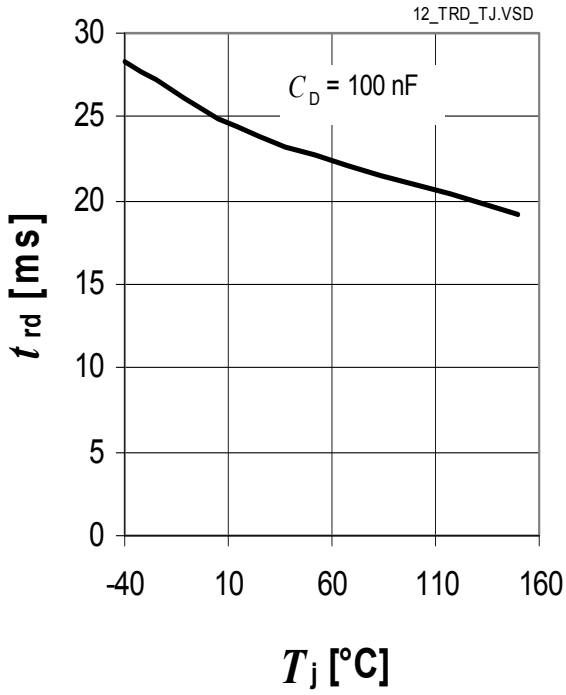
2) parameter not subject to production test; specified by design

5.7 Typical Performance Characteristics Reset

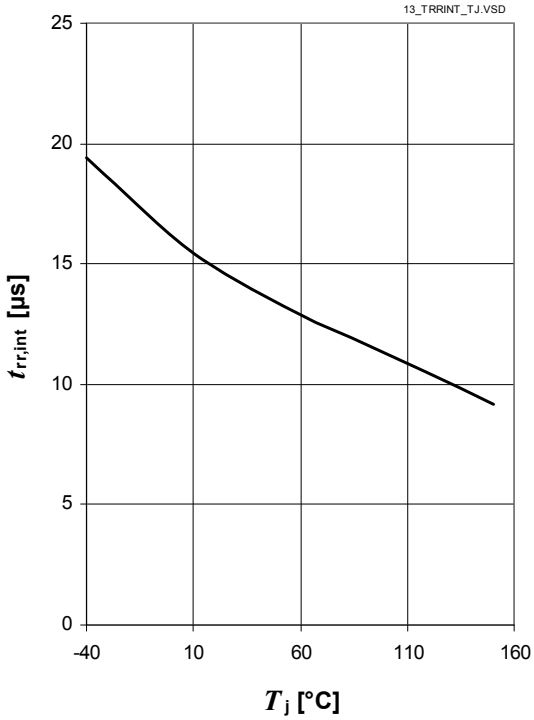
Undervoltage Reset Switching Threshold V_{RT} versus Junction Temperature T_j



Power On Reset Delay Time t_{rd} versus Junction Temperature T_j



Internal Reset Reaction Time $t_{rr,int}$ versus Junction Temperature T_j



Delay Capacitor Discharge Time $t_{rr,d}$ versus Junction Temperature T_j