Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

7 A H-Bridge for DC-Motor Applications TLE 6209 R

Data Sheet

AEC Qualified RoHS

1 Overview

1.1 Features

PG-DSO-20-37, -65

- Delivers up to 6 A continuous and 7 A peak current
- Optimized for DC motor management applications
- Very low $R_{DS\ ON}$ of typ. 150 mΩ @ 25 °C per switch
- Operates at supply voltages of up to 40V
- Overvoltage Protection against transients up to 45 V
- Outputs fully short circuit protected
- Standard SPI-Interface, daisy chain capability
- Adjustable chopper current regulation of up to 7 A
- Temperature monitor with prewarning, warning and shutdown
- Over- and Undervoltage-Lockout
- Open load detection
- Detailed load failure diagnosis by SPI
- Minimized power dissipation due to active free-wheeling
- Low EMI due to voltage slope regulation
- Very low current consumption (typ. 20 µA @ 25 °C) in stand-by (Inhibit) mode
- Enhanced power PG-DSO-Package
- Green Product (RoHS compliant)
- AEC Qualified

Type	Package
TLE 6209 R	PG-DSO-20-37, -65

Functional Description

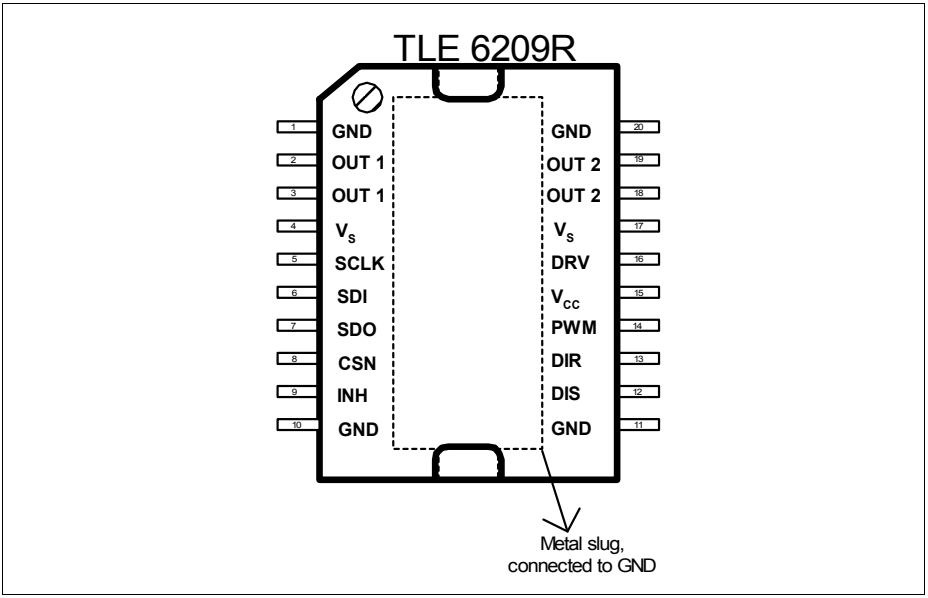
The TLE 6209 R is an integrated power H-Bridge with D-MOS output stages for driving bidirectional loads such as DC-Motors. The design is based on Infineons Smart Power Technology SPT which allows bipolar, CMOS and power D-MOS devices on the same monolithic circuit.

Operation modes forward (cw), reverse (ccw) and brake are invoked by two control pins PWM and DIR. Protection and a reliable diagnosis of overcurrent, openload, short-circuit to ground, to the supply voltage or across the load are integrated. Detailed diagnostic

information is given via the 8 bit SPI status word. An integrated chopper current limitation limits the current e.g. to reduce power dissipation during mechanical block of a DC motor. Several device parameters can be set by the SPI control word. A three-level temperature monitoring with prewarning, warning and shutdown is included for controlled operation under critical power loss conditions. The full protection and diagnosis capability make the device suitable especially for safety relevant applications, e.g. in automotive ECUs.

1.2 Pin Configuration

(top view)



Pin Definitions and Functions

V_S	Power Supply Voltage	V_{CC}	5 V Logic Supply
DRV	Input for Charge pump buffer capacitor	GND	Ground
SDI	Serial Data Input	SDO	Serial Data Output
SCLK	Serial Clock Input	CSN	Chip-Select-Not Input
OUT	Power Output	–	–
PWM	PWM Input	DIR	Direction Input
DIS	Disable Input	INH	Inhibit

1.2.1 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 10, 11, 20	GND	**Ground;** internally connected to cooling tab (heat slug); to reduce thermal resistance place cooling areas and thermal vias on PCB.
2,3	OUT1	**Output 1**; output of D-MOS half bridge 1; external connection between pin 2 and pin 3 is necessary.
4,17	V_S	**Power supply**; needs a blocking capacitor as close as possible to GND; 47 µF electrolytic in parallel to 220 nF ceramic is recommended; external connection between pin 4 and pin 17 is necessary.
5	SCLK	**Serial clock input**; clocks the shiftregister; SCLK has an internal active pull down and requires CMOS logic levels
6	SDI	**Serial data input;** receives serial data from the control device; serial data transmitted to SDI is an 8 bit control word with the Least Significant Bit (LSB) being transferred first; the input has an active pull down and requires CMOS logic levels; SDI will accept data on the falling edge of SCLK-signal; see **Table 1** for input data protocol.
7	SDO	**Serial-Data-Output;** this tri-state output transfers diagnosis data to the control device; the output will remain tri-stated unless the device is selected by a low on Chip-Select-Not (CSN); SDO state changes on the rising edge of SCLK; see **Table 4** for diagnosis protocol.
8	CSN	**Chip-Select-Not input**; CSN is an active low input; serial communication is enabled by pulling the CSN terminal low; CSN input should only be transitioned when SCLK is low; CSN has an internal active pull up and requires CMOS logic levels.
9	INH	**Inhibit input;** has an internal pull down; device is switched in standby condition by pulling the INH terminal low.
12	DIS	**Disable input;** has an internal pull up; the output stages are switched in tristate condition by pulling the DIS terminal high.
13	DIR	**Direction input;** has an internal pull down; TTL/CMOS compatible input.
14	PWM	**PWM input;** has an internal pull down; TTL/CMOS compatible input.
15	V_{CC}	**Logic supply voltage**; needs a blocking capacitor as close as possible to GND; 10 µF electrolytic in parallel to 220 nF ceramic is recommended.

1.2.1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function
16	DRV	**Drive;** Input for external charge pump capacitor C_{DRV}
18,19	OUT2	**Output 2**; output of D-MOS half bridge 2; external connection between pin 2 and pin 3 is necessary.

1.3 Functional Block Diagram

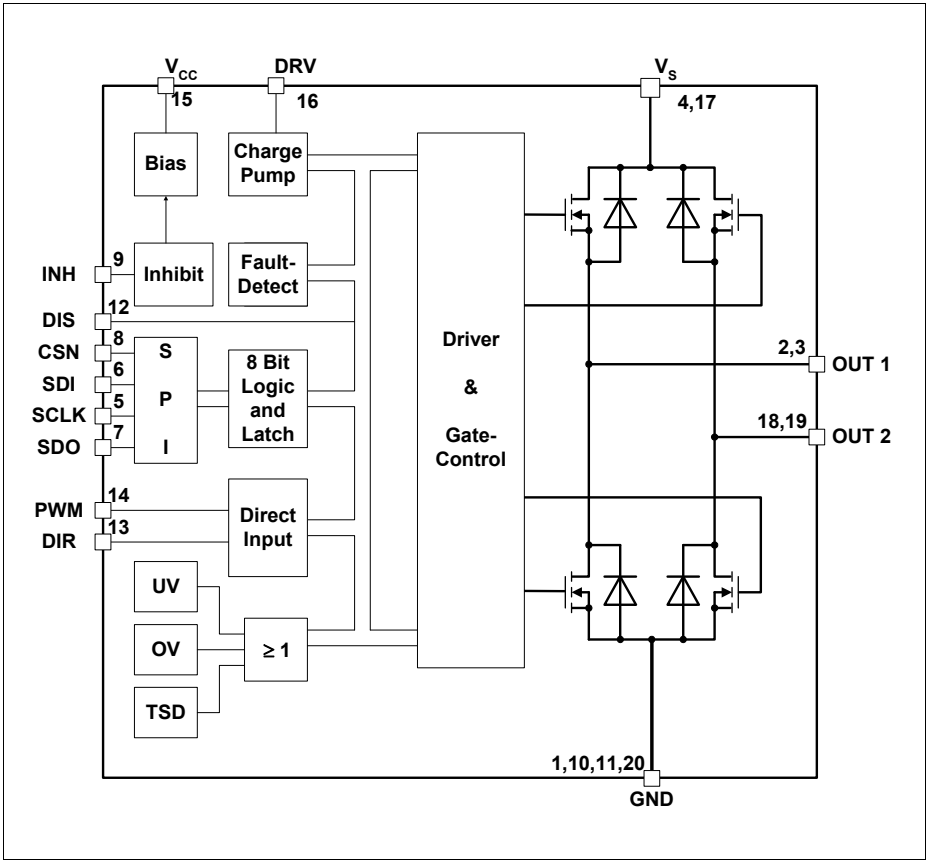


Figure 1 Block Diagram

2 Circuit Description

2.1 Serial Peripheral Interface (SPI)

The SPI is used for bidirectional communication with a control unit. The 8-bit programming word or control word (see **Table 1**) is read in via the SDI serial data input, and this is synchronized with the serial clock input SCLK. The status word appears synchronously at the SDO serial data output (see **Table 4**).

The transmission cycle begins when the chip is selected with the chip-select-not (CSN) input (H to L). When the CSN input changes from L to H, the word which has been read into the shift register becomes the control word. The SDO output switches then to tristate status, thereby releasing the SDO bus circuit for other uses. The SPI allows to parallel multiple SPI devices by using multiple CSN lines. Due to the full duplex shift register, the TLE 6209 R can also be used in daisy-chain configuration.

The settings made by the SPI control word become active at the end of the SPI transmission and remain valid until a different control word is transmitted or a power on reset occurs. At each SPI transmission, the diagnosis bits as currently valid in the error logic are transmitted. The behavior of the diagnosis bits is described in **Section 2.5**.

Table 1 Input Data Protocol

Bit	
7	Status Register Reset: H = reset
6	OVLO: H = on, L = off
5	not used
4	MSB of 2bit chopper-OFF-time
3	LSB of 2bit chopper-OFF-time
2	PWM Operation mode: H = Fast decay, L = Slow decay
1	MSB of 2 bit chopper current limit
0	LSB of 2 bit chopper current limit

Table 2 Programmable Chopper Current Limit I_{L_xx}

Bit 1	Bit 0	Current limit
0	0	I_{L_00}
0	1	I_{L_01}
1	0	I_{L_10}
1	1	I_{L_11}

Note: For actual values, see page 16

Table 3 Programmable Chopper OFF-time t_{OFF_xx}

Bit 4	Bit 3	Chopper-OFF-time
0	0	t_{OFF_00}
0	1	t_{OFF_01}
1	0	t_{OFF_10}
1	1	t_{OFF_11}

Note: For actual values, see page 16

Table 4 Diagnosis Data Protocol

Bit	H = Error/L = no error
7	Power supply fail
6	not used, always H
5	Short to V_S or across the load
4	Short to GND
3	Open load
2	MSB of Temperature Monitoring
1	LSB of Temperature Monitoring
0	Error-Flag

Table 5 Temperature Monitoring

Bit 2	Bit 1	Chip Temperature
0	0	Below Prewarning
0	1	Temperature Prewarning

Table 5 Temperature Monitoring

Bit 2	Bit 1	Chip Temperature
1	0	Temperature Warning
1	1	Overtemperature Shutdown

2.2 Supply

2.2.1 Logic Supply Voltage, Power-On-Reset

The logic is supplied with 5 V by the V_{CC} pin, separated from the power stage supply V_S. The advantage of this system is that information stored in the logic remains intact even in the event of failures in the supply voltage V_S. The power supply failure information can be read out via the SPI. If V_{CC} falls below typically 4.5 V, the logic is shut down, all internally stored data is deleted and the Output Stages are switched to tristate. The IC is restarted on rising V_{CC} with a hysteresis of typically 80 mV

After this restart at increasing V_{CC}, or if the device is activated after having been set into inhibit mode (INH L to H), the IC is initialized by Power-On-Reset (POR). After POR, all SPI control bits are set to L. This setting remains valid until first SPI communication. Also the error bits are reset by POR.

2.2.2 Power Supply Voltage

The power stages are connected to the supply voltage V_S. This voltage is monitored by over voltage (OV) and under voltage (UV) comparators as described in **Section 2.5.6**. The power supply voltage needs a blocking capacitor to GND.

2.3 Direct Inputs

2.3.1 Inhibit (sleep mode)

The INH input can be used to cut off the complete IC. By pulling the INH input to low, the power stages are switched to tristate, and the current consumption is reduced to just a few µA at both the V_S and the V_{CC} input. It also leads to the loss of any data stored. The TLE 6209 R is reinitialized with POR if INH is put to high again. The pin has an internal pull-down.

2.3.2 Disable

The DIS input can be used to disable the output stages. By pulling the DIS input to high the power stages are switched to tristate, regardless of the signals at the DIR and PWM inputs. The DIS input can be used as an emergency disable without resetting the SPI data stored in the IC. It has an internal pull-up.

2.3.3 Direction and PWM

The power stages are controlled by the direct inputs DIR and PWM as given in **Table 6** and further illustrated in **Figure 2**. The DIR input gives the direction of output current, while the PWM input controls whether the current is increased or reduced. The SPI control bit 2 sets the decay mode, i.e. determines what happens if PWM = L. In pulse-width modulated applications, this control scheme allows to supply the PWM-signal always through the same port, using less controller resources.

Table 6 Functional Truth Table

DIR	PWM	MODE (Bit 2)	OUT1	OUT2	Comments
0	1	0 (slow decay)	H	L	Motor turns clockwise
0	0		H	H	Freewheel with slow decay
1	1		L	H	Motor turns counterclockwise
1	0		H	H	Freewheel with slow decay
0	1	1 (fast decay)	H	L	Motor turns clockwise
0	0		L	H	Fast decay
1	1		L	H	Motor turns counterclockwise
1	0		H	L	Fast decay

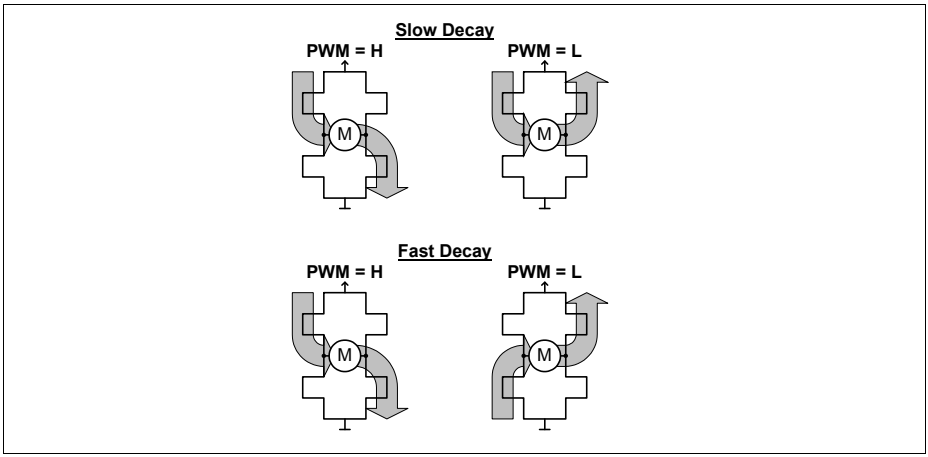


Figure 2 DIR/PWM Control with Slow- and Fast Decay

2.4 Power Stages

The output stages consist of a DMOS H-bridge built by two highside switches and two lowside switches. Integrated circuits protect the outputs against overcurrent and overtemperature if there is a short-circuit to ground or to the supply voltage or across the load. Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes.

2.4.1 Charge Pump

To realize the fast switching times, the charge pump, which generates the voltage necessary to switch on the n-channel D-MOS high-side switches, must be highly efficient. It requires an external capacitor C_{DRV} which is connected to V_S and the charge pump buffer input, DRV. It should be placed as close to the pins as possible.

2.4.2 Chopper Current Limitation

To limit the output current, a chopper current limitation is integrated as shown in **Figure 3**. The current is measured by sense cells integrated in the low-side switches. As soon the current limit I_L is reached, the low-side switch is switched off for a fixed time t_{OFF}. I_L and t_{OFF} can be set by the SPI control bits 0,1, 3 and 4.

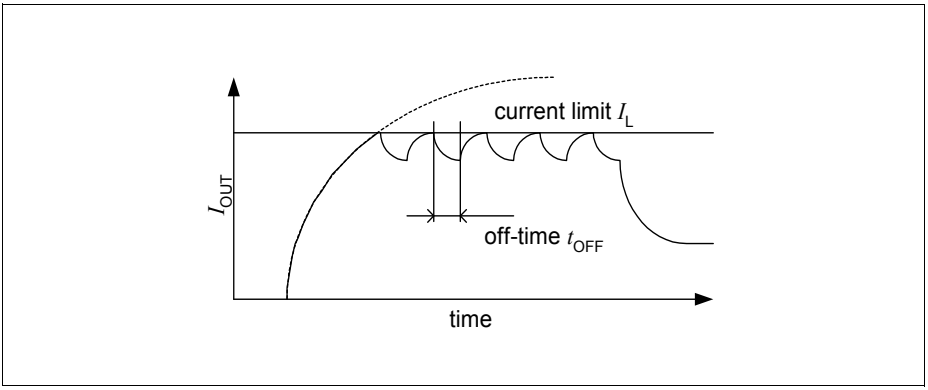


Figure 3 Chopper current limitation

2.4.3 Active Freewheeling

When drivng inductive loads with PWM operation, the dissipated power can be significantly reduced by activating the transistor located parallel to the internal freewheeling diode. This is realized in the TLE 6209 R. When switching an output from L to H, the high-side switch is turned on after a certain dead-time to avoid cross currents flowing through the half bridge.

2.5 Protection and Diagnosis

2.5.1 Short of Output to Ground

The high-side switches are protected against a short of the output to ground by an over current shutdown. If a high-side switch is turned on and the current rises above the high-side shutdown threshold I_{SDH} for longer than the shutdown delay time t_{dOC}, all output transistors are turned off and bit 4 the SPI diagnosis word is set. During the delay time, the current is limited to I_{SC} (typically 20 A). The output stages stay off and the error bit set until a status register reset (bit 7 of SPI control word) is received or a power-on reset is performed.

2.5.2 Short of Output to V_S

Due to the chopper current regulation, the low-side switches are protected against a short to the supply voltage. To detect the short, the first time the current limit is reached, the off-command for the low-side switch is blanked out for 10 µs. If the current rises above the low-side shutdown threshold I_{SDL} during this time, all output transistors are turned off and bit 5 in the SPI diagnosis word is set. The value of the shutdown threshold depends on the current limit that is set via the SPI. The shutdown threshold is 1 A higher than the current limit. The output stages stay off and the error bit set until a status register reset (bit 7 of SPI control word) is received or a power-on reset is performed.

2.5.3 Short Across the Load

The short circuit protection circuits of the high- and low-side switches work independently of each other. In most cases, a short across the load will be detected as a short to V_S because of the longer filter time in the high-side switches t_{dOC} and the higher shutdown threshold I_{SDH}.

2.5.4 Open Load

If the current through the low side transistor is lower than the reference current I_{dOL} in ON-state (PWM = H), a timer is started. After a filter time t_{dOC} an open load failure will be recognized and the status bit 3 is set. If the current exceeds the reference current I_{dOL} the open load timer is reset. If the H-bridge is switched to OFF-state (PWM = L) the timer is stopped but not reset. The timer continues if the H-bridge is switched to ON-state again. There is no reset of the open load timer if the direction is changed using the DIR input in open load condition. The open load error bit is latched and can be reset by the status register reset bit 7 of the SPI control word or a POR.

2.5.5 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the prewarning, warning and shutdown

thresholds. As soon as a threshold is reached, the according status bits are set in the SPI diagnosis word (c.f. **Table 5**). If the overtemperature shutdown threshold is reached, the output stages are turned off. The temperature monitoring messages and the over temperature shutdown are latched and can be reset by the status register reset bit 7 of the SPI control word or a POR.

2.5.6 Power Supply Fail

The power supply Voltage is monitored for over- and under voltage lockout:

- **Under Voltage Lockout**
  If the supply voltage V_S drops below the switch off voltage $V_{UV\,OFF}$, all output transistors are switched off and the power supply fail bit (bit 7 of the SPI diagnosis word) is set. If V_S rises again and reaches the switch on voltage $V_{UV\,ON}$, the power stages are restarted. The error bit, however, is latched and has to be reset by the status register reset bit 7 of the SPI control word.
- **Over Voltage Lockout**
  If the supply voltage V_S rises above the switch off voltage $V_{OV\,OFF}$, all output transistors are switched off and the power supply fail bit (bit 7 of the SPI diagnosis word) is set. If V_S falls again and reaches the switch on voltage $V_{OV\,ON}$, the power stages are restarted. The error bit, however, is latched and has to be reset by the status register reset bit 7 of the SPI control word.
  The OVLO is only active if control bit 6 is H. If the bit is low, the OVLO is deactivated.

2.5.7 Error Flag

Bit 0 of the SPI diagnosis word is an OR of the status bits 1 to 7. It can be read out without full SPI communication as described in **Figure 8**.

3 Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Voltages					
Supply voltage	V_S	– 0.3	40	V	–
Supply voltage	V_S	– 1	45	V	t < 0.5 s; I_S > – 2 A
Logic supply voltage	V_{CC}	– 0.3	5.5	V	0 V < V_S < 40 V
Logic input voltages (SDI, SCLK, CSN, INH, DIS, PWM, DIR)	V_I	– 0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{CC} < 5.5 V
Logic output voltage (SDO)	V_O	– 0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{CC} < 5.5 V
Output voltage (OUT1, OUT2)	V_{OUT}	– 0.3 V	V_S + 1,5V	–	0 V < V_S < 40 V
Charge pump buffer voltage (DRV)	V_{DRV}	V_S – 0.3 V	V_S + 15 V	–	0 V < V_S < 40 V
Currents					
Output current (cont.)	I_{OUT}	–	–	A	internally limited, see page 16 and page 17.
Output current (peak)	I_{OUT}	–	–	A	
Temperatures					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	40	V	After V_S rising above $V_{UV\ ON}$
Supply voltage slew rate	dV_S/dt	–10	10	V/µs	–
Logic supply voltage	V_{CC}	4.75	5.50	V	–
Supply voltage increasing	V_S	– 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	– 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (SDI, SCLK, CSN, INH)	V_I	– 0.3	V_{CC}	V	–
SPI clock frequency	f_{CLK}	–	2	MHz	–
Junction temperature	T_j	– 40	150	°C	–
Thermal Resistances					
Junction pin	R_{thjC}	–	1.5	K/W	measured to pin 1, 10, 11, 20
Junction ambient	R_{thjA}	–	50	K/W	–

3.3 Electrical Characteristics

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Current Consumption						
Quiescent current	I_S	–	–	50	µA	INH = Low; V_S = 13.2 V
Quiescent current	I_S	–	10	30	µA	INH = Low; V_S = 13.2 V; T_j = 25 °C
Logic-Supply current	I_{CC}	–	–	20	µA	INH = Low
Logic-Supply current	I_{CC}	–	2.0	4.0	mA	–
Supply current	I_S	–	2.8	5.0	mA	–
Over- and Under-Voltage Lockout						
UV-Switch-ON voltage	$V_{UV\,ON}$	–	5.4	5.7	V	V_S increasing
UV-Switch-OFF voltage	$V_{UV\,OFF}$	4.4	4.9	5.2	V	V_S decreasing
UV-ON/OFF-Hysteresis	$V_{UV\,HY}$	0.2	0.5	–	V	$V_{UV\,ON} - V_{UV\,OFF}$
OV-Switch-OFF voltage	$V_{OV\,OFF}$	34	37	40	V	V_S increasing
OV-Switch-ON voltage	$V_{OV\,ON}$	28	32	36	V	V_S decreasing
OV-ON/OFF-Hysteresis	$V_{OV\,HY}$	–	5.0	–	V	$V_{OV\,OFF} - V_{OV\,ON}$

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Outputs OUT1-2						
Static Drain-Source-On Resistance						
Source (High-Side) I_{OUT} = – 3 A	$R_{DS\ ON\ H}$	–	140	170	mΩ	5.2 V < V_S < 40 V T_j = 25 °C; C_{DRV} = 33 nF
			–	280	mΩ	5.2 V < V_S < 40 V C_{DRV} = 33 nF
Sink (Low-Side) I_{OUT} = 3 A	$R_{DS\ ON\ L}$	–	130	160	mΩ	5.2 V < V_S < 40 V T_j = 25 °C; C_{DRV} = 33 nF
			–	270	mΩ	5.2 V < V_S < 40 V C_{DRV} = 33 nF
Clamp Diodes Forward Voltage						
Upper	V_{FU}	–	1.0	1.5	V	I_F = 3 A
Lower	V_{FL}	–	1.0	1.5	V	I_F = 3 A

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Open Circuit/Underload Detection						
Detection current	I_{OCD}	30	–	130	mA	–
Delay time	t_{dOC}	2	–	8	ms	–
Current Limits						
Current limit	I_{L_00}	3.4	4	4.6	A	Bit 0 = L; Bit 1 = L;
Current limit	I_{L_01}	4.25	5	5.75	A	Bit 0 = H; Bit 1 = L;
Current limit	I_{L_10}	5.1	6	6.9	A	Bit 0 = L; Bit 1 = H;
Current limit	I_{L_11}	5.95	7	8.05	A	Bit 0 = H; Bit 1 = H;
Low-Side Switch Overcurrent						
Shutdown Threshold	ΔI_{SDL}	0.5	1.0	1.5	A	$\Delta I_{SDL} = I_{SDL} - I_L$
Note: low-side shutdown threshold is guaranteed by design						
Switch-OFF Time during Current Limitation (Chopper OFF-Time)						
OFF-time	t_{OFF_00}	16	24	28	µs	Bit 3 = L; Bit 4 = L;
OFF-time	t_{OFF_01}	32	43	51	µs	Bit 3 = H; Bit 4 = L;
OFF-time	t_{OFF_10}	48	62	74	µs	Bit 3 = L; Bit 4 = H;
OFF-time	t_{OFF_11}	64	80	96	µs	Bit 3 = H; Bit 4 = H;

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High-Side Switch Overcurrent						
High-side shutdown threshold	I_{SDH}	8	12	18	A	–
Shutdown delay time	t_{dSD}	15	25	40	µs	–
Short circuit current	I_{SC}	–	–	25	A	during t_{dSD}
*Note: For short circuit current definition, see **Figure 5**. Short circuit current is guaranteed by design*						
Leakage Current / Output Current in Tristate						
Source-Output-Stage	I_{QLH}	– 120	– 50	–	µA	V_{OUT} = 0 V
Sink-Output-Stage	I_{QLL}	–	0.5	1	mA	V_{OUT} = V_S
Output Delay Times (device not in stand-by for t > 1 ms)						
High-side ON	$t_{d\ ON\ H}$	–	4	10	µs	V_S = 13.2 V, Resistive load of 12 Ω
High-side OFF	$t_{d\ OFF\ H}$	–	0.6	1	µs	
Low-side ON	$t_{d\ ON\ L}$	–	2	3.5	µs	
Low-side OFF	$t_{d\ OFF\ L}$	–	2.5	4	µs	
Output Switching Times (device not in stand-by for t > 1 ms)						
High-side switch rise time	$t_{RISE\ H}$	–	1.8	3.5	µs	V_S = 13.2 V, Resistive load of 12 Ω
High-side switch fall time	$t_{FALL\ H}$	–	0.2	0.8	µs	
Low-side switch rise time	$t_{RISE\ L}$	2	6.5	11	µs	
Low-side switch fall time	$t_{FALL\ L}$	2	4.3	6.5	µs	
*Note: For switching time definitions, see **Figure 6**.*						

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Inhibit Input						
H-input voltage threshold	V_{IINHH}	–	–	0.7	V_{CC}	–
L-input voltage threshold	V_{IINHL}	0.2	–	–	V_{CC}	–
Hysteresis of input voltage	V_{IINHHY}	50	300	500	mV	–
Pull down current (low)	I_{IINHL}	10	25	50	µA	V_{IINH} = 0.2 × V_{CC}
Pull down current (high)	I_{IINHH}	–	–	80	µA	V_{IINH} = 0.7 × V_{CC}
Disable Input						
H-input voltage threshold	V_{IDISH}	–	–	0.7	V_{CC}	–
L-input voltage threshold	V_{IDISL}	0.2	–	–	V_{CC}	–
Hysteresis of input voltage	V_{IDISHY}	50	300	500	mV	–
Pull up current (high)	I_{IDISH}	– 50	– 25	– 10	µA	V_{IDIS} = 0.7 × V_{CC}
Pull up current (low)	I_{IDISL}	– 50	–	–	µA	V_{IDIS} = 0.2 × V_{CC}
Direction/PWM Input						
H-input voltage threshold	V_{IH}	–	–	0.7	V_{CC}	–
L-input voltage threshold	V_{IL}	0.2	–	–	V_{CC}	–
Hysteresis of input voltage	V_{IHY}	50	300	500	mV	–
Pull down current (low)	I_I	10	25	50	µA	V_I= 0.2 × V_{CC}
Pull down current (high)	I_I	–	–	50	µA	V_I= 0.7 × V_{CC}

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
SPI-Interface						
Delay Time from Stand-by to Data In/Power on Reset						
Setup time	t_{set}	–	–	100	µs	–
Logic Inputs SDI, SCLK and CSN						
H-input voltage threshold	V_{IH}	–	–	0.7	V_{CC}	–
L-input voltage threshold	V_{IL}	0.2	–	–	V_{CC}	–
Hysteresis of input voltage	V_{IHY}	50	300	500	mV	–
Pull up current at pin CSN (high)	I_{ICSNH}	– 50	– 25	– 10	µA	V_{CSN} = 0.7 × V_{CC}
Pull up current at pin CSN (low)	I_{ICSNL}	– 50	–	–	µA	V_{CSN} = 0.2 × V_{CC}
Pull down current at pin SDI and SCLK (low)	I_{ISDIL} (I_{ISCLKL})	10	25	50	µA	V_{SDI} (V_{SCLK}) = 0.2 × V_{CC}
Pull down current at pin SDI and SCLK (high)	I_{ISDIH} (I_{ISCLKH})	–	–	50	µA	V_{SDI} (V_{SCLK}) = 0.7 × V_{CC}
Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	15	pF	0 V < V_{CC} < 5.25 V

Note: Input capacitances are guaranteed by design.

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Logic Output SDO						
H-output voltage level	V_{SDOH}	V_{CC} –1.0	V_{CC} –0.85	–	V	I_{SDOH} = 1 mA
L-output voltage level	V_{SDOL}	–	0.25	0.4	V	I_{SDOL} = – 1.6 mA
Tri-state leakage current	I_{SDOLK}	– 10	–	10	µA	V_{CSN} = V_{CC} 0 V < V_{SDO} < V_{CC}
Tri-state input capacitance	C_{SDO}	–	10	15	pF	V_{CSN} = V_{CC} 0 V < V_{CC} < 5.25 V

Note: Input capacitances are guaranteed by design.

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Serial Data Input Timing						
Serial Clock period	t_{PSCLK}	500	–	–	ns	–
Serial Clock high time	t_{SCLKH}	250	–	–	ns	–
Serial Clock low time	t_{SCLKL}	250	–	–	ns	–
Serial Clock low before CSN low	t_{bef}	250	–	–	ns	–
CSN setup time	t_{lead}	250	–	–	ns	–
SCLK setup time	t_{lag}	250	–	–	ns	–
Clock low after CSN high	t_{beh}	250	–	–	ns	–
SDI setup time	t_{SDISU}	125	–	–	ns	–
SDI hold time	t_{SDIHO}	125	–	–	ns	–
Input signal rise time at pin SDI, SCLK and CSN	t_{rSIN}	–	–	100	ns	–
Input signal fall time at pin SDI, SCLK and CSN	t_{fSIN}	–	–	100	ns	–
Serial Data Output Timing						
SDO rise time	t_{rSDO}	–	25	50	ns	C_L = 100 pF
SDO fall time	t_{fSDO}	–	25	50	ns	C_L = 100 pF
SDO enable time	t_{ENSDO}	–	–	125	ns	low impedance
SDO disable time	t_{DISSDO}	–	–	125	ns	high impedance
SDO valid time	t_{VASDO}	–	50	125	ns	V_{DO} < 0.2 V_{CC}; V_{DO} > 0.7 V_{CC}; C_L = 100 pF

3.3 Electrical Characteristics (cont'd)

8 V < V_S < 40 V; 4.75 V < V_{CC} < 5.25 V; INH = High; all outputs open;
– 40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Thermal Prewarning, Warning and Shutdown						
Thermal prewarning junction temperature	T_{jPW}	120	140	160	°C	–
Temperature prewarning hysteresis	ΔT	–	20	–	K	–
Thermal warning junction temperature	T_{jW}	140	160	180	°C	–
Temperature prewarning hysteresis	ΔT	–	20	–	K	–
Thermal shutdown junction temperature	T_{jSD}	160	180	200	°C	–
Temperature shutdown hysteresis	ΔT	–	20	–	K	–
Ratio of W to PW temperature	T_{jW} / T_{jPW}	1.07	1.14	–	–	–
Ratio of SD to W temperature	T_{jSD} / T_{jW}	1.06	1.13	–	–	–

Note: Temperature thresholds are guaranteed by design.

4 Diagrams

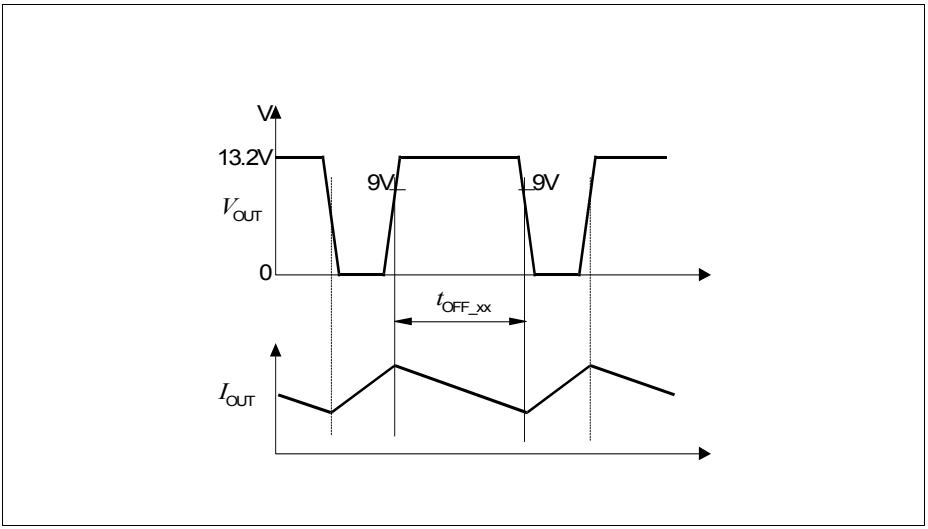


Figure 4 Switch-OFF time during current limitation (chopper OFF-time)

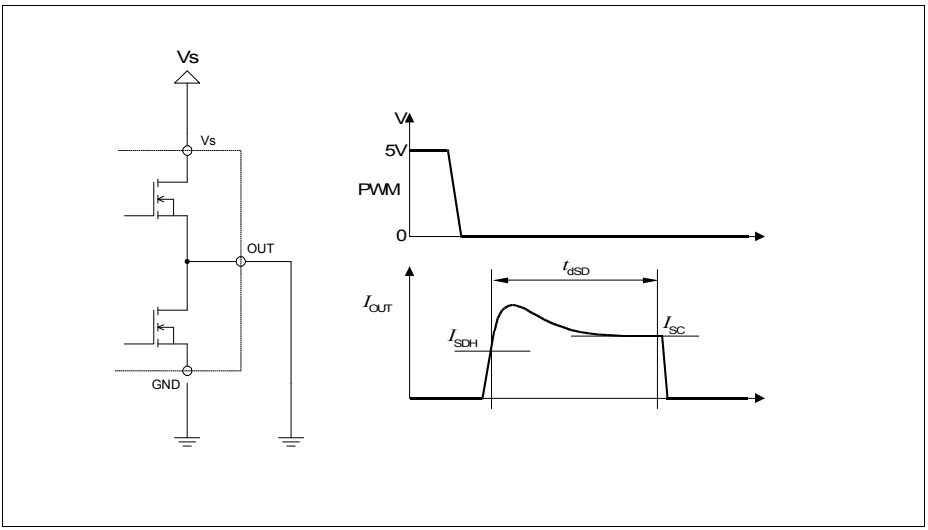


Figure 5 Short circuit of high-side switch to GND

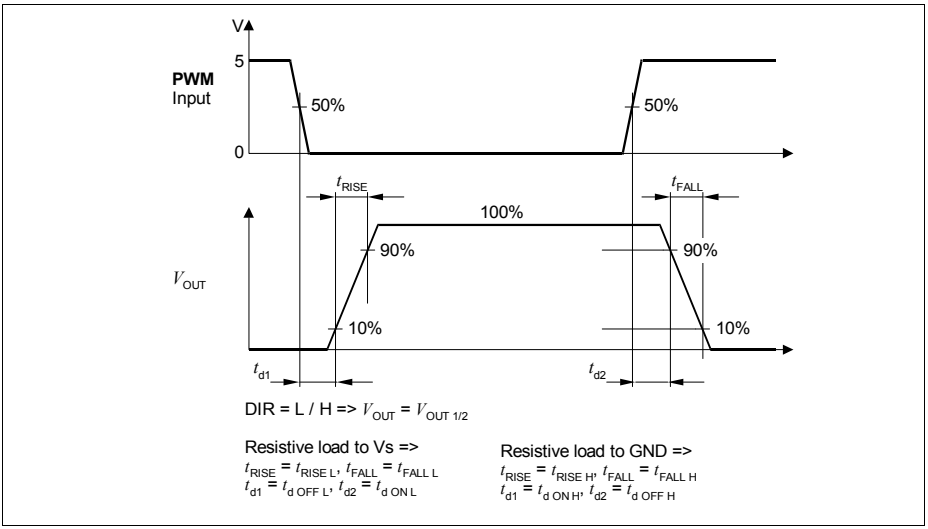


Figure 6 Output Delay and Switching Time Definitions

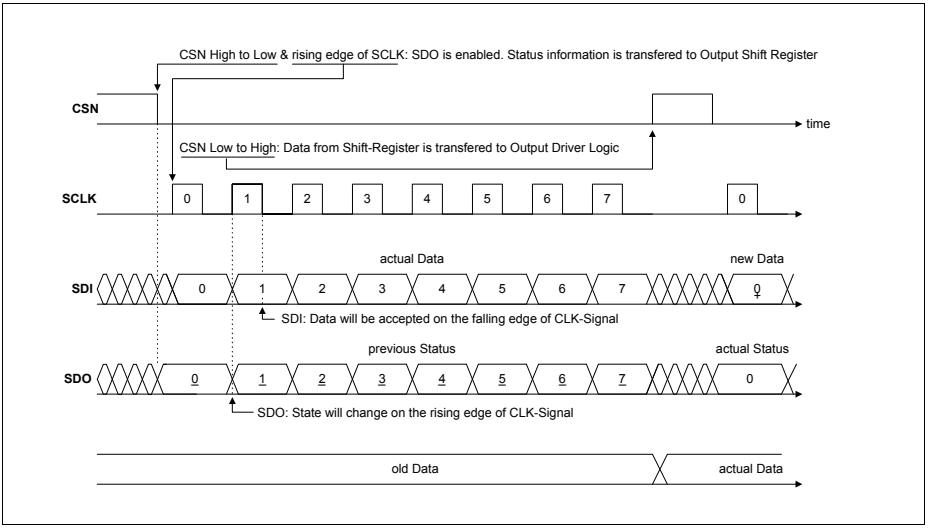


Figure 7 Standard Data Transfer Timing

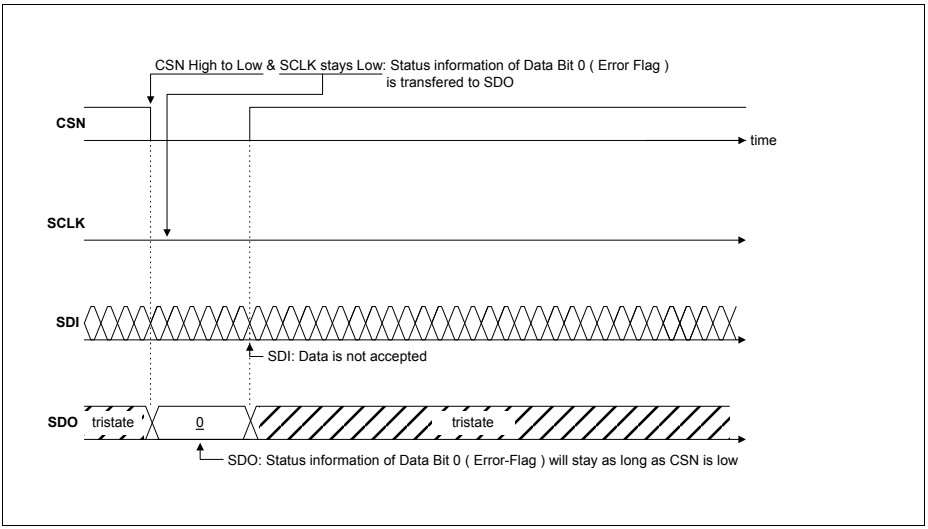


Figure 8 Timing for Error Detection Only

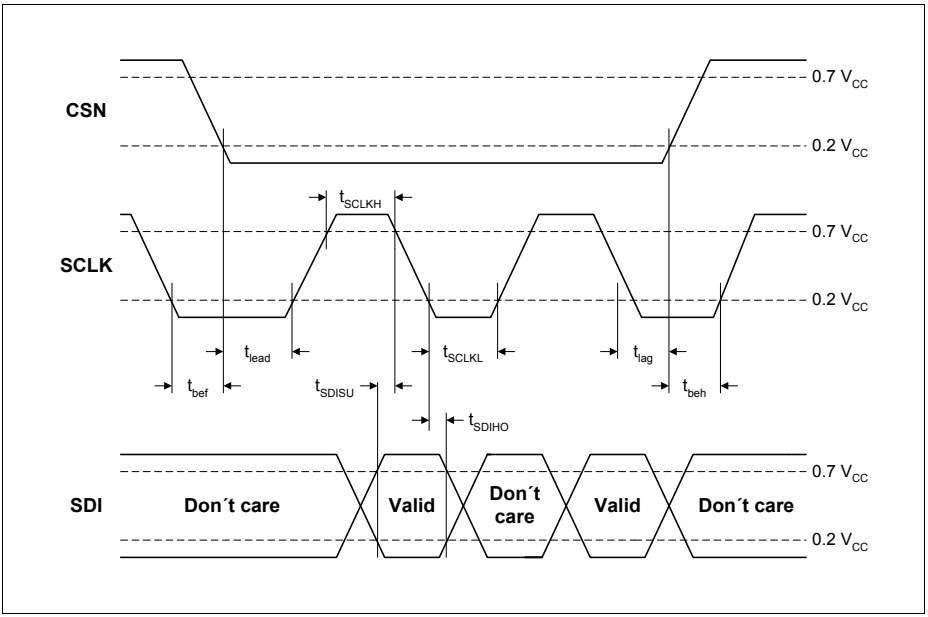


Figure 9 SPI-Input Timing