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18 Channel Smart Lowside Switch

ASSP for Powertrain

Data Sheet

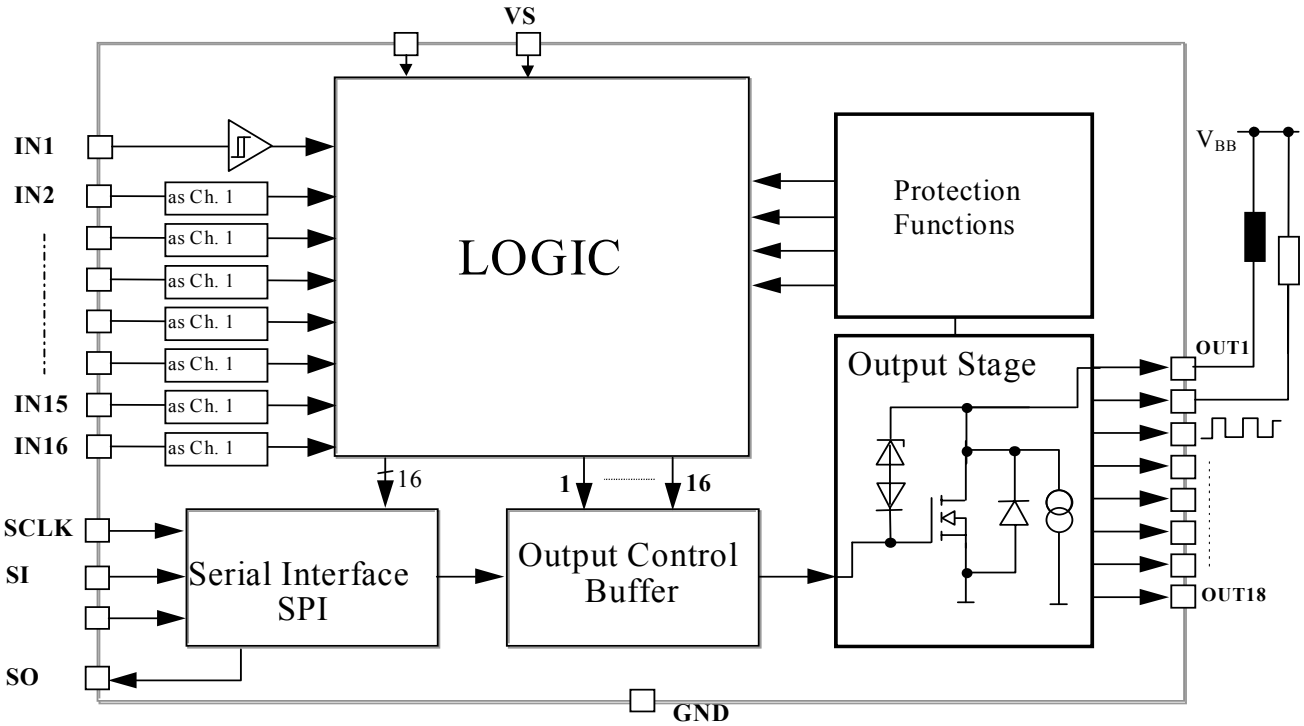
Features

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 16 bit Serial Data Input and Diagnostic Output (2 bit/chan. acc. SPI Protocol)
- Direct Parallel Control of 16 channels for PWM Applications
- Low Quiescent Current
- Compatible with 3.3V Microcontrollers
- Electrostatic discharge (ESD) Protection
- Green Product (RoHS-compliant)
- AEC qualified

PG-MQFP-64-10

General description

18-fold Low-Side Switch (0.35 Ω to 1 Ω) in Smart Power Technology (SPT) with a Serial Peripheral Interface (SPI) and 18 open drain DMOS output stages. The TLE6244X is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via SPI Interface. Additionally 16 of the 18 channels can be controlled direct in parallel for PWM applications. Therefore the TLE6244X is particularly suitable for engine management and powertrain systems.



1. Description

1.1 Short Description

This circuit is available in PG-MQFP-64 package or as chip.

1.1.1 Features of the Power Stages

	Nominal Current	$R_{on,max}$ at T_J = 25°C	static current limitation enabled by SPI	Clamping
OUT1, 2, 5, 6	2.2A	400mΩ	-	70V
OUT3, OUT4	2.2A	380mΩ	-	70V
OUT7, OUT8	1.1A	780mΩ	-	45V
OUT9, OUT10	2.2A	380mΩ	X	45V
OUT11...OUT14	2.2A	380mΩ	-	45V
OUT15, OUT16	3.0A	280mΩ	X	45V
OUT17, OUT18 *)	1.1A	780mΩ	X	45V

*) only serial control possible (via SPI)

Parallel connection of power stages is possible (see 1.13)
Internal short-circuit protection
Phase relation: non-inverting (exception: IN8->OUT8 is inverting)

1.1.2 Diagnostic Features

The following types of error can be detected:
- Short-circuit to U_{Batt} (SCB)
- Short-circuit to ground (SCG)
- Open load (OL)
- Overtemperature (OT)

Individual detection for each output.
Serial transmission of the error code via SPI.

1.1.3 VDD-Monitoring

Low signal at pin $\overline{\text{ABE}}$ and shut-off of the power stages if VDD is out of the permitted range.
Exception: If OUT8 is controlled by IN8, OUT8 will only be switched off by the overvoltage detection and not by undervoltage detection.
The state of VDD can be read out via SPI.

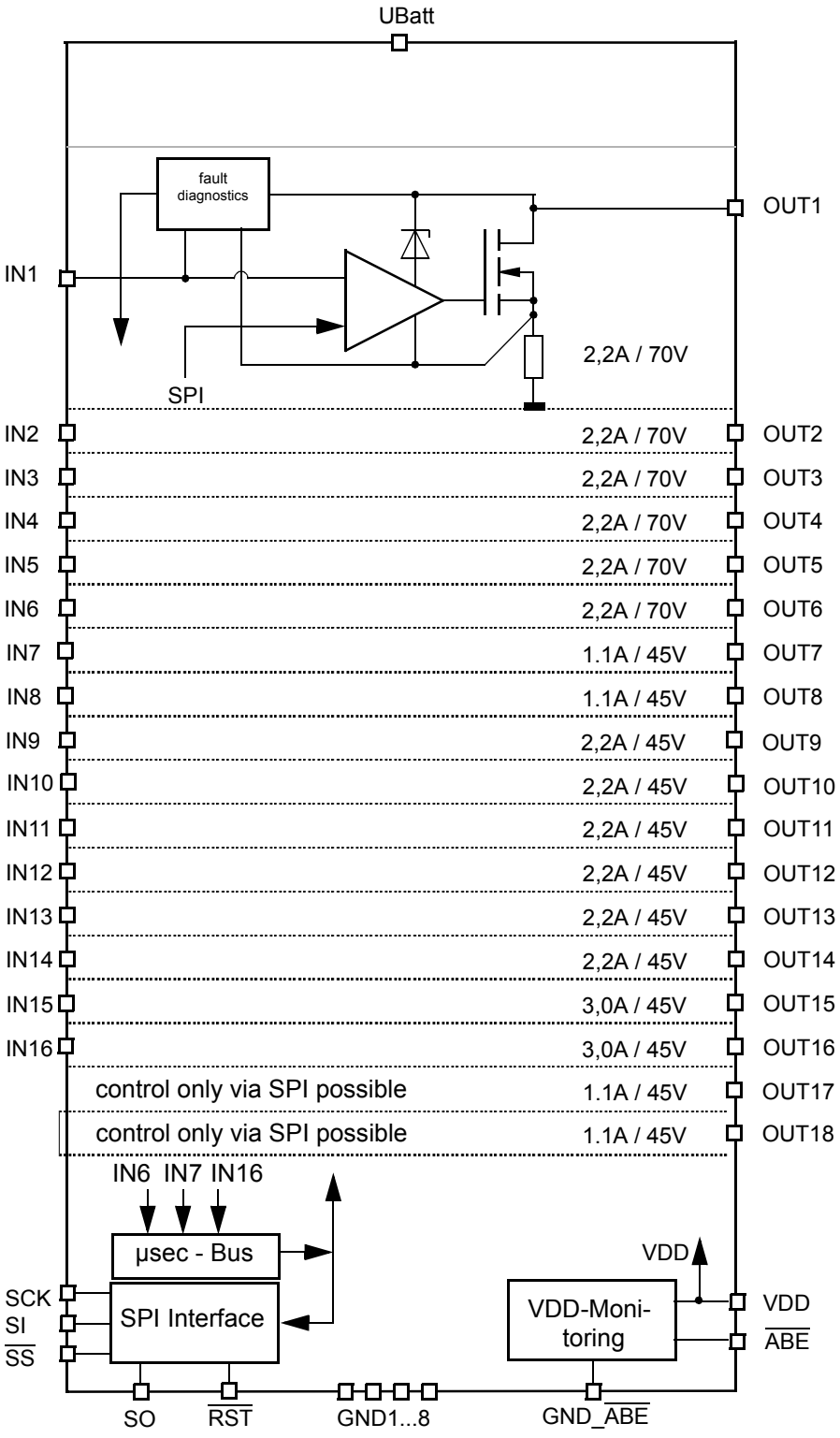
1.1.4 µsec-bus

Alternatively to the parallel and SPI control of the power stages, a high speed serial bus interface can be configured as control of the power stages OUT1...OUT7 and OUT9...OUT16.

1.1.5 Power Stage OUT8

OUT8 can be controlled by SPI or by the pin IN8 only. When controlled by IN8 this power stage is functional if the voltage at the pin VDD is above 3,5V. OUT8 will not be reset by RST. In SPI mode the power stage is fully supervised by the VDD-monitor.

1.2 Block Diagram



1.3 Description of the Power Stages

OUT1... OUT6

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the µsec-bus or via SPI. For T_J = 25°C the on-resistance of the power switches is below 400mΩ.
An integrated zener diode limits the output voltage to 70V typically.

A protection for inverse current is implemented for OUT1... OUT4 for use as stepper-motor control.

OUT9... OUT14

6 non-inverting low side power switches for nominal currents up to 2.2A. Control is possible by input pins, by the µsec-bus or via SPI. For T_J = 25°C the on-resistance of the power switches is below 380mΩ.
An integrated zener diode limits the output voltage to 45V typically.

OUT15, OUT16

2 non-inverting low side power switches for nominal currents up to 3.0A. Control is possible by input pins, by the µsec-bus or via SPI. For T_J = 25°C the on-resistance of the power switches is below 280mΩ.
An integrated zener diode limits the output voltage to 45V typically.

OUT7, OUT8, OUT17, OUT18

4 low side power switches for nominal currents up to 1100mA. Stage 7 is non-inverting, Stage 8 is inverting (IN8 = '1' => OUT8 is active). For the output OUT7 control is possible by the input pin, by the µsec-bus or via SPI, OUT8 is controlled by the input pin IN8 or via SPI, for the outputs OUT17 and OUT18 control is only possible via SPI. For T_J = 25°C the on-resistance of the power switches is below 780mΩ.
An integrated zener diode limits the output voltage to 45V typically.

In order to increase the switching current or to reduce the power dissipation parallel connection of power stages is possible (for additional information see 1.13).
The power stages are short-circuit proof:
Power stages **OUT1...OUT8, OUT11.14**: In case of overload (SCB) they will be turned off after a given delay time. During this delay time the output current is limited by an internal current control loop.
Power stages **OUT9, OUT10, OUT15...OUT18**:
In case of SCB these power stages can be configured for a shut-down mode or for static current limitation. In the shut down mode while SCB they will behave like OUT1..8 or OUT11..14.
In case of static current limitation and SCB the current is limited and the corresponding bit combination is set (early warning) after a given delay time. They will not be turned off. If this condition leads to an overtemperature condition, the output will be set into a low duty cycle PWM (selective thermal shut- down with restart) to prevent critical chip temperature.

There are 3 possibilities to turn the power stages on again:
- turn the power stage off and on, either via serial control (SPI) or via parallel control (input pin, except outputs OUT17 and OUT18) or by the µsec-bus (except OUT8, OUT17,OUT18)
- applying a reset signal.
- sending the instruction "del_dia" by the SPI-interface

The VDD-monitoring locks all power stages, except OUT8 for access by the IN8 input. OUT8 is locked by an internal threshold of 3,5V maximum when controlled by IN8. Otherwise OUT8 is locked by the VDD-monitor.

All low side switches are equipped with fault diagnostic functions:

- short-circuit to U_{Batt}: (SCB) can be detected if switches are turned on
- short-circuit to ground: (SCG) can be detected if switches are turned off
- open load: (OL) can be detected if switches are turned off
- overtemperature: (OT) will only be detected if switches are turned on

The fault conditions SCB, SCG, OL and OT will not be stored until an integrated filtering time is expired (please note for PWM application). If, at one output, several errors occur in a sequence, always the last detected error will be stored (with filtering time). All fault conditions are encoded in two bits per switch and are stored in the corresponding SPI registers. Additionally there are two central diagnostic bits: one specially for OT and one for fault occurrence at any output.

The registers can be read out via SPI. After each read out cycle the registers have to be cleared by the DEL_DIA command.

1.3.1 Power Stage OUT8 (Condensed Description)

1.3.1.1 Control of OUT8 and VDD-Monitoring

OUT8 can be controlled by SPI or by the pin IN8 only, control by µs-bus is not possible. When controlled by IN8 this power stage is functional if the voltage at the pin VDD is above 3,5V. In SPI mode the power stage is fully supervised by the VDD-monitor.
If OUT8 is controlled by IN8, OUT8 will only be switched off by the overvoltage detection and not by undervoltage detection.

1.3.1.2 Phase Relation IN8 - OUT8

The phase relation IN8 -> OUT8 is inverting.
OUT8 is active if IN8 is set to logic '1' (high level, see 3.4.2) in case of parallel access.
On executing the read instruction on RD_INP1/2 the inverted status of IN8 is read back.

1.3.1.3 Reset / Power Stage Diagnostics

If OUT8 is controlled by IN8, OUT8 will not be reseted by RST.
After reset parallel control (by IN8) is active for OUT8.
If UVDD < 4.5V errors are not stored because of the active RST of the external Regulator. Nevertheless
OUT8 is protected against overload.

1.3.1.4 Input Current

The control input IN8 has an internal pull-down current source. Thus the input currents I IN8 are positive (flow into the pin).

1.3.1.5 On Resistance

For OUT8 and 3.5V < UVDD < 4.5V R on increases (see 3.8.5).

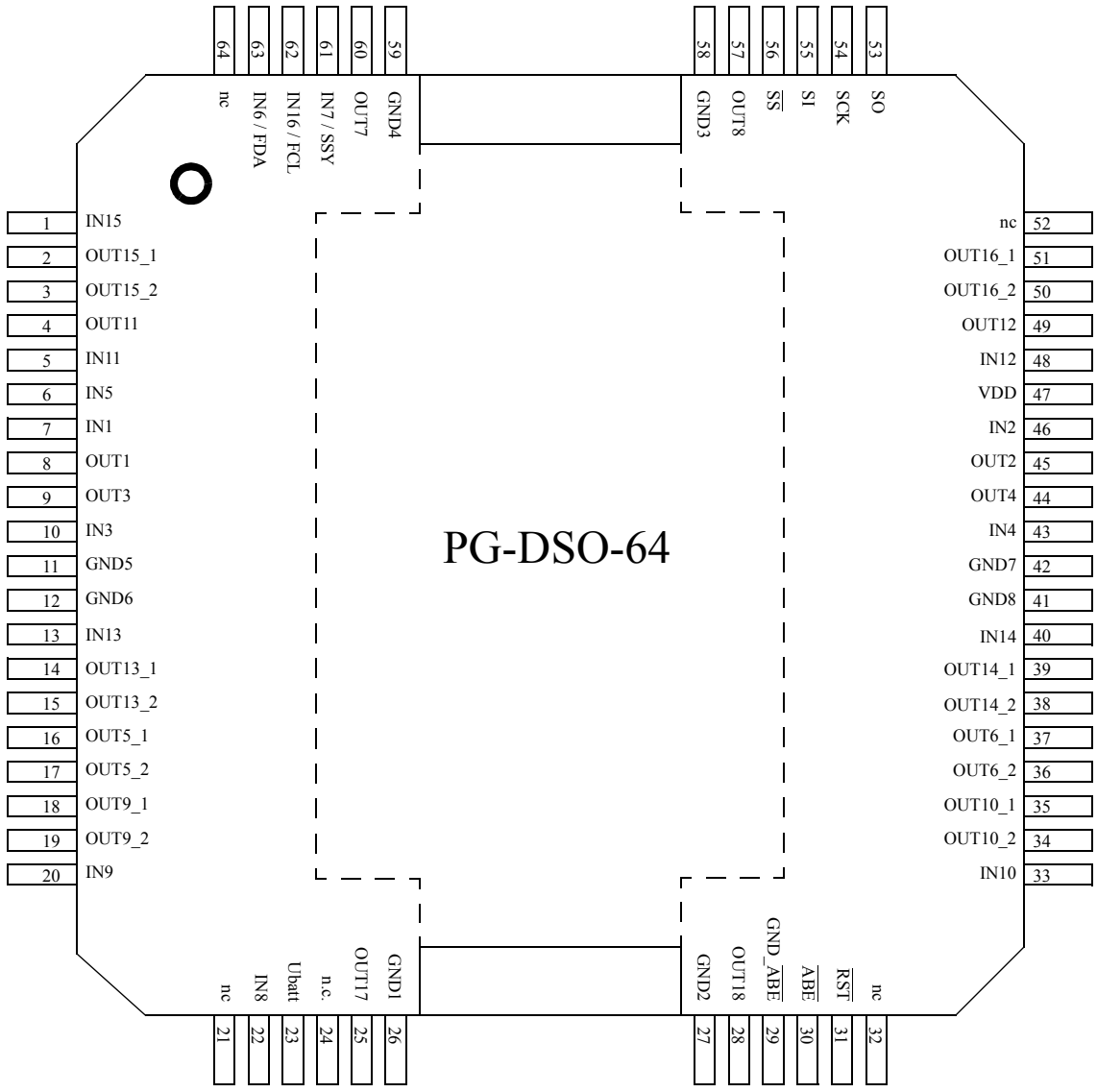
1.3.1.6 Parallel Connection of Power Stages

Parallel connection of power stages with OUT8 and parallel control is prohibited (inverting input IN8). Control via SPI is possible. See 1.13.

1.4 Pinout

Function	Pin	Pin Number
Input 1	IN1	7
Input 2	IN2	46
Input 3	IN3	10
Input 4	IN4	43
Input 5	IN5	6
Input 6 or FDA	IN6	63
Input 7 or SSY	IN7	61
Input 8	IN8	22
Input 9	IN9	20
Input 10	IN10	33
Input 11	IN11	5
Input 12	IN12	48
Input 13	IN13	13
Input 14	IN14	40
Input 15	IN15	1
Input 16 or FCL	IN16	62
Output 1	OUT1	8
Output 2	OUT2	45
Output 3	OUT3	9
Output 4	OUT4	44
Output 5_1	OUT5_1	16
Output 5_2	OUT5_2	17
Output 6_1	OUT6_1	37
Output 6_2	OUT6_2	36
Output 7	OUT7	60
Output 8	OUT8	57
Output 9_1	OUT9_1	18
Output 9_2	OUT9_2	19
Output 10_1	OUT10_1	35
Output 10_2	OUT10_2	34
Output 11	OUT11	4
Output 12	OUT12	49
Output 13_1	OUT13_1	14
Output 13_2	OUT13_2	15
Output 14_1	OUT14_1	39
Output 14_2	OUT14_2	38
Output 15_1	OUT15_1	2
Output 15_2	OUT15_2	3
Output 16_1	OUT16_1	51
Output 16_2	OUT16_2	50
Output 17	OUT17	25
Output 18	OUT18	28
(Note: OUTxy_1 and OUTxy_2 have to be connected externally!)		
Slave Select	$\overline{SS}$	56
Serial Output	SO	53
Serial Input	SI	55
SPI Clock	SCK	54

Supply Voltage VDD	VDD	47
Supply Voltage U_{Batt}	Ubatt	23
GND1	GND1	26
GND2	GND2	27
GND3	GND3	58
GND4	GND4	59
GND5	GND5	11
GND6	GND6	12
GND7	GND7	42
GND8	GND8	41
Sense Ground VDD-Monitoring	$\overline{GND\_ABE}$	29
In-/Output VDD-Monitoring	$\overline{ABE}$	30
Reset (low active)	$\overline{RST}$	31
not connected	nc	21, 24, 32, 52, 64



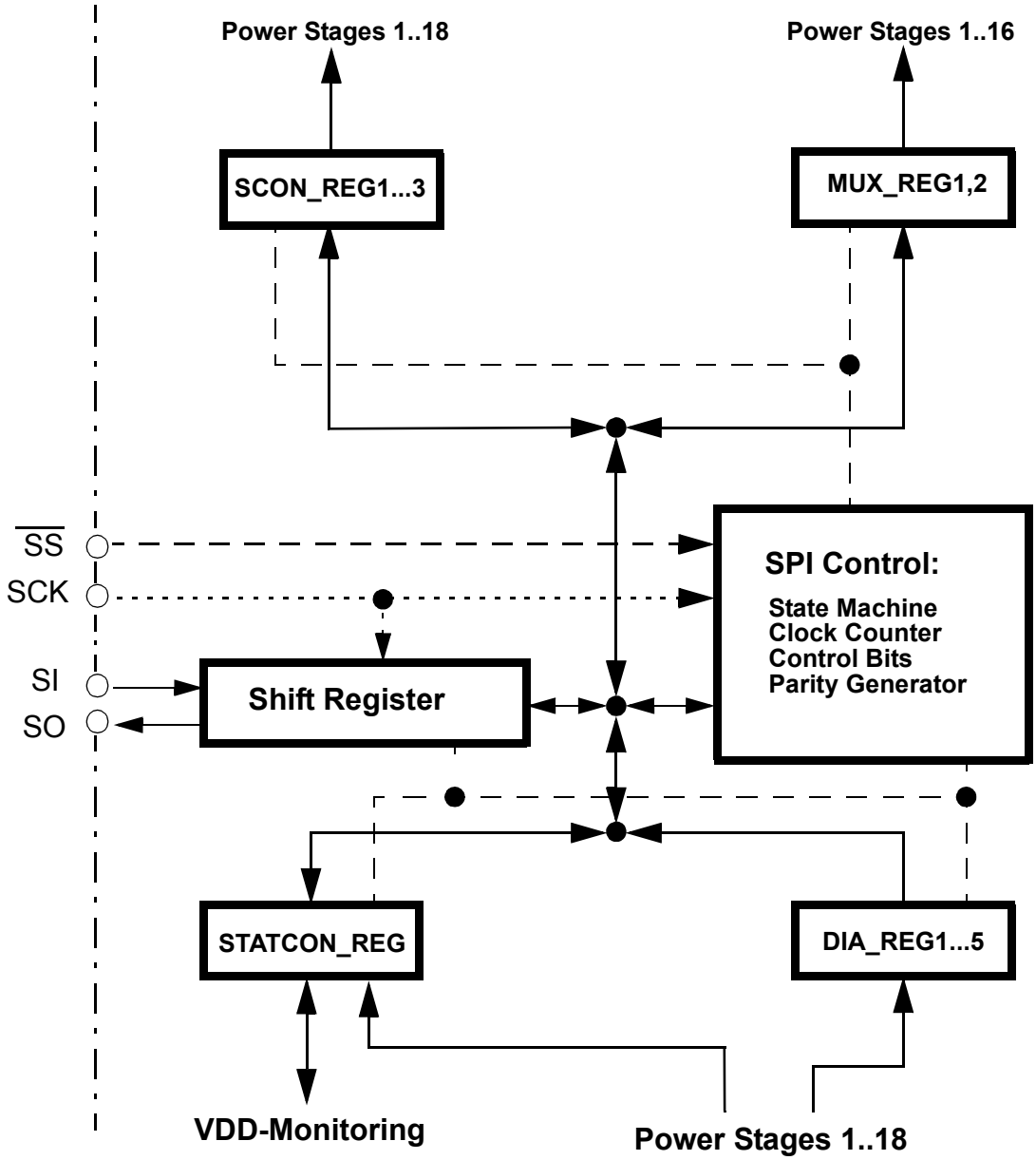
1.5 Function of Pins

IN1 to IN16	Control inputs of the power stages Internal pull-up current sources (exception: IN8 with pull-down current source)
FCL FDA SSY	Clock for the µsec-bus (pin shared with IN16) Data for the µsec-bus (pin shared with IN6) Strobe and Synchronisation for the µsec-bus (pin shared with IN7)
OUT1 to OUT18	Outputs of the power switches Short-circuit proof Low side switches Limitation of the output voltage by zener diodes
VDD	Supply voltage 5V
UBatt	Supply voltage U_{Batt} Pin must not be left open but has to be connected either to U_{Batt} or to V_{DD} (e.g. in commercial vehicles)
GND1 to GND8	Ground pins Ground pins for the power stages (see 2.4) Ground reference of all logic signals is GND1/2
$\overline{RST}$	Reset Active low Locks all power switches regardless of their input signals (except OUT8) Clears the fault registers Resets the µsec-bus interface registers
$\overline{ABE}$	In-/Output VDD-Monitoring Active low Output pin for the VDD-Monitoring Input pin for the shut-off signal coming from the supervisor
GND_$\overline{ABE}$	Sense ground VDD-Monitoring
SI, SO, SCK, $\overline{SS}$	SPI Interface

1.6 SPI Interface

The serial SPI interface establishes a communication link between TLE6244X and the systems microcontroller. TLE6244X always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 5 MBaud.
The TLE6244X is selected by the SPI master by an active slave select signal at $\overline{SS}$ and by the first two bits of the SPI instruction.SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI clock is provided by the master.
In case of inactive slave select signal (High) the data output SO goes into tristate.

Block Diagram:



A SPI communication always starts with a SPI instruction sent from the controller to TLE6244X. During a write cycle the controller sends the data after the SPI instruction, beginning with the MSB. During a reading cycle, after having received the SPI instruction, TLE6244X sends the corresponding data to the controller, also starting with the MSB.

SPI Command/Format:

MSB							
7	6	5	4	3	2	1	0
0	0	INSTR4	INSTR3	INSTR2	INSTR1	INSTR0	INSW

Bit	**Name**	**Description**
7,6	CPAD1,0	Chip Address (has to be ‘0’, ‘0’)
5-1	INSTR (4-0)	SPI instruction (encoding)
0	INSW	Parity of the instruction

Characteristics of the SPI Interface:

1) If the slave select signal at $\overline{SS}$ is High, the SPI-logic is set on default condition, i.e. it expects an instruction.

2) If the 5V-reset ($\overline{RST}$) is active, the SPI output SO is switched into tristate.
The VDD monitoring ($\overline{ABE}$) has no influence on the SPI interface.

3) Verification byte:
Simultaneously to the receipt of an SPI instruction TLE6244X transmits a verification byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial bit pattern and a flag indicating an invalid instruction of the previous access.

4) On a read access the databits at the SPI input SI are rejected. On a writing access or after the DEL_DIA instruction the TLE6244XTLE6244X sets the SPI output SO to low after sending the verification byte. If more than 16 bits are received the rest of the frame is rejected.

5) Invalid instruction/access:
An instruction is invalid, if one of the following conditions is fulfilled:
- an unused instruction code is detected (see tables with SPI instructions)
- in case the previous transmission is not completed in terms of internal data processing
- number of SPI clock pulses counted during active $\overline{SS}$ differs from exactly 16 clock pulses.
A write access and the instruction DEL_DIA is internally suppressed (i.e internal registers will not be affected) in all cases where at the rising (inactive) edge of $\overline{SS}$ the number of falling edges applied to the SPI input SCK during the access is not equal to 16. A write access is also internally suppressed (i.e internal registers will not be affected) if at the rising (inactive) edge of $\overline{SS}$ a 17th bit is submitted (SCK=‘1’).

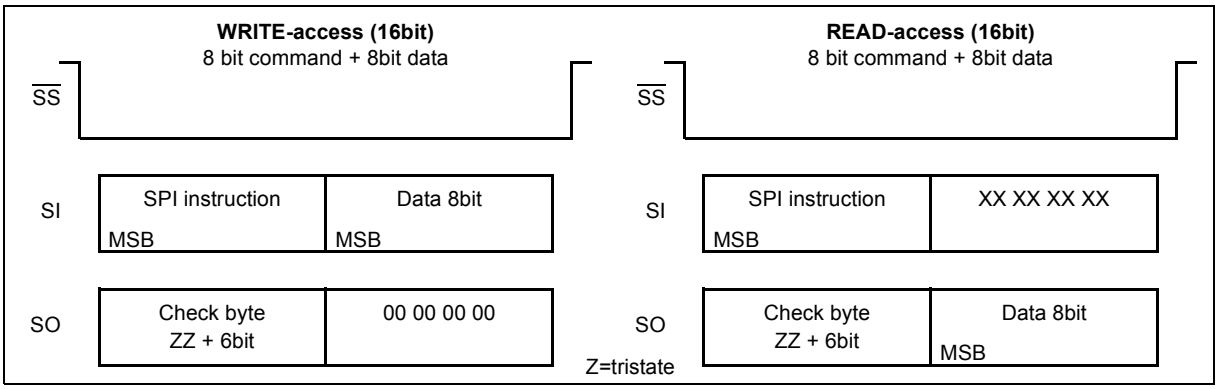
After the bits CPAD1,0 and INSTR (4-0) have been sent from the microcontroller TLE6244X is able to check if the instruction code is valid. If an invalid instruction is detected, any modification on a register of TLE6244X is not allowed and the data byte ‘FFh’ is transmitted after having sent the verification byte. If a valid read instruction is detected the content of the corresponding register is transmitted to the controller after having sent the verification byte (even if bit INSW afterwards is wrong). If a valid write instruction is

detected the data byte ’00h’ is transmitted to the controller after having sent the verification byte (even if bit INSW afterwards is wrong) but modifications on any register of TLE6244 are not allowed until bit INSW is valid, too.

If an invalid instruction is detected bit TRANS_F in the following verification byte is set to ’High’. This bit must not be cleared before it has been sent to the microcontroller.

6) If TLE6244X and additional IC’s are connected to one common slave select, they are distinguished by the chip address (CPAD1, CPAD0). If an IC with 32bit-transmission-format is selected, TLE6232 must not be activated, even if slave select is set to ’low’ and the first two bits of the third byte of the 32bit-transmission are identical to the chip address of TLE6244X.
During the transmission of CPAD1 and CPAD0 the data output SO remains in tristate (see timing diagram of the SPI in chapter 3.9.).

SPI access format:



Verification byte:

MSB							
7	6	5	4	3	2	1	0
Z	Z	1	0	1	0	1	TRANS_F

Bit	**Name**	**Description**
0	TRANS_F	Bit = 1: error detected during previous transfer Bit = 0: previous transfer was recognised as valid State after reset: 0
1		Fixed to High
2		Fixed to Low
3		Fixed to High
4		Fixed to Low
5		Fixed to High
6		send as high impedance
7		send as high impedance

SPI Instructions

SPI Instruction	Encoding			Description
	bit 7,6 CPAD1,0	bit 5,4,3,2,1 INSTR(4...0)	Parity	
RD_IDENT1	00	00000	0	read identifier 1
RD_IDENT2	00	00001	1	read identifier2
WR_STATCON	00	10001	0	write into STATCON_REG
WR_MUX1	00	10010	0	write into MUX_REG1
WR_MUX2	00	10011	1	write into MUX_REG2
WR_SCON1	00	10100	0	write into SCON_REG1
WR_SCON2	00	10101	1	write into SCON_REG2
WR_SCON3	00	10110	1	write into SCON_REG3
WR_CONFIG	00	10111	0	write into CONFIG
RD_MUX1	00	00010	1	read MUX_REG1
RD_MUX2	00	00011	0	read MUX_REG2
RD_SCON1	00	00100	1	read SCON_REG1
RD_SCON2	00	00101	0	read SCON_REG2
RD_SCON3	00	00110	0	read SCON_REG3
RD_STATCON	00	00111	1	read STATCON_REG
DEL_DIA	00	11000	0	resets the 5 diagnostic registers DIA_REG
RD_DIA1	00	01000	1	read DIA_REG1
RD_DIA2	00	01001	0	read DIA_REG2
RD_DIA3	00	01010	0	read DIA_REG3
RD_DIA4	00	01011	1	read DIA_REG4
RD_DIA5	00	01100	0	read DIA_REG5
RD_CONFIG	00	01101	1	read CONFIG
RD_INP1	00	01110	1	read INP_REG1
RD_INP2	00	01111	0	read INP_REG2
		all others		no function

1.6.1 Serial/Parallel Control

Serial/Parallel Control of the Power Stages 1...16 and Serial Control (SPI) of the Power Stages 17 and 18:
The registers MUX_REG1/2 and the bmux-bit prescribe parallel control or serial control (SPI or µsec-bus) of the power stages.

(SPI-Instructions: WR_MUX1...2, RD_MUX1...2, WR_SCON1...3, RD_SCON1...3)

The following table shows the truth table for the control of the power stages 1...18. The registers MUX_REG1, 2 prescribe parallel-control or serial control of the power stages. The registers SCON_REG1...3 prescribe the state of the power stage in case of SPI-serial control. BMUX determines parallel control or control by µsec-bus.
For the power stages 17 and 18 control is exclusively possible via SCON17/18. IN17/18 and MUX17/18 do **not** exist. BMUX has no function for OUT17/18.

$\overline{\text{ABE}}$	$\overline{\text{RST}}$	INx	BMUX	MUXx	SCONx	µsec-REGx	Output OUTx of Power Stage x, x = 1..18
0	0	X	X	X	X	X	OUTx off
0	1	X	X	X	X	X	OUTx off
1	0	X	X	X	X	X	OUTx off
1	1	X	X	0	0	X	SPI Control: OUTx on
1	1	X	X	0	1	X	SPI Control: OUTx off
1	1	0	1	1	X	X	Parallel Control: OUTx on
1	1	1	1	1	X	X	Parallel Control: OUTx off
1	1	X	0	1	X	0	µsec-bus Control: OUTx on
1	1	X	0	1	X	1	µsec-bus Control: OUTx off

Exception: OUT8 is on (active) if IN8 is set to logic ‘1’ (and off if IN8 is set to logic ‘0’) in case of parallel access.

Note: OUT8 cannot be controlled by the µsec-Bus. Refer to section 1.7.

Description of the SPI Registers

Register: MUX_REG1							
7	6	5	4	3	2	1	0
MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

State of Reset: 80H

Access by Controller: Read/Write

Bit	Name	Description
0	MUX0	Serial or parallel control of power stage 1
1	MUX1	Serial or parallel control of power stage 2
2	MUX2	Serial or parallel control of power stage 3
3	MUX3	Serial or parallel control of power stage 4
4	MUX4	Serial or parallel control of power stage 5
5	MUX5	Serial or parallel control of power stage 6
6	MUX6	Serial or parallel control of power stage 7
7	MUX7	Serial or parallel control of power stage 8

Register: MUX_REG2							
7	6	5	4	3	2	1	0
MUX15	MUX14	MUX13	MUX12	MUX11	MUX10	MUX9	MUX8

State of Reset: 00H

Access by Controller: Read/Write

Bit	Name	Description
0	MUX8	Serial or parallel control of power stage 9
1	MUX9	Serial or parallel control of power stage 10
2	MUX10	Serial or parallel control of power stage 11
3	MUX11	Serial or parallel control of power stage 12
4	MUX12	Serial or parallel control of power stage 13
5	MUX13	Serial or parallel control of power stage 14
6	MUX14	Serial or parallel control of power stage 15
7	MUX15	Serial or parallel control of power stage 16

Register: SCON_REG1							
7	6	5	4	3	2	1	0
SCON7	SCON6	SCON5	SCON4	SCON3	SCON2	SCON1	SCON0

State of Reset: FFH		
Access by Controller: Read/Write		
Bit	**Name**	**Description**
0	SCON0	State of serial control of power stage 1
1	SCON1	State of serial control of power stage 2
2	SCON2	State of serial control of power stage 3
3	SCON3	State of serial control of power stage 4
4	SCON4	State of serial control of power stage 5
5	SCON5	State of serial control of power stage 6
6	SCON6	State of serial control of power stage 7
7	SCON7	State of serial control of power stage 8

Register: SCON_REG2							
7	6	5	4	3	2	1	0
SCON15	SCON14	SCON13	SCON12	SCON11	SCON10	SCON9	SCON8

State of Reset: FFH		
Access by Controller: Read/Write		
Bit	**Name**	**Description**
0	SCON8	State of serial control of power stage 9
1	SCON9	State of serial control of power stage 10
2	SCON10	State of serial control of power stage 11
3	SCON11	State of serial control of power stage 12
4	SCON12	State of serial control of power stage 13
5	SCON13	State of serial control of power stage 14
6	SCON14	State of serial control of power stage 15
7	SCON15	State of serial control of power stage 16

Register: SCON_REG3							
7	6	5	4	3	2	1	0
1	1	1	1	1	1	SCON17	SCON16

State of Reset: FFH		
Access by Controller: Read/Write		
Bit	**Name**	**Description**
0	SCON16	State of serial control of power stage 17
1	SCON17	State of serial control of power stage 18
7-2		No function: HIGH on reading

1.6.2 Diagnostics/Encoding of Failures

Description of the SPI Registers

(SPI Instructions: RD_DIA1...5)

Register: DIA_REG1							
7	6	5	4	3	2	1	0
DIA7	DIA6	DIA5	DIA4	DIA3	DIA2	DIA1	DIA0

State of Reset: FFH		
Access by Controller: Read only		
Bit	**Name**	**Description**
1-0	DIA (1-0)	Diagnostic Bits of power stage 1
3-2	DIA (3-2)	Diagnostic Bits of power stage 2
5-4	DIA (5-4)	Diagnostic Bits of power stage 3
7-6	DIA (7-6)	Diagnostic Bits of power stage 4

Register: DIA_REG2							
7	6	5	4	3	2	1	0
DIA15	DIA14	DIA13	DIA12	DIA11	DIA10	DIA9	DIA8

State of Reset: FFH		
Access by Controller: Read only		
Bit	**Name**	**Description**
1-0	DIA (9-8)	Diagnostic Bits of power stage 5
3-2	DIA (11-10)	Diagnostic Bits of power stage 6
5-4	DIA (13-12)	Diagnostic Bits of power stage 7
7-6	DIA (15-14)	Diagnostic Bits of power stage 8

Register: DIA_REG3							
7	6	5	4	3	2	1	0
DIA23	DIA22	DIA21	DIA20	DIA19	DIA18	DIA17	DIA16

State of Reset: FFH

Access by Controller: Read only

Bit	Name	Description
1-0	DIA (17-16)	Diagnostic Bits of power stage 9
3-2	DIA (19-18)	Diagnostic Bits of power stage 10
5-4	DIA (21-20)	Diagnostic Bits of power stage 11
7-6	DIA (23-22)	Diagnostic Bits of power stage 12

Register: DIA_REG4							
7	6	5	4	3	2	1	0
DIA31	DIA30	DIA29	DIA28	DIA27	DIA26	DIA25	DIA24

State of Reset: FFH

Access by Controller: Read only

Bit	Name	Description
1-0	DIA (25-24)	Diagnostic Bits of power stage 13
3-2	DIA (27-26)	Diagnostic Bits of power stage 14
5-4	DIA (29-28)	Diagnostic Bits of power stage 15
7-6	DIA (31-30)	Diagnostic Bits of power stage 16

Register: DIA_REG5							
7	6	5	4	3	2	1	0
1	1	1	UBatt	DIA35	DIA34	DIA33	DIA32

State of Reset: FFH		
Access by Controller: Read only		
Bit	**Name**	**Description**
1-0	DIA (33-32)	Diagnostic Bits of power stage 17
3-2	DIA (35-34)	Diagnostic Bits of power stage 18
4	UBatt	0: Voltage Level at Pin UBatt is below 2V (typically) 1: Voltage Level at Pin UBatt is above 2V (typically) Diagnosis of UBatt is only possible if U_{VDD} > 4.5V Status of UBatt is not latched.
7-5		No function: High on reading

Encoding of the Diagnostic Bits of the Power Stages		
DIA(2*x-1)	DIA(2*x-2)	State of power stage x x = 1..18
1	1	Power stage o.k.
1	0	Short-circuit to U_{Batt} (SCB) / OT
0	1	Open load (OL)
0	0	Short-circuit to ground (SCG)

1.6.3 Configuration

The µsec-bus is enabled by this register. In addition the shut off at SCB can be configured for the power-stages OUT9, OUT10 and OUT15... OUT18.

CONFIG (Read and write)							
7	6	5	4	3	2	1	0
O16-SCB	O15-SCB	O10-SCB	O9-SCB	O18-SCB	O17-SCB	BMUX	1

State of Reset: FFh		
Bit	**Name**	**Description**
0		No function: HIGH on reading
1	BMUX	1: parallel inputs INx enabled 0: µsec-Bus Interface enabled
2	O17-SCB	1: The output OUT17 is switched off in case of SCB 0: The output is not switched off in case of SCB
3	O18-SCB	1: The output OUT18 is switched off in case of SCB 0: The output is not switched off in case of SCB
4	O9-SCB	1: The output OUT9 is switched off in case of SCB 0: The output is not switched off in case of SCB
5	O10-SCB	1: The output OUT10 is switched off in case of SCB 0: The output is not switched off in case of SCB
6	O15-SCB	1: The output OUT15 is switched off in case of SCB 0: The output is not switched off in case of SCB
7	O16-SCB	1: The output OUT16 s switched off in case of SCB 0: The output is not switched off in case of SCB

Description of the µsec-bus see chapter 1.7

1.6.4 Other

Reading the IC Identifier (SPI Instruction: RD_IDENT1):

IC Identifier1 (Device ID)							
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7...0	ID(7...0)	ID-No.: 10101000

Reading the IC revision number (SPI Instruction: RD_IDENT2):

IC revision number							
7	6	5	4	3	2	1	0
SWR3	SWR2	SWR1	SWR0	MSR3	MSR2	MSR1	MSR0

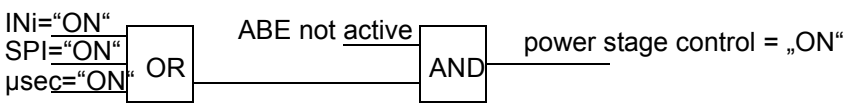
Bit	Name	Description
7...4	SWR(3...0)	Revision corresponding to Software release: 0_{Hex}
3...0	MSR(3...0)	Revision corresponding to Maskset: 0_{Hex}

Reset of the Diagnostic Information (SPI Instruction: DEL_DIA):

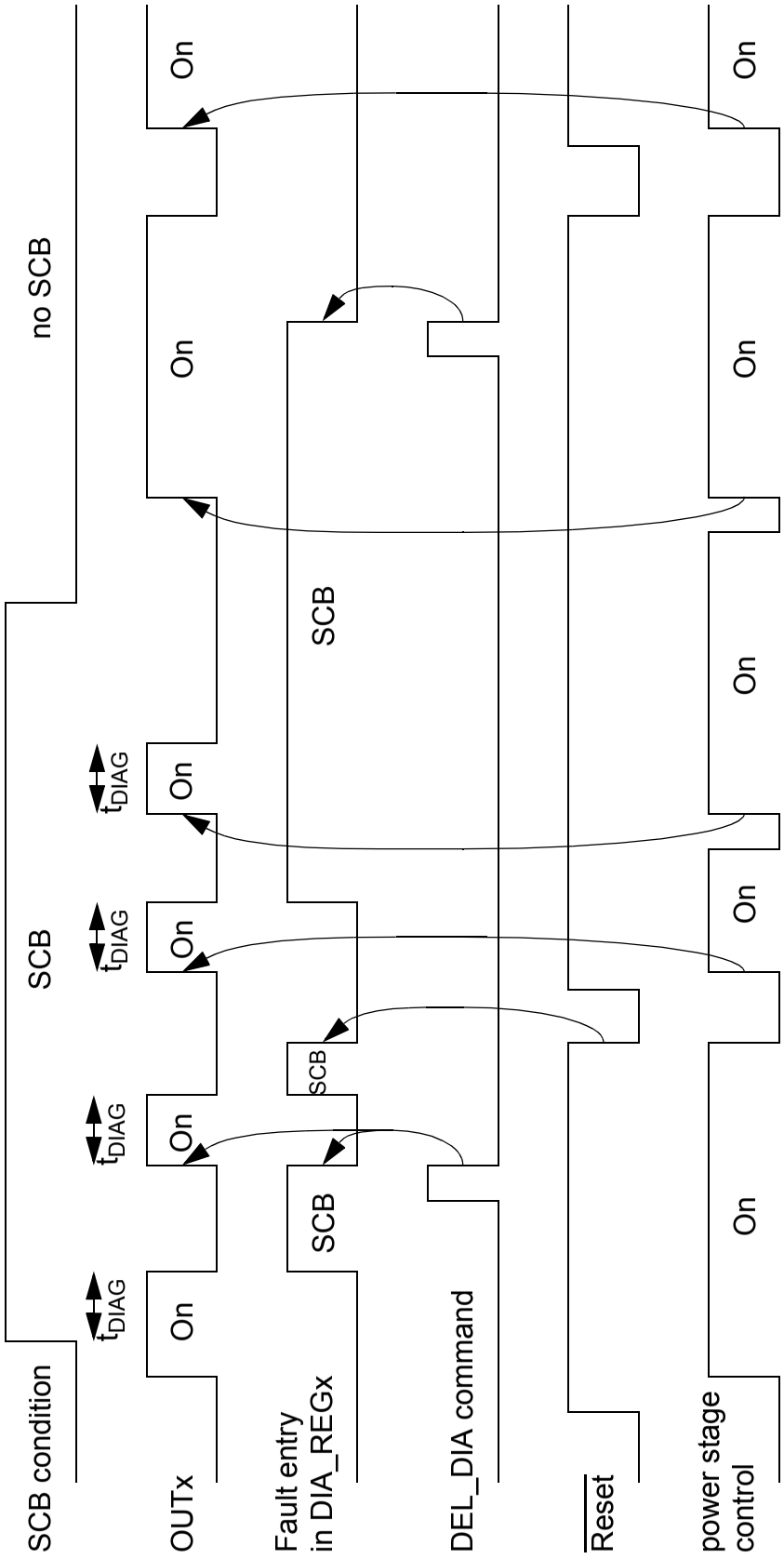
Resets the 5 diagnostic registers DIA_REG1...5 to FFH and the common overtemperature flag in register STATCON_REG (Bit4) to High. These bits are only cleared by the DEL_DIA instruction when there is no failure entry at the input of the registers.
Access is performed like a writing access with any data byte.

In the case a power stage is shut off because of SCB, the output is activated again by the DEL_DIA instruction and the filtering-time is enabled. Therefore in case of SCB the output is activated and shut off after the shutoff delay.
For a power stage in the current limitation mode, the current limitation mode is left, if a DEL_DIA instruction has been received. If there is still the condition for SCB the current limitation mode is entered again.

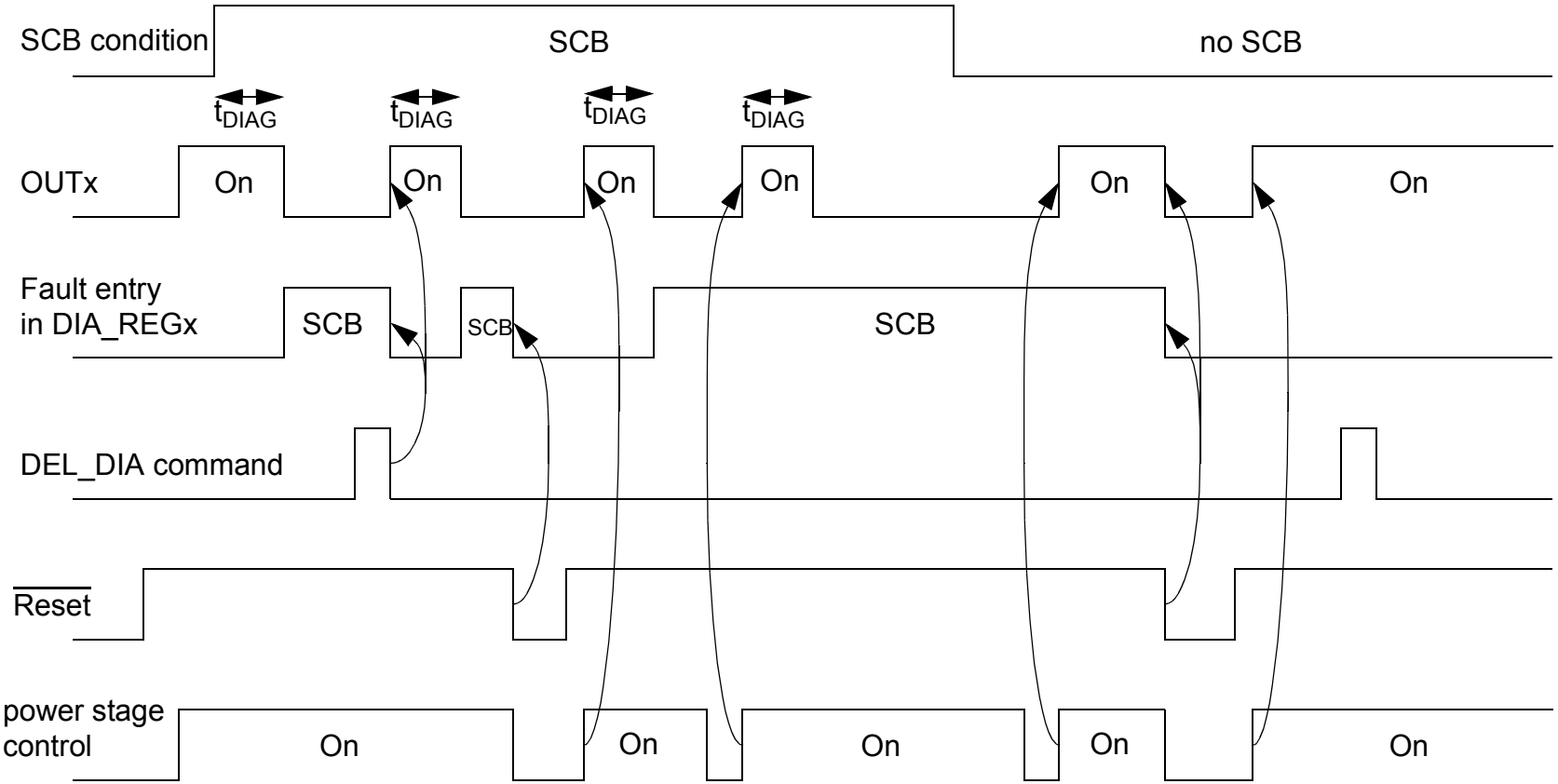
On the following pages the conditions for set and reset of the SCB report in DIA_REGx is shown in several schematics. The signal „power stage control“ is generated as follows:



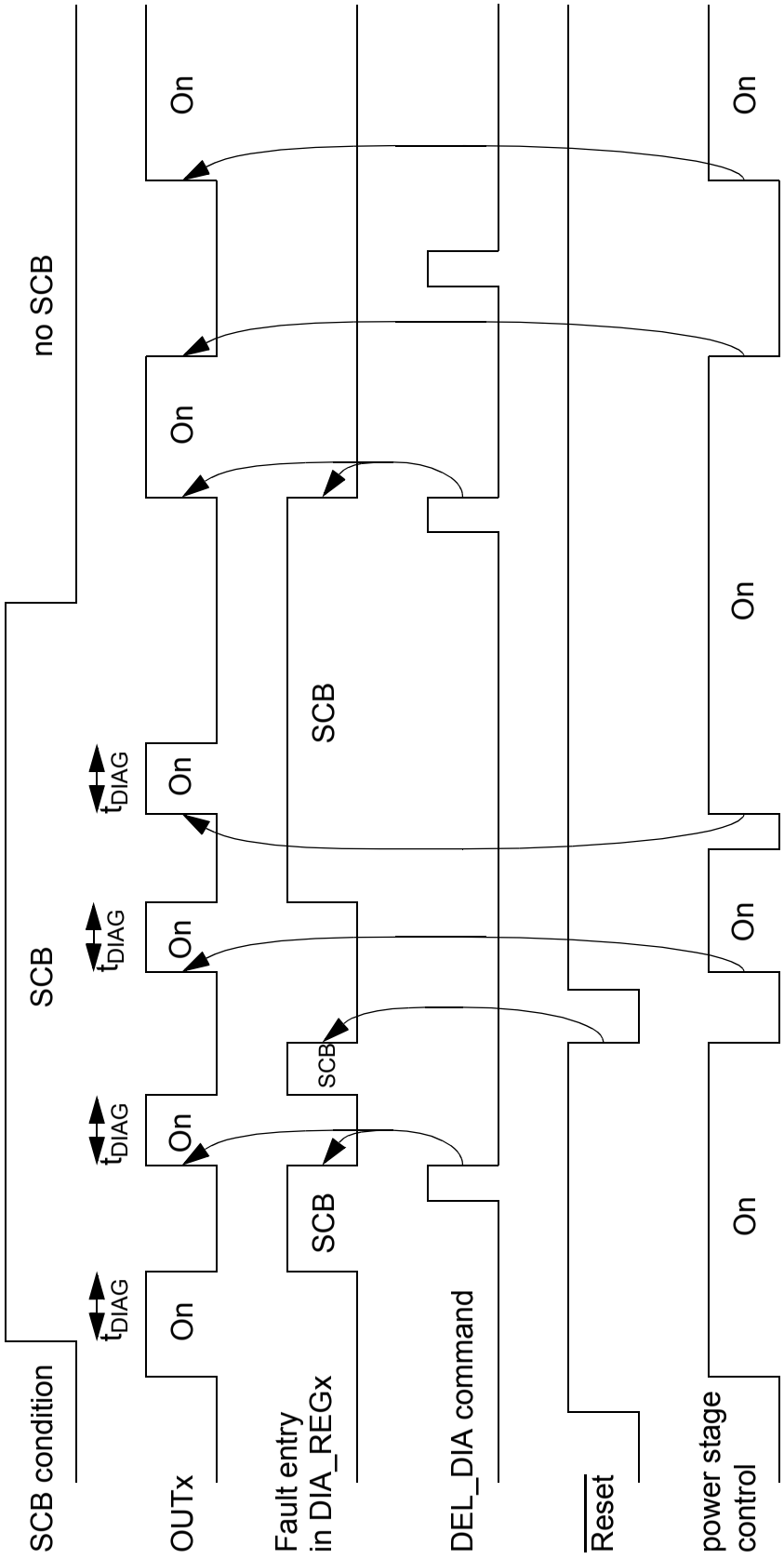
Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by DEL_DIA after SCB condition disappeared and power stage control was toggled



Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by Reset after SCB condition disappeared and power stage control was toggled



Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by DEL_DIA after SCB condition disappeared but power stage control was not toggled



Schematic of SCB report of power stages OUT1...7,9...18 (power stage programmed for shut-off in case of SCB), SCB entry deleted by Reset after SCB condition disappeared but power stage control was <u>not</u> toggled