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TLE6368-G2

Multi-Voltage Processor Power Supply

Data Sheet

Rev. 2.32, Oct. 2010

Automotive Power

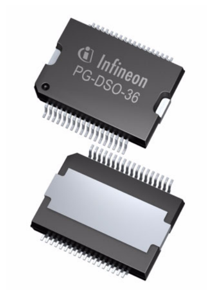
Multi-Voltage Processor Power Supply

TLE6368-G2

1 Overview

1.1 Features

- High efficiency regulator system
- Wide input voltage range from 5.5V to 60V
- Stand-by mode with low current consumption
- Suitable for standard 12V/24V and 42V PowerNets
- Step down converter as pre-regulator:
  5.5V / 1.5A
- Step down slope control for lowest EME
- Switching loss min2010-10imization
- Three high current linear post-regulators with selectable output voltages:
  5V / 800mA
  3.3V or 2.6V / 500mA
  3.3V or 2.6V / 350mA
- Six independent voltage trackers (followers):
  5V / 17mA each
- Stand-by regulator with 1mA current capability
- Three independent undervoltage detection circuits (e.g. reset, early warning) for each linear post-regulator
- Power on reset functionality
- Tracker control and diagnosis by SPI
- All outputs protected against short-circuit
- Power PG-DSO-36-26 package
- Green (RoHS compliant) version of TLE6368-G2
- AEC qualified



PG-DSO-36-26

Type	Package
TLE6368-G2 / SONIC	PG-DSO-36-26 (RoHS compliant)

SMD = Surface Mounted Device

1.2 Short functional description

The **TLE6368-G2** is a multi voltage power supply system especially designed for automotive applications using a standard 12V / 24V battery as well as the new 42V powernet. The device is intended to supply 32 bit micro-controller systems which require different supply voltage rails such as 5V, 3.3V and 2.6V. The regulators for external sensors are also provided.

The **TLE6368-G2** cascades a Buck converter block with a linear regulator and tracker block on a single chip to achieve lowest power dissipation thus being able to power the application even at very high ambient temperatures.

The step-down converter delivers a pre-regulated voltage of 5.5V with a minimum current capability of 1.5A.

Supplied by this step down converter three low drop linear post-regulators offer 5V, 3.3V, or 2.6V of output voltages depending on the configuration of the device with current capabilities of 800mA, 500mA and 350mA.

In addition the inputs of six voltage trackers are connected to the 5.5V bus voltage. Their outputs follow the main 5V linear regulator (Q_LDO1) with high accuracy and are able to drive a current of 17mA each. The trackers can be turned on and off individually by a 16 bit serial peripheral interface (SPI). Through this interface also the status information of each tracker (i.e. short circuit) can be read out.

To monitor the output voltage levels of each of the linear regulators three independent undervoltage detection circuits are available which can be used to implement the reset or an early warning function. The supervision of the µC can be managed by the SPI-triggered window watchdog.

For energy saving reasons while the motor is turned off, the **TLE6368-G2** offers a stand-by mode, where the quiescent current does not exceed 30µA. In this stand-by mode just the stand-by regulator remains active.

The **TLE6368-G2** is based on Infineon Power technology SPT ™ which allows bipolar, CMOS and Power DMOS circuitry to be integrated on the same monolithic circuitry.

1.3 Pin configuration

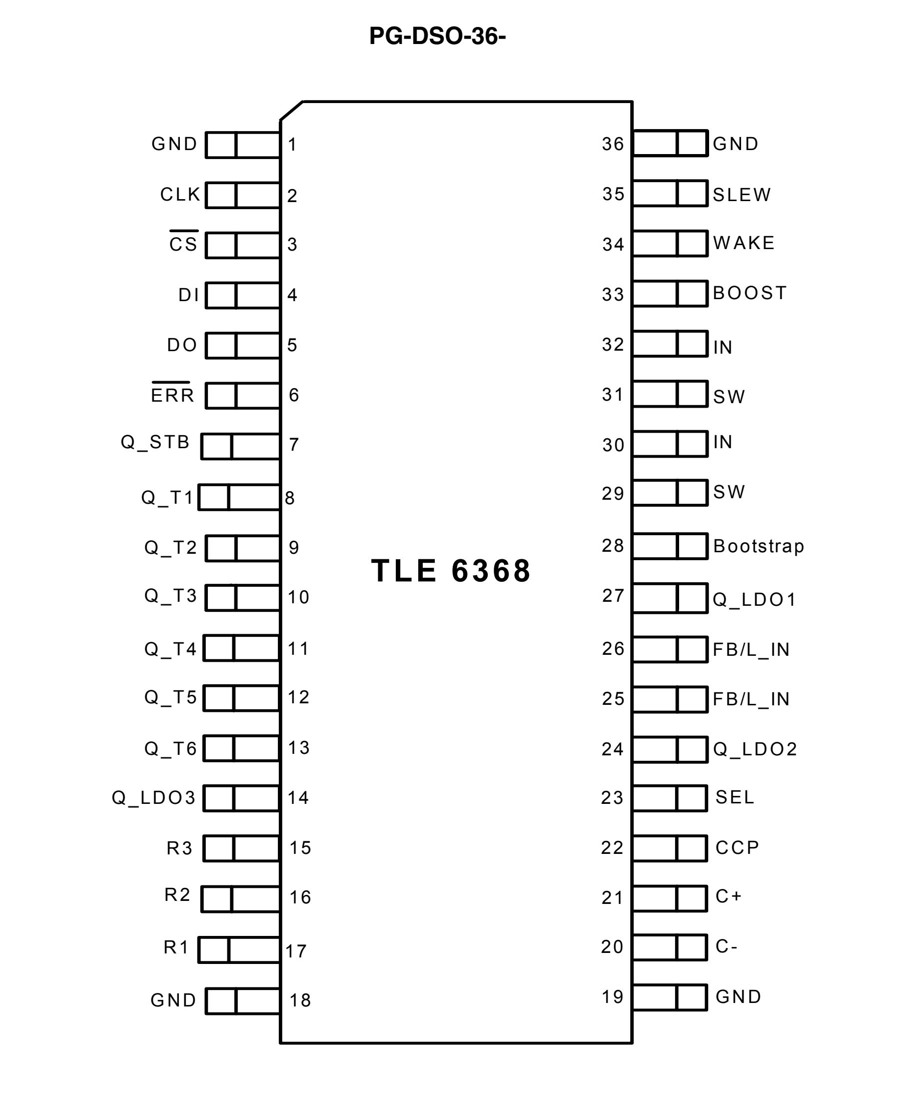


Figure 1 Pin Configuration (Top View),
bottom heat slug and GND corner pins are connected

1.4 Pin definitions and functions

Pin No.	Symbol	Function
1,18,19, 36	GND	**Ground**; to reduce thermal resistance place cooling areas on PCB close to these pins. The GND pins are connected internally to the heat slug at the bottom.
2	CLK	**SPI Interface Clock input**; clocks the shift register; CLK has an internal active pull down and requires CMOS logic level inputs; see also chapter SPI
3	$\overline{\text{CS}}$	**SPI Interface chip select input**; $\overline{\text{CS}}$ is an active low input; serial communication is enabled by pulling the $\overline{\text{CS}}$ terminal low; $\overline{\text{CS}}$ input should only be switched when CLK is low; $\overline{\text{CS}}$ has an internal active pull up and requires CMOS logic level inputs; see also chapter SPI.
4	DI	**SPI Interface Data input;** receives serial data from the control device; serial data transmitted to DI is a 16 bit control word with the Least Significant Bit (LSB) being transferred first; the input has an active pull down and requires CMOS logic level inputs; DI will accept data on the falling edge of CLK-signal; see also chapter SPI
5	DO	**SPI Interface Data output;** this tristate output transfers diagnosis data to the controlling device; the output will remain 3-stated unless the device is selected by a low on Chip-Select $\overline{\text{CS}}$; see also the chapter SPI
6	$\overline{\text{ERR}}$	**Error output**; push-pull output. Monitors failures in parallel to the SPI diagnosis word, reset via SPI. $\overline{\text{ERR}}$ is an active low, latched output.
7	Q_STB	**Standby Regulator Output**; the output is active even when the buck regulator and all other circuitry is in off mode
8	Q_T1	Voltage **Tracker Output T1** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.
9	Q_T2	Voltage **Tracker Output T2** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.
10	Q_T3	Voltage **Tracker Output T3** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.

1.4 Pin definitions and functions (cont'd)

Pin No.	Symbol	Function
11	Q_T4	Voltage **Tracker Output T4** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.
12	Q_T5	Voltage **Tracker Output T5** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.
13	Q_T6	Voltage **Tracker Output T6** tracked to Q_LDO1; bypass with a 1µF ceramic capacitor for stability. It is switched on and off by SPI command. Keep open, if not needed.
14	Q_LDO3	Voltage Regulator **Output 3; 3.3V or 2.6V output;** output voltage is selected by pin SEL (see also 2.2.2); For stability a ceramic capacitor of 470nF to GND is sufficient.
15	R3	**Reset output 3**, undervoltage detection for output Q_LDO3; open drain output; an external pull-up resistor of 10kΩ is required
16	R2	**Reset output 2**, undervoltage detection for output Q_LDO2; open drain output; an external pull-up resistor of 10kΩ is required
17	R1	**Reset output 1**, undervoltage detection for output Q_LDO1 and watchdog failure reset; open drain output; an external pull-up resistor of 10kΩ is required
20	C-	**Charge pump capacitor connection**; Add the fly-capacitor of 100nF between C+ and C-
21	C+	**Charge pump capacitor connection**; Add the fly-capacitor of 100nF between C+ and C-
22	CCP	**Charge Pump Storage Capacitor Output**; Add the storage capacitor of 220nF between pin CCP and GND.
23	SEL	**Select Pin** for output voltage adjust of Q_LDO2 and Q_LDO3 (see also 2.2.2)
24	Q_LDO2	Voltage Regulator **Output 2; 3.3V or 2.6V output;** output voltage is selected by pin SEL (see also 2.2.2); For stability a ceramic capacitor of 470nF to GND is sufficient.
25, 26	FB/L_IN	**Feedback and Linear Regulator Input**; input connection for the Buck converter output

1.4 Pin definitions and functions (cont'd)

Pin No.	Symbol	Function
27	Q_LDO1	Voltage Regulator **Output 1; 5V output;** acts as the reference for the voltage trackers.The SPI and window watchdog logic is supplied from this voltage. For stability a ceramic capacitor of 470nF to GND is sufficient.
28	Bootstrap	**Bootstrap Input**; add the bootstrap capacitor between pin SW and pin Bootstrap, the capacitance value should be 2% of the Buck converter output capacitance
29, 31	SW	**Switch Output;** connect both pins externally through short lines directly to the cathode of the catch diode and the Buck circuit inductance.
30, 32	IN	**Supply Voltage Input;** connect both pins externally through short lines to the input filter/the input capacitors.
33	BOOST	**Boost Input**; for switching loss minimization connect a diode (cathode directly to boost pin) in series with a 100nF ceramic capacitor to the IN pin and from the anode of the diode to the buck converter output a 22Ω resistor. Recommended for 42V applications. In 12/24V applications connect boost directly to IN.
34	WAKE	**Wake Up Input**; a positive voltage applied to this pin turns on the device
35	SLEW	**Slew control Input**; a resistor to GND defines the current slope in the buck switch for reduced EME

1.5 Basic block diagram

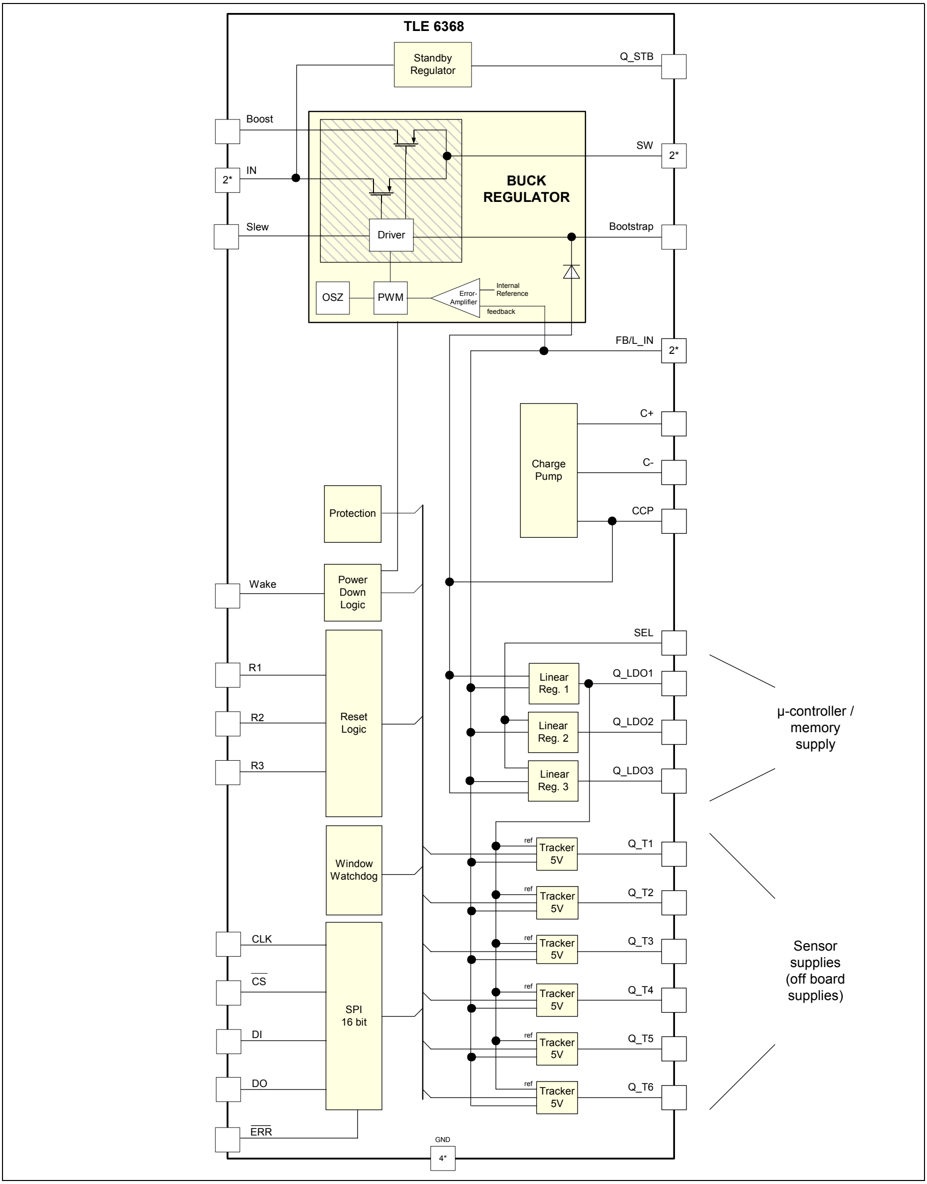


Figure 2 Block Diagram

2 Detailed circuit description

In the following major buck regulator blocks, the linear voltage regulators and trackers, the undervoltage reset function, the watchdog and the SPI are described in more detail.

For applications information e.g. choice of external components, please refer to section 5.

2.1 Buck Regulator

The diagram below shows the internal implemented circuit of the Buck converter, i. e. the internal DMOS devices, the regulation loop and the other major blocks.

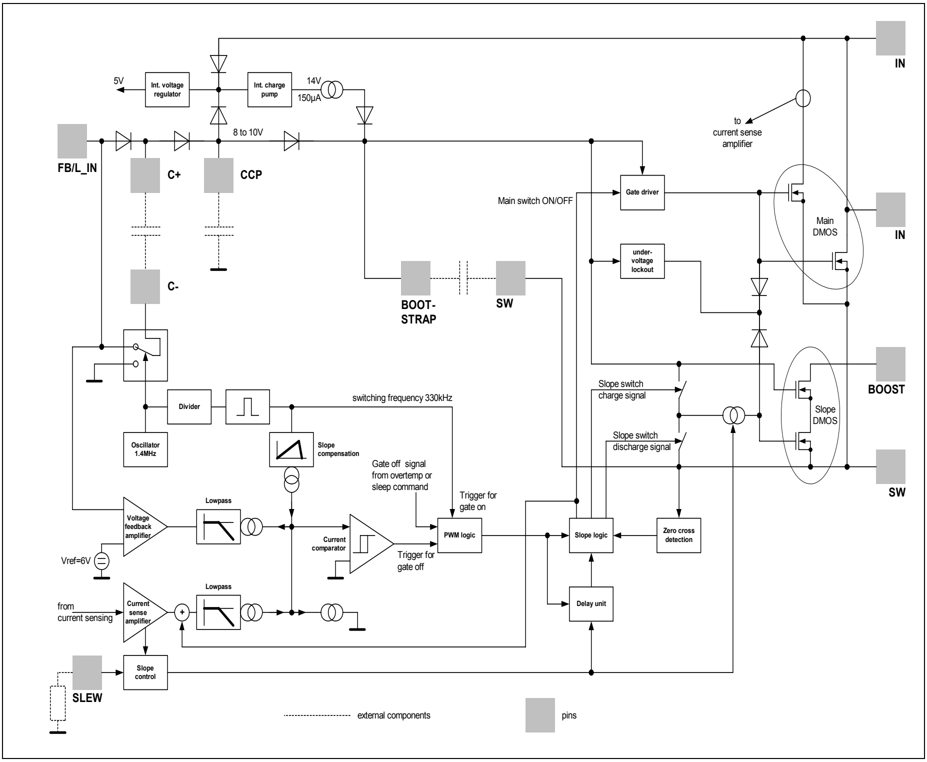


Figure 3 Detailed Buck regulator diagram

The 1.5A Buck regulator consists of two internal DMOS power stages including a current mode regulation scheme to avoid external compensation components plus additional blocks for low EME and reduced switching loss. Figure 3 indicates also the principle how the gate driver supply is managed by the combination of internal charge pump, external charge pump and bootstrap capacitor.

2.1.1 Current mode control scheme

The regulation loop is located at the left lower corner in the schematic, there you find the voltage feedback amplifier which gives the actual information of the actual output voltage level and the current sense amplifier for the load current information to form finally the regulation signal. To avoid subharmonic oscillations at duty cycles higher than 50% the slope compensation block is necessary.
The control signal formed out of those three blocks is finally the input of the PWM regulator for the DMOS gate turn off command, which means this signal determines the duty cycle. The gate turn on signal is set by the oscillator periodically every 3µs which leads to a Buck converter switching frequency around 330kHz.

With decreasing input voltage the device changes to the so called pulse skipping mode which means basically that some of the oscillator gate turn off signals are ignored. When the input voltage is still reduced the DMOS is turned on statically (100% duty cycle) and its gate is supplied by the internal charge pump. Below typical 4.5V at the feedback pin the device is turned off.During normal switching operation the gate driver is supplied by the bootstrap capacitor.

2.1.2 Start-up procedure

To guarantee a device startup even under full load condition at the linear regulator outputs a special start up procedure is implemented. At first the bootstrap capacitor is charged by the internal charge pump. Afterwards the output capacitor is charged where the driver supply in that case is maintained only by the bootstrap capacitor. Once the output capacitor of the buck converter is charged the external charge pump is activated being able to supply the linear regulators and finally the linear regulators are released to supply the loads.

2.1.3 Reduction of electromagnetic emission

In figure 3 it is recognized that two internal DMOS switches are used, a main switch and an auxiliary switch. The second implemented switch is used to adjust the current slope of the switching current. The slope adjustment is done by a controlled charge and discharge of the gate of this DMOS. By choosing the external resistor on the SLEW pin appropriate the current transition time can be adjusted between 20ns and 100ns.

2.1.4 Reducing the switching losses

The second purpose of the slope DMOS is to minimise the switching losses. Once being in freewheeling mode of the buck regulator the output voltage level is sufficient to force the load current to flow, the input voltage level is not needed in the first moment. By a feedback network consisting of a resistor and a diode to the boost pin (connection see section 5) the output voltage level is present at the drain of the switch. As soon as the voltage at the SW pin passes zero volts the handover to the main switch occurs and the traditional switching behaviour of the Buck switch can be observed.

2.2 Linear Voltage Regulators

The Linear regulators offer, depending on the version, voltage rails of 5V, 3.3V and 2.6V which can be determined by a hardware connection (see table at 2.2.2) for proper power up procedure. Being supplied by the output of the Buck pre-regulator the power loss within the three linear regulators is minimized.

All voltage regulators are short circuit protected which means that each regulator provides a maximum current according to its current limit when shorted. Together with the external charge pump the NPN pass elements of the regulators allow low dropout voltage operation. By using this structure the linear regulators work stable even with a minimum of 470nF ceramic capacitors at their output.

Q_LDO1 has 5V nominal output voltage, Q_LDO2 has a hardware programmable output voltage of 3.3V or 2.6V and Q_LDO3 is also programmable to 3.3V or 2.6V (see section 2.2.2). All three regulators are on all the time, if one regulator is not needed a base load resistor in parallel to the output capacitance for controlled power down is recommended.

2.2.1 Startup Sequence Linear Regulators

When acting as a 32 bit µC supply the so-called power sequencing (the dependency of the different voltage rails to each other) is important. Within the TLE6368-G2, the following Startup-Sequence is defined (see also figure 4):

$V_{Q\_LDO2} \leq V_{Q\_LDO1;}\ V_{Q\_LDO3} \leq V_{Q\_LDO1}$

with V_{Q_LDO1}=5V, V_{Q_LDO2} = 2.6V or 3.3V and V_{Q_LDO3} = 2.6V or 3.3V

The power sequencing refers to the regulator itself, externally voltages applied at Q_LDO2 and Q_LDO3 are not pulled down actively by the device if Q_LDO1 is lower than those outputs.

That means for the power down sequencing if different output capacitors and different loads at the three outputs of the linear regulators are used the voltages at Q_LDO2 and Q_LDO3 might be higher than at Q_LDO1 due to slower discharging. To avoid this behaviour three Schottky diodes have to be connected between the three outputs of the linear regulators in that way that the cathodes of the diodes are always connected to the higher nominal rail.

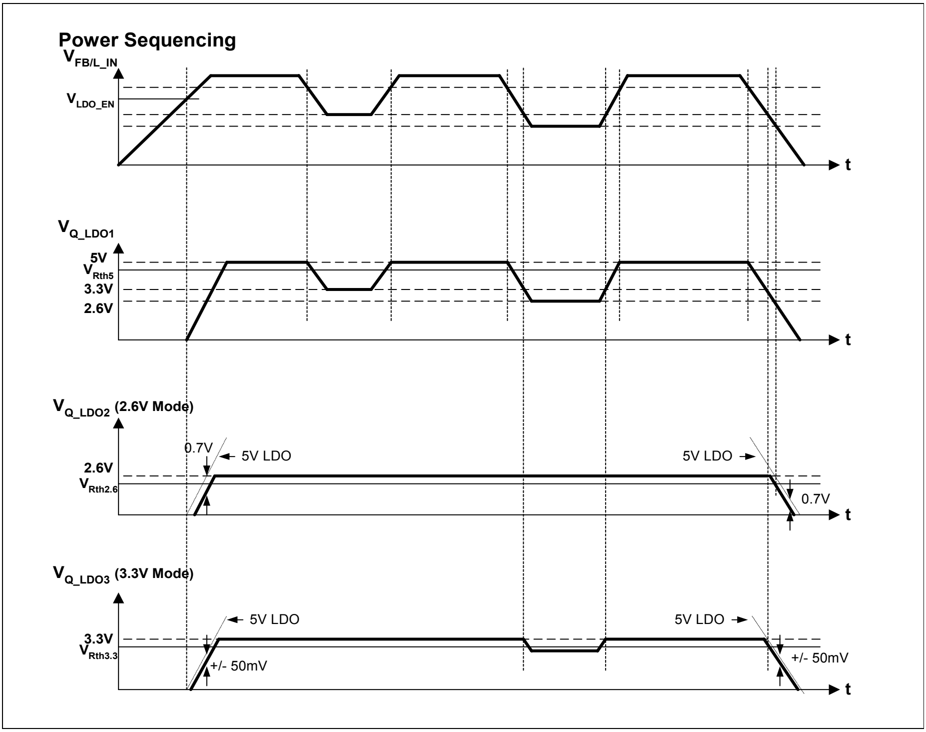


Figure 4 Power-up and -down sequencing of the regulators

2.2.2 Q_LDO2 and Q_LDO3 output voltage selection*

To determine the output voltage levels of the three linear regulators, the selection pin (SEL, pin 23) has to be connected according to the matrix given in the table below.

Definition of Output voltage Q_LDO2 and Q_LDO3

Select Pin SEL connected to	Q_LDO2 output voltage	Q_LDO3 output voltage
GND	3.3 V	3.3 V
Q_LDO1	2.6 V	2.6 V
Q_LDO2	2.6 V	3.3 V

* for different output voltages please refer to the multi voltage supply TLE6361

2.3 Voltage Trackers

For off board supplies i.e. sensors six voltage trackers Q_T1 to Q_T6 with 17mA output current capability each are available. The output voltages match Q_LDO1 within +5 / -15mV. They can be individually turned on and off by the appropriate SPI command word sent by the microcontroller. A ceramic capacitor with the value of 1µF at the output of each tracker is sufficient for stable operation without oscillation.

The tracker outputs can be connected in parallel to obtain a higher output current capability, no matter if only two or up to all six trackers are tied together. For uniformly distributed current density in each tracker internal balance resistors at each output are foreseen internally. By connecting two sets of three trackers in parallel two sensors with more than 50mA each can be supplied, all six in parallel give more than 100mA.

The tracker outputs can withstand short circuits to GND or battery in a range from -4 to +40V. A short circuit to GND is detected and indicated individually for each tracker in the SPI status word. Also an open load condition might be recognized and indicated as a failure condition in the SPI status word. A minimum load current of 2mA is required to avoid open load failure indication. In case of connecting several trackers to a common branch balancing currents can prevent proper operation of the failure indication.

2.4 Standby Regulator

The standby regulator is an ultra low power 2.5V linear voltage regulator with 1mA output current which is on all the time. It is intended to supply the microcontroller in stop mode and requires then only a minimum of quiescent current (<30µA) to extend the battery lifetime.

2.5 Charge Pump

The 1.6 MHz charge pump with the two external capacitors will serve to supply the base of the NPN linear regulators Q_LDO1 and Q_LDO3 as well as the gate of the Buck DMOS transistor in 100% duty cycle operation at low battery condition. The charge pump voltage in the range of 8 to 10V can be measured at pin 22 (CCP) but is not intended to be used as a supply for additional circuitry.

2.6 Power On Reset

A power on reset is available for each linear voltage regulator output. The reset output lines R1, R2 and R3 are active (low) during start up and turn inactive with a reset delay time after Q_LDO1, Q_LDO2 and Q_LDO3 have reached their reset threshold. The reset outputs are open drain, three pull up resistors of 10kΩ each have to be connected to the I/O rail (e.g. Q_LDO1) of the µC. All three reset outputs can be linked in parallel to obtain a wired-OR.

The reset delay time is 8 ms by default and can be set to higher values as 16 ms, 32 ms or 64 ms by SPI command. At each power up of the device in case the output voltage at

Q_LDO1 had decreased below 3.3V (max.), the SPI will reset to the default settings including the 8ms delay time. If the voltage on Q_LDO1 during sleep or power off mode was kept above 3.3V the delay time set by the last SPI command is valid.

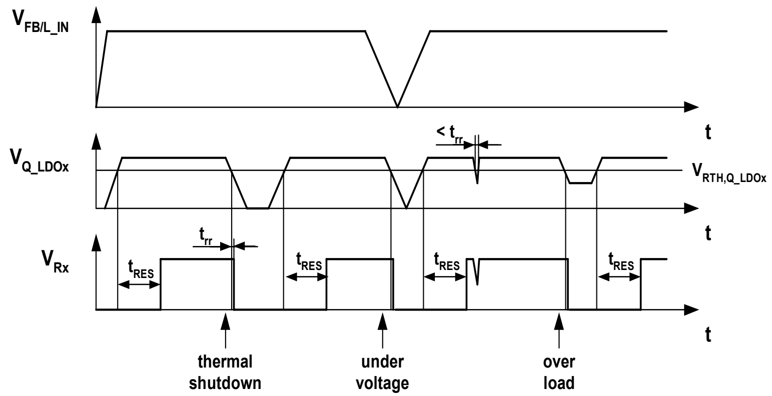


Figure 5 Undervoltage reset timing

2.7 RAM good flag

A RAM good flag will be set within the SPI status word when the Q_LDO1 voltage drops below 2.3V. A second one will be set if Q_LDO2 drops below typical 1.4V. Both RAM good flags can be read after power up to determine if a cold or warm start needs to be processed. Both RAM good flags will be reset after each SPI cycle.

2.8 $\overline{\text{ERR}}$ Pin

A hardware error pin indicates any fault conditions on the chip. It should be connected to an interrupt input of the microcontroller. A low signal indicates an error condition. The microcontroller can read the root cause of the error by reading the SPI register.

2.9 Window Watchdog

The on board window watchdog for supervision of the µC works in combination with the SPI. The window watchdog logic is turned off per default and can be activated by one special bit combination in the SPI command word. When operating, the window watchdog is triggered when $\overline{\text{CS}}$ is low and Bit WD-Trig in the SPI command word is set to “1”. The watchdog trigger is recognized with the low to high transition of the $\overline{\text{CS}}$ signal. To allow reading the SPI at any time without getting a reset due to misinterpretation the WD-Trig bit has to be set to “0” to avoid false trigger conditions.

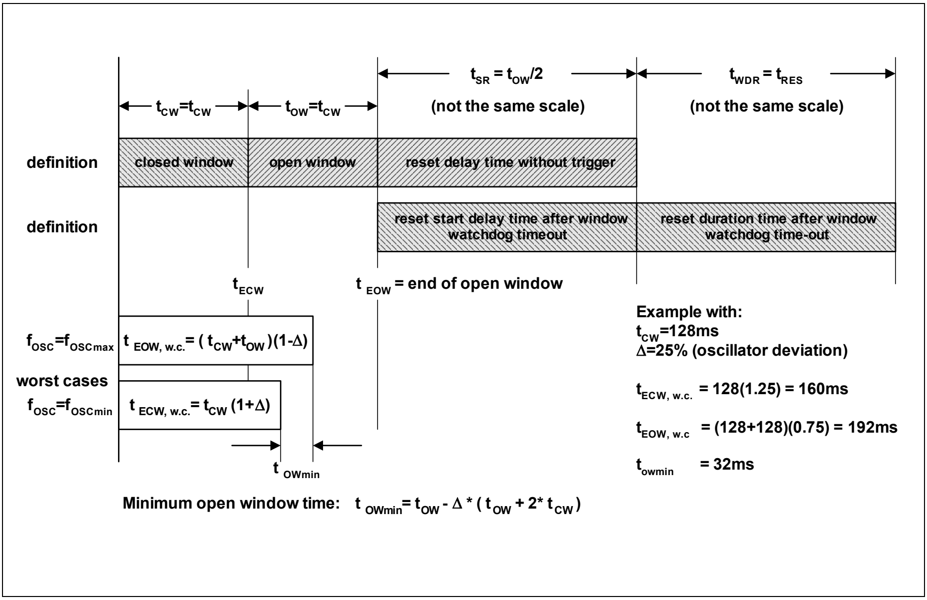


Figure 6 Window watchdog timing definition

Figure 6 shows some guidelines for designing the watchdog trigger timing taking the oscillator deviation of different devices into account. Of importance (w.c.) is the maximum of the closed window and the minimum of the open window in which the trigger has to occur.

The length of the OW and CW can be modified by SPI command. If a change of the window length is desired during the Watchdog function is operating please send the SPI command with the new timing with a "Watchdog trigger Bit" D15=1. In this case the next CW will directly start with the new length.

A minimum time gap of > 1/48 of the actual OW/CW time between a "Watchdog disable" and 'Watchdog enable' SPI-command should be maintained. This allows the internal Watchdog counters to be resetted. Thus after the enable command the Watchdog will start properly with a full CW of the adjusted length.

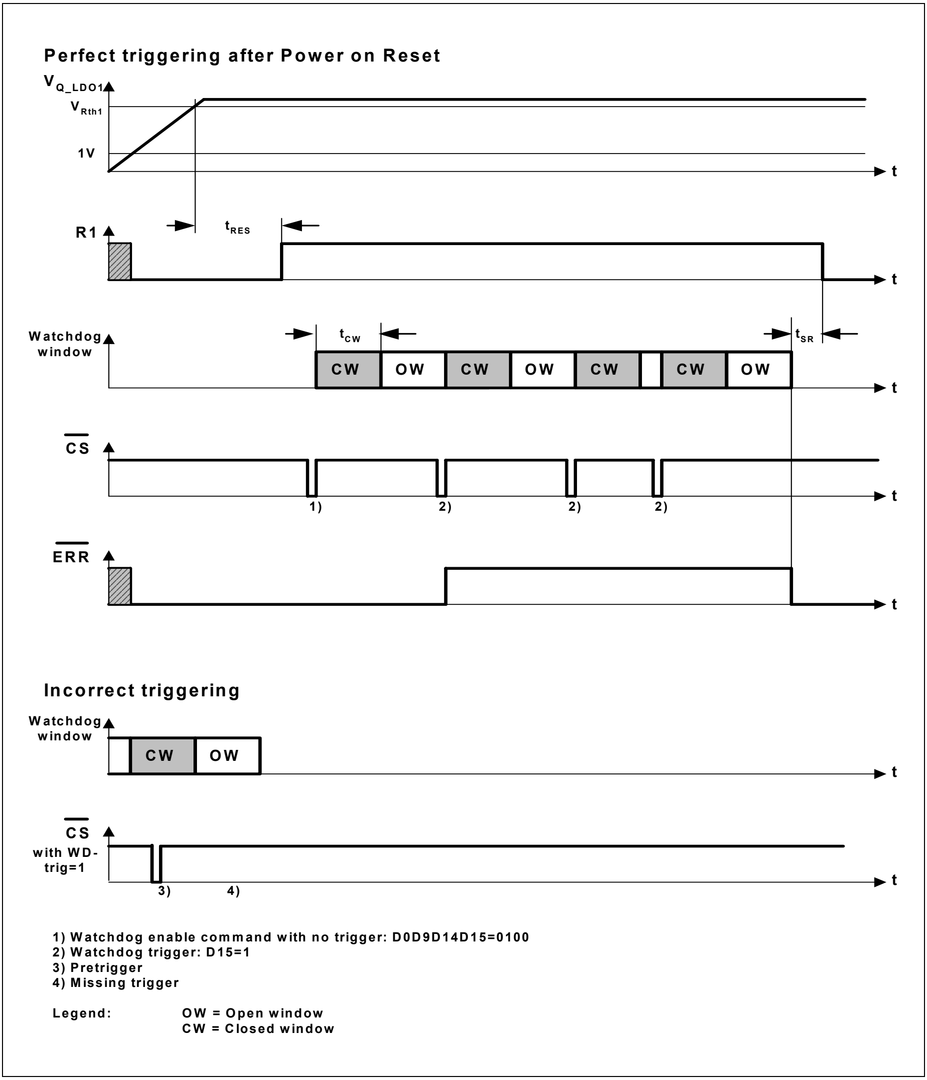


Figure 7 Window watchdog timing

Figure 7 gives some timing information about the window watchdog. Looking at the upper signals the perfect triggering of the watchdog is shown. When the 5V linear regulator Q_LDO1 reaches its reset threshold, the reset delay time has to run off before the closed window (CW) starts. Then three valid watchdog triggers are shown, no effect on the reset line and/or error pin is observed. With the missing watchdog trigger signal the error signal turns low immediately where the reset is asserted after another delay of half the closed window time.

Also shown in the figure are two typical failure modes, one pretrigger and one missing signal. In both cases the error signal will go low immediately the failure is detected with the reset following after the half closed window time.

2.10 Overtemperature Protection

At a chip temperature of more than 150° an error and temperature flag is set and can be read through the SPI. The device is switched off if the device reaches the overtemperature threshold of 170°C. The overtemperature shutdown has a hysteresis to avoid thermal pumping.

2.11 Power Down Mode

The **TLE6368-G2** is started by a static high signal at the wake input or a high pulse with a minimum of 50µs duration at the Wake input (pin 34). Voltages in the range between the turn on and turn off thresholds for a few 100µs must be avoided!

By SPI command (“Sleep”-bit, D8, equals zero) all voltage regulators including the switching regulator except the standby regulator can be turned off completely only if the wake input is low. In the case the Wake input is permanently connected to battery the device cannot be turned off by SPI command, it will always turn on again.
For stable “on” operation of the device the “Sleep”-bit, D8 has to be set to high at each SPI cycle!

When powering the device again after power down the status of the SPI controlled devices (e.g. trackers, watchdog etc.) depends on the output voltage on Q_LDO1. Did the voltage at Q_LDO1 decrease below 3.3V the default status (given in the next section) is set otherwise the last SPI command defines the status.

2.12 Serial Peripheral Interface

A standard 16 bit SPI is available for control and diagnostics. It is capable to operate in a daisy chain. It can be written or read by a 16 bit SPI interface as well as by an 8 bit SPI interface.

The 16-bit control word (write bit assignment, see Figure 8) is read in via the data input DI, synchronous to the clock input CLK supplied by the µC beginning with the LSB D0. The diagnosis word appears in the same way synchronously at the data output DO (read bit assignment, see figure 9), so with the first bit shifted on the DI line the first bit appears on the DO line.

The transmission cycle begins when the TLE6368-G2 is selected by the “not chip select” input $\overline{CS}$ (H to L). After the $\overline{CS}$ input returns from L to H, the word that has been read in at the DI line becomes the new control word. The DO output switches to tristate status at this point, thereby releasing the DO bus circuit for other uses. For details of the SPI timing please refer to Figures 10 to 13.

The SPI will be reset to default values given in the following table “write bit meaning” if the RAM good flag of Q_LDO1 indicates a cold start (lower output voltage than 3.3V). The register content of the SPI - including watchdog timings and reset delay timings - is maintained if the RAM good flag of Q_LDO1 indicates a warm start (i.e. Q_LDO1 did not decrease below 3.3V).
For details please refer to **Application Note TLE6368 SPI**.

2.12.1 Write mode

The following tables show the bit assignment to the different control functions, how to change settings with the right bit combination and also the default status at power up.

2.12.2 Write mode bit assignment

BIT	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D 15
Name	WD_ OFF1	NOT assigned	T1- control	T2- control	T6- control	T4- control	T5- control	T6- control	sleep	WD_ OFF2	reset 1	reset 2	WD1	WD2	WD_ OFF3	WD_ TRIG
Default	1	X	1	1	1	1	1	1	1	0	1	1	0	0	1	0

Figure 8 Write Bit assignment

Write Bit meaning

Function	**Bit**	**Combination**	**Default**
Not assigned	D1	X	X
Tracker 1 to 6 - control: turn on/off the individual trackers	D2 D3 D4 D5 D6 D7	0: OFF 1: ON	1
Power down: send device to sleep	D8	0: SLEEP 1: NORMAL	1

Write Bit meaning

Function	Bit	Combination	Default
Reset timing: Reset delay time t_{RES} valid at warm start	D10D11	00: 64ms 10: 32ms 01: 16ms 11: 8ms	11
Window watchdog timing: Open window time t_{OW} and closed window time t_{CW} valid at warm start	D12D13	00: 128ms 10: 64ms 01: 32ms 11: 16ms	00
Window watchdog function: Enable /disable window watchdog	D0D9D14	010: ON 1xx: OFF x0x: OFF xx1: OFF	101
Window watchdog trigger: Enable / disable window watchdog trigger	D15	0: not triggered 1: triggered	0

2.12.3 Read mode

Below the status information word and the bit assignments for diagnosis are shown.

2.12.3.1 Read mode bit assignment

BIT	DO	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D 15
Name	ERROR	temp_ warn	T1- status	T2- status	T3- status	T4- status	T5- status	T6- status	RAM Good 1	RAM Good 2	WD Window	R-Error1	R-Error2	R-Error3	WD Error	DC/DC status
Default	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1

Figure 9 Read Bit assignment

Read Bit meaning

Function	Type	Bit	Combination	Default
Error indication, explanation see below this table	Latched	D0	0: normal operation 1: fail function	0
Overtemperature warning	Not latched	D1	0: normal operation 1: prewarning	0

Read Bit meaning

Function	Type	Bit	Combination	Default
Status of Tracker Output Q_T[1:6],only if output is ON	Not latched	D2 D3 D4 D5 D6 D7	1: settled output voltage 0:Tracker turned off or shorted output. Also open load may possibly be indicated as 0.[1)]	1
Indication of cold start/warm start, Q_LDO1	Latched	D8	0: cold start 1: warm start	0
Indication of cold start/warm start, Q_LDO2	Latched	D9	0: cold start 1: warm start	0
Indication for open or closed window	Not latched	D10	0: open window 1: closed window	0
Reset condition at output Q_LDO1	Not latched	D11	0: normal operation 1: Reset R1	0
Reset condition at output Q_LDO2	Not latched	D12	0: normal operation 1: Reset R2	0
Reset condition at output Q_LDO3	Not latched	D13	0: normal operation 1: Reset R3	0
Watchdog Error	Latched	D14	0: normal operation 1: WD error	0
DC/DC converter status	Not latched	D15	0: off 1: on	1

1) Min. load current to avoid ’0’ signal caused by open load is 2mA.

Error bit D0:

The error output $\overline{\text{ERR}}$ is low and the error bit indicates fail function if the temperature prewarning or the watchdog error is active, further if one RAM good indicates a cold start or if a voltage tracker does not settle within 1ms when it is turned on.

2.12.4 SPI Timings

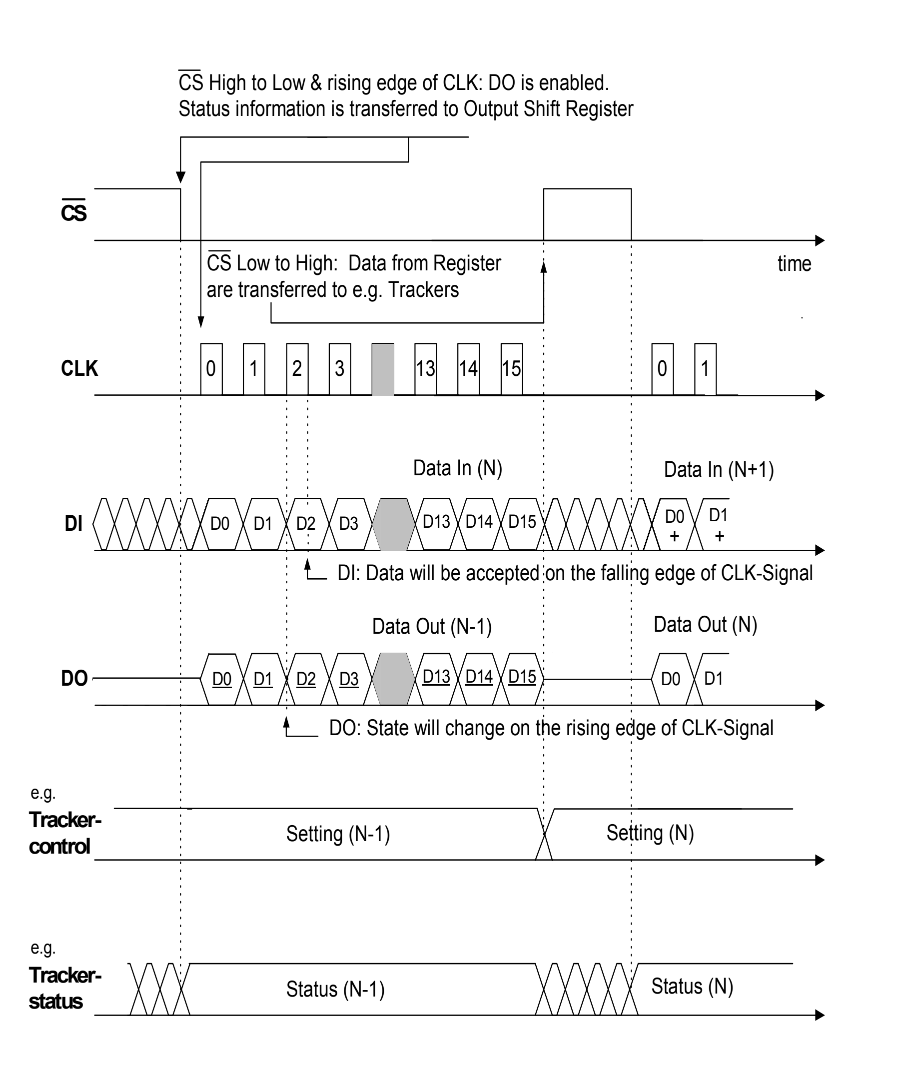


Figure 10 SPI Data Transfer Timing

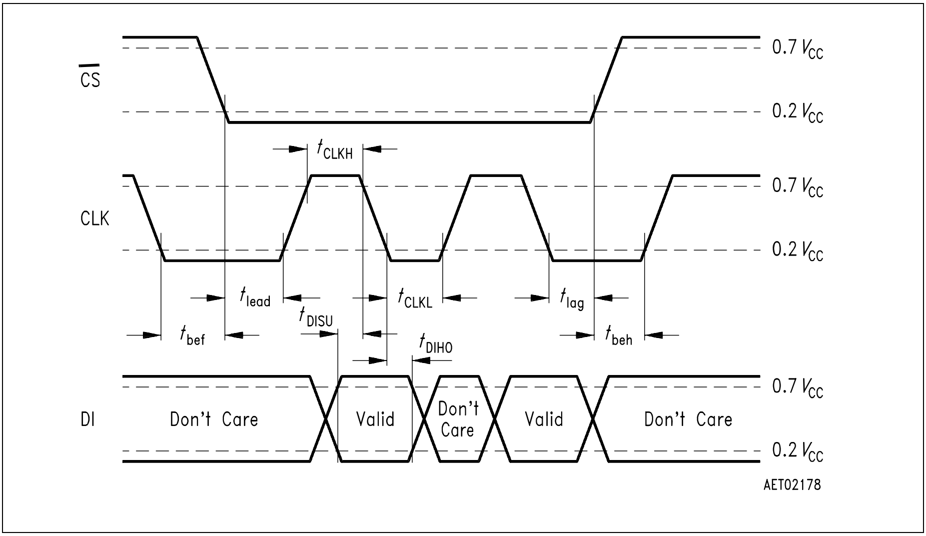


Figure 11 SPI-Input Timing

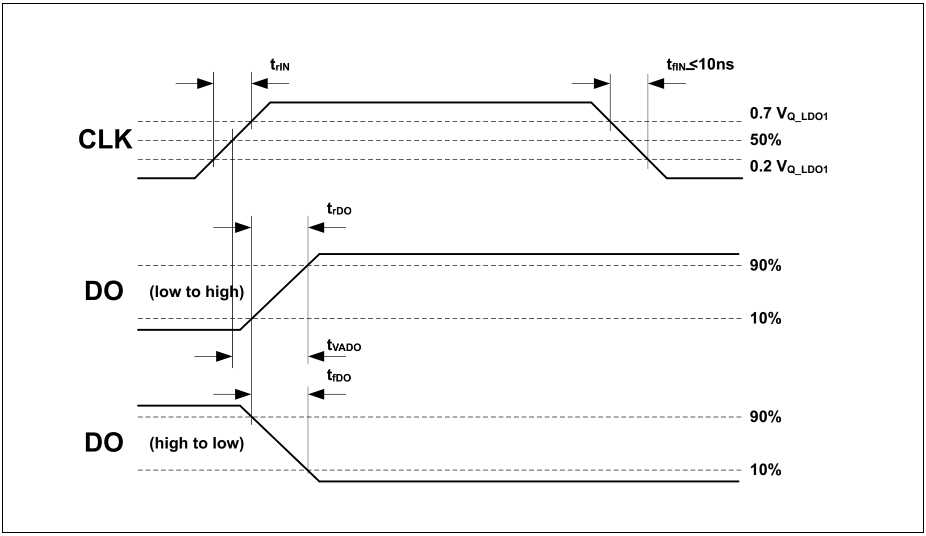


Figure 12 DO Valid Data Delay Time and Valid Time

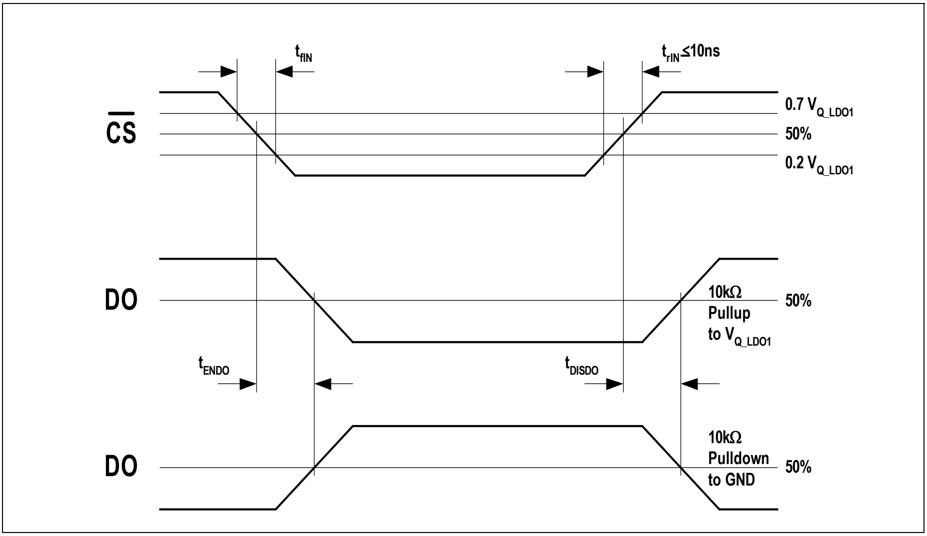


Figure 13 DO Enable and Disable Time

3 Characteristics

3.1 Absolute Maximum Ratings

Item	Parameter	Symbol	Limit Values		Unit	Test Condition
			Min.	Max.		
3.1.1	**Supply Voltage Input IN**					
	Voltage	V_{IN}	-0.5	60	V	–
	Voltage	V_{IN}	-1.0	60	V	T_j = -40 °C
	Current	I_{IN}	–	–	–	
3.1.2	**Buck-Switch Output SW**					
	Voltage	V_{SW}	-2	V_S+0.5	V	–
	Current	I_{SW}	–	–	–	
3.1.3	**Feedback and Linear Voltage Regulator Input**					
	Voltage	V_{FB/L_IN}	-0.5	8	V	–
	Current	I_{FB/L_IN}	–	–	–	
3.1.4	**Bootstrap Connector Bootstrap**					
	Voltage	$V_{Bootstrap}$	V_{SW}-0.5V	V_{SW}+10V	V	
	Voltage	$V_{Bootstrap}$	-0.5	70	V	
	Current	$I_{Bootstrap}$	–	–	–	Internally limited
3.1.5	**Boost Input**					
	Voltage	V_{Boost}	-0.5	60	V	–
	Current	I_{Boost}	–	–	–	Internally limited
3.1.6	**Slope Control Input Slew**					
	Voltage	V_{Slew}	-0.5	6	V	–
	Current	I_{Slew}	–	–	–	Internally limited
3.1.7	**Charge Pump Capacitor Connector C-**					
	Voltage	V_{CL}	-0.5	V_{FB/L_IN} +0.5	V	
	Current	I_{CL}	-150	+150	mA	

3.1.8	**Charge Pump Capacitor Connector C+**					
	Voltage	V_{CH}	-0.5	13	V	
	Current	I_{CH}	-150	+150	mA	
3.1.9	**Charge Pump Storage Capacitor CCP**					
	Voltage	V_{CCP}	-0.5	12	V	
	Current	I_{CCP}	-150	–	mA	
3.1.10	**Standby Voltage Regulator output Q_STB**					
	Voltage	V_{Q_Stb}	-0.5	6	V	–
	Current	I_{Q_Stb}	–	–	–	Internally limited
3.1.11	**Voltage Regulator output voltage Q_LDO1**					
	Voltage	V_{Q_LDO1}	-0.5	6	V	–
	Current	I_{Q_LDO1}	–	–	–	Internally limited
3.1.12	**Voltage Regulator output voltage Q_LDO2**					
	Voltage	V_{Q_LDO2}	-0.5	6	V	–
	Current	I_{Q_LDO2}	–	–	–	Internally limited
3.1.13	**Voltage Regulator output voltage Q_LDO3**					
	Voltage	V_{Q_LDO3}	-0.5	6	V	–
	Current	I_{Q_LDO3}	–	–	–	Internally limited
3.1.14	**Voltage Tracker output voltage Q_T1**					
	Voltage	V_{Q_T1}	-4	40	V	–
	Current	I_{Q_T1}	–	–	mA	Internally limited
3.1.15	**Voltage Tracker output voltage Q_T2**					
	Voltage	V_{Q_T2}	-4	40	V	–
	Current	I_{Q_T2}	–	–	mA	Internally limited
3.1.16	**Voltage Tracker output voltage Q_T3**					
	Voltage	V_{Q_T3}	-4	40	V	–
	Current	I_{Q_T3}	–	–	mA	Internally limited
3.1.17	**Voltage Tracker output voltage Q_T4**					
	Voltage	V_{Q_T4}	-4	40	V	–
	Current	I_{Q_T4}	–	–	mA	Internally limited