Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

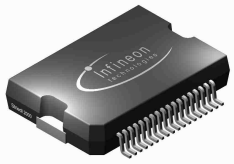
Smart Octal Low-Side Switch

Features

- Full Protection
  - Overload
  - Overtemperature
  - Overvoltage
- Low Quiescent Current< 10µA
- 16 bit SPI (for Daisychain)
- Direct Parallel Control of Four Channels
- PWM input (demux)
- Parallel Inputs High or Low Active Programmable
- Programmable functions
  - Boollean operation
  - Overload behavior
  - Overtemperature behavior
  - Switching time
- General Fault Flag
- Digital Ports Compatible to 5V and 3,3 V Micro Controllers
- **E**lecto**s**tatic **D**ischarge (ESD) Protection
- Full reverse current capability without latchup or loss of function

Product Summary

Supply voltage	V_S	4.5 – 5.5	V
Drain source clamping voltage	$V_{DS(AZ)max}$	60	V
On resistance	R_{ON}	0.8	Ω



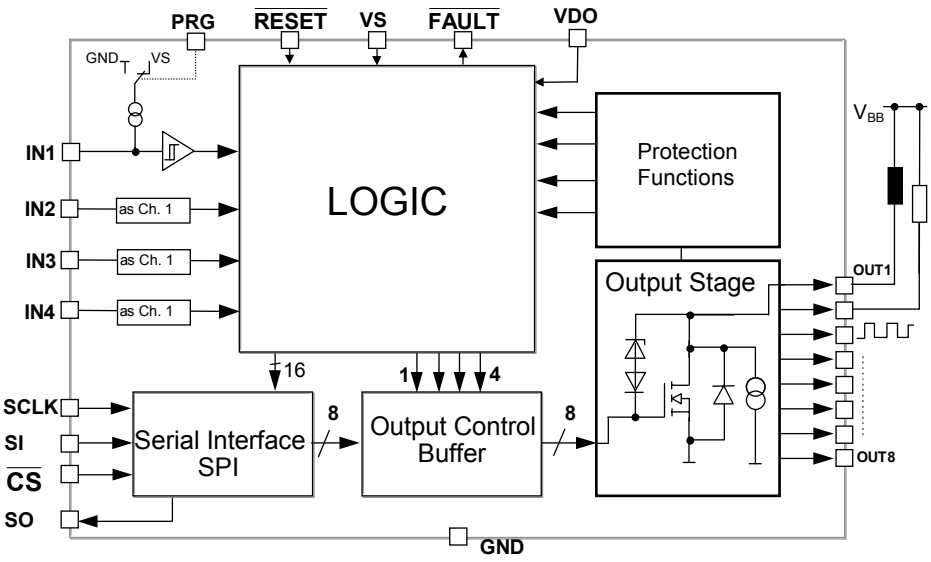
Power P-DSO 36

P-DSO-24

General description

Octal Low-Side Switch in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and eight open drain DMOS output stages. The TLE 7230 R/G is protected by embedded protection functions and designed for automotive applications.

Detailed Block Diagram



Power SO 36 package

Pin Description

Pin	Symbol	Function
1	GND	Ground
2	NC	not connected
3	NC	not connected
4	OUT1	Output Channel 1
5	OUT2	Output Channel 2
6	IN1	Input Channel 1
7	IN2	Input Channel 2
8	VS	Supply Voltage
9	Reset	Reset
10	CS	Chip Select
11	PRG	Program
12	IN3	Input Channel 3
13	IN4	Input Channel 4
14	OUT3	Output Channel 3
15	OUT4	Output Channel 4
16	NC	not connected
17	NC	not connected
18	GND	Ground
19	GND	Ground
20	NC	not connected
21	NC	not connected
22	OUT5	Output Channel 5
23	OUT6	Output Channel 6
24	NC	not connected
25	VDO	Supply for digital Outputs
26	Fault	General Fault Flag
27	SO	Serial Data Output
28	SCLK	Serial Clock
29	SI	Serial Data Input
30	NC	not connected
31	NC	not connected
32	OUT7	Output Channel 7
33	OUT8	Output Channel 8
34	NC	not connected
35	NC	not connected
36	GND	Ground

Heat Slug internally connected to ground pins

Pin Configuration (Top view)

1	GND	GND	36
2	NC	NC	35
3	NC	NC	34
4	Out1	Out8	33
5	Out2	Out7	32
6	IN1	NC	31
7	IN2	NC	30
8	VS	SI	29
9	Reset	SCLK	28
10	CS	SO	27
11	PRG	Fault	26
12	IN3	VDO	25
13	IN4	NC	24
14	Out3	Out6	23
15	Out4	Out5	22
16	NC	NC	21
17	NC	NC	20
18	GND	GND	19

Power- P-DSO-36

SO 24 package (thermal enhanced)

Pin Description

Pin	Symbol	Function
1	CS	Chip Select
2	IN	Mappable input
3	OUT3	Output Channel 3
4	OUT4	Output Channel 4
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	OUT5	Output Channel 5
10	OUT6	Output Channel 6
11	VDO	Supply for digital Outputs
12	SO	Serial Data Output
13	SCLK	Serial Clock
14	SI	Serial Data Input
15	OUT7	Output Channel 7
16	OUT8	Output Channel 8
17	GND	Ground
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	OUT1	Output Channel 1
22	OUT2	Output Channel 2
23	VS	Supply Voltage
24	Reset	Reset

Heat Slug internally connected to ground pins

Pin Configuration (Top view)

1	**CS**	**Reset**	**24**
2	**IN**	**Vs**	**23**
3	**Out3**	**Out2**	**22**
4	**Out4**	**Out1**	**21**
5	**GND**	**GND**	**20**
6	**GND**	**GND**	**19**
7	**GND**	**GND**	**18**
8	**GND**	**GND**	**17**
9	**Out5**	**Out8**	**16**
10	**Out6**	**Out7**	**15**
11	**VDO**	**SI**	**14**
12	**SO**	**SCLK**	**13**

P-DSO-24

Maximum Ratings for T_j = – 40°C to 150°C

Parameter	Symbol	Values	Unit
Supply Voltage	V_S	-0.3 ... + 6	V
Continuous Drain Source Voltage (OUT1...OUT8)	V_{DS}	48	V
Input Voltage, All Inputs and Data Lines	V_{IN}	- 0.3 ... + 6	V
Operating Temperature Range Storage Temperature Range	T_j T_{stg}	- 40 ... + 150 - 55 ... + 150	°C
Output Current per Channel (see el. characteristics)	$I_{D(lim)}$	$I_{D(lim)min}$	A
Reverse current per channel	I_R	- $I_{D(lim)min}$	A
Output Clamping Energy (single pulse) I_D = 0.5 A	E_{AS}	tbd	mJ
Electro**s**tatic **D**ischarge **V**oltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 – 1993 Output 1-8 Pins All other Pins	 V_{ESD} V_{ESD}	 2000 2000	 V V
DIN Humidity Category, DIN 40 040		E	
IEC Climatic Category, DIN IEC 68-1		40/150/56	
Thermal Resistance junction – case (Power SO-36, all channels on) junction – case (SO-24, all channels on)	 R_{thJC} R_{thJC}	 tbd tbd	 K/W

Electrical Characteristics

Parameter and Conditions V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)		Symbol	Values			Unit
			min	typ	max	
1. Power Supply, Reset						
Supply Voltage[1]		V_S	4.5	--	5.5	V
Supply Current		I_S	--	1	2	mA
Supply Current (reset mode)	Reset = L	$I_{S(reset)}$	--		10	µA
Minimum Reset Duration		$t_{Reset,min}$	10	--	--	µs
2. Outputs						
ON Resistance V_S = 5 V; I_D = 500 mA	T_J = 25°C T_J = 150°C	$R_{DS(ON)}$	-- --	0.8 --	1 1.7	Ω
Output Clamping Voltage	Output OFF	$V_{DS(AZ)}$	48	--	60	V
Current Limit		$I_{D(lim)}$	1		2	A
Output Leakage Current	V_{Reset} = L V_{bb}=12V	$I_{D(lkg)}$	--	--	5	µA
Turn-On Time	I_D = 0.5 A, resistive load	t_{ON}	--		15 / 60	µs
Turn-Off Time	I_D = 0.5 A, resistive load	t_{OFF}	--		15 / 60	µs
3. Digital Inputs						
Input Low Voltage		V_{INL}	- 0.3	--	1.0	V
Input High Voltage		V_{INH}	2.0	--	--	V
Input Voltage Hysteresis		V_{INHys}		100		mV
Input Pull Down/Up Current (IN1 ... IN4)		$I_{IN(1..4)}$		50		µA
PRG, Reset Pull Up Current		$I_{IN(PRG,Res)}$		50		µA
Input Pull Down Current (SI, SCLK)		$I_{IN(SI,SCLK)}$		20		µA
Input Pull Up Current (CS)		$I_{IN(CS)}$		20		µA
4. Digital Outputs (SO, Fault**)**						
SO High State Output Voltage	I_{SOH} = 2 mA	V_{SOH}	V_{VDO} - 0.4	--	--	V
SO Low State Output Voltage	I_{SOL} = 2.5 mA	V_{SOL}	--	--	0.4	V
Output Tri-state Leakage Current	$\overline{CS}$ = H, 0 ≤ V_{SO} ≤ V_S	I_{SOlkg}	-10	0	10	µA
Fault Output Low Voltage	I_{FAULT} = 1.6 mA	V_{FAULTL}	--	--	0.4	V

[1] For V_S < 4.5V the power stages are switched according the input signals and data bits or are definitely switched off.

Electrical Characteristics cont.

Parameter and Conditions	Symbol	Values			Unit
V_S = 4.5 to 5.5 V ; T_j = - 40 °C to + 150 °C ; Reset = H (unless otherwise specified)		min	typ	max	
5. Diagnostic Functions					
Open Load Detection Voltage	$V_{DS(OL)}$		V_S -2		V
Output Pull Down Current	$I_{PD(OL)}$		90		µA
Fault Delay Time	$t_{d(fault)}$		100		µs
Overload switch off delay time	$T_{d(off)}$	10		50	µs
Short to Ground Detection Voltage	$V_{DS(SHG)}$		V_S -2.9		V
Short to Ground Detection Current	I_{SHG}		-100		µA
Overload Threshold Current	$I_{D(lim)\ 1...8}$	1		2	A
Overtemperature Shutdown Threshold[2]	$T_{th(sd)}$	175	--	200	°C
Hysteresis[2]	T_{hys}	--	10	--	K
6. SPI-Timing (for V_{VDO} = 4.5V to 5.5V)					
Serial Clock Frequency (depending on SO load)	f_{SCK}	DC	--	5	MHz
Serial Clock Period (1/fclk)	$t_{p(SCK)}$	200	--	--	ns
Serial Clock High Time	t_{SCKH}	50	--	--	ns
Serial Clock Low Time	t_{SCKL}	50	--	--	ns
Enable Lead Time (falling edge of CS to rising edge of CLK)	t_{lead}	250	--	--	ns
Enable Lag Time (falling edge of CLK to rising edge ofCS)	t_{lag}	250	---	--	ns
Data Setup Time (required time SI to falling of CLK)	t_{SU}	20	--	--	ns
Data Hold Time (falling edge of CLK to SI)	t_H	20	--	--	ns
Disable Time @ C_L = 50 pF[2]	t_{DIS}	--	--	150	ns
Transfer Delay Time[3] (CS high time between two accesses)	t_{dt}	tbd	--	--	ns
Data Valid Time C_L = 50 pF[2]	t_{valid}	--	tbd		ns
C_L = 100 pF[2]		--	tbd		
C_L = 220 pF[2]		--	tbd		

[2] This parameter is not subject to production test

[3] This time is necessary between two write accesses. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200µs.

Functional Description

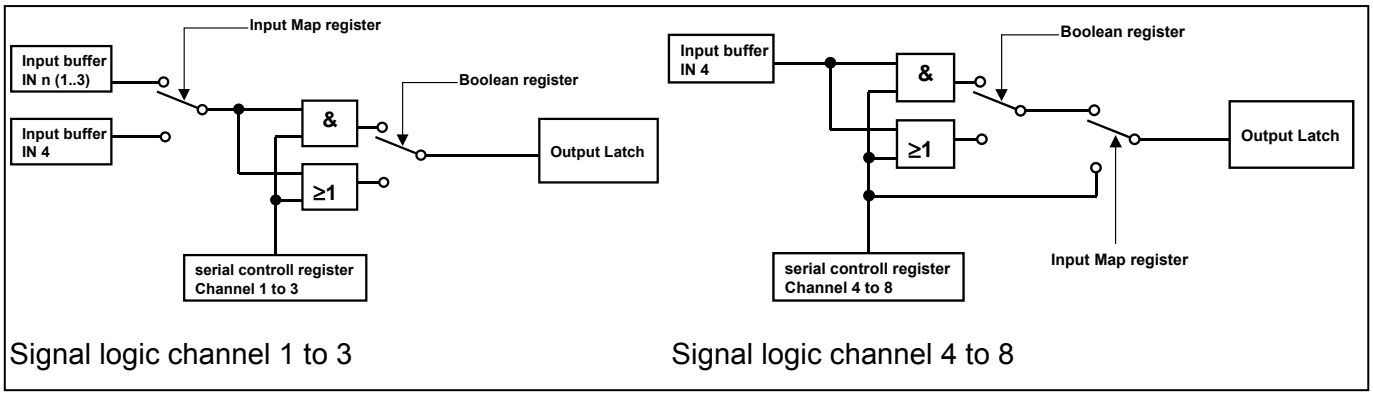
The TLE 7230 R/G is an octal-low-side power switch which provides a serial peripheral interface (SPI) to control the 8 power DMOS switches, as well as diagnostic feedback. The power transistors are protected[4)] against overload (current limitation), overtemperature and against overvoltage by an active zener clamp. The diagnostic logic recognizes a fault condition which can be read out via the serial diagnostic output (SO).

Output Stage Control: Parallel Control or SPI Control
The Output stages can be controlled by parallel Inputs or by SPI command. The IC can be programmed (by SPI) to switch the outputs according to the corresponding SPI command bit or to a combination of SPI bit and parallel input signal. The logic combination of parallel and serial signal is programmable by SPI (Boolean operation) to logic "AND" or "OR" The respective SPI databits are high active, the parallel Inputs are high or low active according to the PRG pin (see pin description).

Boolean operation:
The logic combination of the parallel and the serial input signal can be configured by an SPI command for each of the 8 channels individually. Logic "AND" or logic "OR" is possible.

parallel in	serial in	Output "OR"	Output "AND"
off	off	off	off
off	on	on	off
on	off	on	off
on	on	on	on

Mappable parallel input (IN 4):
By SPI Command the parallel input 4 (IN4 or IN) can be defined as parallel input for one or more power outputs. Depending on the Input Map Register this input can be used to controll one up to eight of the parallel outputs. Default operation: IN4 / IN is the parallel input for channel 4.



Signal logic channel 1 to 3 Signal logic channel 4 to 8

Switching speed / Slew rate:
The switching speed / slew rate of all 8 channels can be configured by SPI for slow or fast switching speed (1:5) for each channel individually.

Overtemperature Behavior:
Each channel has an overtemperature sensor and is individually protected against overtemperature. As soon as overtemperature occurs the channel is immediately turned off and the overtmperature information is reported by diagnosis. In this case there are two different behaviours of the affected channel that can be selected by SPI (for all channels individually).
Autorestart: as long as the input signal of the channel remains on (e.g. parallel input high) the channel turns automatically on again after cooling down.

[4])The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently.

Latching: After overtemperature shutdown the channel stays off until the overtemperature latch is reset by a new L→H transition of the input signal.
Note: The overtemperature sensors of the output channels are only active if the channel is turned on.

Low Quiescent current mode (Sleep mode) :
By applying ay low signal at the Reset Pin the device can be set to Sleep mode. In this mode all outputs are turned off, the diagnosis and biasing is disabled, the diagnosis and the on/off register are reseted and the current consumption drastically reduced (<10µA). After a reset the outputs are Off, except the outputs are controlled by parallel inputs.

Overload Protection:
The IC can be programmed to react in different ways to overload.
Only Current limit: The IC actively limits the current to the specified current lmit value. If the current limitation is active for longer than the fault filtering time this fault is reported and stored in the Fault register. The channel is not shutdown.
Current limit + shutdown: The IC actively limits the current to the specified current lmit value. If this current limit is active for more than the specified Overload switch off delay time the affected channel is turned off and the fault is reported and stored in the fault register. To turn on the channel again this overload latch has to be reset before with an L→ H transition of the input signal (parallel /SPI depending on the programmed operation).

Pin description:

OUTPUT 1 to 8 – Drain pins of the 8 channels. Output pins and connected to the load.

GND – Ground pins.

IN 1 to 3 – Parallel Input Pins of the channels 1 to 3

IN 4 / IN – Mappable parallel Input Pin. Can be assigned to different outputs by SPI command. Default Output is OUT4

PRG - Program pin. PRG = High (V_S): Parallel inputs 1 to 4 are high active
PRG = Low (GND): Parallel inputs 1 to 4 are low active.
If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the channels 1 to 4 are switched OFF.
PRG pin itself is internally pulled up when it is not connected.

Reset - If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.

Fault - There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the eight channels. This fault indication can be used to generate a µC interrupt. Therefore a ‘diagnosis’ interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.

VDO – Supply pin of the push-pull digital output drivers. This pin can be used to vary the high-state output voltage of the SO pin.
Vs – Logic supply pin. This pin is used to supply the integrated circuitry.

CS – Chip Select of the SPI

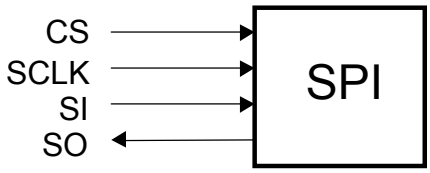
SO – Signal Output of the **S**erial **P**eripheral **I**nterface

SI – Signal Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull down structure.

SCLK – Clock Input of the **S**erial **P**eripheral **I**nterface. The pin has an internal pull down structure

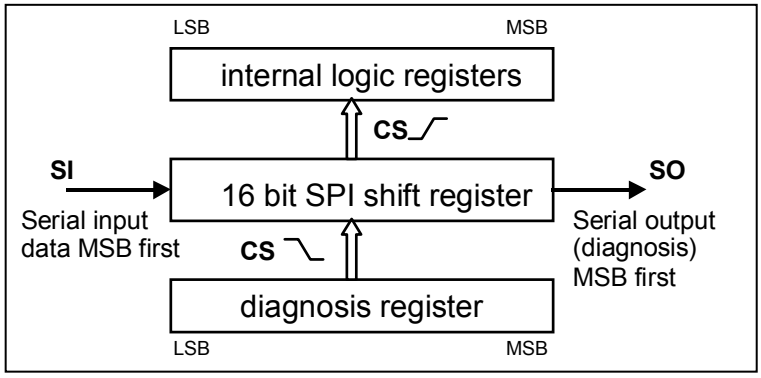
SPI

The SPI is a **S**erial **P**eripheral **I**nterface with 4 digital pins and an 16 bit shift register. The SPI is used to configure and program the device, turn on and off channels and to read detailed diagnostic information.



SPI Signal Description:

CS - Chip Select. The system microcontroller selects the TLE 7230 R/G by means of the CS pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.



CS = H : Any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

CS = H→L :

- diagnostic information is transferred from the diagnosis register into the SPI shift register. (in sleep mode no tranfer of diagnostic information)
- serial input data can be clocked into the SPI shift register from then on
- SO changes from high impedance state to logic high or low state corresponding to the SO bits

CS = L : SPI is working like a shift register. With each clock signal at the SCLK pin the state of the SI is read into the SPI shift-register (falling clock edge) and one diagnosis bit is written out of SO (rising rising edge).

CS = L→H:

- transfer of SI bits from SPI shift register into the internal logic registers
- reset of diagnosis register if sent command was valid

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of CS. The SPI of the TLE7230G/R has a modulo 8 counter integrated. If the number of clock signals is not an integer multiple of 8 the SPI will not accept the data in the shift register and the fault register will not be reset.

SCLK - Serial Clock. The serial clock pin clocks the internal SPI shift register of the TLE7230G/R. The serial input (SI) accepts data into the input SPI shift register on the falling edge if while the serial output (SO) shifts diagnostic information out of the SPI shift register on the rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select CS makes any transition.

SI - Serial Input. Serial data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read in on the falling edge . Input data is latched in the SPI shift register and then transferred to the internal registers of the logic.

The input data consist of 16 bit, made up of x control bits and y data bits. The control word is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see SPI Commands).

SO - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit (MSB) first. SO is in a high impedance state until the CS pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge.

SPI Control and Commands:

	MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
SI:	CMD		x	x	x	ADDR			DATA							

SO standard diagnosis

SO:	Ch 8	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1

SO after read command in previous frame

SO:	0	1	0	0	0	ADDR	DATA

CMD **Command :**

0 0 : Diagnosis Only :
Reads out the diagnosis register. This command has no other influence on the device.

0 1 : Read register :
With the next SO dataframe the content of the addressed register will be sent.

1 0 : Reset Registers
Sets back all internal registers. Logic registers to default and Fault registers to no error.

1 1 : Write register :
The data of the SI word will be written to the addressed register.

No valid Commands :
If the first 8 bit of the SI word contain no valid bit combination it will not lead to an reaction (register value change, switching channels, ...) of the IC. After Chip Select giong L→H the diagnosis register will not be reset.

ADDR **Address :**
Pointer to register for read and write command

DATA **Data:**
Data written to or read from register selected by address ADDR

Ch x **Standard diagnosis for channel x:**
Details see "SPI Diagnostics"

Register Description:

Name	Nr.	7	6	5	4	3	2	1	0	ADDR	default
MAP	1	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	0 0 1	08_H
BOL	2	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	0 1 0	00_H
OVL	3	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	0 1 1	00_H
OVT	4	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	1 0 0	00_H
SLE	5	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	1 0 1	00_H
STA	6	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	1 1 0	00_H
CTL	7	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	1 1 1	00_H

Input Mapping Rgister (MAP**)**
Defined to which outputs the IN4 / IN is assigned (can be one up to all)
0.. No connection to IN4 / IN
1.. Output can be controlled with IN4 / IN pin

Boolean operation Register (BOL**)**
The logic operation for serial and parallel control signal is defined for all channels individually
0.. Logic "OR"
1.. Logic "AND"

Overload Behavior Rgister (OVL**)**
The overload behavior of a single channel is defined.
0.. Current limit without shutdown of the channel
1.. Current limit with latching overload shutdown of the channel

Overtemperature Behavior Register (OVT**)**
The overtemperature behavior of a single channel is defined.
0.. Autorestart after cooling down
1.. Latching shutdown on overtemperature

Switching Speed / Slew Rate Register (SLE**)**
The switching speed of the channels is defined
0.. fast (10µs)
1.. slow (50µs)

Output State Register (STA**)**
Reads back the state of the output (read only register)
0: DMOS off
1: DMOS on

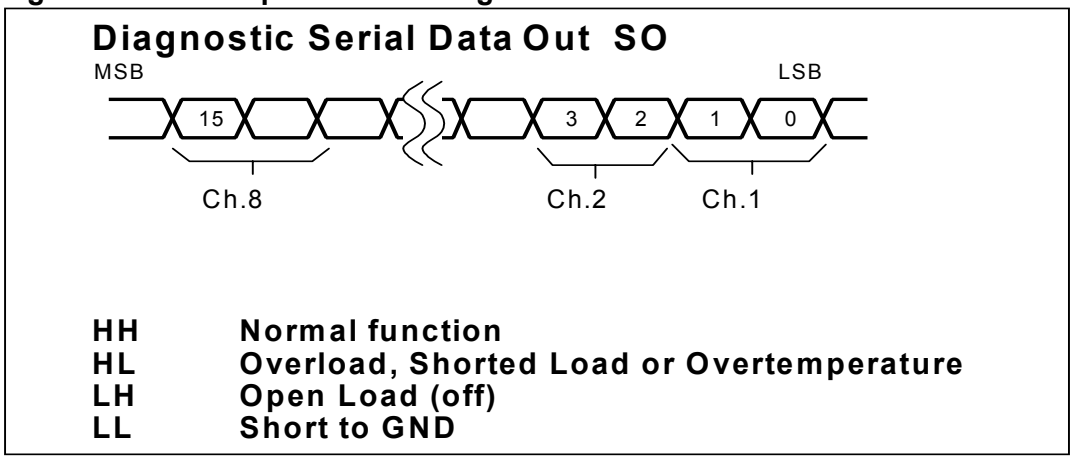
Serial Output Control Register (CTL**)**
Sets the serial controll bits for switching the output stages.
0: Output off
1: Output on

SPI Diagnostics:

As soon as a fault occurs for longer than the fault filtering time, the fault information is latched into the diagnosis register (and the Fault pin will change from high to low state). A new error on the same channel will over-write the old error report. Serial data out pin (SO) is in a high impedance state when CS is high. If CS receives a LOW signal, all diagnosis bits can be shifted out serially. If the sent com-

mand was valid the rising edge of CS will reset all diagnosis registers and restart the fault filtering time. In case of an invalid command the device will ignore the data bits and the diagnosis register will not be reset at the rising CS edge.

Figure 1: Two bits per channel diagnostic feedback



For Full Diagnosis there are two diagnostic bits per channel configured as shown in Figure 1.
Normal function: The bit combination **HH** indicates that there is no fault condition, i.e. normal function.
Overload, Shorted Load or Overtemperature: HL is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition. The second reason for this bit combination is overtemperature of the corresponding channel.
Open load: LH is set when open load is detected (in off state of the channel)
Short to GND : LL is set when this condition is detected (in off state)

Timing Figures

Figure 5: Power Outputs

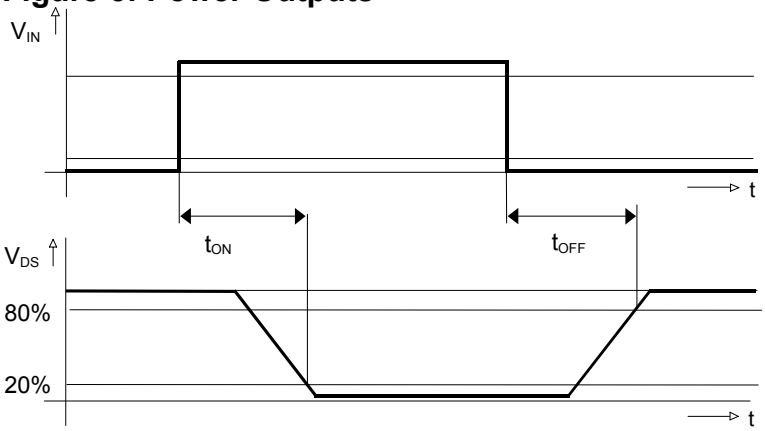


Figure 6: Serial Interface Timing Diagram

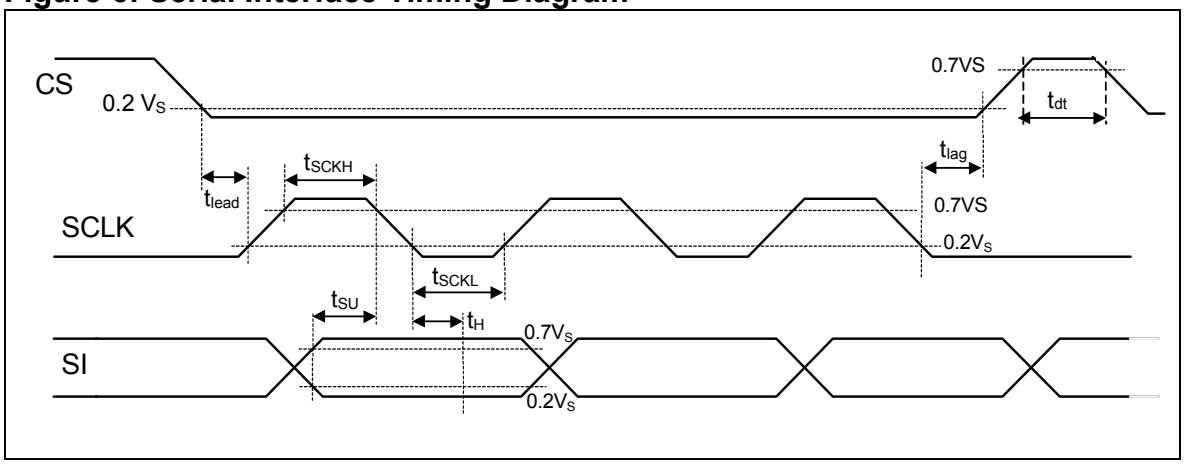
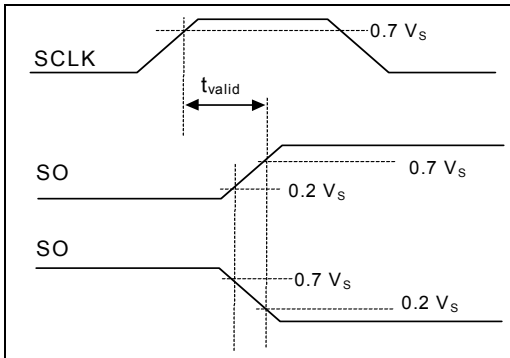
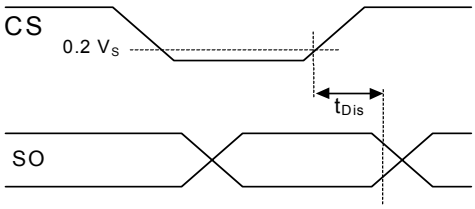


Figure 7: Input Timing Diagram

SO Valid Time Waveforms



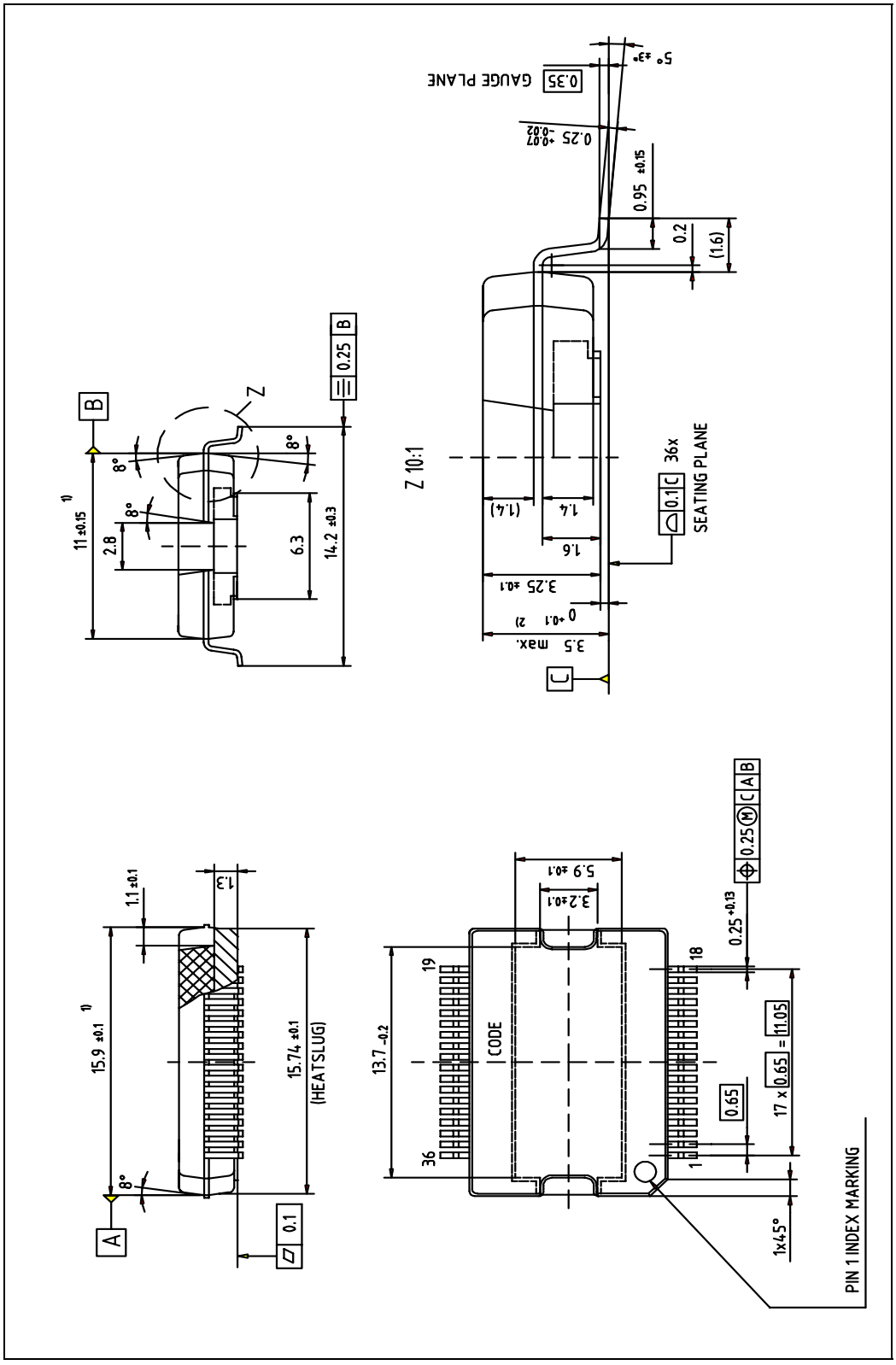
Enable and Disable Time Waveforms



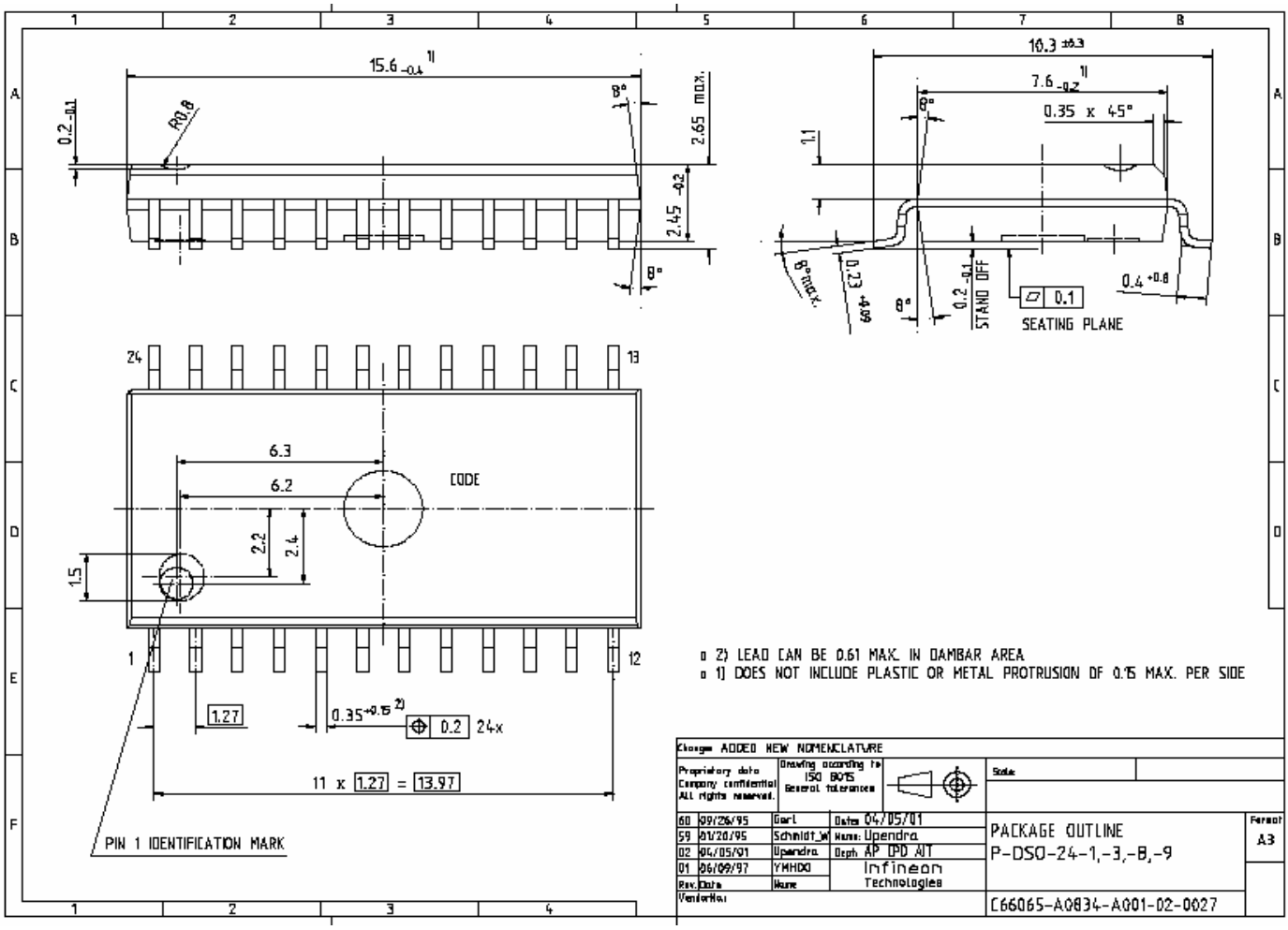
(all dimensions in mm)

P-DSO 36-12

Ordering Code	
TLE 7230 R	



P-DSO 24	Ordering Code
TLE 7230 G	



Published by
Infineon Technologies AG,
Bereichs Kommunikation
St.-Martin-Strasse 76,
D-81541 München

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.