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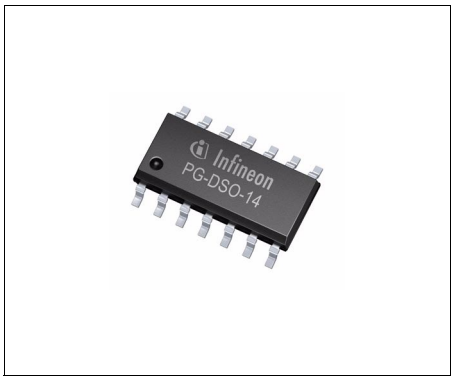
TLE7231G

SPIDER - 4 channel low-side driver

Automotive Power

Table of Contents

1 Overview



PG-DSO-14-1

Features

- 4 channel low-side relay driver
- 8-bit SPI for diagnostics and control
- SPI providing Daisy Chain Capability
- Very wide range for digital Supply Voltage
- An input pin provides flexible and straightforward PWM operation
- Stable behavior at Under Voltage
- Green Product (RoHS compliant)
- AEC Qualified

Table 1 Product Summary

Digital supply voltage	V_{DD}	3.0 V ... 5.5 V
Analog supply voltage	V_{DDA}	4.5 V ... 5.5 V
ON State resistance at T_j = 150°C for each channel	$R_{DS(ON)}$	2.2 Ω
Nominal load current	$I_{D\ (nom,min)}$	320 mA
Overload switch off threshold	$I_{D\ (OVL,max)}$	950 mA
Output leakage current per channel at 25 °C	$I_{D\ (STB,max)}$	1 µA
Drain to Source clamping voltage	$V_{DS(AZ)}$	41 V
SPI clock frequency	f_{SCLK}	5 MHz

Diagnostic Features

- Latched diagnostic information via SPI
- Over temperature monitoring
- Over load detection in ON state
- Open load detection in OFF state

Type	Package	Marking
TLE7231G	PG-DSO-14-1	TLE7231G

Protection Functions

- Short circuit
- Over load
- Over temperature
- Electrostatic discharge (ESD)

Application

- All types of resistive, inductive and capacitive loads
- Especially designed for driving relays in automotive applications

Description

The TLE7231G is a four channel low-side relay switch (1 Ω per channel) in PG-DSO-14-1 package providing embedded protective functions. It is especially designed as a relay driver for automotive applications. The 8-bit serial peripheral interface (SPI) is provided for control and diagnostics of the device and the loads. The SPI interface provides daisy-chain capability.

The TLE7231G is equipped with an input pin that can be individually routed to the output control of each channel and therefore offer complete flexibility in design and PCB layout. The input multiplexer is controlled via SPI.

The device provides many diagnostics of the load enabling both open load and short circuit detection. The SPI diagnostic bits indicate any eventual latched fault condition.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. Temperature sensors are available for each channel in order to protect the device against over temperature.

The power transistors are made of N-channel vertical power MOSFETs. The inputs are CMOS compatible and are referenced to Ground. The device is monolithically integrated in Smart Power Technology.

2 Block Diagram

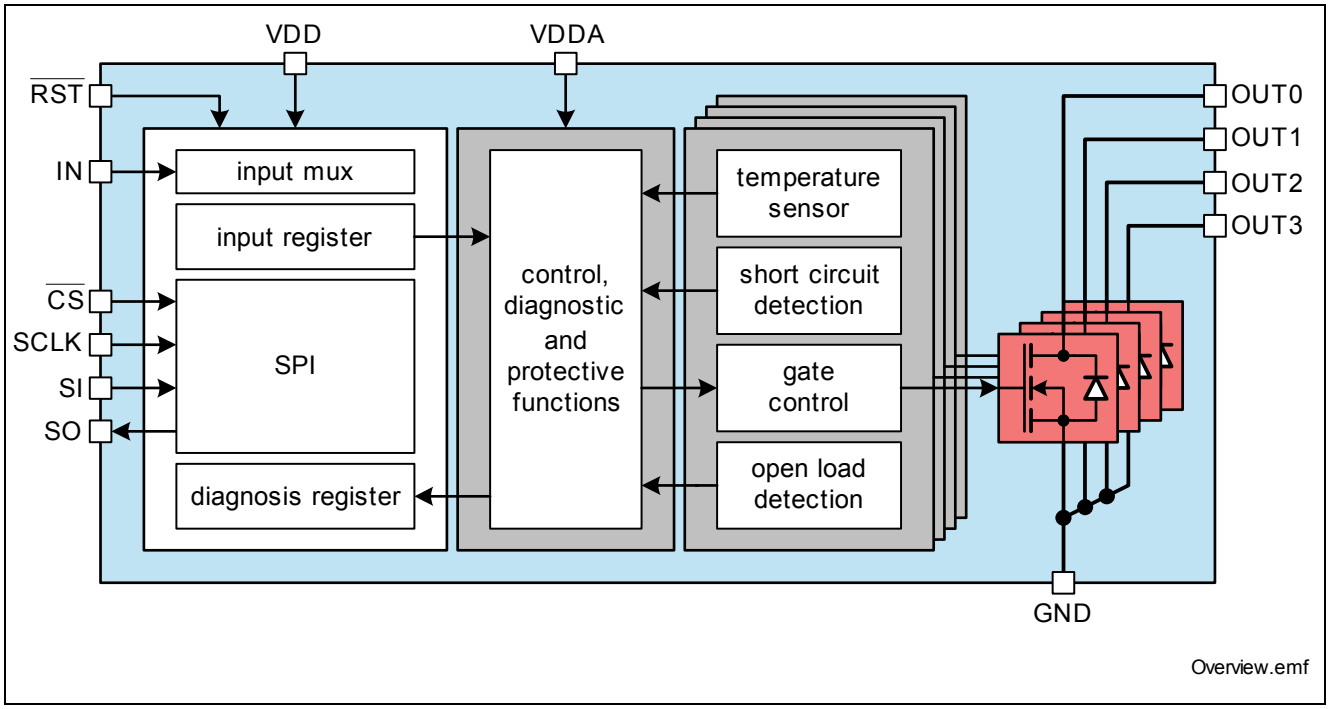


Figure 1 Block Diagram TLE7231G

2.1 Voltage and current naming definition

Following figure shows all the terms used in this datasheet, with associated convention for positive values.

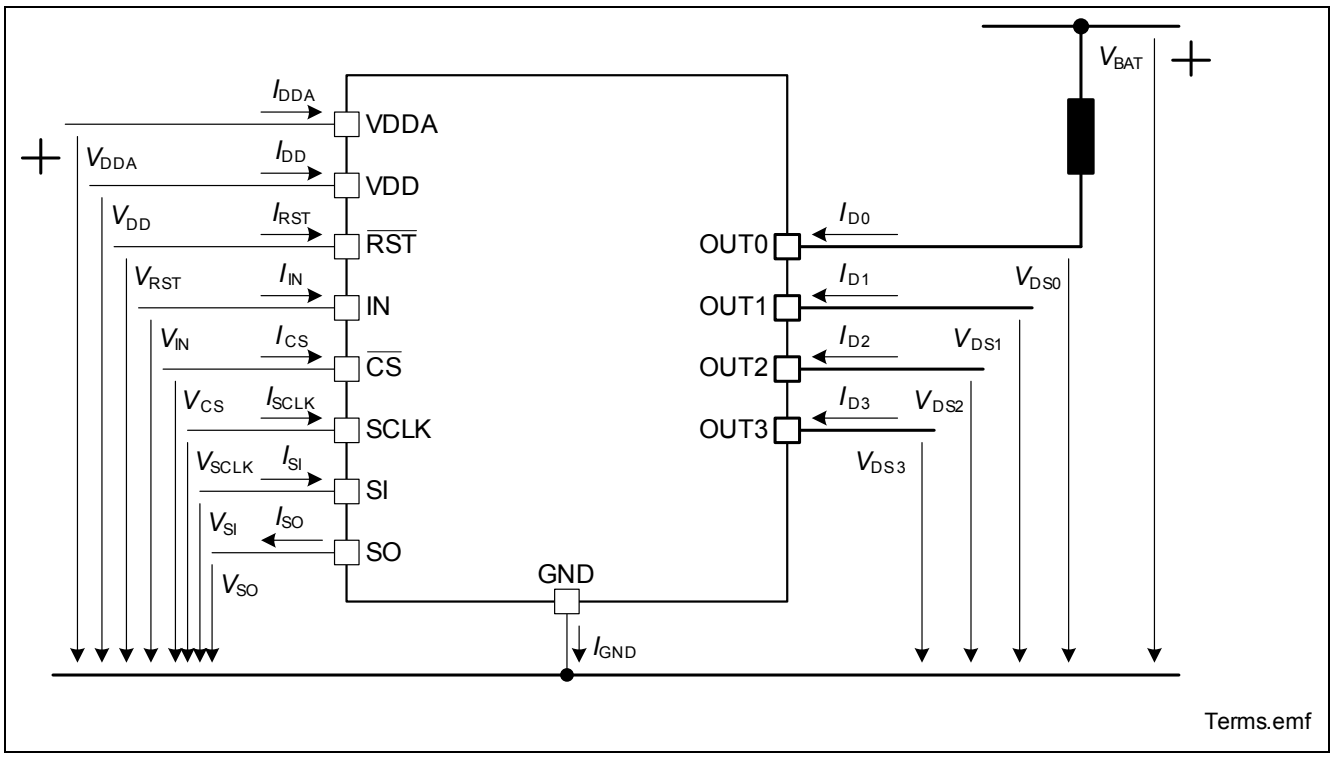


Figure 2 Terms of TLE7231G

In all tables of electrical characteristics is valid: channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS3}).

All SPI register bits are marked as follows: `PARAMETER` (e.g. `IN0`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment

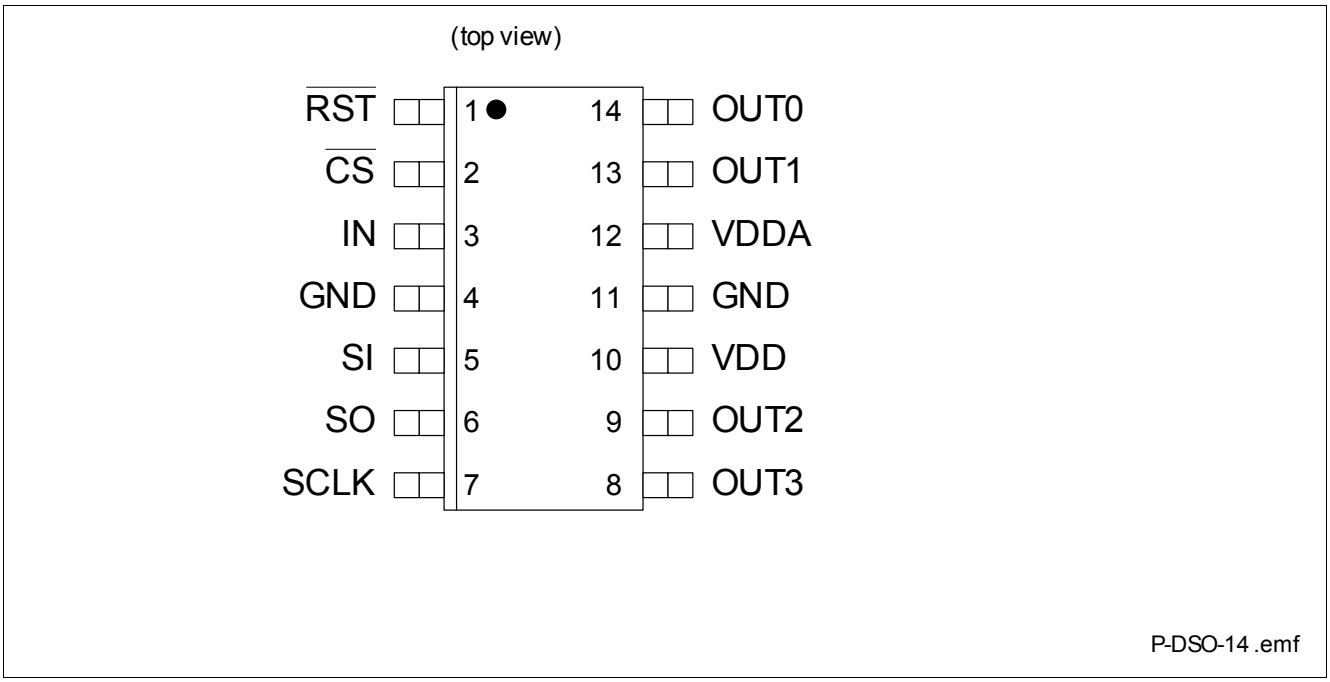


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	I/O [1]		Function
Power Supply				
10	VDD	-		**Digital Supply Voltage;** Connected to 5 V Voltage with Reverse protection Diode and Filter against EMC
12	VDDA	-		**Analog Supply Voltage;** Positive supply voltage for power switches gate control
11,4	GND	-		**Ground;** common ground for digital, analog and power
Power Stages				
14	OUT0	O		**Output Channel 0;** Drain of power transistor channel 0
13	OUT1	O		**Output Channel 1;** Drain of power transistor channel 1
9	OUT2	O		**Output Channel 2;** Drain of power transistor channel 2
8	OUT3	O		**Output Channel 3;** Drain of power transistor channel 3
Inputs				
3	IN	I	PD	**Control Input;** Digital input 3.3 V or 5 V. In case of not used keep open.
1	$\overline{\text{RST}}$	I	PD	**Reset Input Pin;** Digital input 3.3 V or 5 V. Low active
SPI				
2	$\overline{\text{CS}}$	I	PU	**SPI Chip Select;** Digital input 3.3 V or 5 V. Low active
7	SCLK	I	PD	**Serial Clock;** Digital input 3.3 V or 5 V

Pin	Symbol	I/O [1]		Function
5	SI	I	PD	**Serial Data In;** Digital input 3.3 V or 5 V
6	SO	O		**Serial Data Out;** Digital input 3.3 V or 5 V

1) O: Output, I: Input,
PD: pull-down resistor integrated,
PU pull-up resistor integrated

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

T_J = -40 °C to +150 °C; V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V.

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Power Supply						
4.1.1	Digital supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.2	Analog supply voltage	V_{DDA}	-0.3	5.5	V	–
Power Stages						
4.1.3	Load current	I_D	-0.5	0.5	A	–
4.1.4	Output voltage for short circuit protection (single pulse)	V_D	–	36	V	–
4.1.5	Voltage at power transistor	V_{DS}	–	41	V	active clamped
4.1.6	Maximum energy dissipation one channel	E_{AS}			mJ	[2]
	single pulse		–	65		$T_{J(0)}$ = 85 °C $I_{D(0)}$ = 0.35 A
	single pulse		–	30		$T_{J(0)}$ = 150 °C $I_{D(0)}$ = 0.25 A
	repetitive (1 · 10^4 cycles) repetitive (1 · 10^6 cycles)	E_{AR}	– –	18 13		$T_{J(0)}$ = 150 °C $I_{D(0)}$ = 0.25 A $I_{D(0)}$ = 0.17 A
Logic Pins						
4.1.7	Voltage at input pin	V_{IN}	-0.3	5.5	V	–
4.1.8	Voltage at reset pin	V_{RST}	-0.3	V_{DD} + 0.3	V	[3]
4.1.9	Voltage at chip select pin	V_{CS}	-0.3	V_{DD} + 0.3	V	[3]
4.1.10	Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	[3]
4.1.11	Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	[3]
4.1.12	Voltage at serial output pin	V_{SO}	-0.3	V_{DD} + 0.3	V	[3]
Temperatures						
4.1.13	Junction Temperature during operation	T_J	-40	150	°C	–
4.1.14	Dynamic temperature increase while switching	ΔT_J	–	60	°C	–
4.1.15	Storage Temperature	T_{STG}	-55	150	°C	–
ESD Susceptibility						
4.1.16	ESD Resistivity Output Input / SPI	V_{ESD}	 -4 -2	 4 2	kV	HBM[4]

1) Not subject to production test, specified by design.

2) Pulse shape represents inductive switch off: $I_D(t) = I_D(0) \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

3) V_{DD} + 0.3 V < 5.5 V
4) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001-2010

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Digital supply voltage	V_{DD}	3.0	5.5	V	–
4.2.2	Analog supply voltage	V_{DDA}	4.5	5.5	V	–
4.2.3	Digital supply current all channels ON	$I_{DD(ON)}$	–	100	µA	–
4.2.4	Analog supply current all channels ON	$I_{DDA(ON)}$	–	3	mA	–
4.2.5	Analog supply turn-ON time	$t_{DDA(ON)}$	15	–	µs	V_{DDA} = 0 V to 5 V (linear)

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.6	Junction to Solder Point	R_{thJSP}	–	–	39	K/W	pin 4,11[1)]
4.3.7	Junction to Ambient	R_{thJA}	–	70	–	K/W	[1)2)]

1) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_A = 25 °C. Ch0 to Ch3 are dissipating 1 W power (0.25 W each).
2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package PG-DSO-14) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_A = 25 °C, Ch0 to Ch3 are dissipating 1 W power (0.25 W each).

5 Power Supply

The TLE7231G is supplied by two power supply lines V_{DD} and V_{DDA}. The digital power supply line V_{DD} is designed to be functional at a very wide voltage range. The analog power supply V_{DDA} supports 5 V supply.

Power-on reset functions have been implemented for both supply lines. After start-up of the power supply, all SPI registers are reset to their default values and the device remains in idle mode. Capacitors between VDD and GND pins, and VDDA and GND pins are recommended.

A reset pin is available. At low logic level at this pin, all registers are set to their default values and the quiescent supply currents are minimized.

The V_{DD} supply line is used for the I/O buffer circuits of the SPI pins, therefore the voltage on the SO pin is always related to this supply voltage. A capacitor between pins V_{DD} and GND is recommended (especially in case of EMI).

To enable the Daisy chain functionality it is necessary to have V_{DD} and V_{DDA} in the specified functional range.

The device provides a sleep mode to minimize current consumption, which also resets the register banks. It is controlled by a low active reset pin ($\overline{RST}$) which disables the device and minimize the current consumption. The table below gives an overview of the different power modes.

Table 2 Power modes[1)]

Power mode	State Description	RESET (low active)	V_{DD}	V_{DDA}	SCLK	
SLEEP	Device at minimum current consumption	low	X	X	0 Hz	
IDLE	Device operational, all channels OFF no diagnosis activated	high	ON	ON	0 Hz	
ON	Device operational with enabled channels and diagnostic currents active	high	ON	ON	5 MHz (max)	

1) low: pin input is digital low,
high: pin input is digital high,
X: pin state don't care,
ON: voltage on this analog supply pin is in the specified functional range

6 Power Stages

The TLE7231G is a four channel low-side relay switch.

The power stages are made of N-channel vertical power MOSFET transistors.

6.1 Input Circuit

The TLE7231G has an input pin, that can be configured to be used for control of the output stages. The `INn` parameter of the SPI provide the following operation modes:

- channel is in off mode without diagnosis
  (if all channels are programmed to this mode, the device goes into idle mode)
- channel is switched according to signal level at input pin IN
- channel is switched on
- channel is switched off with active diagnosis

Figure 4 shows the input circuit of TLE7231G.

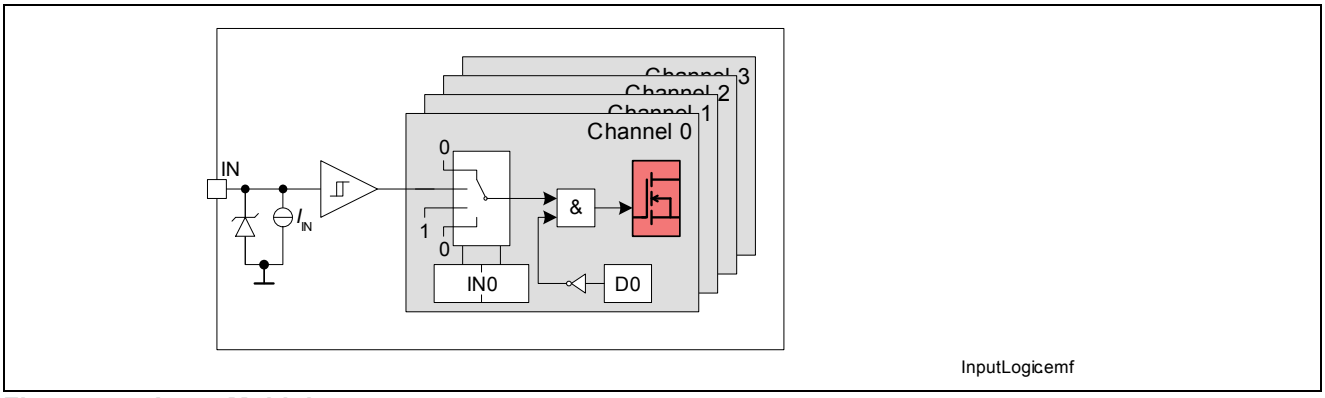


Figure 4 Input Multiplexer

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses. After power-on reset, the device enters idle mode.

6.2 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited.

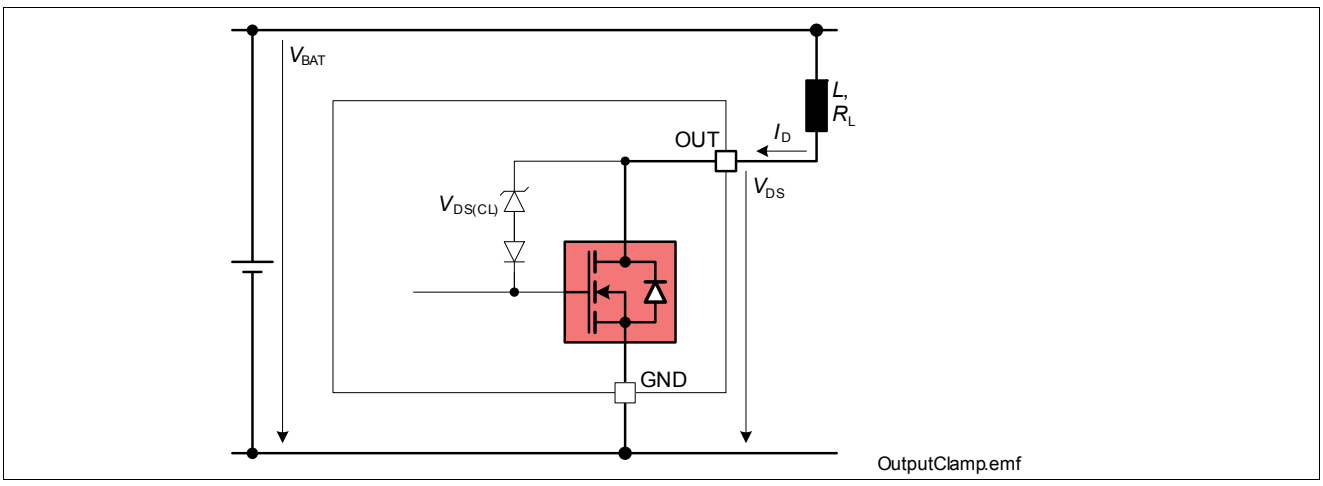


Figure 5 Output Clamp Implementation

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE7231G.

This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{BAT} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_D}{V_{BAT} - V_{DS(CL)}}\right) + I_D \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_D^2 \cdot \left(1 - \frac{V_{BAT}}{V_{BAT} - V_{DS(CL)}}\right)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

6.3 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the `IN` bits of the serial peripheral interface SPI. The switching times t_{ON} and t_{OFF} are designed equally.

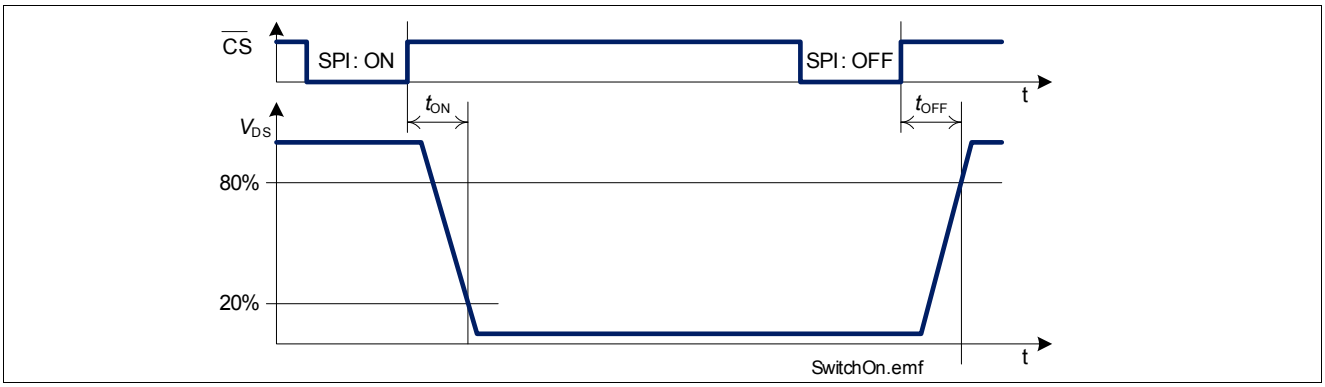


Figure 6 Switching a Resistive Load

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to **Chapter 9.3** for details on operation modes.

The listed switching times are not valid, when switching to or from stand-by mode.

6.4 Electrical Characteristics Power Stages

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
6.4.1	Digital supply voltage	V_{DD}	3.0	–	5.5	V	–
6.4.2	Digital supply current all channels ON	$I_{DD(ON)}$	–	–	100	µA	V_{DD} = V_{DDA} = 5 V V_{RST} = V_{CS} = V_{DD} V_{SCLK} = 0 V V_{IN} = 0 V

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.4.3	Digital supply idle current	$I_{DD(idle)}$	–	–	20	µA	f_{SCLK} = 0 Hz V_{RST} = V_{CS} = high
6.4.4	Digital supply sleep current	$I_{DD(sleep)}$	–	–	 1 2 5	µA	V_{RST} = 0 V T_J = 25 °C [1] T_J = 85 °C [1] T_J = 150 °C
6.4.5	Digital power-on reset threshold voltage	$V_{DD(PO)}$	–	–	3.0	V	–
6.4.6	Analog supply voltage	V_{DDA}	4.5	–	5.5	V	–
6.4.7	Analog supply current all channels ON	$I_{DDA(ON)}$	–	–	3	mA	–
6.4.8	Analog supply idle current	$I_{DDA(idle)}$	–	–	 25 50 100	µA	V_{CS} = V_{DD} V_{SI} = 0 V V_{SCLK} = 0 V T_J = 25 °C [1] T_J = 85 °C [1] T_J = 150 °C
6.4.9	Analog supply sleep current	$I_{DDA(sleep)}$	–	–	 1 3 5	µA	V_{CS} = V_{DD} V_{RST} = 0 V T_J = 25 °C [1] T_J = 85 °C [1] T_J = 150 °C
6.4.10	Analog power-on reset threshold voltage	$V_{DDA(PO)}$	–	–	4.5	V	–
Output Characteristics							
6.4.11	On-State resistance per channel	$R_{DS(ON)}$	–	 1.0 2.0	 2.2	Ω	I_D = 250 mA T_J = 25 °C [1] T_J = 150 °C
6.4.12	Nominal load current	$I_{D(nom)}$	320	340	–	mA	[2]
6.4.13	Output leakage current (per channel)	$I_{D(OFF)}$	–	–	 1 2 5	µA	V_{DS} = 13.5 V T_J = 25 °C [1] T_J = 85 °C [1] T_J = 150 °C
6.4.14	Output clamping voltage	$V_{DS(CL)}$	41	–	54	V	–
Input Pin Characteristics							
6.4.15	L level of pin IN	$V_{IN(L)}$	0	–	0.7	V	–
6.4.16	H level of pin IN	$V_{IN(H)}$	2.0	–	5.5	V	–
6.4.17	L-input pull-down current through pin	$I_{IN(L)}$	3	12	80	µA	V_{DD} = 5 V [1] V_{IN} = 0.6 V

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.4.18	H-input pull-down current through pin	$I_{IN(H)}$	10	40	80	µA	V_{DD} = 5 V V_{IN} = 5 V
6.4.19	L level of pin RST	$V_{RST(L)}$	0	–	0.2* V_{DD}		–
6.4.20	H level of pin RST	$V_{RST(H)}$	0.4* V_{DD}	–	V_{DD}		–
6.4.21	L-input pull-down current through pin RST	$I_{RST(L)}$	3	12	80	µA	V_{DD} = 5 V 1) V_{RST} = 0.6 V
6.4.22	H-input pull-down current through pin RST	$I_{RST(H)}$	10	40	80	µA	V_{DD} = 5 V V_{RST} = 5 V
Timings							
6.4.23	Sleep wake-up time	$t_{wu(sleep)}$	–	–	200	µs	–
6.4.24	Reset duration	$t_{RST(L)}$	1	–	–	µs	–
6.4.25	Turn-on time V_{DS} = 20% V_{BAT}	t_{ON}	5	–	60	µs	V_{BAT} = 13.5 V I_D = 250 mA, resistive load
6.4.26	Turn-off time V_{DS} = 80% V_{BAT}	t_{OFF}	10	–	60	µs	V_{BAT} = 13.5 V I_D = 250 mA, resistive load

1) Not subject to production test, specified by design

2) calculated value based on following parameters:
all channels on with equal load current, $R_{DS(ON)} = R_{DS(ON,150°C)}$, T_a = 85 °C, $T_{J,max}$ = 150 °C, $R_{th} = R_{thJA(typ)}$

7 Protection Functions

Note: The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

7.1 Over Load Protection

The TLE7231G is protected against over load or short circuit of the load. After time $t_{OFF(OVL)}$, the over loaded channel n switches off and therefore the corresponding diagnostics flag Dn is set. The channel can be switched on after clearing the diagnostics flag as described in chapter 8. Please refer to **Figure 7** for details.

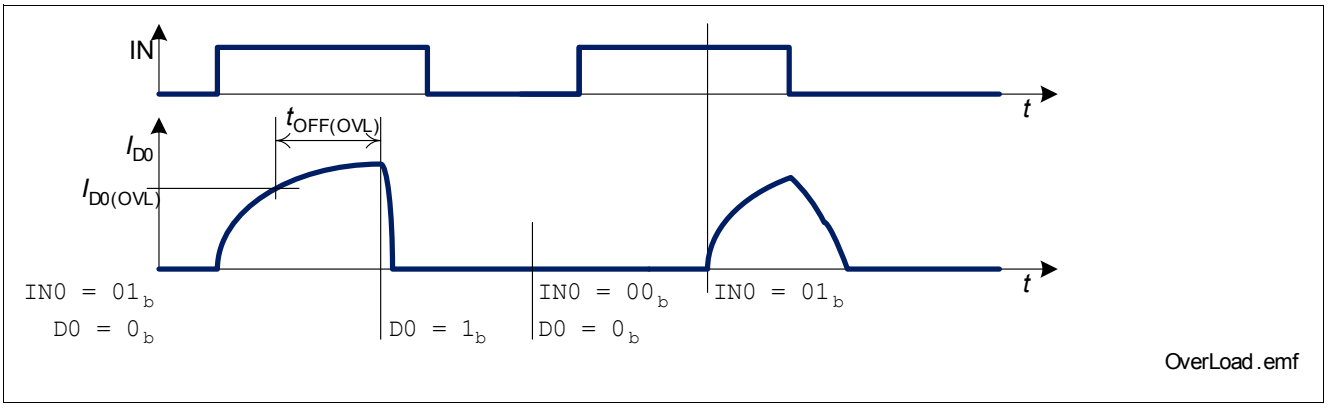


Figure 7 Shut Down at Over Load

7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel n to switch off to prevent destruction. Then the according diagnostics flag Dn is set. The channel can be switched on after clearing the diagnosis flag and a junction temperature decrease of ΔT_J. Please refer to **Chapter 8** for information on diagnostics features.

7.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power transistor causes increased power dissipation. The reverse current through the intrinsic body diode of the power transistor has to be limited by the connected load. The V_{DD} and V_{DDA} supply pins must be externally protected against reverse polarity. The over temperature and over load protection are not active during reverse polarity.

7.4 Electrical Characteristics Protection

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Over Load Protection							
7.4.1	Over load detection current	$I_{D(OVL)}$	0.5	–	0.95	A	–
7.4.2	Over load shut-down delay time	$t_{OFF(OVL)}$	5	–	60	µs	–
Over Temperature Protection							
7.4.3	Thermal shut down temperature	$T_{J(SC)}$	150	170[1)]	–	°C	–
7.4.4	Thermal hysteresis	ΔT_J	–	10	–	K	[1)]

1) Not subject to production test, specified by design

8 Diagnostic Features

The SPI of TLE7231G provides diagnosis information about the device and about the load. The diagnosis information of the protective functions of channel n is latched in the diagnosis flag Dn. The open load diagnosis of channel n is latched in the diagnosis flag OLn. Both flags are cleared by INn = 00_B and the diagnosis current $I_{D(PD)}$, which is a small pull down current, is disabled.

Following table shows possible failure modes and the according protective and diagnostic action.

Failure Mode	Comment
Open Load or short circuit to GND	**Diagnosis, when channel n is switched on:** INn = 01_B: if input pin is high: none INn = 10_B: none **Diagnosis, when channel n is switched off:** INn = 00_B: none, diagnosis flags are cleared and the diagnosis current is switched off INn = 01_B: if input pin is low, according to voltage at the output pin, the flag OLn is set after time $t_{d(OL)}$ INn = 11_B: according to voltage level at the output pin, flags OLn are set after time $t_{d(OL)}$
Over temperature	When over temperature occurs, the affected channel n is switched off. The according diagnosis flag Dn is set. The diagnosis flags are latched until they have been cleared by INn = 00_B. The over temperature detection is active in ON-state as well as OFF-state.
Over Load (Short Circuit)	When over load is detected at channel n, the affected channel is switched off after time $t_{OFF(OVL)}$ and the dedicated diagnosis flag Dn is set. The diagnosis flags are latched until they have been cleared by INn = 00_B.

8.1 Open Load Diagnosis timing

The TLE7231G offers a open load diagnosis for each channel in OFF mode.

The time $t_{d(OL)}$ is applied to filter short time events.

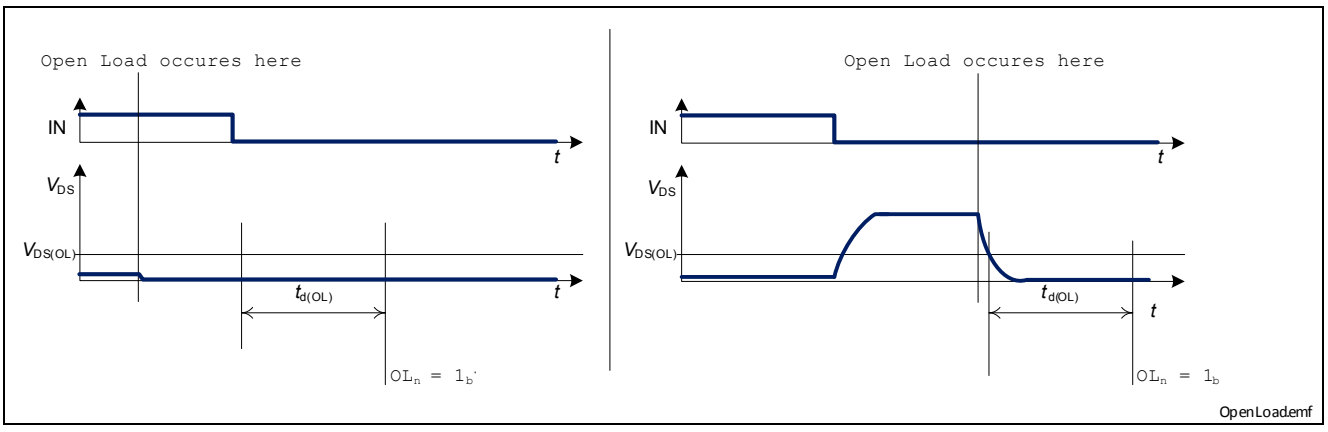


Figure 8 Open Load timing

8.2 Electrical Characteristics Diagnostic

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
OFF State Diagnosis							
8.2.1	Open load detection threshold voltage	$V_{DS(OL)}$	1.0	–	2.5	V	–
8.2.2	Output pull-down diagnosis current per channel	$I_{D(PD)}$	30	–	100	µA	V_{DS} = 13.5 V
8.2.3	Open load diagnosis delay time	$t_{d(OL)}$	30	–	200	µs	–
ON State Diagnosis							
8.2.4	Over load detection current	$I_{D(OVL)}$	0.5	–	0.95	A	–
8.2.5	Over load detection delay time	$t_{OFF(OVL)}$	5	–	60	µs	–

9 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred. The interface provides daisy chain capability.

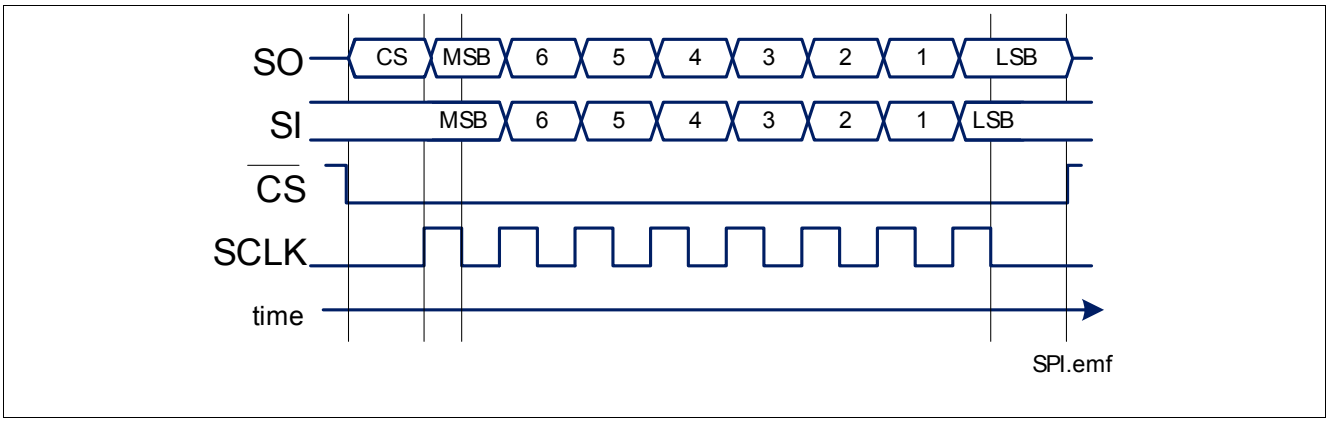


Figure 9 Serial Peripheral Interface

The SPI protocol is described in **Chapter 9.3**. It is reset to the default values after power-on reset.

9.1 SPI Signal Description

$\overline{CS}$ - Chip Select:

The system micro controller selects the TLE7231G by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition: ⎺_

- The diagnosis information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. The transmission error flag is set after any kind of reset, so a reset between two SPI commands is indicated. For details, please refer to **Figure 10**. This information stays available to the first rising edge of SCLK.

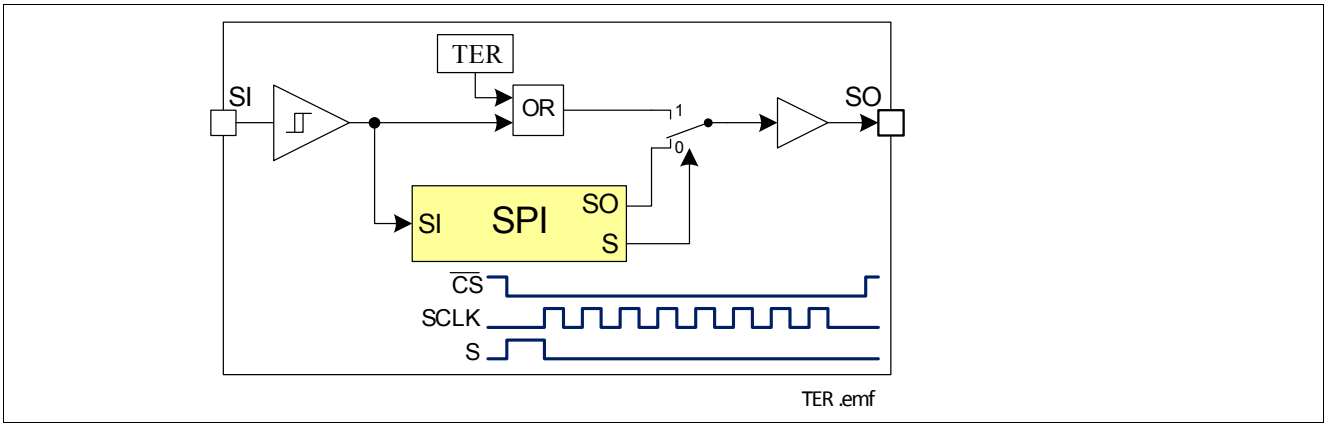


Figure 10 Transmission Error Flag on SO Line

$\overline{CS}$ Low to High transition:

Data from shift register is transferred into the input matrix register only, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input:

Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. Please refer to **Chapter 9.3** for further information.

SO - Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Chapter 9.3** for further information.

9.2 Daisy Chain Capability

The SPI of TLE7231G provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 11**), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

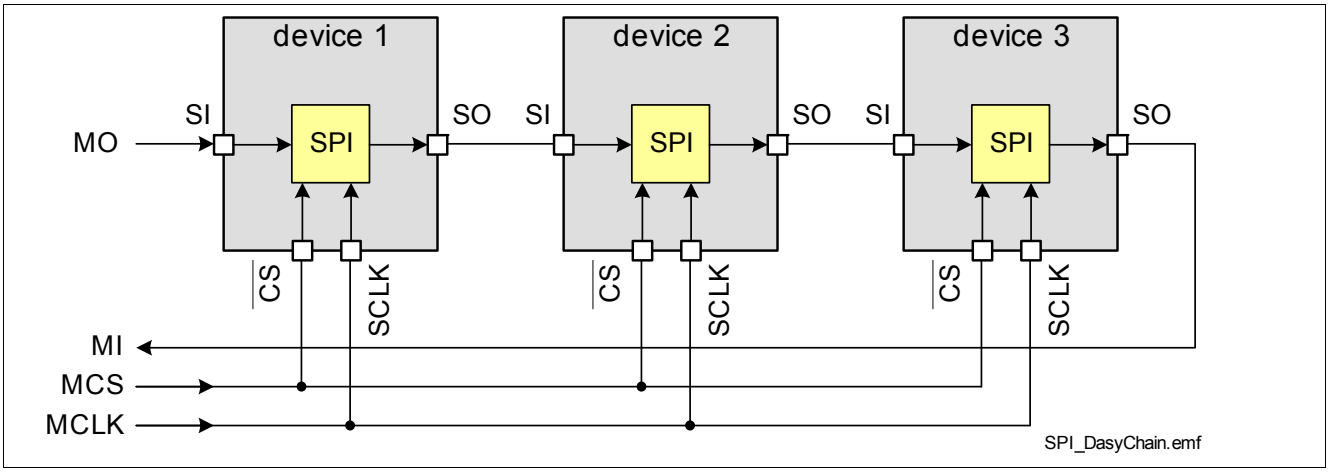


Figure 11 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 8 SCLK cycles, the data transfer for one device has been finished. In single chip configuration, the $\overline{CS}$ line must transit from low to high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using three devices in daisy chain, three times 8 bits have to be shifted through the devices. After that, the $\overline{MCS}$ line must transit from low to high (see **Figure 12**).

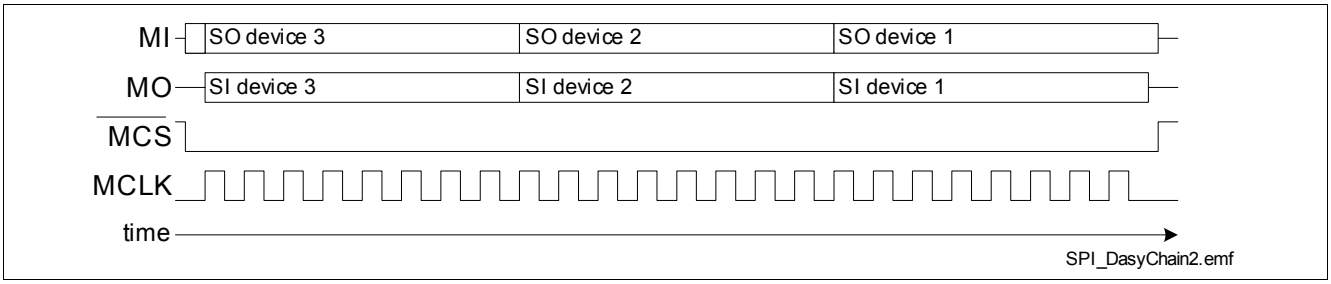


Figure 12 Data Transfer in Daisy Chain Configuration

9.3 SPI Protocol

The SPI protocol of the TLE7231G provides two registers. The input register and the diagnosis register. The diagnosis register contains four pairs of diagnosis flags, the input register contains the input multiplexer configuration. After power-on reset, all register bits are cleared to 0.

SI

7	6	5	4	3	2	1	0
IN3		**IN2**		**IN1**		**IN0**	

Field	Bits	Type	Description
INn (n = 3-0)	7:6, 5:4, 3:2, 1:0	W	Input Register Channel n **00_B** Idle Mode: Fast channel switched off. Diagnosis flags are cleared. Diagnosis current is disabled. 01_B Input Direct drive Mode: Channel is switched according to signal at input pin. Diagnosis current is enabled in OFF-state. 10_B ON Mode: Channel is switched on. Diagnosis current is enabled. 11_B OFF Mode: Channel is switched off. Diagnosis current is enabled.

SO **Reset Value: 100_H**

CS[1)]	7	6	5	4	3	2	1	0
TER	**OL3**	**D3**	**OL2**	**D2**	**OL1**	**D1**	**OL0**	**D0**

1) This bit is valid between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Field	Bits	Type	Description
TER	CS	R	**Transmission Error** 0 Previous transmission was successful (modulo 8 clocks received). **1** Previous transmission failed or first transmission after reset.
OLn (n = 3-0)	7, 5, 3, 1	R	**Open Load Flag of channel n** **0** Normal operation. 1 Open load has occurred in OFF state.
Dn (n = 3-0)	6, 4, 2, 0	R	**Diagnosis Flag of channel n** **0** Normal operation. 1 Over load or over temperature switch off has occurred in ON state.

9.4 Timing Diagrams

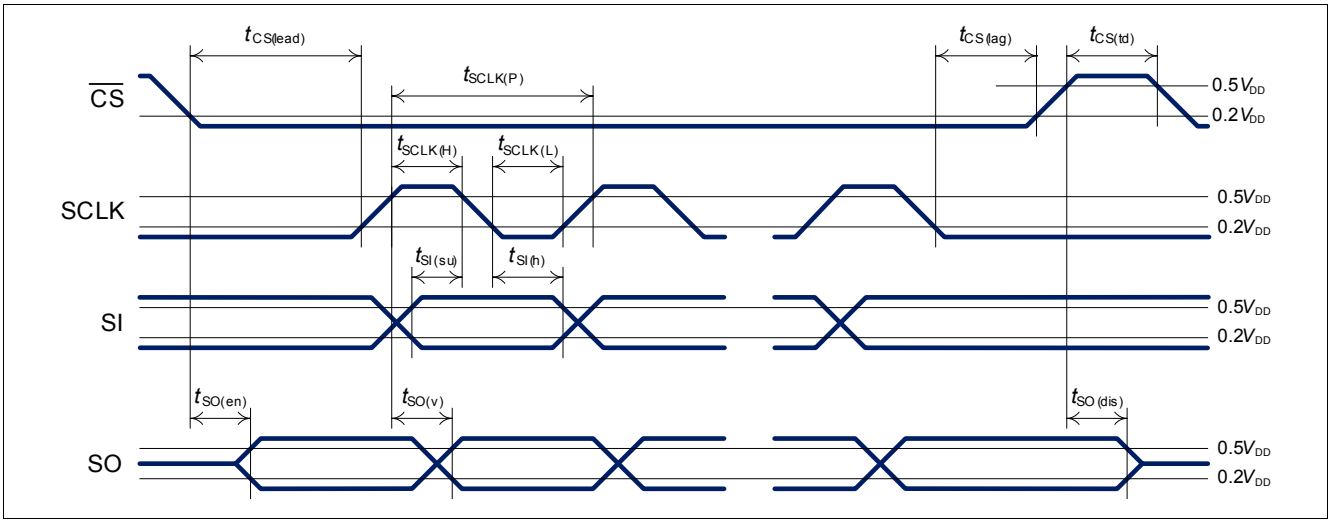


Figure 13 Timing Diagram

9.5 Electrical Characteristics SPI

V_{DD} = 3.0 V to V_{DDA}, V_{DDA} = 4.5 V to 5.5 V, T_J = -40 °C to +150 °C
All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)
typical values: V_{DD} = 5.0 V, V_{DDA} = 5.0 V, T_J = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
9.5.1	L level of pin $\overline{CS}$ SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	–	0.2* V_{DD}		–
9.5.2	H level of pin $\overline{CS}$ SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	0.5*V_{DD}	–	V_{DD}		–
9.5.3	L-input pull-up current through $\overline{CS}$	$I_{CS(L)}$	5	17	40	µA	V_{CS} = 0 V
9.5.4	H-input pull-up current through $\overline{CS}$	$I_{CS(H)}$	3	15	40	µA	[1] V_{CS} = 2 V
9.5.5	L-input pull-down current through pin SCLK SI	 $I_{SCLK(L)}$ $I_{SI(L)}$	3	12	80	µA	[1] V_{SCLK} = 0.6 V V_{SI} = 0.6 V
9.5.6	H-input pull-down current through pin SCLK SI	 $I_{SCLK(H)}$ $I_{SI(H)}$	10	40	80	µA	 V_{SCLK} = 5 V V_{SI} = 5 V
Output Characteristics (SO)							
9.5.7	L level output voltage	$V_{SO(L)}$	0	–	0.4	V	I_{SO} = -2 mA
9.5.8	H level output voltage	$V_{SO(H)}$	V_{DD}- 0.5 V	–	V_{DD}		I_{SO} = 1.5 mA
9.5.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
9.5.10	Serial clock frequency	f_{SCLK}	0	–	5	MHz	–
9.5.11	Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	–
9.5.12	Serial clock high time	$t_{SCLK(H)}$	50	–	–	ns	–
9.5.13	Serial clock low time	$t_{SCLK(L)}$	50	–	–	ns	–
9.5.14	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	250	–	–	ns	–
9.5.15	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	250	–	–	ns	–
9.5.16	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	250	–	–	ns	–
9.5.17	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	–