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SPIDER - TLE7236G

8 Channel High-Side and Low-Side Relay Switch with Limp Home Mode and Cranking

Automotive Power

Table of Contents

SPI Driver for Enhanced Relay Control **TLE7236G**

1 Overview

PG-DSO-20-45

Features

- 8 bit SPI for diagnostics and control, providing daisy chain capability
- Very wide range for digital supply voltage
- Two configurable input pins offer complete flexibility for PWM operation
- Stable behavior at under voltage
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7236G is an eight channel high-side and low-side power switch in PG-DSO-20-45 package providing embedded protective functions. It is especially designed for standard relays and LEDs in automotive applications.

The output stages incorporate two low-side, four high-side and two auto configuring high-side or low-side switches.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the load. For direct control, there are two input pins available.

The TLE7236G provides a micro controller fail-safe function which is activated via a high signal at the limp home input pin. There is a power supply integrated in the device to ensure this functionality even without digital supply voltage.

The integrated power supply is designed to fulfill cranking mode requirements.

The power transistors are built by N-channel power MOSFETs. The device is monolithically integrated in Smart Power Technology.

Type	Package	Marking
TLE7236G	PG-DSO-20-45	TLE7236G

Table 1 Product Summary

Operating range power supply voltage	V_{bb}	4.0 … 28 V
Digital supply voltage	V_{DD}	3.0 … 5.5 V
Typical On-State resistance at 25 °C	$R_{DS(ON)}$	
high-side: 2 channels (Relay)		0.85 Ω
high-side: 2 channels (Generic, LED)		1.6 Ω
auto configuring: 2 channels (Relay, Supplies)		0.85 Ω
low-side: 2 channels (Relay)		0.85 Ω
Nominal load current (all channels active)	$I_{L(nom, min)}$	
Relay		280 mA
LED, Generic		140 mA
Over load switch off threshold	$I_{DS(OVL, min)}$	500 mA
Output leakage current per channel at 25 °C	$I_{DS(OFF, max)}$	1 µA
Drain to source clamping voltage	$V_{DS(CL, min)}$	41 V
Source to ground clamping voltage	$V_{bb(CL, max)}$	-16 V
SPI clock frequency	$f_{SCLK(max)}$	5 MHz

Protective Functions

- Over load and short circuit protection
- Thermal shutdown
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Latched diagnostic information via SPI
- Open load detection in OFF-state
- Over load detection in ON-state
- Over temperature

Crank Mode

- Integrated power supply enables secure operation at low battery voltage

Limp Home / Fail-Safe Functions

- Limp home activation via pin LHI
- Limp home configuration via input pins

Applications

- Especially designed for driving relays and LEDs in automotive applications
- All types of resistive and inductive loads
- Suitable to switch 5 V power supply lines by auto configuring channels

Detailed Description

The TLE7236G is an eight channel high-side and low-side relay switch providing embedded protective functions. The output stages incorporate two low-side switches (0.85 Ω per channel), four high-side switches (two channels with 0.85 Ω and two channels with 1.6 Ω) and two auto-configuring high-side or low-side switches (0.85 Ω per channel). The auto-configuring switches can be utilized in high-side or low-side configuration just by connecting the load accordingly. They are also suitable to switch a 5 V supply line in high-side configuration. Protective and diagnostic functions adjust automatically to the chosen configuration.

The 8 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices in one SPI chain by using the same number of micro-controller pins.

The outstanding feature of this octal relay switch enables the output channels to keep their state at low battery voltage. This is realized by an integrated power supply, especially designed to fulfill cranking mode requirements (Vbb = 4 V) independent from digital power supply (V_{DD}). The SPI functionality is given only when the digital power supply is available.

Furthermore, the TLE7236G is equipped with two input pins that can be individually routed to the output control of each channel thus offering complete flexibility in design and PCB-layout. The input multiplexer is controlled via SPI.

In limp home mode (fail-safe mode), the input pins are directly routed to the configurable output channels 4 and 5. The limp home mode operates independently of digital power supply and is activated via pin LHI.

The device provides full diagnosis of the load via open load, over load and short circuit detection. SPI diagnosis flags indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. There are temperature sensors available for each channel to protect the device against over temperature.

The device protects itself with a build in reverse polarity protection which prohibits intrinsic current flow through the logic during reverse polarity. However the output stages still incorporate a reverse diode where current can flow through during reverse polarity.

The power transistors are built by N-channel power MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

2 Block Diagram

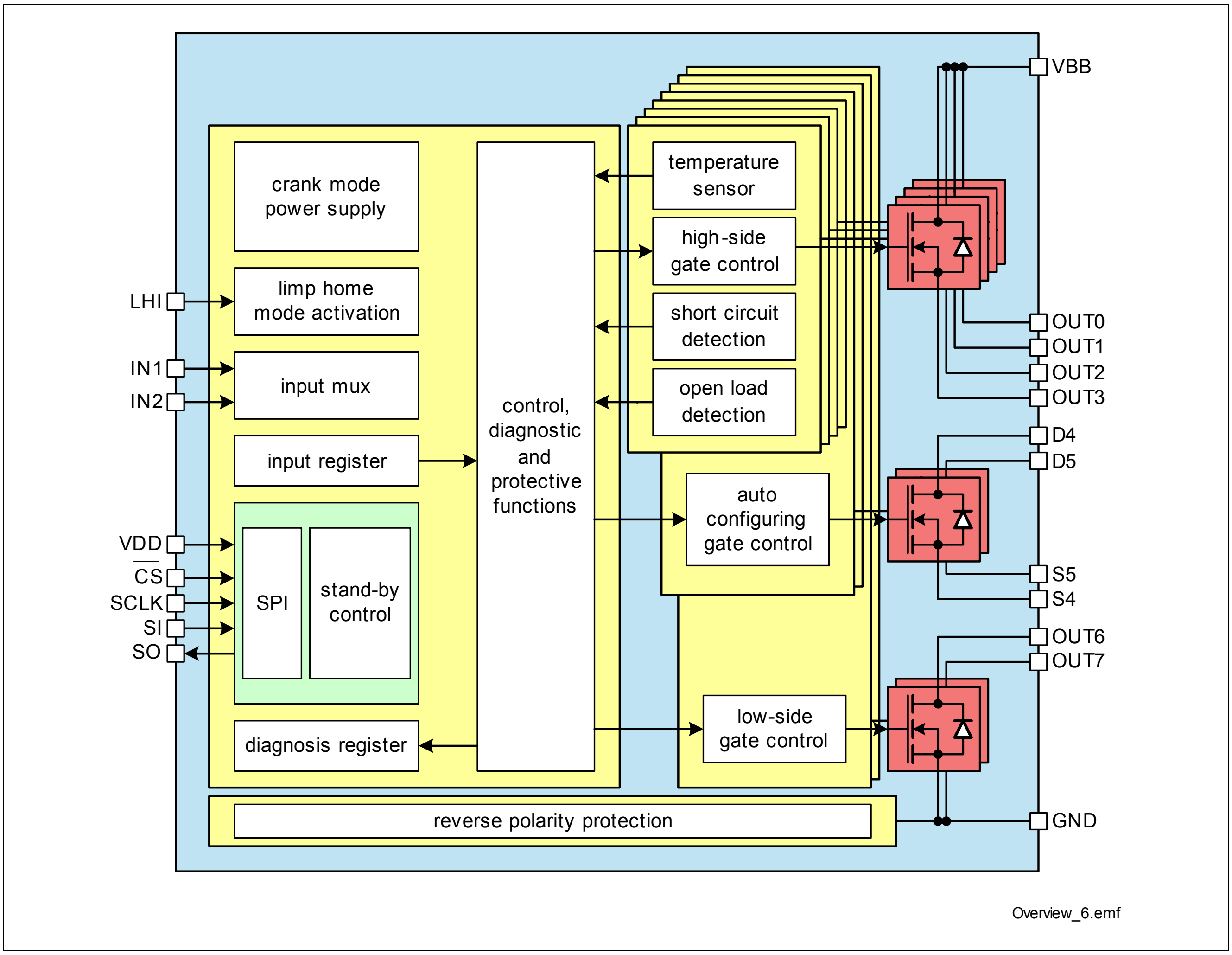

Figure 1 Block Diagram

2.1 Terms

Figure 2 shows all terms used in this data sheet.

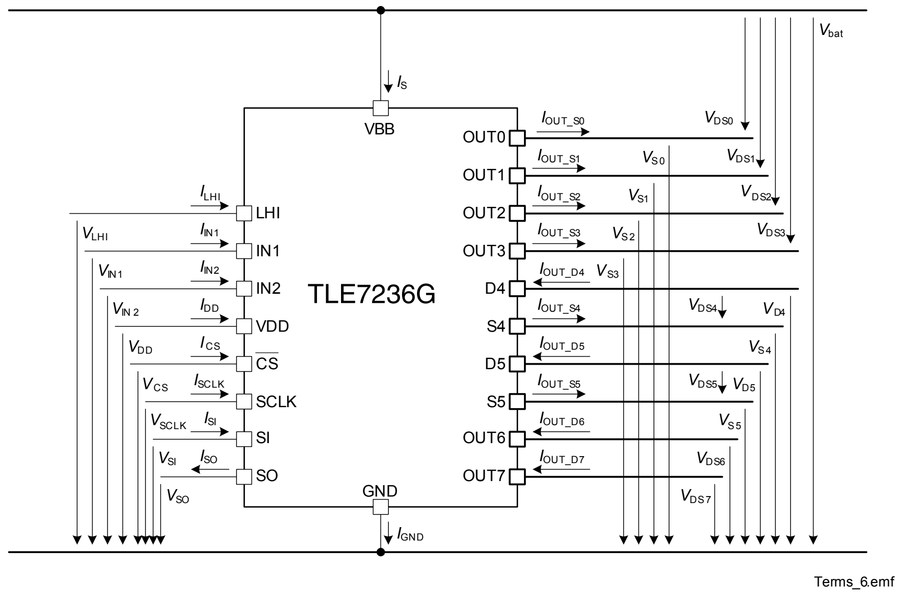

Figure 2 Terms

In all tables of the electrical characteristics is valid:

Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS7}). In order to make the description of output currents easier, the load current I_{Out} is equivalent to the drain current I_{OUT_D} in low-side configuration and the source current I_{OUT_S} in high-side configuration.

All SPI register bits are marked as follows: `ADDR.PARAMETER (e.g. ICR01.INX1)`. In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment

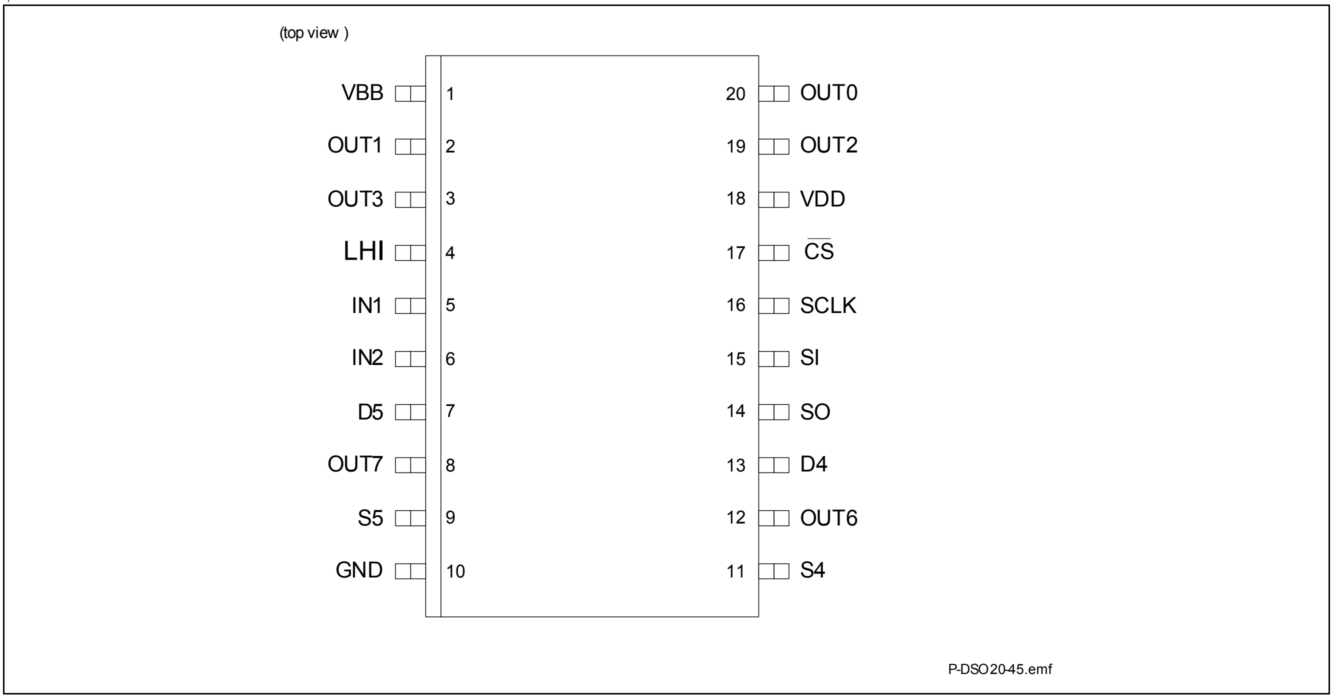

Figure 3 Pin Configuration PG-DSO20-45

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply			
18	VDD	-	Digital power supply
1	VBB	-	Power supply
10	GND	-	Digital, analog and power ground
Power Stages			
20	OUT0	O	Source of high side power transistor channel 0
2	OUT1	O	Source of high side power transistor channel 1
19	OUT2	O	Source of high side power transistor channel 2
3	OUT3	O	Source of high side power transistor channel 3
13	D4	O	Drain of auto configuring power transistor 4
11	S4	O	Source of auto configuring power transistor 4
7	D5	O	Drain of auto configuring power transistor 5
9	S5	O	Source of auto configuring power transistor 5
12	OUT6	O	Drain of low side power transistor channel 6
8	OUT7	O	Drain of low side power transistor channel 7
Inputs			
4	LHI	I	Limp home activation input pin (pull down)

Pin	Symbol	I/O	Function
5	IN1	I	Input multiplexer input 1 pin (pull down)
6	IN2	I	Input multiplexer input 2 pin (pull down)
SPI			
17	$\overline{CS}$	I	SPI Chip select (pull up)
16	SCLK	I	Serial clock
15	SI	I	Serial data in
14	SO	O	Serial data out

4 Electrical Characteristics

4.1 Absolute Maximum Ratings [1)]

Stresses above the ones listed here may affect device reliability or may cause permanent damage to the device. The values below are not considering combinations of different maximum conditions at one time

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Absolute Maximum Ratings[1)]

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
Power Supply						
4.1.1	Power supply voltage	V_{bb}	-16	40	V	-16V max. 2 minutes
4.1.2	Digital supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Power supply voltage for full short circuit protection (single pulse) (T_j = -40 °C … 150 °C)	$V_{bat(SC)}$	0	28	V	–
Power Stages						
4.1.4	Load current	I_L			A	–
	channel 0, 1, 4, 5, 6, 7		-0.5	0.5		
	channel 2, 3		-0.25	0.25		
4.1.5	Voltage at power transistor	V_{DS}	–	41	V	–
4.1.6	Power transistor's source voltage	V_{Out_S}	-16	–	V	–
4.1.7	Power transistor's drain voltage	V_{Out_D}	–	41	V	–
4.1.8	Max. energy dissipation one channel single pulse for ch. 0, 1, 4, 5, 6, 7	E_{AS}			mJ	2)
			–	65		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.35 A
			–	50		$T_{j(0)}$ = 150 °C $I_{D(0)}$= 0.250 A
4.1.9	Maximum energy dissipation one channel repetitive pulses for ch. 0, 1, 4, 5, 6, 7	E_{AR}			mJ	2)
	$1 \cdot 10^4$ cycles		–	18		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.250 A
	$1 \cdot 10^6$ cycles		–	13		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.220 A
4.1.10	Max. energy dissipation one channel single pulse for ch. 2,3	E_{AS}			mJ	2)
			–	50		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.250 A
			–	30		$T_{j(0)}$ = 150 °C $I_{D(0)}$= 0.250 A

1) not subject to production test

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Absolute Maximum Ratings[1)]

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions
			min.	max.		
4.1.11	Maximum energy dissipation one channel repetitive pulses for ch. 2,3	E_{AR}			mJ	2)
	$1 \cdot 10^4$ cycles		–	12		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.180 A
	$1 \cdot 10^6$ cycles		–	11		$T_{j(0)}$ = 105 °C $I_{D(0)}$ = 0.180 A
Logic Pins						
4.1.12	Voltage at input pins	V_{IN}	-0.3	V_{DD} + 0.3	V	3)
4.1.13	Voltage at LHI pin	V_{LHI}	-0.3	5.5	V	–
4.1.14	Voltage at chip select pin	V_{CS}	-0.3	V_{DD} + 0.3	V	3)
4.1.15	Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	3)
4.1.16	Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	3)
4.1.17	Voltage at serial output pin	V_{SO}	-0.3	V_{DD} + 0.3	V	3)
Temperatures						
4.1.18	Junction Temperature	T_j	-40	150	°C	–
4.1.19	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.20	ESD susceptibility on all pins	V_{ESD}	-2	2	kV	HBM[4)]

1) not subject to production test
2) Pulse shape represents inductive switch off: $I_L(t) = I_L(0) * (1 - t / t_{pulse})$; $0 < t < t_{pulse}$
3) V_{DD} + 0.3 V < 5.5 V
4) ESD susceptibility, HBM according to EIA/JESD 22-A114

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range for Nominal Operation	$V_{bb(nom)}$	9	16	V	–
4.2.2	upper Supply Voltage Range for Extended Operation	$V_{bb(ext),up}$	16	28	V	Parameter Deviations possible
4.2.3	lower Supply Voltage Range for Extended Operation	$V_{bb(ext),low}$	4	9	V	Parameter Deviations possible
4.2.4	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Thermal Resistance[1)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case, bottom	$R_{thJC,back}$	–	–	25	K/W	2)
4.3.2	Junction to Case, top	$R_{thJC,top}$	–	–	30	K/W	2)
4.3.3	Junction to Pin (5,6,15 or 16)	R_{thJPin}	–	–	23	K/W	2)
4.3.4	Junction to Ambient (1s0p, min. footprint)	$R_{thJA,min}$	–	80	–	K/W	3)
4.3.5	Junction to Ambient (1s0p+300mm^{2}Cu)	$R_{thJA,300}$	–	65	–	K/W	4)
4.3.6	Junction to Ambient (1s0p+600mm^{2}Cu)	$R_{thJA,600}$	–	60	–	K/W	5)
4.3.7	Junction to Ambient (2s2p)	$R_{thJA,2s2p}$	–	52	–	K/W	6)

1) Not subject to production test
2) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_a = 85 °C. Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
3) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with minimal footprint copper area and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
4) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 300mm^2 and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
5) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).
6) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_a = 85 °C, Ch1 to Ch8 are dissipating 1 W power (0.125 W each).

5 Power Supply

The TLE7236G is supplied by two supply voltages V_{bb} and V_{DD}. The V_{bb} supply line is connected to a battery feed and used by the power switches and by an integrated power supply for the register banks. The internal power supply is designed to hold the state of the power switches including the configuration stored in the control register bank during cranking down to 4V. There is an under voltage reset function implemented for the V_{bb} power supply. After start-up of the power supply, all SPI registers are reset to their default values and the device is in sleep mode (standby). The SPI command CMD.WAKE = 1 is switching the device to operation mode (ON), while a command CMD.STB = 1 send the device to sleep mode (standby) again.

The V_{DD} supply line is used by the SPI shift register related circuitry and for driving the SO line. As a result, the daisy chain function is available as soon as V_{DD} is provided in the specified range independent of V_{bb}. A capacitor between pins V_{DD} and GND is recommended (especially in case of EMI).

5.1 Operation Modes

There is a limp home functionality implemented in the TLE7236G, which is activated via pin LHI. Please refer to **Section 5.2** for details.

The device provides a sleep mode (stand by) to minimize current consumption, which also resets the register banks. It is entered and left by dedicated SPI commands . The sleep mode current is minimized only when limp home is inactive. After limp home, the device enters sleep mode automatically.

The internal power supply is designed for low voltage cranking condition down to V_{bb} = 4 V. During cranking, the output channels keep their state as before configured via SPI independent of V_{DD} supply voltage. If V_{DD} = 0 V the SPI can not be used as the output and input levels refer to V_{DD}, but the device keep the current state until either the limp home mode is triggered or the V_{DD} voltages comes back and therefore the SPI Interface works again.

The following table shows the operation modes depending on V_{bb}, V_{DD} and the limp home input signal LHI.

Operation Modes

VBB	0 V	0 V	0 V	4 V	4 V	4 V	12 V	12 V	12 V	12 V
VDD	0 V	5 V	5 V	0 V	0 V	3 V	0 V	0 V	5 V	5 V
LHI	X	0 V	5 V	0 V	4 V	0 V	0 V	5 V	0 V	5 V
Switches operating	-	-	-	✓	✓	✓	✓	✓	✓	✓
Limp Home	-	-	-	-	✓	-	-	✓	-	✓
SPI & daisy-chain	-	✓	✓	-	-	✓	-	-	✓	✓
Register Banks	reset	reset	reset	✓	reset	✓	✓	reset	✓	reset
Diagnostic functions	-	-	-	-	-	-	✓	-	✓	-

5.2 Limp Home Mode

The TLE7236G offers the capability of driving dedicated channels during fail-safe operation of the system. This limp home mode is activated by a high signal at pin LHI. In limp home mode, the SPI registers are reset and the input pins are directly routed to the auto configuring channels (channel 4 and 5). As a result, the limp home operation can be chosen for high-side and low-side driven loads.

Due to the integrated power supply, limp home operation is independent of digital power supply V_{DD}. In case of stand-by, a high signal at pin LHI will wake up the device. After limp home operation, the device enters sleep mode in any case.

5.3 Reset

There are several reset trigger implemented in the device. A reset switches off all channels and sets the registers to default values. After any kind of reset, the transmission error flag (TER) is set.

Under Voltage Reset:

During this device condition a read on SPI always delivers the Standard Diagnostic Frame with a TER flag. This under voltage reset is released when all the supply voltages levels are above under voltage threshold.

Reset Command: There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `CMD.RST` = 1, a reset is triggered.

Limp Home Mode: In limp home mode, the SPI write-registers are reset. The SPI interface is operating normally, so the limp home bit LHI as well as the diagnosis flags can be read, but no command is accepted until the device leaves the Limp home operation.

5.4 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Power Supply V_{bb}							
5.4.1	Supply voltage for full operation	V_{bb}	9	–	28	V	
5.4.2	Supply voltage for restricted operation (no open load currents and detection)	V_{bb}	4	–	9	V	R_L = 80 Ω V_{DS} < 1.5 V
5.4.3	Under voltage reset threshold voltage	$V_{bb(UV)}$	–	–	4	V	
5.4.4	Operating current	I_S	–	–	15	mA	V_{bb} = 16 V
			–	–	12	mA	1) V_{bb} = 16 V all diagnosis off
5.4.5	Sleep mode current with disconnected loads (stand by)	$I_{S(Sleep)}$	–	–	10	µA	V_{bb} = 16 V V_{LHI} = 0 V AWK= 0 T_j = 25 °C 1)
			–	–	13		T_j = 85 °C 1)
			–	–	20		T_j = 150 °C
Digital Power Supply V_{DD}							
5.4.6	Logic supply voltage	V_{DD}	3.0	–	5.5	V	
5.4.7	Under voltage reset threshold voltage	$V_{DD(PO)}$	–	–	3.0	V	
5.4.8	Logic supply current	I_{DD}	–	–	0.2	mA	f_{SCLK} = 0 Hz V_{CS} = 0 V AWK= 1 V_{CS} = 0V
5.4.9	Logic supply sleep mode current	$I_{DD(Sleep)}$	–	–	20	µA	V_{CS} = V_{DD} AWK = 0 T_j = 25 °C 1)
			–	–	20		T_j = 85 °C 1)
			–	–	40		T_j = 150 °C
Timings							
5.4.10	Sleep mode wake-up time	$t_{wu(Sleep)}$	–	–	200	µs	1)
5.4.11	V_{bb} under voltage reset delay time	$t_{bb(UVR)}$	–	–	1	µs	1)
5.4.12	V_{DD} under voltage reset delay time	$t_{DD(UVR)}$	–	–	1	µs	1)

1) Not subject to production test, specified by design.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected at V_{bb} = 13.5 V, V_{DD} = 5.0 V, T_j = 25 °C.

6 Power Stages

The TLE7236G is an eight channel high-side and low-side relay switch. The power stages are built by N-channel vertical power MOSFET transistors. The gates of the high-side switches are controlled by charge pumps.

6.1 Input Circuit

There are two input pins available at TLE7236G, which can be configured to be used for control of the output stages. The INXn parameter of the input configuration register provide following possibilities:

- channel is switched off
- channel is switched according to signal level at input pin IN1
- channel is switched according to signal level at input pin IN2
- channel is switched on

Figure 4 shows the input circuit of TLE7236G.

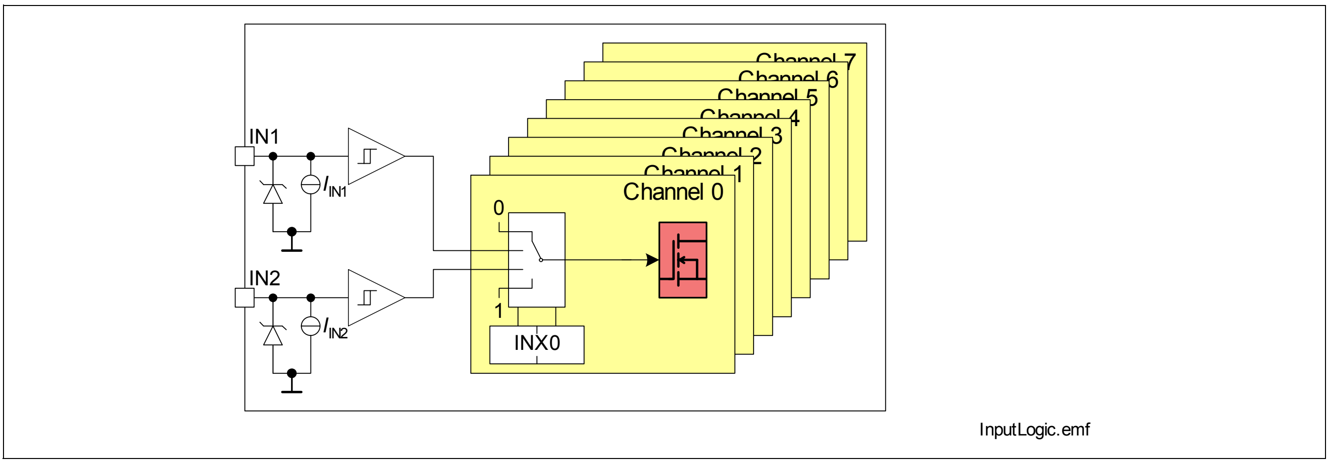

Figure 4 Input Multiplexer

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

6.2 Channels 4 and 5

The TLE7236G provides two auto-configuring high-side or low-side switches (channels 4 and 5). They adjust the diagnostic and protective functions according their potentials at drain and source automatically.

In high-side configuration, the load is connected between ground and source of the power transistors (S4 or S5). The drain of the power transistors (D4 and D5) can be connected to any potential between GND-pin potential and VBB-pin potential. When the drain is connected to VBB, the channel behave like the other high side channels. The drain can also be connected to a 5 V power supply and the source pin will be utilized as switched 5 V supply line.

In low-side configuration, the source of the power transistors are to be connected to GND.

The configuration can be chosen for each of these channels individually, so it is feasible to connect one channel in low-side and the other in high-side configuration.

6.3 Inductive Output Clamp

When switching off inductive loads with low-side switches, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. For the high-side channels, the potential at pin OUT drops below ground potential to $V_{S(CL)}$. The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited by the max. clamping energy E_{AR} see electrical characteristics **“E_{AR}” on Page 10**.

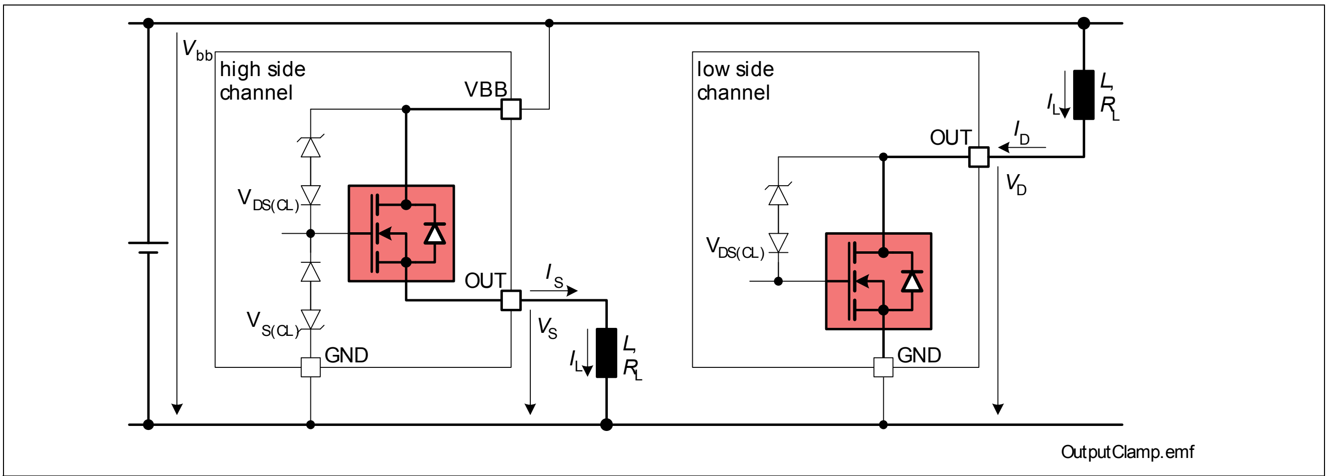

Figure 5 Output Clamp Implementation

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE7236G. This energy can be calculated with following equations:

$$E = V_{D(CL)} \cdot \left[\frac{V_{bb} - V_{D(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{bb} - V_{D(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L} \qquad \textbf{Low-side} \qquad (1)$$

$$E = (V_{bb} - V_{S(CL)}) \cdot \left[\frac{V_{S(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{S(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L} \qquad \textbf{High-side} \qquad (2)$$

These equations simplify under the assumption of $R_L = 0$:

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{bb} - V_{D(CL)}}\right) \qquad \textbf{Low-side} \qquad (3)$$

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bb}}{V_{S(CL)}}\right) \qquad \textbf{High-side} \qquad (4)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

6.4 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the `INX` bits of the serial peripheral interface (SPI). The switching times t_{ON} and t_{OFF} are designed equally.

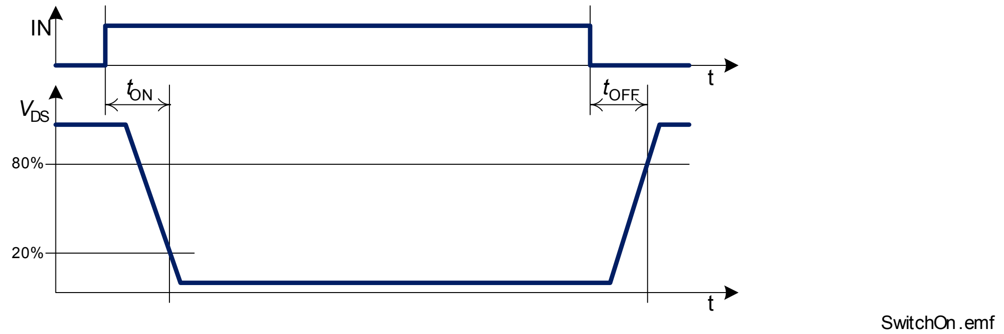

Figure 6 Switching a Resistive Load

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to **Section 9.3** for details on SPI protocol.

6.5 Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.5.1	On-State resistance channel 0, 1, 4, 5, 6, 7	$R_{DS(ON)}$	–	0.85	–	Ω	I_L = 220 mA T_j = 25 °C
			–	1.4	1.8		T_j = 150 °C
	channel 2, 3		–	1.6	–		I_L = 110 mA T_j = 25 °C
			–	2.6	3.8		T_j = 150 °C
6.5.2	Nominal load current	$I_{Out(nom)}$				mA	all channels on T_a = 100 °C $T_{j,max}$ = 150 °C based on R_{thja}
	channel 0, 1, 4, 5, 6, 7		280	410	–		[1]
	channel 2, 3		140	205	–		[1]
6.5.3	Output leakage current in sleep mode	$I_{Out(Sleep)}$	–	–	1	µA	V_{DS} = 13.5 V T_j = 25 °C[1]
			–	–	2		T_j = 85 °C [1]
			–	–	5		T_j = 150 °C
6.5.4	Output clamping voltage	$V_{OUT\_S(CL)}$	–	–	-16	V	–
		$V_{OUT\_DS(CL)}$	41	–	–	V	–
Input Characteristics							
6.5.5	L level of pin IN & LHI	$V_{IN(L)}$	0	–	0.6	V	–
6.5.6	H level of pin IN & LHI	$V_{IN(H)}$	1.8	–	5.5	V	–
6.5.7	Input voltage hysteresis at pin IN	ΔV_{IN}	–	0.1	–	V	[1]
6.5.8	L-input pull-down current through pin IN	$I_{IN(L)}$	1.5	–	–	µA	V_{IN} = 0.6 V [1]
6.5.9	H-input pull-down current through pin IN	$I_{IN(H)}$	10	40	80	µA	V_{IN} = 5 V
Timings							
6.5.10	Turn-on time V_{DS} = 20% V_{bat} channel 0, 1,4,5	t_{ON}	–	–	100	µs	V_{bb} = 13.5 V resistive load I_{DS}= 250 mA
	channel 2, 3		–	–	100		I_{DS}= 120 mA
	channel 6,7		–	–	100		I_{DS} = 250 mA

Unless otherwise specified: V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
6.5.11	Turn-off time V_{DS} = 80% V_{bb}	t_{OFF}				µs	V_{bb} = 13.5 V resistive load
	channel 0, 1, 4, 5		–	–	100		I_{DS} = 250 mA
	channel 2, 3 (HS)		–	–	100		I_{DS} = 120 mA
	channel 6, 7 (LS)		–	–	100		I_{DS} = 250 mA

1) Not subject to production test, specified by design.

6.6 Command Description

Input Configuration Registers

ICR01 **000_B**

3	2	1	0
INX1		**INX0**	
rw		rw	

ICR23 **001_B**

3	2	1	0
INX3		**INX2**	
rw		rw	

ICR45 **010_B**

3	2	1	0
INX5		**INX4**	
rw		rw	

ICR67 **011_B**

3	2	1	0
INX7		**INX6**	
rw		rw	

Field	Bits	Type	Description
INXn n = 7 to 0	[3:2], [1:0]	rw	**Input Multiplexer Configuration Channel n** **00** Channel n is switched off 01 Channel n is switched by input 1 10 Channel n is switched by input 2 11 Channel n is switched on

7 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

7.1 Over Load Protection

The TLE7236G is protected in case of over load or short circuit of the load. After time $t_{OFF(OVL)}$, the over loaded channel `n` switches off and the according diagnosis flag `Dn` is set. The channel can be switched on after clearing the protection latch by command `CMD.CPL` = 1. The CPL command clears itself with the next valid SPI communication frame. Please refer to **Figure 7** for details.

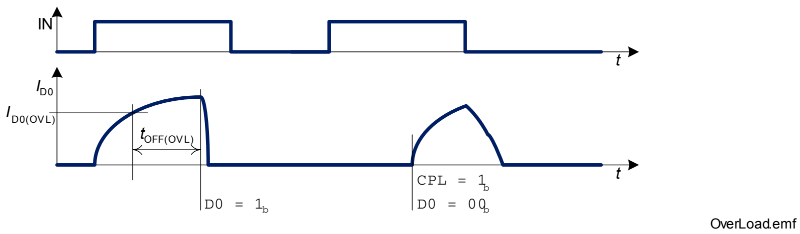

Figure 7 Shut Down at Over Load

7.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel to switch off to prevent destruction. The according diagnosis flag is set. This flag is also set in OFF state, if the regarding channel temperature is too high.The channel can be only switched on after clearing the protection latch by SPI command `CMD.CPL` = 1. The CPL command clears itself with the next valid SPI communication frame. Please refer to **“Diagnostic Features” on Page 24** for information on diagnosis features.

7.3 ESD protection

There is a designed in protection against ESD disturbances up to the specified limit by using the defined model. Please see electrical characteristics **“ESD susceptibility on all pins” on Page 11**

7.4 Reverse Polarity Protection

There is a reverse polarity protection implemented in the TLE7236G. This protection has to be divided into two parts. First the protection of the control circuits and second in the protection of the power transistors.

The control circuits are reverse polarity protected by protective measures in the ground connection. In case of reverse polarity, there is no current flow through the control circuits. To ensure this functionality, the GND pin and the substrate connections SUB must not be connected to the same potential. This means, the copper area dedicated for cooling will be connected at SUB and needs to be electrically isolated from GND.

The digital pins need serial resistors if the connected input stages are not floating to ground.

The power transistors contain intrinsic body diodes that cause power dissipation. The reverse current through these intrinsic body diodes has to be limited by the connected loads. The over temperature and over load protection are not active during reverse polarity.

7.5 Loss of V_{bb}

In case of loss of V_{bb} connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from V_{bb} to ground. Then for example, a diode (see D2 in **Figure 14 “Application Diagram” on Page 36**) can be placed.

7.6 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{DD} = 5.0 V, V_{BAT} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Over Load Protection							
7.6.1	Over load detection current at channel 0,1,4,5,6,7	$I_{Out(OVL)}$	0.5		1.0	A	
7.6.2	Over load detection current at channel 2,3	$I_{Out(OVL)}$	0.22		0.5	A	
7.6.3	Over load shut-down delay time	$t_{OFF(OVL)}$			60	µs	
Over Temperature Protection							
7.6.4	Thermal shut down temperature	$T_{j(SC)}$	150	170[1]		°C	

1) Not subject to production test, specified by design

8 Diagnostic Features

The SPI of TLE7236G provides diagnosis information about the device and about the load. The diagnosis information of the protective functions of channel n is latched in the diagnosis flags Dn. It is cleared by the SPI command CMD.CPL = 1. The CPL command clears itself with the next valid SPI communication frame.
The open load diagnosis of channel n is latched in the diagnosis flag OLn. This flag is cleared by reading the according diagnosis register.

Following table shows possible failure modes and the according protective and diagnostic action.

Failure Mode	Comment
Open Load	Diagnosis, when channel n is switched on: none Diagnosis, when channel n is switched off: according to voltage level at the output pin, flag OLn is set after time $t_{d(OL)}$. A diagnosis current can be enabled by SPI command DCCR.DCENn = 1.
Over Temperature	When over temperature occurs, the according diagnosis flag Dn is set. If the affected channel n was active it is switched off. The diagnosis flags are latched until they have been cleared by SPI command CMD.CPL = 1.
Over Load (Short Circuit)	When over load is detected at channel n, the affected channel is switched off after time $t_{OFF(OVL)}$ and the dedicated diagnosis flag Dn is set. The diagnosis flags are latched until they have been cleared by SPI command CMD.CPL = 1.

8.1 Electrical Characteristics

Unless otherwise specified:
V_{DD} = 3.0 V to 5.5V, V_{BAT} = 9.0 V to 16V, T_j = -40 °C to +150 °C
typical values: V_{BAT} = 13.5 V, V_{DD} = 5.0 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
OFF State Diagnosis							
8.1.1	Open load diagnosis delay time	$t_{d(OL)}$	100	–	250	µs	–
High Side Channels 0,1,2,3							
8.1.2	Open load detection threshold voltage for Channel 0,1,2,3	$V_{D(OL0..3)}$	2.3	–	3.9	V	[1]
8.1.3	Output diagnosis current channel 0,1,2,3	$I_{L(DC0..3)}$	50	–	300	µA	measured at $V_{D(OL)}$ threshold
Configurable Channels 4,5							
8.1.4	Open load detection threshold voltage for Channel 4,5 in all configurations	$V_{D(OL4,5)}$	1	–	2.2	V	[1]
8.1.5	Output diagnosis current channel 4,5 in high side configuration	$I_{L(DCHS)}$	80	–	300	µA	measured at $V_{D(OL)}$ threshold
8.1.6	Output diagnosis current channel 4,5 in low side configuration	$I_{L(DCLS)}$	20	–	100	µA	measured at $V_{D(OL)}$ threshold
Low side Channels 6,7							
8.1.7	Open load detection threshold voltage for Channel 6,7	$V_{D(OL6,7)}$		–	2.2	V	[1]
8.1.8	Output diagnosis current channel 6,7	$I_{L(DC6,7)}$	50	–	100	µA	measured at VOL threshold
ON State Diagnosis (see also Protection in Chapter 7)							
8.1.9	Over load detection current at channel 0,1,4,5,6,7	$I_{L(OVL)}$	0.5	–	1.0	A	–
8.1.10	Over load detection current at channel 2,3	$I_{L(OVL)}$	0.22	–	0.5	A	–
8.1.11	Over load detection delay time at channel 0,1,4,5,6,7	$t_{OFF(OVL)}$	–	–	60	µs	–

1) Open load detection voltages are referenced to ground