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SPIDER - TLE 7240SL

8 Channel Protected Low-Side Relay Switch

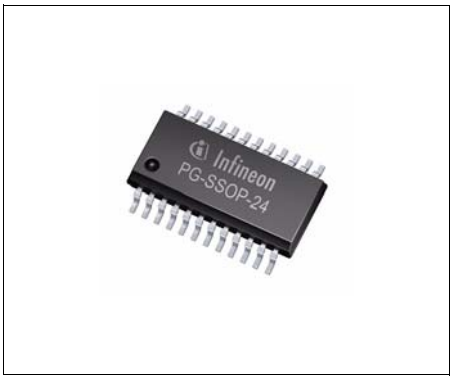
Automotive Power

Table of Contents

1 Overview

Features

- 4 input pins providing flexible PWM configuration
- Limp home functionality (direct driving) provided by a dedicated pin
- 16 bit SPI for diagnostics and control
- Daisy chain capability also compatible with 8bit SPI devices
- Very wide range of digital supply voltage
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP-24-7

Description

The SPIDER - TLE 7240SL is a eight channel low-side switch in PG-SSOP-24-7 package providing embedded protective functions.

It is especially designed as relay driver in automotive applications.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the load.

For direct control and PWM there are four input pins available.

The device is monolithically integrated. The power transistors are built by N-channel MOSFETs.

Table 1 Basic Electrical data

Digital supply voltage	V_{DD}	3.0 V ... 5.5 V
Analog supply voltage	V_{DDA}	4.5 V ... 5.5 V
Max. ON State resistance at T_j = 150°C for each channel	$R_{DS(ON,max)}$	3.0 Ω
Nominal load current	$I_{L\ (nom)}$	210 mA
Overload switch off threshold	$I_{D\ (OVL,max)}$	950 mA
Output leakage current per channel at 25 °C	$I_{D\ (STB,max)}$	1 µA
Drain to Source clamping voltage	$V_{DS(AZ)}$	41 V
Maximum SPI clock frequency	$f_{SCLK,max}$	5 MHz

Diagnostic Features

- latched diagnostic information via SPI register
- Overtemperature monitoring
- Overload detection in ON state
- Open load detection in OFF state

Type	Package	Marking
SPIDER - TLE 7240SL	PG-SSOP-24-7	TLE7240SL_A

Protection Functions

- Short circuit
- Over load
- Over temperature
- Electrostatic discharge (ESD)

Application

- All types of resistive, inductive and capacitive loads
- Especially designed for driving relays in automotive applications

Detailed Description

The SPIDER - TLE 7240SL is a eight channel low-side relay switch designed for typical automotive relays providing embedded protective functions. The PG-SSOP-24-7 package is used to get a footprint optimized solution. The 16 bit serial peripheral interface (SPI) is utilized for control and diagnosis of the device and the loads. The SPI interface provides daisy chain capability.

The SPIDER - TLE 7240SL is equipped with four input pins that can be individually routed to the output control of their dedicated channels thus offering flexibility in design and PCB layout. The input multiplexer is controlled via SPI.

There is a dedicated limp home pin LHI which provides a straightforward usage of the input pins as dedicated driver for four outputs.

The device provides full diagnosis of the load, which is open load as well as short circuit detection. The SPI diagnosis bits indicate latched fault conditions that may have occurred.

Each output stage is protected against short circuit. In case of over load, the affected channel switches off. There are temperature sensors available for each channel to protect the device in case of over temperature.

The device is supplied by two power supply lines. The analog supply supports 5 V, the digital supply offers a very wide flexibility in supply voltage ranging from 3.0 V up to 5.5 V.

The power transistors are built by N-channel vertical power MOSFETs. The inputs are ground referenced CMOS compatible. The device is monolithically integrated in Smart Power Technology.

In terms of PCB layout improvement, all output pins are available at one side of the device. The other side bundles the signals to the micro-controller.

2 Block Diagram

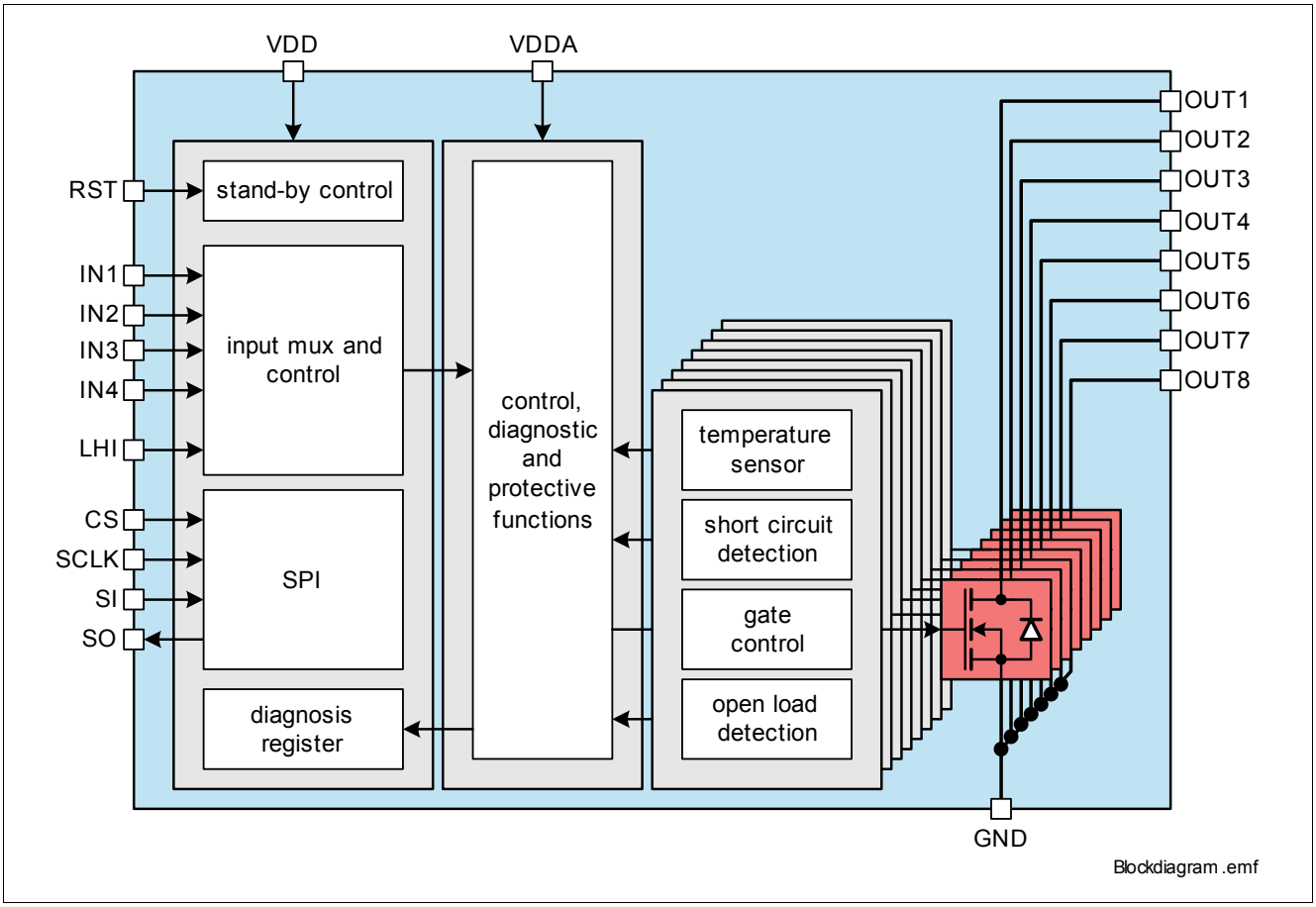


Figure 1 Block Diagram for the SPIDER - TLE 7240SL

3 Pin Configuration

3.1 Pin Assignment

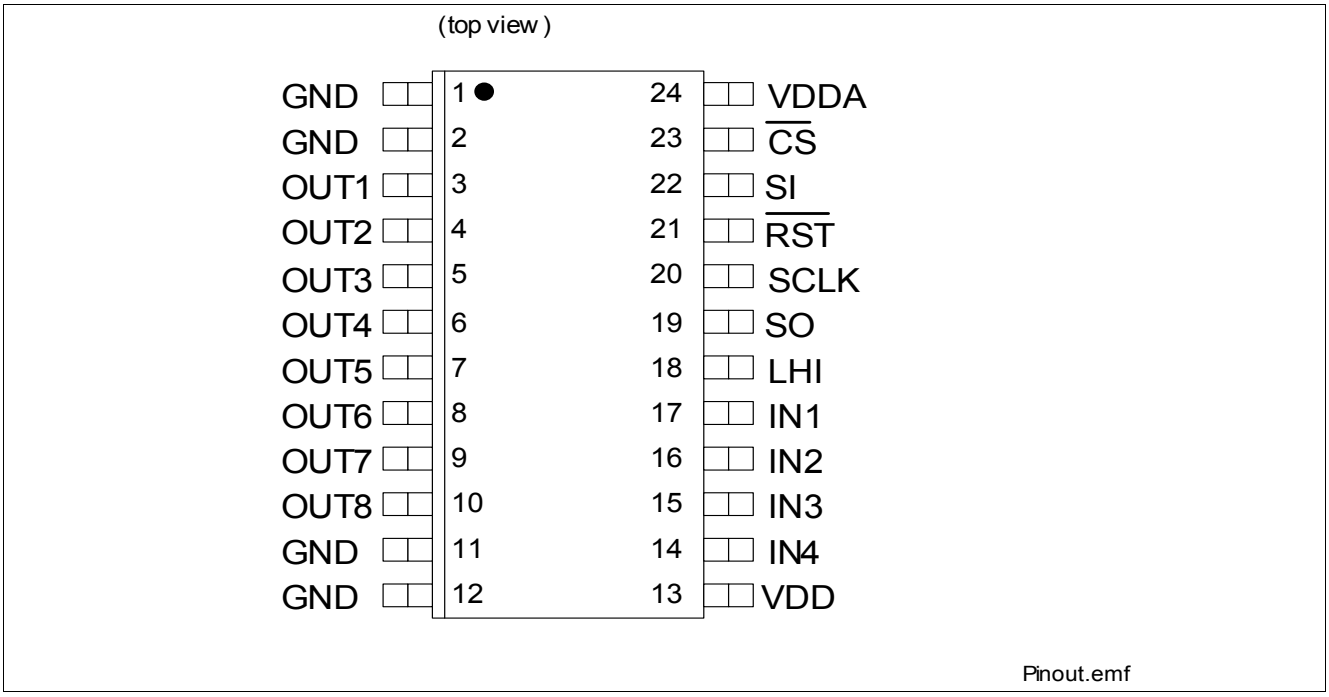


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

[20]

Pin	Symbol	I/O [1]		Function
Power Supply				
13	VDD	-		**Digital Supply Voltage;** Connected to 3.3V or 5V Voltage with Reverse protection Diode and Filter against EMC
24	VDDA	-		**Analog Supply Voltage;** Connected to 5V Voltage with Reverse protection Diode and Filter against EMC
1,2,11,12	GND	-		**Ground;** common ground for digital, analog and power
Power Stages				
3	OUT1	O		**Output Channel 1;** Drain of power transistor channel 1
4	OUT2	O		**Output Channel 2;** Drain of power transistor channel 2
5	OUT3	O		**Output Channel 3;** Drain of power transistor channel 3
6	OUT4	O		**Output Channel 4;** Drain of power transistor channel 4
7	OUT5	O		**Output Channel 5;** Drain of power transistor channel 5
8	OUT6	O		**Output Channel 6;** Drain of power transistor channel 6
9	OUT7	O		**Output Channel 7;** Drain of power transistor channel 7
10	OUT8	O		**Output Channel 8;** Drain of power transistor channel 8
Inputs				
17	IN1	I	PD	**Control Input;** Digital input 3.3 V or 5V. In case of not used keep open.
16	IN2	I	PD	**Control Input;** Digital input 3.3 V or 5V. In case of not used keep open.

Pin	Symbol	I/O [1]		Function
15	IN3	I	PD	**Control Input;** Digital input 3.3 V or 5V. In case of not used keep open.
14	IN4	I	PD	**Control Input;** Digital input 3.3 V or 5V. In case of not used keep open.
18	LHI	I	PD	**Limp Home;** Digital input 3.3 V or 5V. In case of not used keep open.
21	$\overline{\text{RST}}$	I	PD	**Reset input pin;** Digital input 3.3 V or 5V. Low active
SPI				
23	$\overline{\text{CS}}$	I	PU	**SPI chip select;** Digital input 3.3 V or 5V. Low active
20	SCLK	I	PD	**serial clock;** Digital input 3.3 V or 5V.
22	SI	I	PD	**serial data in;** Digital input 3.3 V or 5V.
19	SO	O		**serial data out;** Digital output with voltage level referring to V_{DD}.

1) O: Output, I: Input,
PD: pull-down resistor integrated,
PU: pull-up resistor integrated

3.3 Voltage and Current naming definition

Figure 3 shows all the terms used in this data sheet, with associated convention for positive values.

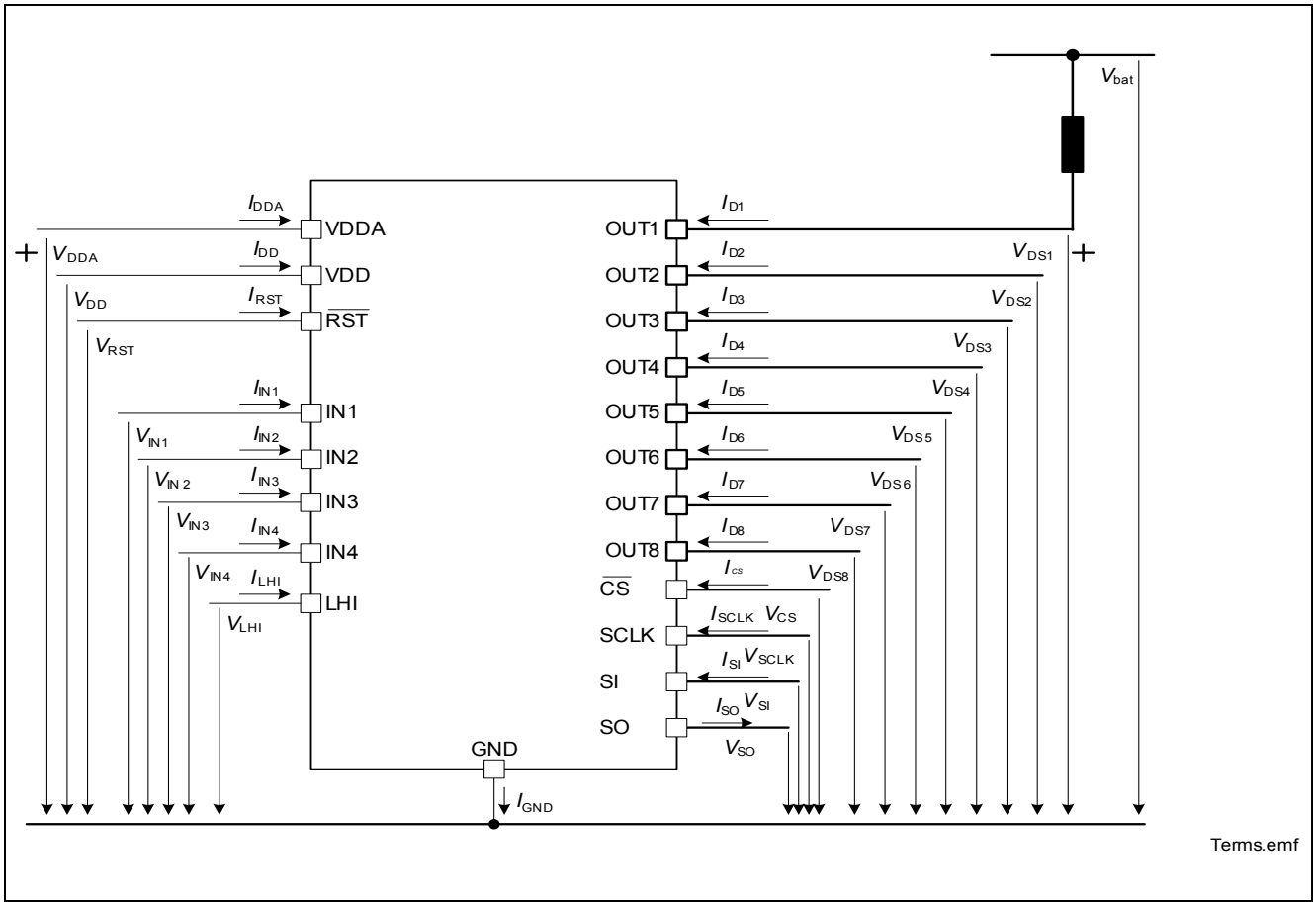


Figure 3 Terms

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1]

Unless otherwise specified: T_j = -40 ·C to +150 ·C; V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V

all voltages with respect to ground, positive current flowing into pin

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Power Supply						
4.1.1	Digital supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.2	Analog supply voltage	V_{DDA}	-0.3	5.5	V	–
4.1.3	Output voltage for short circuit protection (single pulse)	V_{OUT}	0	36	V	–
Power Stages						
4.1.4	Load current	I_D	-0.5	0.5	A	–
4.1.5	Voltage at power transistor	V_{DS}	–	41	V	active clamped
4.1.6	Maximum energy dissipation one channel	E_{AS}			mJ	[2] V_{bat}=16V, V_{clamp}=45V,
	single pulse		–	25		$T_{j(0)}$ = 150 °C $I_{D(0)}$ =0.40 A
	repetitive (1 · 10^4 cycles)	E_{AR}	–	13		$T_{j(0)}$ = 105 °C $I_{D(0)}$ =0.30 A
	repetitive (1 · 10^6 cycles)		–	11		$T_{j(0)}$ = 105 °C $I_{D(0)}$ =0.30 A
Logic Pins						
4.1.7	**IN1,IN2,IN3,IN4;**Voltage at input pins	V_{IN}	-0.3	5.5	V	–
4.1.8	**RST;** Voltage at reset pin	V_{RST}	-0.3	5.5	V	–
4.1.9	**LHI;** Voltage at limp home input pin	V_{LHI}	-0.3	5.5	V	–
4.1.10	**CS;** Voltage at chip select	V_{CS}	-0.3	V_{DD} + 0.3	V	[3]
4.1.11	**SCLK;** Voltage at serial clock pin	V_{SCLK}	-0.3	V_{DD} + 0.3	V	[3]
4.1.12	**SI;** Voltage at serial input pin	V_{SI}	-0.3	V_{DD} + 0.3	V	[3]
4.1.13	**SO;** Voltage at serial output pin	V_{SO}	-0.3	V_{DD} + 0.3	V	[3]
Temperatures						
4.1.14	Junction Temperature	T_j	-40	150	°C	–
4.1.15	Storage Temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.16	ESD Resistivity	V_{ESD}	-4	4	kV	HBM[4]

1) Not subject to production test, specified by design.

2) Pulse shape represents inductive switch off: $I_{D(t)} = I_{D(0)} \times (1 - t / t_{pulse})$; $0 < t < t_{pulse}$

3) level must not exceed V_{DD}+0.3V < 5.5 V

4) ESD susceptibility, HBM according to EIA/JESD 22-A114

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Digital supply voltage	V_{DD}	3.0	5.5	V	–
4.2.1	Analog supply voltage	V_{DDA}	4.5	5.5	V	–
4.2.2	extended supply range	V_{DDA}	4.0	4.5		parameter deviations are possible
4.2.3	Digital Supply current in reset mode	$I_{DD(RST)}$	–	10	µA	T_j = 85 °C
4.2.4	Digital supply current (all channels active)	$I_{DD(ON)}$	–	0.5	mA	V_{DD} = V_{DDA} = 5 V V_{RST} = V_{CS} = V_{DD} V_{SCLK} = 0 V V_{IN} = 0 V
4.2.5	Analog supply current (all channels active)	$I_{DDA(ON)}$	–	5	mA	–
4.2.6	Analog supply turn-ON time	$t_{DDA(ON)}$	15	–	µs	V_{DDA} = 0V to 5V (linear)

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.7	Junction to Soldering Point	R_{thJSP}	–	–	25	K/W	1) 2)
4.3.8	Junction to Ambient (1s0p+600mm^{2}Cu)	R_{thJA}	–	68	–	K/W	1) 3)
4.3.9	Junction to Ambient (2s2p)	R_{thJA}	–	62	–	K/W	1) 4)

1) Not subject to production test, specified by design

2) Specified R_{thJSP} value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature). T_a = 25 °C. LS1 to LS8 are dissipating 1 W power (0.125 W each).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-3 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600mm^2 and 70 µm thickness. T_a = 25 °C, LS1 to LS8 are dissipating 1 W power (0.125 W each).

4) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). T_a = 25 °C, LS1 to LS8 are dissipating 1 W power (0.125 W each).

5 Input and Power Stages

The SPIDER - TLE 7240SL is a eight channel low-side relay switch.

The power stages are built by N-channel vertical power MOSFET transistors.

5.1 Power Supply

The SPIDER - TLE 7240SL is supplied by two power supply lines V_{DD} and V_{DDA}.

The digital power supply line V_{DD} is designed to be functional at a very wide voltage range. The analog power supply V_{DDA} supports 5 V supply.

There are power-on reset functions implemented for both supply lines. After start-up of the power supply, all SPI registers are reset to their default values and the device is in idle mode. Capacitors at pins V_{DD} -GND and V_{DDA} -GND are recommended.

There is a reset pin available. Low level at this pin causes all registers to be set to their default values and the quiescent supply currents are minimized.

5.1.1 Limp Home Mode

The SPIDER - TLE 7240SL offers the capability of driving dedicated channels during eventual fail-safe operation of the system. This limp home mode is activated by a high signal at pin LHI. In this mode, the SPI registers are reset and the input pins are directly routed to their corresponding channels OUT1 to OUT4, see **Table 2** for details. OUT5 to OUT8 are turned off in limp home mode. Furthermore, the SPI is ignored and all input pin are referred to V_{DDA} in order to ensure a defined operation mode if the digital supply or the microcontroller fail.

A high signal on LHI overrides a Reset signal on RST. In case of a limp home during standby the device will therefore wake up and enter the limp home mode.

After limp home operation all registers are reset and the device enters in standby mode following low logic RST state, or returns to idle (all channels OFF). Next SPI transmission will receive a TER Flag.

Input	controlled Output
IN1	OUT1
IN2	OUT2
IN3	OUT3
IN4	OUT4

Table 2 Routing during limp home mode

5.2 Input Circuit

There are four input pins available at SPIDER - TLE 7240SL, which can be configured to be used for control of the output stages. The `INn` parameter of the SPI selects the input pin to be used. **Figure 4** shows the input circuit of SPIDER - TLE 7240SL.

During Limp home mode a default routing is switched and the SPI commands are ignored.

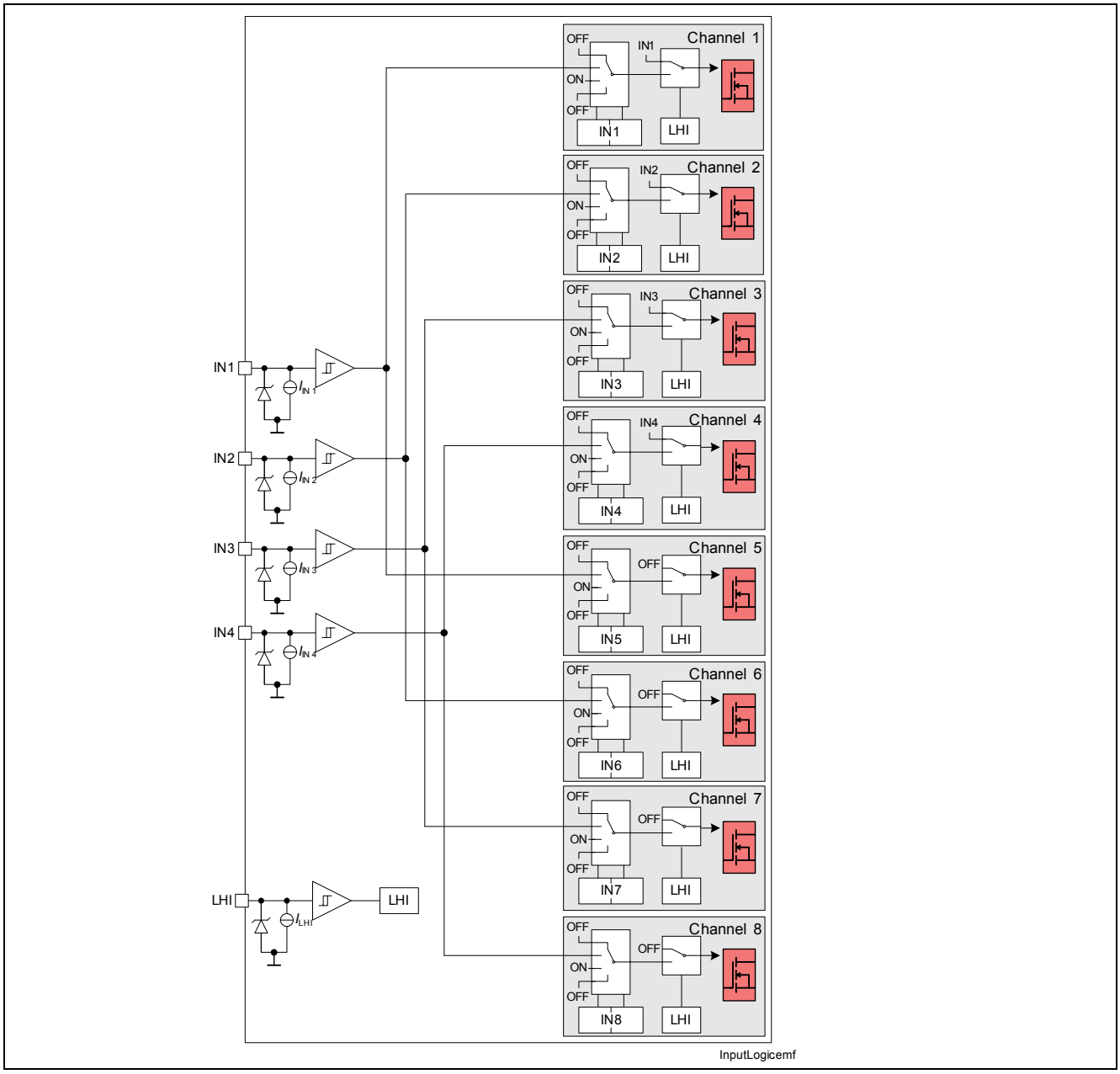


Figure 4 Input matrix and logic

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses. After power-on reset, the device enters idle mode (all channel OFF).

5.2.1 Inductive Output Clamp

When switching off inductive loads, the potential at pin OUT rises to $V_{DS(CL)}$ potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent destruction of the device, see **Figure 5** for details. Nevertheless, the maximum allowed load inductance is limited.

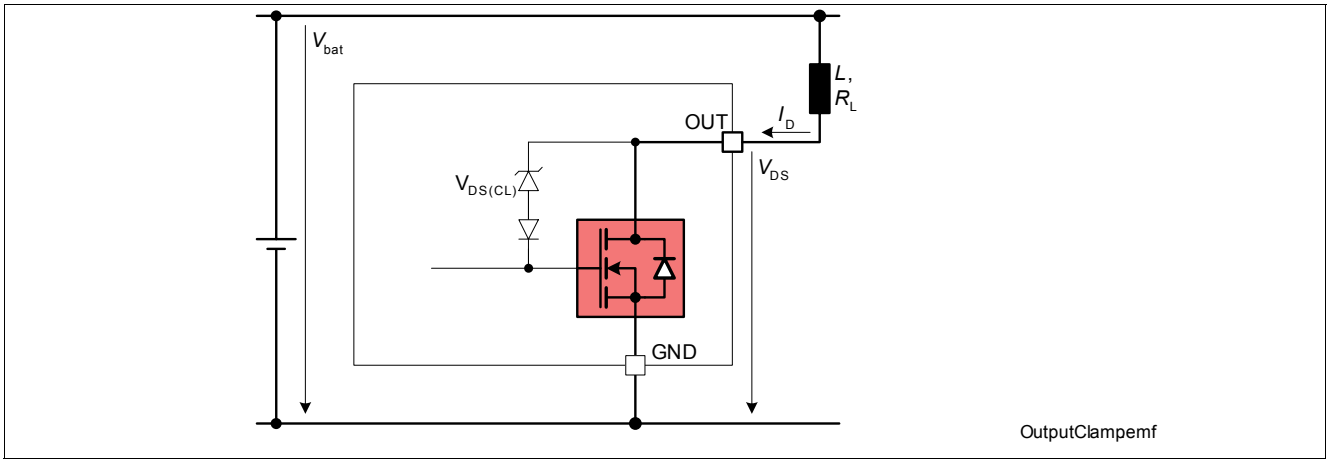


Figure 5 Output Clamp Implementation

Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the SPIDER - TLE 7240SL. This energy can be calculated with following equation:

$$E = V_{DS(CL)} \cdot \left[\frac{V_{bat} - V_{DS(CL)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_{bat} - V_{DS(CL)}}\right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under the assumption of R_L = 0:

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 - \frac{V_{bat}}{V_{bat} - V_{DS(CL)}}\right)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component.

5.2.2 Timing Diagrams

The power transistors are switched on and off with a dedicated slope via the IN bits of the serial peripheral interface SPI. The switching times t_{ON} and t_{OFF} are designed equally.

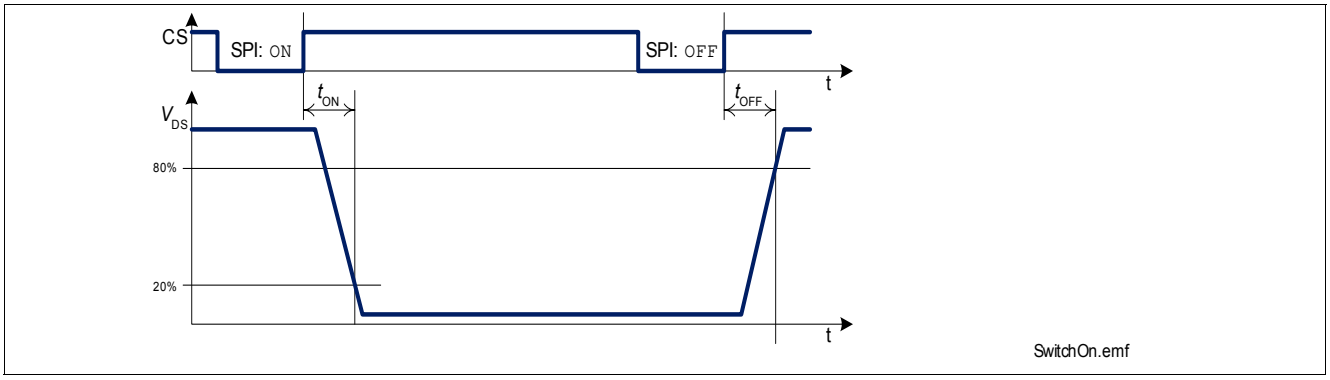


Figure 6 Switching a Resistive Load

In input mode, a high signal at the input pin is equivalent to a SPI ON command and a low signal to SPI OFF command respectively. Please refer to **Section 8.3** for details on operation modes.

5.3 Input and Power Stages Characteristics

Note: Characteristics show the deviation of parameter at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Supply and Input

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Power Supply							
5.3.1	Digital supply voltage	V_{DD}	3.0	–	5.5	V	–
5.3.2	Digital supply current, all channels ON	$I_{DD(ON)}$	–	–	0.5	mA	V_{DD} = V_{DDA} = 5 V V_{RST} = V_{CS} = V_{DD} V_{SCLK} = 0 V V_{IN} = 0 V
5.3.3	Digital supply stand-by current, all channels in stand-by mode	$I_{DD(STB)}$	 – – –	 – – –	 20 20 40	µA	f_{SCLK} = 0 Hz V_{CS} = V_{DD} T_j = 25 °C [1] T_j = 85 °C [1] T_j = 150 °C
5.3.4	Digital supply reset current	$I_{DD(RST)}$	 – – –	 – – –	 10 10 20	µA	V_{RST} =V_{LHI} = 0 V T_j = 25 °C [1] T_j = 85 °C [1] T_j = 150 °C
5.3.5	Digital power-on reset threshold voltage	$V_{DD(PO)}$	–	–	2.7	V	–
5.3.6	Analog supply voltage	V_{DDA}	4.5	–	5.5	V	–
5.3.7	Analog supply current all channels ON	$I_{DDA(ON)}$	–	–	5	mA	–
5.3.8	Analog supply stand-by current all channels in stand-by mode	$I_{DDA(STB)}$	 – – –	 – – –	 20 20 40	µA	V_{CS} = V_{DD} V_{SI} = 0 V V_{SCLK} = 0 V T_j = 25 °C [1] T_j = 85 °C [1] T_j = 150 °C
5.3.9	Analog supply reset current	$I_{DDA(RST)}$	– – – –	– – – –	 5 5 20	µA	V_{RST} =V_{LHI} = 0 V T_j = 25 °C [1] T_j = 85 °C [1] T_j = 150 °C
5.3.10	Analog power-on reset threshold voltage	$V_{DDA(PO)}$	–	–	4.0	V	–

Electrical Characteristics: Supply and Input

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Output characteristics							
5.3.11	On-State resistance per channel	$R_{DS(ON)}$	–	1.5	–	Ω	I_L = 180 mA T_j = 25 °C 1)
			–	2.2	3.0		I_L = 180 mA T_j = 150 °C
5.3.12	Nominal load current	$I_{L(nom)}$	210	–	–	mA	1)all channels on T_a = 85 °C $T_{j,max}$ = 150 °C based on $R_{thja,2s2p}$
5.3.13	Output leakage current in stand-by mode (per channel)	$I_{D(STB)}$	– – –	– – –	1 2 5	µA	V_{DS} = 13.5 V T_j = 25 °C 1) T_j = 85 °C 1) T_j = 150 °C
5.3.14	Output clamping voltage	$V_{DS(CL)}$	41	–	54	V	–
Input Characteristics							
5.3.15	L level of pins IN1..IN4 and LHI	$V_{IN(L)}$	0	–	0.6	V	–
5.3.16	H level of pins IN1..IN4 and LHI	$V_{IN(H)}$	2.0	–	5.5	V	2)
5.3.17	L-input pull-down current through pin IN	$I_{IN(L)}$	3	12	80	µA	1) V_{IN} = 0.6 V
5.3.18	H-input pull-down current through pin IN	$I_{IN(H)}$	10	40	80	µA	V_{DD} = 5.5 V V_{IN} = V_{DD}
Reset Characteristics							
5.3.19	L level of pin RST	$V_{RST(L)}$	0	–	0.2* V_{DD}		–
5.3.20	H level of pin RST	$V_{RST(H)}$	0.4* V_{DD}	–	V_{DD}		–
5.3.21	L-input pull-down current through pin RST	$I_{RST(L)}$	3	12	80	µA	1) V_{RST} = 0.6 V
5.3.22	H-input pull-down current through pin RST	$I_{RST(H)}$	10	40	80	µA	V_{DD} = 5.5 V V_{RST} = V_{DD}
Timings							
5.3.23	Reset wake-up time	$t_{wu(RST)}$	–	–	200	µs	–
5.3.24	Reset and LHI signal duration	$t_{RST(L)}$	50	–	–	µs	–
5.3.25	Turn-on time V_{DS} = 20% V_{bat} all channels	t_{ON}	–	30	50	µs	V_{bat} = 13.5 V resistive load I_{DS} = 180 mA
5.3.26	Turn-off time V_{DS} = 80% V_{bb} all channels	t_{OFF}	–	30	50	µs	V_{bat} = 13.5 V resistive load I_{DS} = 180 mA

1) Not subject to production test, specified by design.

2) level must not exceed V_{DD}+0.3V < 5.5 V

6 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

6.1 Over Load Protection

The SPIDER - TLE 7240SL is protected in case of over load or short circuit of the load. After time $t_{OFF(OVL)}$, the over loaded channel `n` switches off and the according diagnosis flag `Dn` is set.The channel can be switched on after clearing the diagnosis flag. Please refer to **Figure 7** for details.

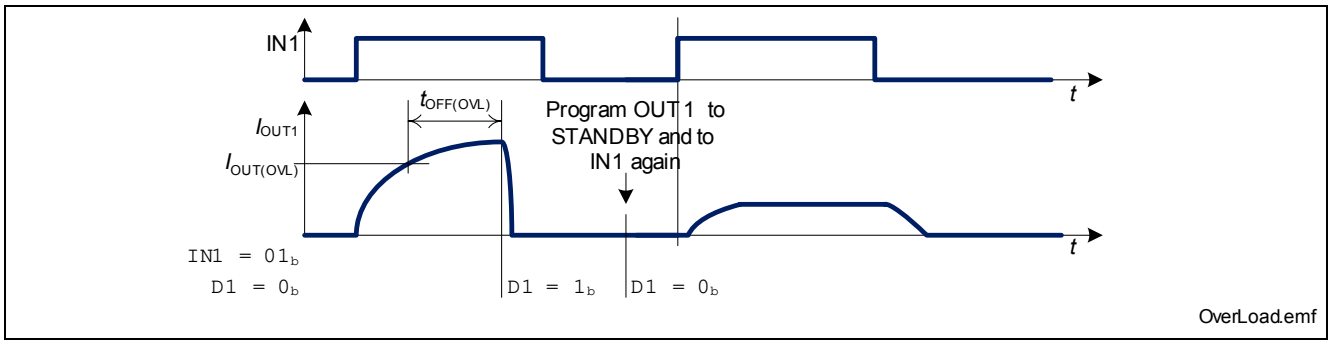


Figure 7 Shut down at over load

The current sink to ground ensures that the channels switch off in case of open input pin. The zener diode protects the input circuit against ESD pulses. After power-on reset, the device enters idle mode.

6.2 Over Temperature Protection

A temperature sensor for each channel causes an overheated channel `n` to switch off to prevent destruction and the according diagnosis flag `Dn` is set. The channel can be switched on after clearing the diagnosis flag. Please refer to **Chapter 7.1** for information on diagnosis features.

6.3 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diode of the power transistor causes power dissipation. The reverse current through the intrinsic body diode of the power transistor has to be limited by the connected load. The V_{DD} and V_{DDA} supply pins must be protected against reverse polarity externally. The over temperature and over load protection is not active during reverse polarity.

6.4 Protection Characteristics

Note: Characteristics show the deviation of parameter at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Protection

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Over Load Protection							
6.4.1	Over load detection current all channels	$I_{D(OVL)}$	0.5	–	0.95	A	– –
6.4.2	Over load shut-down delay time	$t_{OFF(OVL)}$	3	–	50	µs	–
Over Temperature Protection							
6.4.3	Thermal shut down temperature	$T_{j(SC)}$	150	170[1)]	–	°C	–

1) Not subject to production test, specified by design

7 Diagnosis Features

The SPI of SPIDER - TLE 7240SL provides diagnosis information about the device and about the load. There are following diagnosis flags implemented:

The diagnosis information of the protective functions of channel n is latched in the diagnosis flag *Dn*.

The open load diagnosis of channel n is latched in the diagnosis flag *OLn*.

Both flags are cleared by programming the specific channel to Standby (STB).

Failure Mode	Comment
Open Load or short circuit to ground	Diagnosis, when channel n is switched on: none Diagnosis, when channel n is switched off: according to voltage level at the output pin, flag OLn is set after time $t_{d(OL)}$. When the channel is in OFF there is Diagnosis active, in Standby the Diagnosis is not enabled
Over Temperature	When over temperature occurs, the according diagnosis flag Dn is set. If the affected channel n was active it is switched off. The diagnosis flags are latched until they have been cleared by programming the channel STB.
Over Load (Short Circuit)	When over load is detected at channel n, the affected channel is switched off after time $t_{OFF(OVL)}$ and the dedicated diagnosis flag Dn is set. The diagnosis flags are latched until they have been cleared by programming the channel STB

7.1 Diagnosis Characteristics

Note: Characteristics show the deviation of parameter at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Diagnosis

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
OFF State Diagnosis							
7.1.1	Open load detection threshold voltage	$V_{DS(OL)}$	1.0	–	2.5	V	–
7.1.2	Output pull-down diagnosis current per channel	$I_{D(PD)}$	–	–	80	µA	V_{DS} = 13.5 V
7.1.3	Open load diagnosis delay time	$t_{d(OL)}$	30	–	200	µs	–
ON State Diagnosis							
7.1.4	Over load detection current	$I_{D(OVL)}$	0.5	–	0.95	A	–
7.1.5	Over load detection delay time	$t_{OFF(OVL)}$	3	–	50	µs	–

8 Serial Peripheral Interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).

The SPI is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and $\overline{CS}$. Data is transferred by the lines SI and SO at the data rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a data access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. A modulo 8 counter ensures that data is taken only, when a multiple of 8 bit has been transferred, while the minimum of 16 bit is also taken into consideration. Therefore the interface provides daisy chain capability even with 8 bit SPI devices.

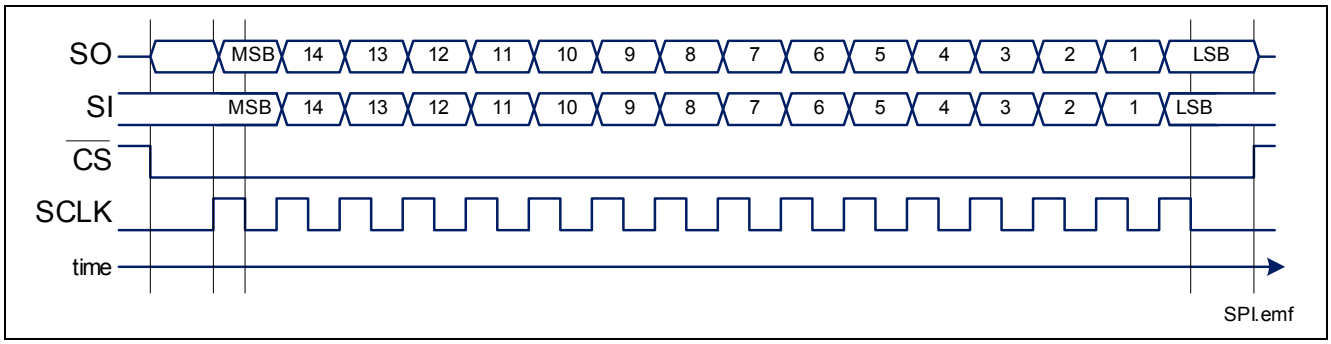


Figure 8 Serial peripheral interface

The SPI protocol is described in **Section 8.3**. It is reset to the default values after power-on reset.

8.1 SPI Signal Description

$\overline{CS}$ - Chip Select:

The system micro controller selects the SPIDER - TLE 7240SL by means of the $\overline{CS}$ pin. Whenever the pin is in low state, data transfer can take place. When $\overline{CS}$ is in high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

$\overline{CS}$ High to Low transition: ⎺_

- The diagnosis information is transferred into the shift register.
- SO changes from high impedance state to high or low state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. As a result, even in daisy chain configuration, a high signal indicates a faulty transmission. The transmission error flag is set after any kind of reset, so a reset between two SPI commands is indicated. For details, please refer to **Figure 9**. This information stays available to the first rising edge of SCLK.

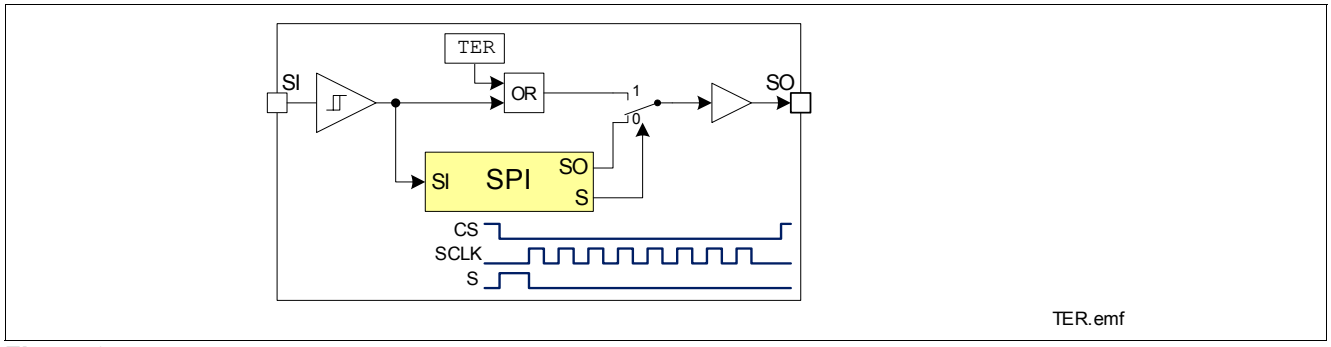


Figure 9 Transmission Error Flag on SO Line

$\overline{CS}$ Low to High transition:

Data from shift register is transferred into the input matrix register only, when after the falling edge of $\overline{CS}$ exactly a multiple (1, 2, 3, …) of eight SCLK signals have been detected, while the minimum valid length is of course 16 clocks for the 16 register bits of SPIDER-TLE7240SL.

SCLK - Serial Clock:

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select $\overline{CS}$ makes any transition.

SI - Serial Input:

Serial input data bits are shifted in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. Please refer to **Section 8.3** for further information.

SO - Serial Output:

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the $\overline{CS}$ pin goes to low state. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 8.3** for further information.

8.2 Daisy Chain Capability

The SPI of SPIDER - TLE 7240SL provides daisy chain capability. In this configuration several devices are activated by the same $\overline{CS}$ signal $\overline{MCS}$. The SI line of one device is connected with the SO line of another device (see **Figure 10**), which builds a chain. The ends of the chain are connected with the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK, which is connected to the SCLK line of each device in the chain.

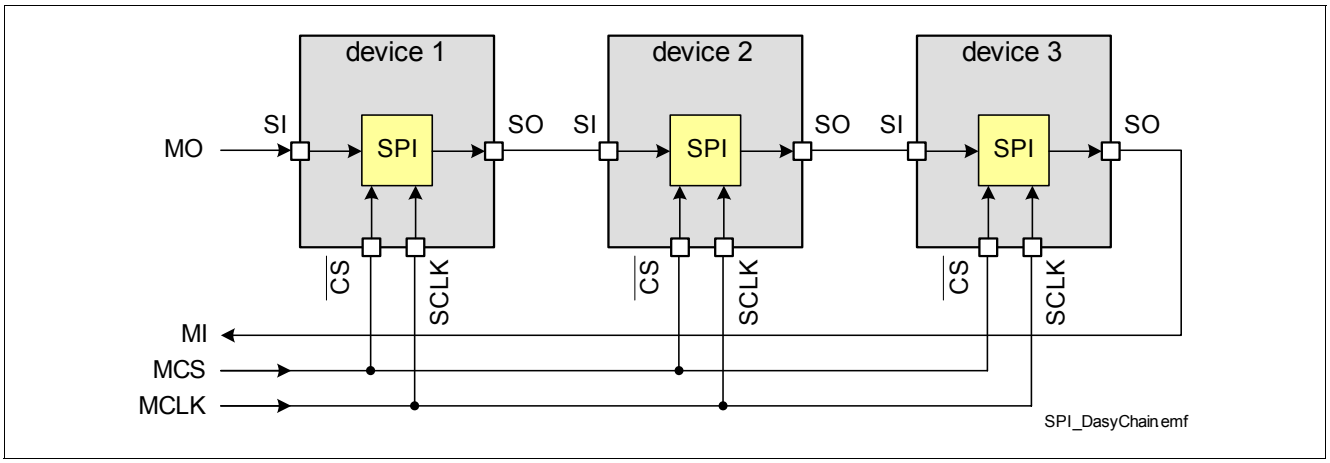


Figure 10 Daisy Chain Configuration

In the SPI block of each device, there is one shift register where one bit from SI line is shifted in each SCLK. The bit shifted out can be seen at SO. After 16 SCLK cycles, the data transfer for one SPIDER-TLE7240SL has been finished. In single chip configuration, the $\overline{CS}$ line must go high to make the device accept the transferred data. In daisy chain configuration the data shifted out at device #1 has been shifted in to device #2. When using multiple devices in daisy chain, the number of bits must be correspond with the number of register bits. **Figure 11** is showing a example with 3 SPI devices, where #1 and #3 are 16 bit SPI and #2 has a 8 bit SPI. To get a successful transmission, there have to be 2* 16 bit + 1* 8bit shifted through the devices. After that, the $\overline{MCS}$ line must go high.

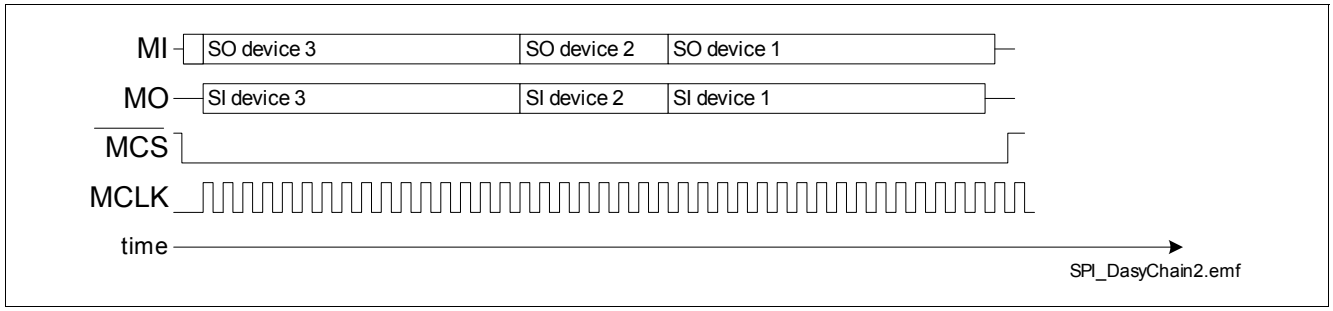


Figure 11 Data Transfer in Daisy Chain Configuration

8.3 SPI Protocol

The SPI protocol of the SPIDER - TLE 7240SL provides two registers. The input register and the diagnosis register. The diagnosis register contains eight pairs of diagnosis flags, the input register contains the input multiplexer configuration. After power-on reset, all register bits are set to 1 and the device is in idle mode.

SI **Default: $FFFF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IN8		**IN7**		**IN6**		**IN5**		**IN4**		**IN3**		**IN2**		**IN1**	

Field	Bits	Type	Description
INn (n = 8 - 1)	15:14, 13:12, 11:10, 9:8, 7:6, 5:4, 3:2, 1:0	W	**Input Register Channel n** 00_B Stand-by Mode: Channel is switched off. Diagnosis flags are cleared. Diagnosis current is disabled. 01_B Input Mode: Channel is switched according to signal at input pin. Diagnosis current is enabled in OFF-state. 10_B ON Mode: Channel is switched on. **11_B** OFF Mode: Channel is switched off. Diagnosis current is enabled.

Note: If all channels are programmed to Standby, the device changes to power down status with minimum current consumption (sleep mode).

SO **Reset Value: 10000_H**

CS[1)]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TER	**OL8**	**D8**	**OL7**	**D7**	**OL6**	**D6**	**OL5**	**D5**	**OL4**	**D4**	**OL3**	**D3**	**OL2**	**D2**	**OL1**	**D1**

1) This bit is valid between $\overline{CS}$ hi -> lo and first SCLK lo -> hi transition.

Field	Bits	Type	Description
TER	CS	R	**Transmission Error** 0 Previous transmission was successful (modulo 8 clocks received, minimum 16 bit). **1** Previous transmission failed or first transmission after reset.
OLn (n = 8 - 1)	15,13, 11,9,7, 5, 3, 1	R	**Open Load Flag of channel n** **0** Normal operation. 1 Open load has occurred in OFF state.
Dn (n = 8 - 1)	14,12, 10,8,6, 4, 2, 0	R	**Diagnosis Flag of channel n** **0** Normal operation. 1 Over load or over temperature switch off has occurred in ON state.

8.3.1 Timing Diagrams

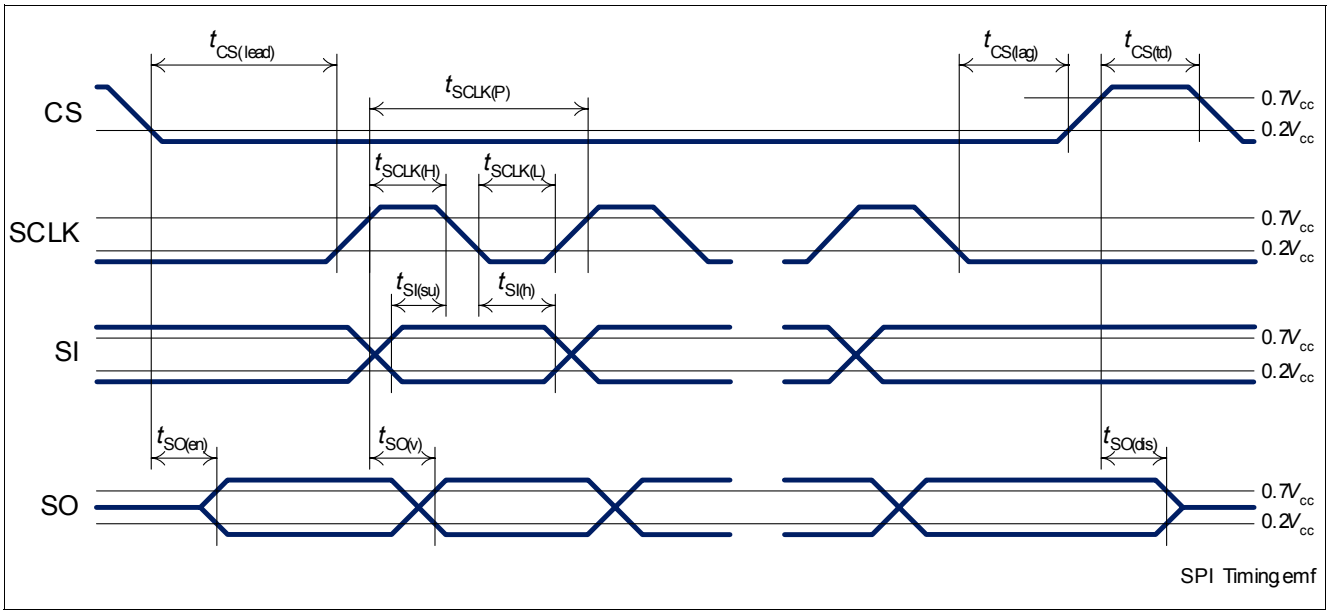


Figure 12 Timing Diagram

8.4 SPI Characteristics

Note: Characteristics show the deviation of parameter at given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.

Electrical Characteristics: Serial Peripheral Interface (SPI)

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Input Characteristics ($\overline{CS}$, SCLK, SI)							
8.4.1	L level of pin $\overline{CS}$ SCLK SI	 $V_{CS(L)}$ $V_{SCLK(L)}$ $V_{SI(L)}$	0	–	0.2* V_{DD}		–
8.4.2	H level of pin $\overline{CS}$ SCLK SI	 $V_{CS(H)}$ $V_{SCLK(H)}$ $V_{SI(H)}$	0.4* V_{DD}	–	V_{DD}		–
8.4.3	L-input pull-up current through $\overline{CS}$	$I_{CS(L)}$	3	17	40	µA	V_{CS} = 0 V
8.4.4	H-input pull-up current through $\overline{CS}$	$I_{CS(H)}$	3	15	40	µA	1) V_{CS} = 0.4*V_{DD}
8.4.5	L-input pull-down current through pin SCLK SI	 $I_{SCLK(L)}$ $I_{SI(L)}$	3	12	80	µA	1) V_{SCLK} = 0.6 V V_{SI} = 0.6 V
8.4.6	H-input pull-down current through pin SCLK SI	 $I_{SCLK(H)}$ $I_{SI(H)}$	10	40	80	µA	 V_{SCLK} = V_{DD} V_{SI} = V_{DD}
Output Characteristics (SO)							
8.4.7	L level output voltage	$V_{SO(L)}$	0	–	0.6	V	I_{SO} = -2 mA
8.4.8	H level output voltage	$V_{SO(H)}$	V_{DD} - 0.4 V	–	V_{DD}		I_{SO} = 1.5 mA
8.4.9	Output tristate leakage current	$I_{SO(OFF)}$	-10	–	10	µA	V_{CS} = V_{DD}
Timings							
8.4.10	Serial clock frequency	f_{SCLK}	0	–	5	MHz	1)
8.4.11	Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	1)
8.4.12	Serial clock high time	$t_{SCLK(H)}$	50	–	–	ns	1)
8.4.13	Serial clock low time	$t_{SCLK(L)}$	50	–	–	ns	1)
8.4.14	Enable lead time (falling $\overline{CS}$ to rising SCLK)	$t_{CS(lead)}$	250	–	–	ns	1)
8.4.15	Enable lag time (falling SCLK to rising $\overline{CS}$)	$t_{CS(lag)}$	250	–	–	ns	1)
8.4.16	Transfer delay time (rising $\overline{CS}$ to falling $\overline{CS}$)	$t_{CS(td)}$	250	–	–	ns	1)2)
8.4.17	Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	1)

Electrical Characteristics: Serial Peripheral Interface (SPI)

All voltages with respect to ground, positive current flowing into pin
unless otherwise specified: V_{DD} = 3.0 V to V_{DDA}, V_{DDA}= 4.5V to 5.5V, T_j = -40 ·C to +150 ·C

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
8.4.18	Output enable time (falling $\overline{CS}$ to SO valid)	$t_{SO(en)}$	–	–	200	ns	C_L = 50 pF 1)
8.4.19	Output disable time (rising $\overline{CS}$ to SO tri-state)	$t_{SO(dis)}$	–	–	200	ns	C_L = 50 pF 1)
8.4.20	Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	C_L = 50 pF 1)

1) Not subject to production test, specified by design.

2) Diagnosis flag update needs the time specified in **Chapter 7.1** to get valid information

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Figure 13 shows a simplified application circuit. VDD and VDDA need to be externally reverse polarity protected.

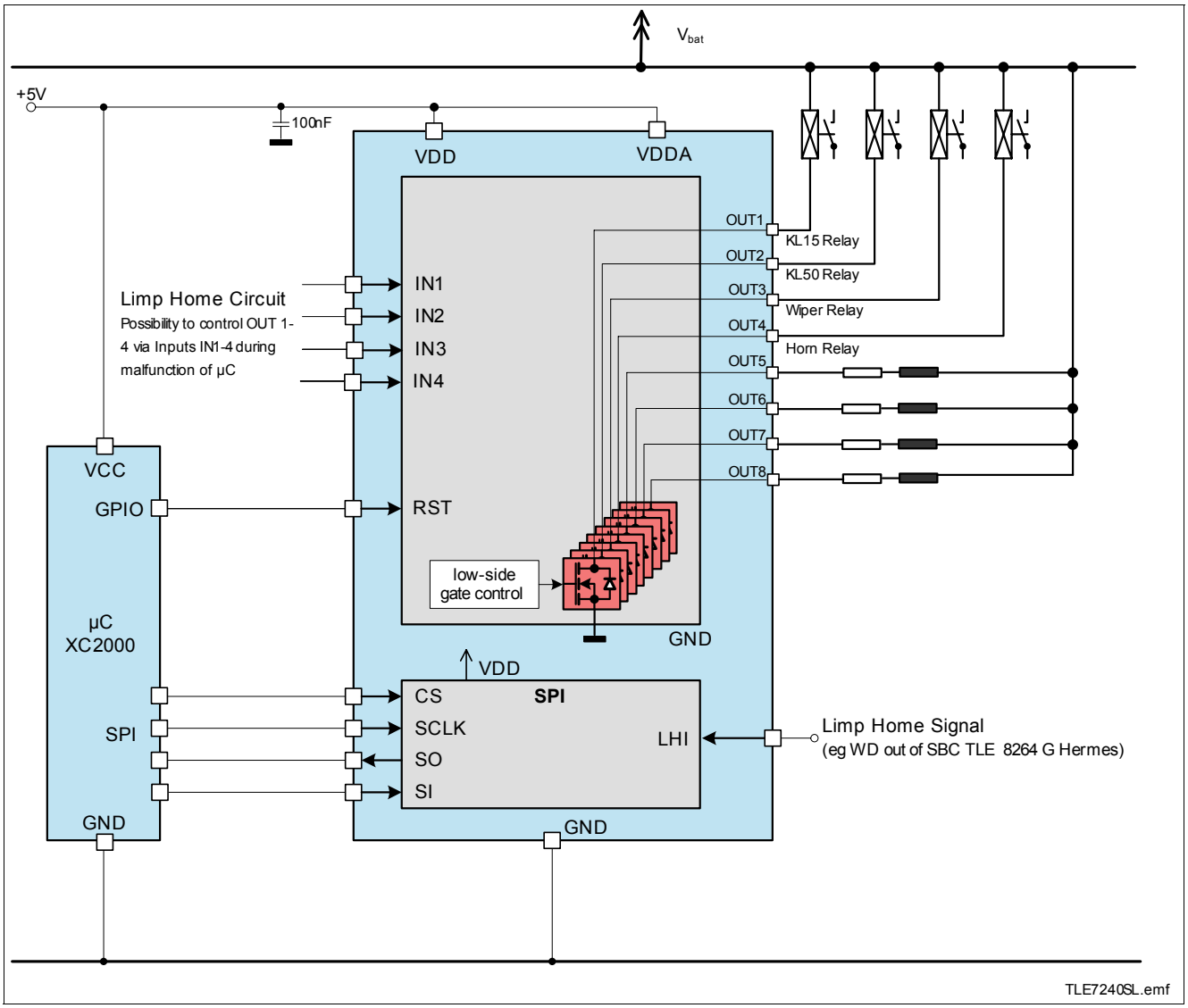


Figure 13 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

For further information you may contact **http://www.infineon.com/spider**