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TLE 7241E

Dual Channel Constant Current Control Solenoid Driver

Automotive Power

Never stop thinking

Table of Contents

Dual Channel Constant Current Control Solenoid Driver **TLE 7241E**

AEC Qualified RoHS

1 Overview

PG-DSO-20-27

1.1 Features

- Two Fully Independent Channels
- Integrated N-channel DMOS transistors
- Programmable Average Current with 10-bit resolution via SPI
  - I_{avg} range = 0 to 1000 mA (typical)
- Programmable Superimposed Dither
  - Programmable Frequency (41 Hz to 1 kHz typ)
  - Programmable Amplitude (12.5 to 390 mVpp typ)
  - Programmable Hysteresis (40 to 110 mVpp typ)
- Interface and Control
  - 16-bit SPI (Serial Peripheral Interface) daisy chainable
  - A single “Default” pin to disable both channels and reset the programmable registers of both channels
  - 5.0 V and 3.3 V logic compatible I/O
  - The contents of all registers can be verified via SPI
  - Operation with or without external reference possible
- Protection
  - Overcurrent
  - Overvoltage
  - Overtemperature
- Diagnostics
  - Overcurrent / shorted solenoid
  - Overtemperature
  - Open load
  - Short to GND
- Green Product (RoHS compliant)
- AEC Qualified

Type	Ordering Code	Package
TLE 7241E	on request	PG-DSO-20-27

1.2 Applications

- Variable force solenoids (e.g. automatic transmission solenoids)
- Constant current controlled solenoids like
  - Idle Speed Control
  - Exhaust Gas Recirculation
  - Valve control
  - Suspension Control

1.3 General Description

The TLE 7241E is a dual channel constant current control solenoid driver with integrated DMOS power transistors. The average load current can be programmed to a value in the range of 0 mA to 1000 mA (with a 1 Ω external sense resistor) with 10 bits of resolution. Load current is controlled using a hysteretic control scheme with a programmable hysteresis value. A triangular “dither” waveform can be superimposed on the switching current waveform in order to improve the transfer function of the solenoid. The amplitude and frequency of the dither waveform are programmable by the SPI interface. The device is protected from damage due to overcurrent, overvoltage and overtemperature conditions, and is able to diagnose and report open loads, shorted loads, and loads shorted to ground.

Note: An external free-wheeling diode must be provided when using the TLE 7241E in constant current control mode, otherwise the IC will be damaged.

For best accuracy, an external 2.5 V reference voltage should be supplied at the REF pin. The TLE 7241E also includes an internal 2.5 V reference voltage, which can be selected by connecting the REF pin to ground. The reference voltage selection (internal or external) can be verified via the SPI interface.

Application Block Diagram

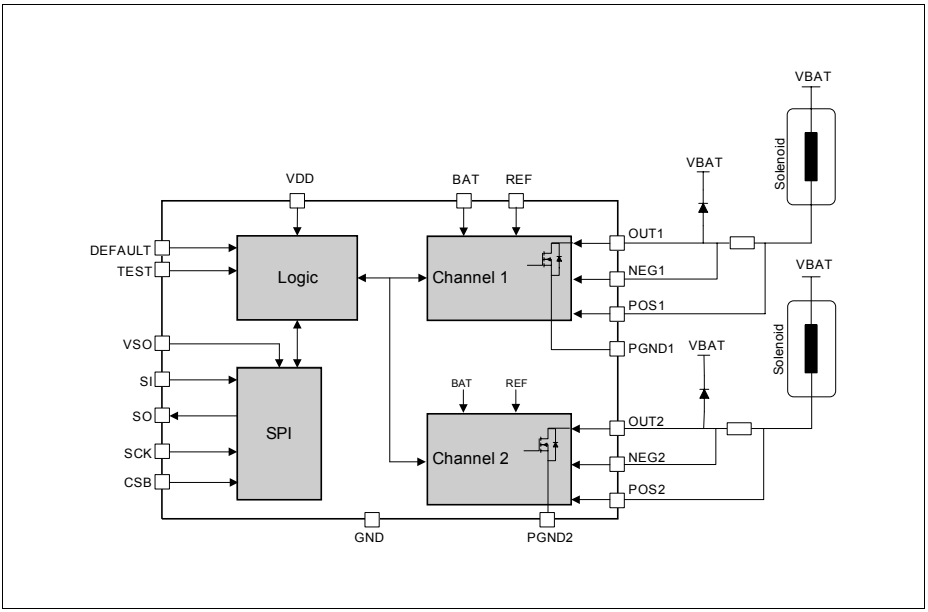

Figure 1 Basic Application Diagram

Detailed Block Diagram

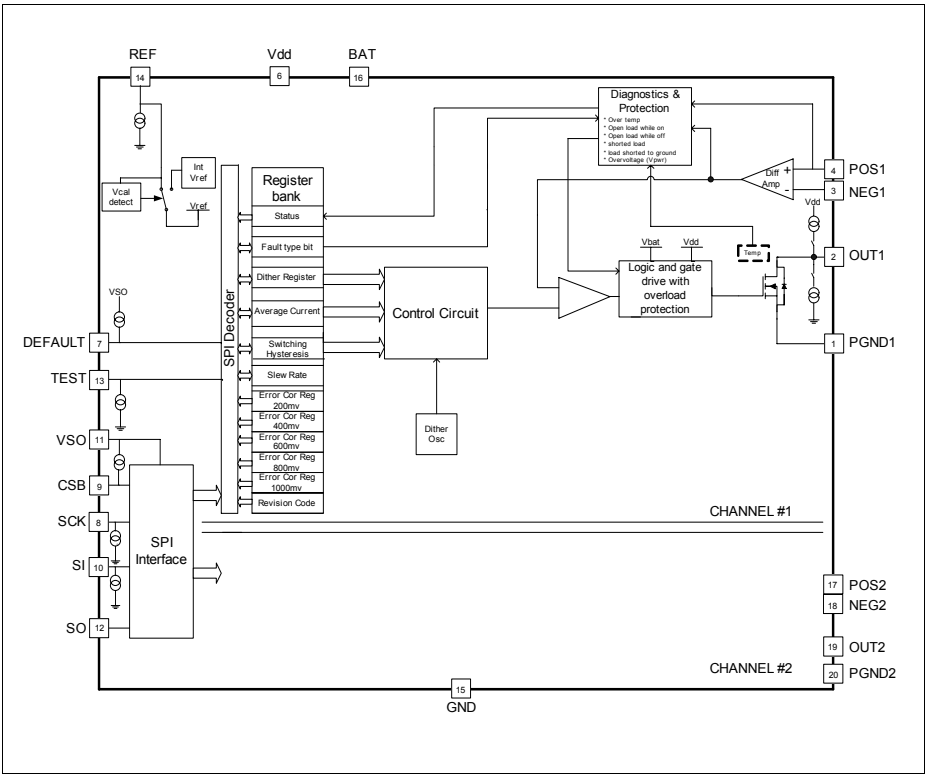

Figure 2 Detailed Block Diagram

2 Pin Configuration

Pin Assignment

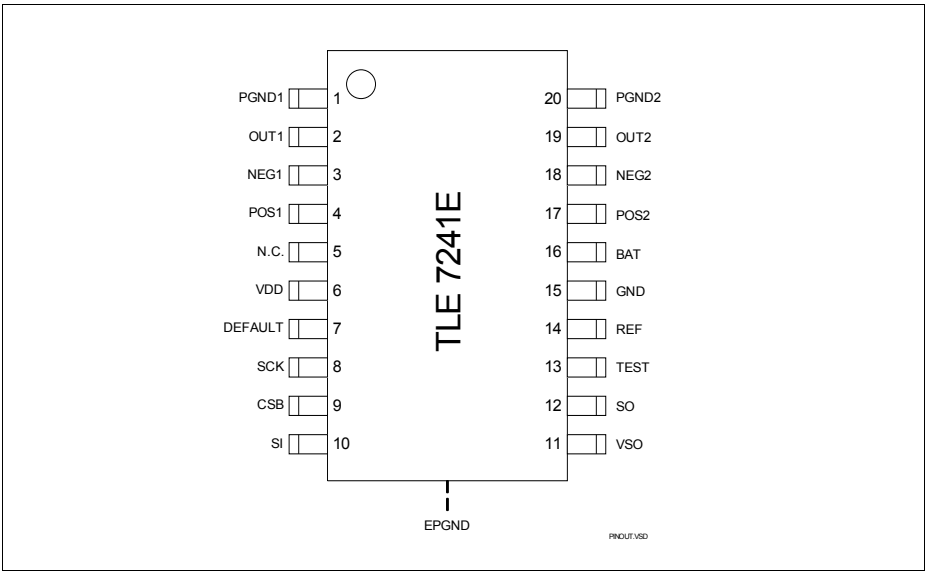

Figure 3 Pin-Out

Pin Definitions and Functions

Pin	Pin Name	Pin Description
1	PGND1	**Power Ground Channel 1;** internally connected to PGND2
2	OUT1	**Output Channel 1**; Drain of Output DMOS; connect to negative terminal of external sense resistor
3	NEG1	**Negative Sense Pin Channel 1**; connect to negative terminal of external sense resistor with dedicated trace
4	POS1	**Positive Sense Pin Channel 1**; connect to positive terminal of external sense resistor with dedicated trace
5	NC	**Not Connected;** not bonded internally
6	V_{DD}	**Logic Supply Voltage;** connect a ceramic capacitor to GND near the device
7	DEFAULT	**Control Input;** Active high digital input. 3.3V and 5.0V logic compatible. In case of not used, connect to ground

Pin Definitions and Functions (cont'd)

Pin	Pin Name	Pin Description
8	SCK	**SPI Clock**; Digital input pin. 3.3V and 5.0V logic compatible
9	CSB	**Chip Select Bar**; Active low digital input pin. 3.3V and 5.0V logic compatible
10	SI	**Serial Data Input;** 3.3V and 5.0V logic compatible
11	V_{SO}	**SPI Supply Voltage;** connect a ceramic capacitor to GND near the device
12	SO	**Serial Data Output**; Supplied by Vso pin
13	TEST	**Test Pin;** connect to GND
14	REF	**Voltage Reference;** connect to external 2.5 V reference, or connect to GND to enable internal reference.
15	GND	**Ground**; signal ground
16	BAT	**BAT Input;** connect to the solenoid supply voltage through a series resistor. Connect a ceramic capacitor to GND near the device
17	POS2	**Positive Sense Pin Channel 2**; connect to positive terminal of external sense resistor with dedicated trace
18	NEG2	**Negative Sense Pin Channel 2**; connect to negative terminal of external sense resistor with dedicated trace
19	OUT2	**Output Channel 2**; Drain of Output DMOS; connect to negative terminal of external sense resistor
20	PGND2	**Power Ground Channel 2;** internally connected to PGND1
Exposed Lead Frame	EPGND	**GND;** Should be connected to GND, PGND1 and PGND2 and to the ground plane of the ECU

Note: If a channel is unused, the OUTx, NEGx, and POSx pins should be connected together.

3 Maximum Ratings

Absolute Maximum Ratings[1)]

T_j = -40 to 150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Notes
			Min.	Max.		
Voltages						
M.1	Supply Voltage	BAT V_{DD} V_{SO}	-0.3 -0.3 -0.3	50 6.0 6.0	Vdc Vdc Vdc	–
M.2	Analog Input Voltage	POSx NEGx POSx-NEGx	-0.3 -0.3 -0.3	50 50 20	Vdc Vdc Vdc	–
M.3	Output Voltage	OUTx	-0.3	50	Vdc	–
M.4	Digital Input Voltage	REF TEST SI SCK CSB DEFAULT	-0.3 -0.3 -0.3 -0.3 -0.3 -0.3	min. (6.0, V_{DD} + 0.3) 6.0 6.0 6.0 min. (6.0, V_{SO} + 0.3) min. (6.0, V_{SO} + 0.3)	Vdc Vdc Vdc Vdc Vdc Vdc	–
M.5	Digital Output Pin Voltage	SO	-0.3	min. (6.0, V_{SO} + 0.3)	Vdc	–
M.6	Dynamic Clamp Voltage T_{clamp} < 2.0 ms	BAT POSx NEGx OUTx	-1.5 -1.5 -1.5 -1.5	– – – –	V V V V	–
M.7	Ground Pin Voltage (GND)	GND	-0.3	0.3	Vdc	–
M.8	Difference between PGND1 and PGND2	PGNDx	-0.3	0.3	Vdc	–
Others						
M.9	Biased Junction Temperature	T_j	-40	150	°C	–
M.10	Storage Temperature	T_{st}	-55	150	°C	–
M.11	Single Clamp Energy (OUTx) I=1.0A Tj=150 °C	E_{max}	–	30	mJ	–

Absolute Maximum Ratings[1] (cont'd)

T_j = -40 to 150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Notes
			Min.	Max.		
M.12	ESD HBM all pins EIA/JESD22-A 114B (1.5 K Ω, 100 pF)	–	-2	+2	kV	–
M.13	ESD MM all pins EIA/JESD22-A115A (0 Ω, 200 pF)	–	-200	200	V	–

1) Not subject to production test, specified by design

All voltages are with respect to PGND1 & 2. Positive current flows into the pin unless otherwise specified.

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4 Functional Range

Functional Range

T_j = -40 to 150 °C; V_{REF} = 2.5V

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
F.1	Voltage at BAT	V_{BAT}	9	18	V	–
F.2	Voltage at V_{DD}	V_{DD}	4.75	5.25	V	–
F.3	Voltage at VSO	V_{VSO}	3.1	V_{DD} + 0.3 or 5.25V	V	–
F.4	Voltage at SI, SCK	V_{IN1}	-0.3	V_{DD} + 0.3	V	–
F.5	Voltage at CSB, DEFAULT, SO	V_{IN2}	-0.3	V_{SO} + 0.3	V	–
F.6	Voltage at POS1, POS2, NEG1, NEG2, OUT1, OUT2	V_{OUT}, V_{POS}, V_{NEG}	-0.3	50	V	–
F.7	Voltage Difference POS1-NEG1, POS2-NEG2	V_{POS} - V_{NEG}	0	1.23	V	–
F.8	Voltage at PGND1, PGND2, GND	V_{GND}	-0.3	0.3	V	–
F.9	SPI Clock Frequency	f_{clk}		3.2	MHz	C_{SO} = 200 pF max; V_{VSO} = 5 V
F.10	Junction Temperature	T_j	-40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.1 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
G.1	Junction to Case[1)]	R_{thjC}			5.2	K/W	2)
G.2	Junction to Ambient[1)]	R_{thjA}		26		K/W	2) 3)

1) Not subject to production test, specified by design.
2) Both channels on with 1W power dissipation per channel
3) Specified RthJA value is according to Jedec JESD51-2, -5, -7 at natural convection on FR4 2s2p board. The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70mm Cu, 2 x 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner layer.

5 Functional Description and Electrical Characteristics

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

5.1 Supply and Reference

The device has incorporated a power-on reset circuit. This feature will reset the commanded average current to 0 mA (device off), and will reset the programmable registers to their default values. The fault register bits are reset during power on reset. The device will remain off until a valid command is received. The device will also be reset in the case of an undervoltage condition on the pin V_{DD}. Note that if the voltage on the pin *REF* pin is greater than the voltage on the pin $V_{DD,}$ a current will flow from the *REF* pin to the V_{DD} pin.

Electrical Characteristics [1]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2]	Max.		
5.1.1	REF Bias Current	I_{REF}	-20	–	20	µA	V_{REF} = 2.5 V (includes leakage current and a small current sink)
5.1.2	V_{DD} 5 V Supply Current	I_{DD}	–	–	15	mA	V_{DD} = 5.25 V; CSB = 5.0 V; DAC = 3FF
5.1.3	V_{SO} I/O Supply Current	I_{SO}	–	–	1	mA	V_{SO} = 5.25 V; CSB = 5.0 V
5.1.4	BAT Supply Current	I_{BAT}	–	–	1	mA	V_{DD} = 5.25 V; CSB = 5.0 V
5.1.5	V_{DD} Power-On Reset Threshold	V_{POR}	2.5	–	3.5	V	Power-On Reset Threshold
5.1.6	Internal Reference Voltage	V_{IREF}	2.45	2.5	2.55	V	Tested at wafer test.

1) Positive current flow is into the device.

2) Target @T_J = 25 °C

5.2 Input/Output

The DEFAULT pin is an active high input. A weak pull-up current (typical 15 µA) on this pin ensures a defined level when this pin is not connected (e.g. open pin). An active high signal on the DEFAULT pin sets the commanded current for both channels to 0 mA, and resets all programmable registers to their default values. Any SPI commands that are received while the DEFAULT pin is high will be ignored, and the SO pin will remain in a high impedance state.

The fault register bits are not cleared when the Default pin is asserted.

Upon coming out of default mode, the commanded current will remain at 0 mA, device off, and the programmable registers will remain at their default values.

The DEFAULT pin must be asserted high whenever the voltage on the pin V_{DD} is less than the minimum V_{DD} operating voltage (4.75 V), otherwise the electrical characteristic specifications (see table below) may not be met. The diagnostic functions are not operational when the V_{DD} voltage is less than 4.75V.

The TEST pin is an active high pin. This pin must be connected directly to ground in the application, as it is only used for IC test purposes. A passive pull-down resistor in the device ensures a logic low value when the pin is not connected.

Electrical Characteristics [1]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2]	Max.		
5.2.1	DEFAULT Input Bias Current	$I_{DEFAULT}$	-25	-10	-5	µA	$V_{DEFAULT}$ = 0 V; Pull-up source is pin V_{SO}
5.2.2	TEST Pull-down Resistor	R_{TEST}	–	20	–	kΩ	–
5.2.3	SI, SCK, CSB, DEFAULT Input Threshold	V_{IH}	2.0	–	–	V	SCK is specified by design, not subject to production test.
5.2.4	SI, SCK, CSB, DEFAULT Input Threshold	V_{IL}	–	–	0.8	V	SCK is specified by design, not subject to production test.
5.2.5	SO Output High Voltage	V_{OH}	0.8 V_{SO}	–	–	V	SO I_o = -1 mA
5.2.6	SO Output Low Voltage	V_{OL}	–	–	0.4	V	SO I_o = 1 mA

1) Positive current flow is into the device.

2) Target @T_J = 25 °C

5.3 Power Output

The slew rate of the voltage on the pins OUT1 and OUT2 are programmable via the SPI interface. The fast settings are intended for fast switching solenoids (low inductance) to minimize power dissipation within the TLE 7241E, and to minimize DC current error due to overshooting the switch points. The slower slew rates can be used with slower switching solenoids (high inductance) to improve radiated emissions from the wiring harness.

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.3.1	OUTx rise and fall times Slew Rate reg = 0	OUTx t_R and t_F	0.25	0.5	1	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.2	OUTx rise and fall times Slew Rate reg = 1	OUTx t_R and t_F	0.5	1	2	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.3	OUTx rise and fall times Slew Rate reg = 2	OUTx t_R and t_F	1	2	4	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.4	OUTx rise and fall times Slew Rate reg = 3	OUTx t_R and t_F	2.5	5	10	µs	Threshold: 4 V to 10 V V_{BAT} = 14 V; R_{load} = 5 Ω
5.3.5	OUTx Output Off Leakage (00_H)	I_{DSS}	–	–	10	µA	V_{DS} = 24 V
5.3.6	OUTx Output Off Leakage (00_H)	I_{DSS}	–	–	3	mA	V_{DS} = V_{CLAMP} - 1V V_{CLAMP} is the measured clamp voltage (**Item 5.4.1.3**)
5.3.7	OUTx[3)] Driver on Resistance	$R_{DS(ON)}$	–	240	450	mΩ	Driver on Resistance @T_J = 150 °C

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Electrical Distributions must be performed on this parameter as defined in the AEC-Q100 Specification Table 2 test 27.

5.4 Protection and Control

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.1	POS/NEG IBIAS	POS/NEG IBIAS	-500	–	500	µA	DAC command =3FF POS=NEG=0V & POS=NEG=17V
5.4.2	POS/NEG LEAKAGE	POS/NEG LEAKAGE	20	40	60	µA	Fault typing bit = 0, Zero Current, POS = NEG = 14 V
			-20	0	20	µA	Fault typing bit = 1, Zero Current, POS = NEG = 14 V

1) Positive current flow is into the device.

2) T_J = 25 °C

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

5.4.1 Overvoltage Sensing and Protection

When the voltage on the BAT pin exceeds the Overvoltage Shutdown Threshold (see table below, **Item 5.4.1.1**), the output channel will shut off to protect the IC from excessive power dissipation. A short filter with a typical value of 6.5 µs is included to prevent undesired shutdown due to short transient voltage spikes. Although SPI communication will remain functional, the output will remain off. The device will resume normal operation when the BAT voltage has dropped below the overvoltage hysteresis level. Note that the programmable registers are not reset, and the dither counter continues to operate during an overvoltage event.

Both channels are disabled when an overvoltage condition is detected.

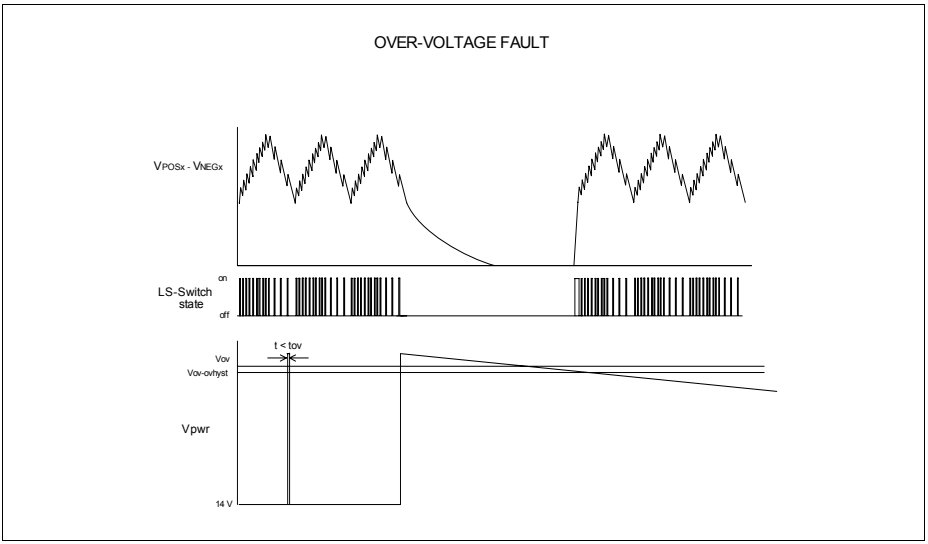

Figure 4 Overvoltage Shutdown

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.1.1	BAT Overvoltage Shutdown	OV	30	35	40	Vdc	Ramp up BAT until outputs Off
5.4.1.2	BAT Overvoltage hysteresis	OV_{HYST}	–	1.0	–	Vdc	Ramp BAT down until outputs On[3)]
5.4.1.3	OUTx Active Clamp Voltage	V_{clamp}	50	53	60	V	I_d = 20 mA, output off

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, specified by design.

5.4.2 Overcurrent / Short to V_{BAT} Sensing

An overcurrent fault is detected by sensing the voltage at the POS input pin. A comparator is used to detect the voltage while the gate drive is on. When the voltage at the POS input pin exceeds the short circuit / overcurrent threshold (see table below, **Item 5.4.2.3**) for a time greater than the short sense time (see table below, **Item 5.4.2.1**)

the driver will be turned off and the Overcurrent / Short to V_{BAT} (V_{SHT}) fault bit will be latched until the fault register is read via SPI. The driver will remain in the off condition for the short circuit refresh time (see table below, **Item 5.4.2.2**). After the refresh time, the driver will automatically turn on again. If the short condition is no longer present, the channel will operate normally. If the short circuit condition persists, the driver will be cycled off after the short sense time once again. The refresh time has been chosen for minimal increase in power dissipation during a continuous fault condition.

In order to prevent false detection of an overcurrent / short to V_{BAT} fault during an “off to on” transition of the low-side output transistor, the detection circuit is disabled for a blanking time (see **“Electrical Characteristics” on Page 31**, **Item 5.5.1.1** and **Item 5.5.1.2**) after the transistor is enabled (see **Figure 16** and **Figure 17**).

The output transistor control circuit includes a current limit feature that will limit the transistor current to a maximum value (see table below, **Item 5.4.2.4**) in order to protect the device from excessive current flow.

If a new average current command or configuration command is received for a shorted channel while that channel is within the short circuit refresh time, the new data will be stored but the channel will remain in the off state until the refresh time expires. The new data will become active when the short circuit condition is released.

The Overcurrent / Short to VBAT detection is channel specific.

Note: An Overcurrent / Short to VBAT fault is not detected if the average current command is <50 mA (with 1 W sense resistor).

Note: An overcurrent / short to V_{BAT} fault is latched until read via the MISO return word.

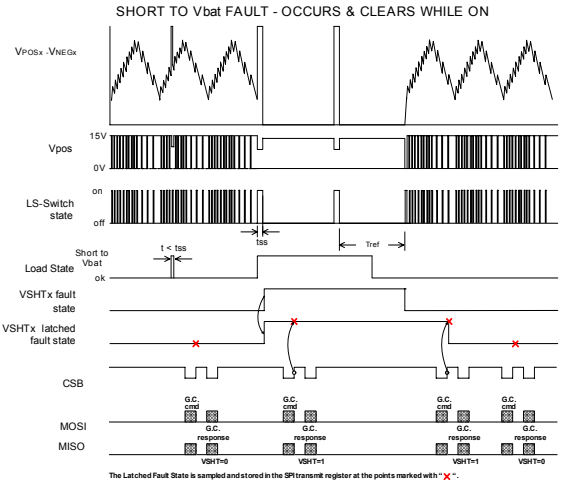

Figure 5 Short to V_{BAT} - Channel On

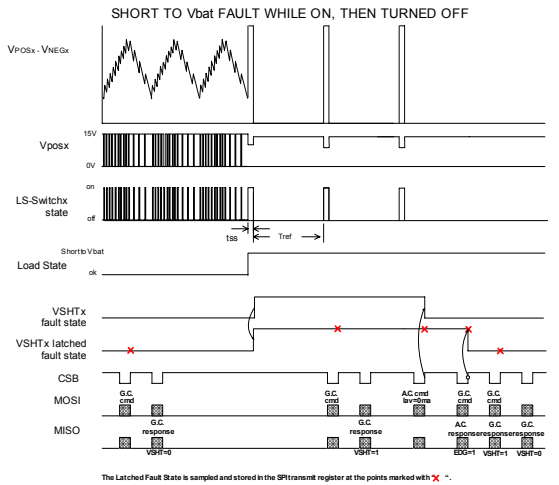

Figure 6 Short to V_{BAT} - Channel On Then Turned Off

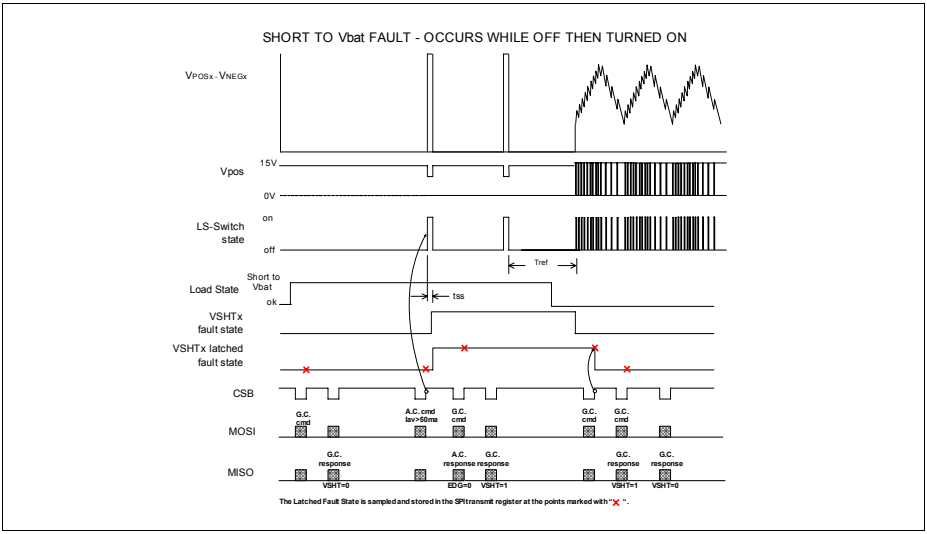

Figure 7 Short to V_{BAT} - Channel Off Then Turned On

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.2.1	OUTx Short Sense Time	t_{ss}	30	60	90	µs	50 - 50 Threshold
5.4.2.2	OUTx Short Refresh Time	t_{ref}	3	14	24	ms	50 - 50 Threshold
5.4.2.3	OUTx Short circuit/ Overcurrent Fault Threshold	$V_{VSHTOCT}$	2.0	2.5	3.0	Vdc	V_{REF} = 2.5 V
5.4.2.4	OUTx Current Limit	I_{dlim}	3.0	5.0	6.0	A	V_{BAT} = 14 V; V_{DD} = 5V; output on

1) Positive current flow is into the device.

2) T_J = 25 °C

5.4.3 Open Load / Short to Ground Detection

The OLSG fault bit is set under the following conditions.

Operating Condition #1

The average current command is > 50 mA (with 1 Ω sense resistor) and the low-side driver is ON (solenoid current is increasing).

The OLSG (open load/short to ground) fault bit will be set if the low-side transistor remains on for a time greater than the on state open sense time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.3**).

Operating Condition #2

The average current command is > 50 mA (with 1 Ω sense resistor) and the low-side driver is OFF.

The OLSG fault bit is set if the voltage on the NEGx pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.5**).

Operating Condition #3

The average current command is < 50 mA (with a 1 Ω sense resistor) and the fault typing bit = 0.

The OLSG (open load/short to ground) fault bit will be set if the POS pin voltage is less than the off state open load threshold (**"Electrical Characteristics" on Page 20**, **Item 5.4.2.3**) for longer than the off state open load sense time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.4**) or the NEG pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.5**). A pull-down current (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.1**) will be activated between the POS pin and ground when the Fault Typing bit = 0.

Operating Condition #4

The average current command is < 50 mA (with a 1 Ω sense resistor) and the fault typing bit = 1.

The OLSG fault bit will be set when the voltage on the pin POSx is below the off state open load threshold (**"Electrical Characteristics" on Page 20**, **Item 5.4.2.3**) for the a time greater than $t_{os(off)}$ (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.4**) or the NEG pin is less than the NEG pin OLSG threshold voltage (**"Electrical Characteristics" on Page 23**, **Item 5.4.3.6**) for a time greater than the NEG pin OLSG delay time

(**“Electrical Characteristics” on Page 23**, **Item 5.4.3.5**). A pull-up current (**“Electrical Characteristics” on Page 23**, **Item 5.4.3.2**) will be activated between V_{DD} and the POS pin when the Fault Typing bit = 1.

Distinguishing between Open Load and Short to Ground Faults

When an Open Load/Short to Ground is flagged, to distinguish between Open Load and Short-To-Ground, a general configuration command word must be sent three times to the appropriate channel with the fault typing bit set, and the average current must be programmed to zero. Check the OL/SG fault bit from the third write. A ‘0’ signifies Open Load, ‘1’ signifies Short-To-Ground. A short to ground will still be flagged for 0 mA command current. Note that setting the fault typing bit under both normal & fault conditions does not change the status of the output or the current flowing.

The fault typing bit enables a 40 µA pull-up current on the POS pin when high, and enables a 40 µA pull-down current on the POS pin when low.

Electrical Characteristics [1)]

T_j = -40 to 150 °C; V_{BAT} = 9 V to 18 V; V_{DD} = 4.75 V to 5.25 V

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions and Instructions
			Min.	Typ.[2)]	Max.		
5.4.3.1	POS Open detect current	I_{OL}	20	40	60	µA	Fault typing bit = 0, Zero Current
5.4.3.2	POS Load short to ground detect	I_{SG}	-60	-40	-20	µA	Fault typing bit = 1, Zero Current, POS = NEG = 2 V
5.4.3.3	OUTx On-State open sense time – POS pin	$t_{os}(on)$	6	12	24	ms	50 - 50 Threshold[3)]
5.4.3.4	OUTx Off-State open sense time – POS pin	$t_{os}(off)$	30	60	90	µs	50 - 50 Threshold[3)]
5.4.3.5	NEGx Open load / short to ground filter time – NEG pin	T_{OLSG_N} (off)	30	60	90	µs	–
5.4.3.6	NEGx Open load / short to ground detection threshold – NEG pin	V_{OLSG_N}	2.0	2.8	3.6	V	–

1) Positive current flow is into the device.

2) T_J = 25 °C

3) Not subject to production test, tested by scanpath.

Diagnostics Timing Diagrams

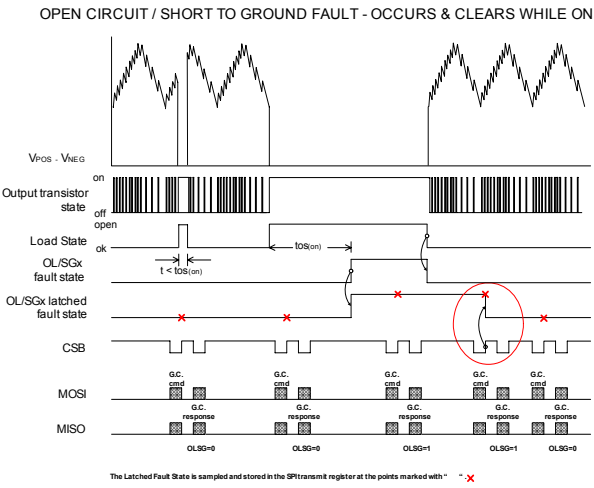

Figure 8 Open Load / Short to Ground Fault - Channel On

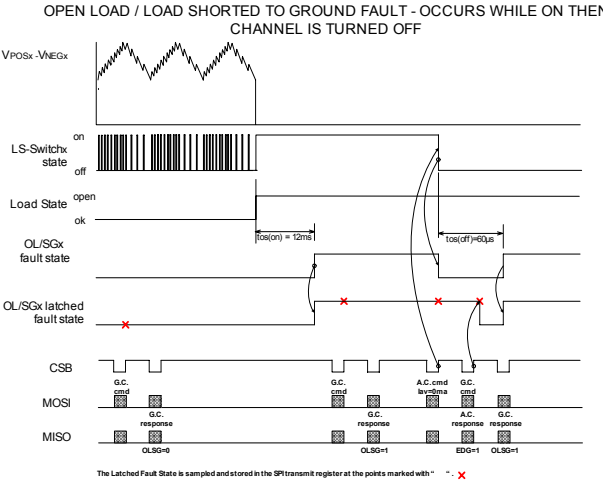

Figure 9 Open Load / Short to Ground - Channel On Then Turned Off

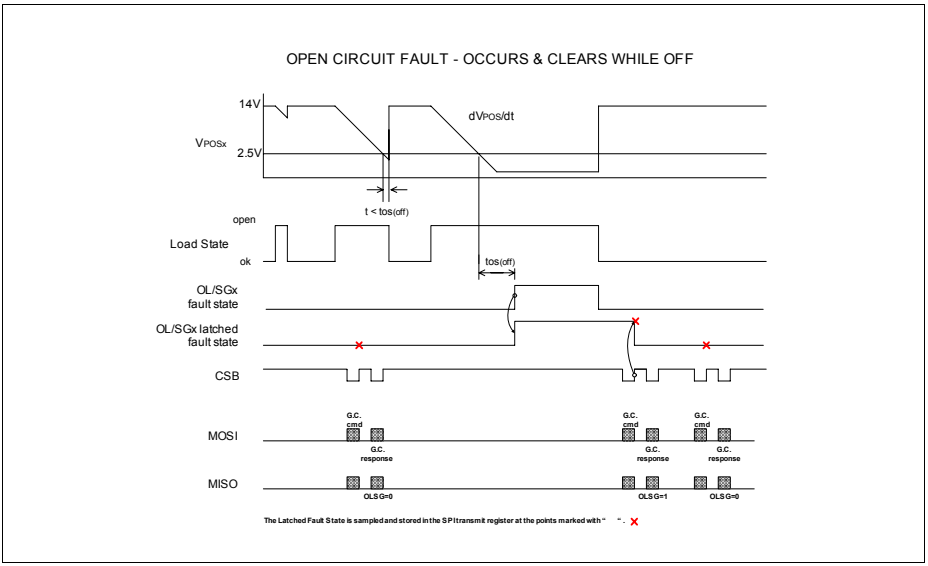

Figure 10 Open Load Short to Ground - Channel Off

$$\frac{\mathrm{d}V_{POS}}{\mathrm{d}t} = \frac{-(i_{OL} - i_{Rrecirc})}{(C_{POS} + C_{NEG} + C_{OUT})} \quad (1)$$

i_{OL} = open load detection pull down current (5.4.3.1)

$i_{Rrecirc}$ = reverse leakage current of recirculation diode

C_{POS} = external capacitance on the POS pin

C_{NEG} = external capacitance of the NEG pin

C_{OUT} = external capacitance on the OUT pin